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All Nodes Voltage Regulation and Line Loss Minimization in Loop Distribution Systems Using UPFC

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Abstract
Voltage regulation and line loss minimization in distribution networks are challenging problems, particularly when it is not economic to upgrade the entire feeder system. This paper presents a new method for achieving line loss minimization and all nodes voltage regulation in the loop distribution systems, simultaneously, by using UPFC, one of the most important FACTS devices. First, the line loss minimum conditions in loop system are presented. Then, load voltage regulation is applied under line loss minimum conditions. Reference voltage of the controlled node is determined based on the assumption that this voltage can subsequently improve all node voltages to be within the permissible range. Also, the proposed control scheme of the UPFC series converter, to regulate all node voltages under line loss minimization, is presented. The effectiveness of the proposed control scheme has been verified experimentally.

Index Terms
loop distribution system, voltage regulation, line loss minimization, series compensation, UPFC.

I. INTRODUCTION
Concerns over global warming have led to international efforts to address reductions in greenhouse gas emissions. Since energy supplies are one of the main contributors in these emissions, the operation and design standards for distribution networks have recently changed. The most important of these is the energy saving. Also, among all power quality issues, voltage drop is the most severe one that can lead to tremendous losses to the customers. Therefore, voltage is one of the most important elements of the electric power quality.
Distribution networks are typically of two types, radial or loop. It is well understood that radial distribution systems are more desirable than loop systems, and distribution engineers have preferred them because they use simple and inexpensive protection schemes. Also, when a fault occurs in the radial network, the faulted part can be isolated fast from the system to avoid the influence of the fault. However, there is high possibility of unbalanced power flow among feeders due to the different loads, which in turn causes high power loss and high voltage drop. In heavy loaded feeders, the voltage at the far end point may be beyond the allowed voltage limit. In order to operate distribution system effectively, loop system configuration has been proposed to balance the power flow, to reduce the power loss and to regulate the load voltages. However, short circuit current will increase, and fault location detecting method in loop systems has not yet been established [1].

Recent research in distribution systems has been focused on voltage regulation and line loss minimization. Some of them proposed reconfiguring radial distribution system to loop one using the existing infrastructure. In [2], the reliable operation of loop distribution system was achieved by installing a high speed protective relay to prevent fault expansion. In [3, 4], back-to-back (BTB) loop power flow controller and loop balancer controller are installed to connect the adjacent feeders to perform loop system. In [5, 6], a looping wire is used to reconfigure two radial feeders to loop system, and used the BTB converter to overcome problem of increase/decrease voltages. In addition, many papers considering loss reduction and voltage regulation in distribution systems, using FACTS devices, have been published [7–13]. Most of them used STATCOM, shunt active filter, series-shunt power converter and BTB converter to regulate and balance load voltages and to reduce line loss by reactive power injection. However, these literatures did not consider load voltage regulation and line loss minimization simultaneously.

In [14], the authors have proposed the line loss minimum conditions in loop distribution systems, and experimentally achieved them by using Unified Power Flow Controller (UPFC). Also, in [15], the authors have proposed a new control technique for UPFC to regulate load voltage to be equal in magnitude to source voltage under line loss minimization. However, these methods cannot guarantee all node voltages to be within the permissible voltage limit.

In this paper, the authors wish to deal with the UPFC as a centralized control device with the aim of attaining a better service quality, in terms of all nodes voltage regulation and power loss minimization in loop distribution system, simultaneously. Whenever the voltage profile violates voltage restriction, the control strategy is determined to keep voltage level along the feeders within pre-specified range, ± 5% of the nominal voltage. The proposed control scheme of the UPFC is presented. All nodes voltage regulation and line loss minimization in loop system are experimentally investigated by using laboratory prototype in a 200V, 6kVA system.

II. LINE LOSS MINIMUM CONDITIONS [14]

Fig. 1 shows a simple model of the distribution system. In this model, impedances of line 1, 2 and 3 are $Z_1 = R_1 + j\omega L_1$, $Z_2 = R_2 + j\omega L_2$ and $Z_3 = R_3 + j\omega L_3$, respectively. The load impedances are $Z_{l1}$ and $Z_{l2}$. The other systems, connected to this system, are represented by a current source $I_L$. The system is reconfigured to be loop system by connecting the adjacent ends of line 2 and line 3, using loop wire. Fig. 2 shows the approximate model of the system shown in Fig. 1.
The load currents $I_{L1}$ and $I_{L2}$, and the other systems current $I_L$ are assumed to be constant. Also, the line currents $I_{oi}(i=1, 2, 3 \text{ and } 4)$ flow in each line in the same direction (counter clock-wise). According to the line currents and the system parameters, the total line loss $P_l$ in the loop system can be formulated as follows:

$$P_l = \sum_{i=1}^{3} R_i |I_{oi}|^2$$

$$= R_{loop} \left| I_{o1} - \frac{R_2 I_{L1} + R_2 I_{L2} + (R_2 + R_3) I_L}{R_{loop}} \right|^2$$

$$- \frac{R_2 I_{L1} + R_2 I_{L2} + (R_2 + R_3) I_L}{R_{loop}} I_{m1}^2$$

$$+ R_2 |I_{L1} + I_{L2} + I_L|^2 + R_3 |I_L|^2$$

(1)

where:

$$R_{loop} = \sum_{i=1}^{3} R_i$$

(2)

Since the second, third and fourth parts in (1) are constants, because the currents $I_{L1}$, $I_{L2}$ and $I_L$ are assumed to be constants, the first part is the only part that can be used to obtain the line loss minimum conditions. These conditions can be obtained by equating the first part in (1) with zero. In this case, the total line loss $P_{l_{min}}$ in loop system can be formulated as follows:

$$P_{l_{min}} = \sum_{i=1}^{3} R_i |I_{mi}|^2$$

(3)

where $I_{mi} (i=1, 2, \text{ and } 3)$ is the line current that flows in the loop lines in case of line loss minimization. The loss minimum line currents can be formulated as follows:

$$I_{m1} = \frac{R_2 I_{L1} + R_2 I_{L2} + (R_2 + R_3) I_L}{R_{loop}}$$

$$I_{m2} = \left( \frac{R_1 + R_3}{R_{loop}} \right) I_{L1} + \left( \frac{R_1 + R_3}{R_{loop}} I_{L2} + R_1 I_L \right)$$

$$I_{m3} = \frac{R_2 I_{L1} + R_2 I_{L2} - R_3 I_L}{R_{loop}}$$

(4)

The difference between the currents $I_{oi}$ and $I_{mi}$ is defined as the loop current $I_{loop}$ that circulates in loop system in the same direction, and can be formulated as follows:

$$I_{loop} = I_{oi} - I_{mi} = -\frac{1}{R_{loop}} \sum_{i=1}^{3} j \omega L_i I_{oi}$$

(5)

The line loss minimum conditions in loop systems can be realized by eliminating the loop current $I_{loop}$ from the
system, which can be achieved if any of the following conditions is realized [14]:

\[
\frac{R_1}{L_1} = \frac{R_2}{L_2} = \frac{R_3}{L_3}
\]

(6)

\[
\sum_{i=1}^{3} j\omega L_i I_{i0} = 0
\]

(7)

III. VOLTAGE REGULATION UNDER LINE LOSS MINIMUM CONDITIONS

Load voltage regulation problems in distribution systems are commonly solved by using STATCOM, which has the ability to control voltage magnitude by compensating reactive power. However, STATCOM cannot control the line loss in loop distribution systems. On the other hand, series compensators, such as UPFC, have the ability to regulate load voltage and to minimize line loss simultaneously in the loop distribution system.

The main object of this paper is to minimize the total line loss and to regulate the load voltages in loop distribution system, simultaneously. The line loss minimum conditions can be achieved if the loop current is eliminated from the loop system. Under this condition, the load voltages can be controlled in order to keep it within the permissible voltage range, ± 5% of the nominal source voltage. Fig. 3 shows a simple model of loop distribution system that is used to simplify the idea of voltage regulation under line loss minimum condition. In this model, \( \hat{V}_s, \hat{V}_1 \) and \( \hat{V}_r \) are assumed to be source voltage, load 1 voltage and (load 2 and load 3) voltage, respectively. The series voltage source, \( \hat{V}_c \), is assumed to be a controlled series voltage that is used to regulate the load voltages. The controlled series voltage \( \hat{V}_c \) is inserted to the loop system by the UPFC series converter. Therefore, the voltage \( \hat{V}_c \) is assumed to be controlled in both voltage magnitude and phase angle.

A. Before installing the controlled series voltage \( \hat{V}_c \)

Fig. 4(a) shows the phasor diagram of the line currents and node voltages in the loop system shown in Fig. 3. The permissible voltage range is defined by the lower and upper voltage limits. It is cleared that the node 2 voltage \( \hat{V}_r \) is less than the lower voltage limit and lag behind the source voltage \( \hat{V}_s \) by the angle \( \theta \). Therefore, series compensation can be used to control node 2 voltage in order to regulate all node voltages to be within the permissible voltage limit.

B. After installing the controlled series voltage \( \hat{V}_c \)

Installing a series voltage source in a loop distribution system affects the power flow and hence changes all the node voltages. Based on the superposition theorem, the change in node 1 and node 2 voltages due to the installation of the controlled series voltage \( \hat{V}_c \) in the loop system shown in Fig. 3 can be formulated as follows:

\[
\begin{align*}
\Delta \hat{V}_1 &= -\hat{V}_c \frac{\hat{Z}_1}{\hat{Z}_{loop}} \\
\Delta \hat{V}_r &= \hat{V}_c \frac{\hat{Z}_2}{\hat{Z}_{loop}}
\end{align*}
\]

(8)

where:
\( \dot{V}_c \) is the series injected voltage, 
\( \dot{Z}_{t_{\text{loop}}} \) is the summation of the loop impedances.

Fig. 4(b,c) shows the phasor diagram of all line currents and node voltages after installing the controlled series voltage \( \dot{V}_c \). The phasor diagrams are drawn based on the change in each node voltage due to the installation of \( \dot{V}_c \). The value of the controlled series voltage \( \dot{V}_c \) is determined according to its function in the loop distribution system and the change in each node voltage can be calculated based on (8). Since the controlled series voltage \( \dot{V}_c \) realize its function by controlling the node 2 voltage, the phasor lines, representing the change in each node voltage, are drawn to show the overall change related to node 2 voltage. Also, the line currents \( \dot{I}_{0i} \) and their components (\( \dot{I}_{mi} \) and \( \dot{I}_{t_{\text{loop}}} \)) are drawn in the phasor diagram based on (4) and (5). The focus of the phasor diagram, shown in Fig. 4(b,c), is the relation between the change in the node 2 voltage and the loop current.

In the system shown in Fig. 3, if the controlled series voltage \( \dot{V}_c \) is installed to achieve loss minimum condition, node 2 voltage changes to be \( \dot{V}_{r_{a}} \), which is still less than the lower voltage limit and lag behind source voltage \( \dot{V}_s \) by the angle \( \theta^* \), as shown in Fig. 4(b). In this case, node 2 voltage can be formulated as follows:

\[
\dot{V}_{r_{a}} = \dot{V}_{r} + \dot{V}_c \frac{\dot{Z}_2}{Z_{t_{\text{loop}}}}
\]  

(9)

where:
- \( \dot{V}_r \) is the load voltage before installing \( \dot{V}_c \),
- \( \dot{V}_{r_{a}} \) is the load voltage after installing \( \dot{V}_c \).

Inserting a controlled series voltage in loop system to achieve line loss minimization affects all voltages in the system. However, Fig. 4(b) shows that this method cannot guarantee all node voltages to be within the permissible voltage range.

Fig. 4(c) shows the phasor diagram of the distribution system, shown in Fig. 3, with the effect of using \( \dot{V}_c \) to achieve load voltage regulation under line loss minimum condition. Based on the loop current, total power loss shown in (1) can be formulated as follows:

\[
P_l = \sum_{i=1}^{3} R_i |\dot{I}_{0i}|^2 = \sum_{i=1}^{3} R_i |\dot{I}_{mi}|^2 + R_{t_{\text{loop}}} |\dot{I}_{t_{\text{loop}}}|^2
\]  

(10)

Equation (10) shows that any circle centered by the current \( \dot{I}_{mi} \), due to the change in loop current, has constant power loss. The change in loop current will change the node 2 voltage by \( \Delta V \), as shown in Fig. 4(c). The resultant node 2 voltage can be formulated as follows:

\[
\begin{align*}
\dot{V}_{r_{a}} &= \dot{V}_{r_{a}} + \Delta V \\
\Delta V &= \dot{Z}_2 \dot{I}_{t_{\text{loop}}}
\end{align*}
\]  

(11)

Equation (11) shows that changing the loop current to draw a circle around its center \( \dot{I}_{mi} \) causes the node 2 voltage to draw a similar circle around its center \( \dot{V}_{r_{a}} \) that also has constant power loss. In case of line loss minimization, the loop current is zero and hence the radius of both circles is zero. As the loop current increases, the radius of these
circles and hence total line loss increase, too. The tangential point, point (P), between the circle centered by $V_{ra}$ and the circle of source voltage loci, represents the point at which node 2 voltage equals in magnitude to source voltage under loss minimum condition. In general, controlling node 2 voltage to be lag behind $V_s$ by the angle $\theta^*$, means controlling the voltage under line loss minimum condition [15]. However, controlling the node 2 voltage to be equal in magnitude to source voltage under line loss minimum condition cannot guarantee all node voltages to be within the permissible voltage range. According to (8), the change in node 2 voltage causes an opposite change in the node 1 voltage, that may cause the node 1 voltage to be less than the lower voltage limit.

In this paper, the reference magnitude of node 2 voltage is controlled to be in-between points $L$ and $U$, as shown in Fig. 4(c), in order to achieve all node voltages within the permissible voltage range under line loss minimum condition. The reference magnitude will start at point (p), then changes toward point (L) or (U) according to the voltage at node 1 in order to realize all node voltages in between the permissible voltage limit.

IV. PROPOSED CONTROL SCHEME

The proposed control scheme has been developed to meet the following objectives, simultaneously:

- Minimize total power loss in loop distribution systems.
- Regulate all node voltages to be within permissible voltage range.

Fig. 5 shows the loop distribution system model controlled by the UPFC. In this model, the UPFC series converter is represented by series voltage source connected at line 2, whereas the shunt converter is disregarded because its current is not as large as the distribution line current. The distribution system model has three nodes that their voltages can be controlled by the UPFC.

Fig. 6 shows the control flow chart of the UPFC series converter. First, the reference voltage of the UPFC series converter is calculated based on the line loss minimum condition. If any node voltage is outside the permissible voltage limit, UPFC will control the node 2 voltage to be equal in magnitude to source voltage under line loss minimization. In this case, if the voltage at node 1 or node 3 is still out of the limit, node 2 voltage magnitude will be controlled in order to keep them within the limit. In all cases, the reference angle of node 2 voltage is $\theta^*$ to control the node voltages under loss minimization.

Fig. 7 shows the proposed control block diagram of the UPFC series converter to achieve all nodes voltage regulation under line loss minimization by controlling node 2 voltage. The difference between reference and actual node 2 voltage is controlled by using PI controller to obtain the reference current of the UPFC line (Line 2), which is used to calculate the reference voltage of UPFC series converter $V_r$. The parameters in control block diagram are transformed from three-phase axis to the p-q axis using Park/Clarke transformation [18]. Also, the control technique used in this paper does not require any data about the loads, because in practical distribution systems, loads are continuously varying.

In order to achieve line loss minimization in the loop system, node 2 reference voltage can be formulated as follows:

$$V_{r}^* = |V_{ra}| \angle \theta^*$$  \hspace{1cm} (12)
Reference voltage for loss minimization can be calculated by using the line currents that flow in loop lines under loss minimum condition \( (I_{mi}, (i=1, 2, 3, \text{ and } 4)) \) and the line parameters [15]. In order to calculate these currents, first the UPFC circulating current, \( I_{upfc} \), is calculated as follows:

\[
I_{upfc} = \frac{V_c}{Z_{loop}}
\]  

(13)

The line currents that flow in loop system lines before installing UPFC \( (I_{0i}, (i=1, 2, 3, \text{ and } 4)) \) can be estimated by subtracting the UPFC circulating current, shown in (13), from the loop system line currents as follows:

\[
I_{0i} = I_i - I_{upfc}
\]  

(14)

By using the currents \( I_{0i} \), shown in (14), the loop current can be calculated as in (5). The line currents that flow in loop lines under loss minimum condition \( (I_{mi}, (i=1, 2, 3, \text{ and } 4)) \) can be calculated as follows:

\[
I_{mi} = I_{0i} - I_{loop}
\]  

(15)

By using the currents \( I_{mi} \), shown in (15), and the line parameters, the load voltage \( V_{ra} \), and hence the phase shift angle \( \theta^* \) can be calculated from the p-q axis components of \( V_{ra} \) as follows:

\[
V_{ra} = V_s - Z_1 I_{m1} + V_c - Z_2 I_{m2}
= V_s + Z_4 I_{m4} + Z_3 I_{m3}
\]  

(16)

\[
\theta^* = \tan^{-1}\left(\frac{V_{raq}}{V_{rap}}\right)
\]  

(17)

If the series injected voltage, for line loss minimization, cannot guarantee all node voltages to be within the permissible voltage limit, node 2 voltage magnitude should be controlled in order to achieve all node voltages within the limit. First, node 2 reference voltage is controlled to be equal in magnitude to source voltage and lag behind it by the angle \( \theta^* \) as follows [15]:

\[
V_r^* = |V_s| \angle \theta^*
\]  

(18)

In this case, estimated voltages of node 1 and node 3 are calculated in order to check the voltage value. Estimated reference voltage of UPFC series converter \( V^* \) and its circulating current \( I_{upfc} \) can be calculated as follows:

\[
V_c^* = (V_r^* - V_r) \frac{Z_{loop}}{Z_3 + Z_4}
\]  

(19)

\[
I_{upfc} = \frac{V_c^*}{Z_{loop}}
\]  

(20)
In (19), the node 2 voltage before installing UPFC, $V_r$, is calculated using line currents ($I_{0i}$, $i=1, 2, 3, and 4$), shown in (14). The estimated currents, that flow in loop system lines in case of controlling node 2 voltage as in (18), are calculated by adding the circulating current shown in (20) to the line currents ($I_{0i}$, $i=1, 2, 3, and 4$), and the resultant line currents are used to calculate the estimated voltages at node 1 and node 3.

If the series injected voltage still cannot guarantee voltages at node 1 and node 3 to be within the permissible voltage limit, an additional block diagram can be used in order to keep all node voltages within the limit, as shown in Fig. 7(b). The inputs of this additional block diagram can be node 1 or node 3 voltage, depending on which one of them is out of the limit. The reference values of node 1 and node 3 voltages can be the lower or the upper voltage limit according to the value of node voltage. In this case, node 2 reference voltage can be formulated as follows:

$$V_r^* = |V_n| (1 - \alpha) \angle \theta^*$$

where $\alpha$ is the voltage limit controller.

V. EXPERIMENTAL SYSTEM CONFIGURATION

A. Loop Distribution System Configuration

In order to demonstrate the effectiveness of using UPFC to realize all nodes voltage regulation and total line loss minimization in the loop distribution systems simultaneously, a simple laboratory model of the distribution system is used. Fig. 8 shows the 6kVA, 200V laboratory model including the distribution system and the UPFC. The distribution system consists of four sets three-phase lines, line 1, 2, 3 and 4. First, the system works as two radial feeders fed from same voltage source. Then, by using the loop wire to connect nodes $V_{2a}$ and $V_{2b}$ in parallel, the system is reconfigured to work as loop system with same line parameters. Installing loop wire makes the two node voltages $V_{2a}$ and $V_{2b}$ as one, known as $V_r$. The parameters of the whole system are listed in Table I.

B. UPFC Circuit Configuration

Fig. 8 shows the configuration of UPFC used in the experimental system. It consists of combined series and shunt converters connected back to back to each other through a common dc-link capacitors. The series converter, which acts as a controllable voltage source $v_r$, is used to inject a controlled voltage in series with the distribution line and thereby to force the power flow to a desired value. The shunt converter, which acts as a controllable current source $i_c$, is used to regulate the dc-link voltage by adjusting the amount of active power drawn from the distribution line to meet the real power needed by the series converter. In addition, the shunt converter has the capability of controlling reactive power [16].

The UPFC series and shunt converters, shown in Fig. 8, have been built as a three-phase PWM converter with IGBT SKM100GB124D as the power device. The DSP TMS320VC33 is selected as the controller for both converters. The shunt converter is connected in parallel with the distribution line via a three-phase transformer. The series converter, multilevel converter, consists of three single-phase H-bridge converters. The ac terminals of each H-bridge converter are
connected in series with the distribution line through a single-phase transformer. The switching and sampling frequency for series and shunt converters are 2.45 and 4.9 kHz, respectively.

The main function of the UPFC series converter is to realize all nodes voltage regulation and line loss minimization in the loop distribution system, simultaneously. Controlling the loop system by using UPFC requires detecting all line currents flowing in the loop lines, which in practical distribution system seems difficult. In [17], the authors have proposed a new method for estimating all line currents and voltages in four lines loop system, and applied this method to achieve total line loss minimization. In this method, the detected signals are UPFC line current $I_2$ and node voltage $V_r$ in addition to the main source voltage $V_s$ and its injected current $I_0$. The currents $i_c$, $i_0$, and $i_2$ are detected by using normal current sensors. Also, the voltages $V_{dc}$, $V_r$, and $V_s$ are detected by using normal voltage sensors. The outputs of the current and voltage sensors are connected to the AD converters in order to use in the DSP controller.

VI. EXPERIMENTAL RESULT

The laboratory model of loop distribution system shown in Fig. 8 is carried out before and after installing UPFC. In each case, line currents, all node voltages, and power loss in each line are measured and listed in Table II for comparison. All line currents, voltages, and total power loss, shown in Table II, are measured by using the Digital Power Meters (Yokogawa WT1600) that are connected simultaneously in the sending and receiving ends of each line in the experimental system. The power loss in each line is calculated from the difference between the sending and receiving powers.

A. Before Installing UPFC

The laboratory model shown in Fig. 8 is carried out first as two radial feeders fed from the same voltage source. Then, the system works as loop by connecting nodes $V_{2a}$ and $V_{2b}$ in parallel using loop wire. Installing loop wire makes the two node voltages $V_{2a}$ and $V_{2b}$ as one known as $V_r$. Table II shows the experimental results of all line currents, loop current, all node voltages, and total line loss in the radial and loop configurations. In the radial configuration node voltages $V_3$ and $V_{2b}$ are less than the lower voltage limit (190 V). Although reconfiguring the system to work as loop one enhances the loop wire voltage $V_r$, it is still less than the lower voltage limit.

B. After Installing UPFC

Experimental system shown in Fig.8 is carried out as loop distribution system after installing UPFC. First, UPFC is used to achieve line loss minimum condition. Then, UPFC is used to regulate node 2 voltage to be equal in magnitude to the nominal voltage under line loss minimum condition. Finally, UPFC is used to regulate all node voltages to be within permissible voltage range, $200 \pm 5\%$, under line loss minimum condition. In each case, the line currents, node voltages, and total line loss are measured and listed in table II for comparison.
1) Line Loss Minimization: UPFC is installed in the loop system to achieve line loss minimum condition by controlling node 2 voltage to be as shown in (12). Table II shows the experimental results of all line currents, loop current $i_{\text{loop}}$, all node voltages, UPFC series converter voltage $v_c$, and total line loss. Fig. 9 shows the experimental waveforms of loop current, UPFC series converter voltage, reference and actual node 2 voltage in the p-q axis, reference and actual line 2 current in the p-q axis, reference and actual phase shift angle between the source and node 2 voltages, and RMS line voltage of each node in the loop system before and after installing UPFC. Experimental results show that, UPFC eliminates the loop current from loop system and hence minimize the total line loss by 7.3%. However, the node 2 voltage is still less than the lower voltage limit.

2) Node Voltage Equal in Magnitude to Nominal Source Voltage under Loss Minimization: UPFC is installed in the loop system to regulate node 2 voltage to be equal in magnitude to the nominal source voltage (200V) under line loss minimum condition by controlling node 2 voltage to be as shown in (18). Table II and Fig. 10 show the experimental results in the loop system before and after installing UPFC. Experimental results show that, the UPFC regulates the node 2 voltage to be equal in magnitude to the nominal source voltage. However, the total line loss increases by 5.1% and the node 1 voltage decreases and becomes less than the lower voltage limit.

3) All Nodes Voltage Regulation under Loss Minimization: UPFC is installed in the loop system to achieve all node voltages to be within the permissible voltage limit under line loss minimum condition by controlling node 2 voltage to be as shown in (21). In this case controlling the system to be under loss minimum condition is achieved by controlling node 2 voltage to be lag behind source voltage by the angle $\theta$. Also, the reference magnitude of node 2 voltage is controlled in order to achieve all node voltages to be within the limit. Table II and Fig. 11 show the experimental results of loop system before and after installing UPFC. It is cleared that, after installing UPFC, the reference and actual values agree well with each other.

According to the control flow chart shown in Fig. 6, The UPFC starts with controlling node 2 voltage to achieve line loss minimization, and the estimated values have been used to check if the voltage at each node is within the permissible voltage limit or not. Fig. 12 shows the estimated and actual voltages of all nodes in case of controlling node 2 voltage to achieve line loss minimum condition. Since the estimated values of node 2 voltage, in case of loss minimization, is less than the lower voltage limit, the reference magnitude of node 2 voltage is changed to be equal to the nominal source voltage magnitude (200V). In this case, estimated values have been used to check if node 1 and node 3 voltages are within the limit or not. Fig. 13 shows the estimated and actual voltages of node 1 and node 3 in case of controlling node 2 voltage to be equal in magnitude to source voltage under line loss minimization. Since the estimated values of node 1 voltage is less than the lower voltage limit, the reference magnitude of node 2 voltage is changed to be as shown in (21) using the voltage limit controller ($\alpha$). In this case, the reference voltage of node 1, shown in Fig. 7(b), is equal to the lower voltage limit (190V), and the sign of $\alpha$ is positive as shown in Fig. 11. Experimental results show that after installing UPFC, all node voltages are within the limit, loop current decreases by 22.7% from its original value, and hence total line loss reduces by 2%. Also, estimated and actual values of the node voltages, shown in Fig. 12 and Fig. 13, agree well with each other.
Fig. 14 shows the calculated results of all node voltages in the system shown in Fig. 8, connected as two radial feeders and as loop system, before and after installing UPFC to achieve line loss minimum condition, and to achieve node 2 voltage equal in magnitude to source voltage under line loss minimization, assuming that source voltage is 200V. It is cleared that, in radial configuration the node voltages \( V_{26} \) and \( V_3 \) are less than the lower voltage limit, 190V. Also, in the loop configuration before and after installing UPFC to achieve line loss minimum condition, node 2 voltage is less than the lower voltage limit. In addition, after installing UPFC to achieve node 2 voltage equal in magnitude to source voltage, the node 1 voltage has become less than the lower voltage limit. Therefore, controlling node 2 voltage as shown in (21) is necessary to guarantee all node voltages to be within the permissible voltage range.

Fig. 15 shows a comparison between theoretical and experimental results of total line loss in radial system, loop system without UPFC, and loop system with UPFC that is used to achieve line loss minimum condition, to achieve load voltage equal in magnitude to the nominal source voltage, and to achieve all node voltages to be within the permissible voltage limit under loss minimization. Also, Fig. 16 shows the RMS line-to-line node voltages in each case. It is cleared that, only in the last case all node voltages are within the permissible voltage limit under loss minimization.

VII. CONCLUSION

This paper has presented the line loss minimum conditions and the control scheme of UPFC to regulate all node voltages to be within the permissible voltage range under loss minimization in the loop distribution systems. Regulating node voltages under line loss minimization has been achieved by controlling the phase angle of the controlled voltage. Installing UPFC to minimize the total line loss or to regulate the load voltage to be equal in magnitude to the nominal source voltage under loss minimization cannot guarantee all node voltages to be within the permissible voltage limit. In order to achieve all nodes voltage regulation, the reference voltage magnitude has been controlled depending on the estimated voltages at all nodes in the loop system. Node voltage estimation has been proposed and the estimated voltages at each node agree well with their actual values. Experimental results prove that, the UPFC has a great capability to regulate all node voltages to be within the permissible voltage range under line loss minimum condition in the loop distribution systems.
REFERENCES


Fig. 4. Phasor diagram of the loop distribution system.

Fig. 5. Model of the system in case study.

Fig. 6. Control steps of UPFC series converter.

(a) Main block control circuit.

(b) Node voltage limit control.

Fig. 7. Control scheme of UPFC series converter.


Fig. 8. Experimental system configuration.

**TABLE I**

<table>
<thead>
<tr>
<th>System Parameters (200 V - 6 kVA base)</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Source voltage $v_s$</td>
<td>203 V, 60 Hz</td>
</tr>
<tr>
<td>Load $R_{L,1}$</td>
<td>30 Ω (0.22 p.u.)</td>
</tr>
<tr>
<td>Load $R_{L,2a}$</td>
<td>80 Ω (0.08 p.u.)</td>
</tr>
<tr>
<td>Load $R_{L,2b}$</td>
<td>26.7 Ω (0.25 p.u.)</td>
</tr>
<tr>
<td>Load $R_{L,3}$</td>
<td>60 Ω (0.11 p.u.)</td>
</tr>
<tr>
<td>Line 1 $L_1$</td>
<td>6.0 mH (0.34 p.u.)</td>
</tr>
<tr>
<td>Line 1 $R_1$</td>
<td>0.6 Ω (0.09 p.u.)</td>
</tr>
<tr>
<td>Line 2 $L_2$</td>
<td>6.0 mH (0.34 p.u.)</td>
</tr>
<tr>
<td>Line 2 $R_2$</td>
<td>0.8 Ω (0.12 p.u.)</td>
</tr>
<tr>
<td>Line 3 $L_3$</td>
<td>6.0 mH (0.34 p.u.)</td>
</tr>
<tr>
<td>Line 3 $R_3$</td>
<td>1.2 Ω (0.18 p.u.)</td>
</tr>
<tr>
<td>Line 4 $L_4$</td>
<td>6.0 mH (0.34 p.u.)</td>
</tr>
<tr>
<td>Line 4 $R_4$</td>
<td>1.2 Ω (0.18 p.u.)</td>
</tr>
<tr>
<td>Capacitor $C$</td>
<td>3000 μF</td>
</tr>
<tr>
<td>Input $L$ of shunt conv.</td>
<td>2.0 mH</td>
</tr>
<tr>
<td>DC link voltage $V_{dc}$</td>
<td>100 V</td>
</tr>
<tr>
<td>Switching time $T_s$</td>
<td>204 μs</td>
</tr>
<tr>
<td>Main PI gains $K_p, K_I$</td>
<td>10 A/V, 20 A/V/sec</td>
</tr>
<tr>
<td>Voltage limit PI gains $K_{pH}, K_{IH}$</td>
<td>0.2 A/V, 0.3 A/V/sec</td>
</tr>
</tbody>
</table>


[12] O. Senturk and A. Hava, “High performance harmonic isolation and load voltage regulation of the three-phase series active filter utilizing the
Fig. 9. Experimental waveforms of loop system before and after installing UPFC [Case (1)].

<table>
<thead>
<tr>
<th>TABLE II</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
</tr>
<tr>
<td>EXPERIMENTAL RESULTS BEFORE AND AFTER INSTALLING UPFC</td>
</tr>
<tr>
<td>------------------------------------</td>
</tr>
<tr>
<td>Before UPFC</td>
</tr>
<tr>
<td>Radial</td>
</tr>
<tr>
<td>---------</td>
</tr>
<tr>
<td>$I_1$  [A]</td>
</tr>
<tr>
<td>$I_2$</td>
</tr>
<tr>
<td>$I_3$</td>
</tr>
<tr>
<td>$I_4$</td>
</tr>
<tr>
<td>$I_{loop}$</td>
</tr>
<tr>
<td>$V_x$  [V]</td>
</tr>
<tr>
<td>$V_i$</td>
</tr>
<tr>
<td>$V_{2a}$</td>
</tr>
<tr>
<td>$V_{2b}$</td>
</tr>
<tr>
<td>$V_0$</td>
</tr>
<tr>
<td>$V_c$  [V]</td>
</tr>
<tr>
<td>$P_{loss}$ [W]</td>
</tr>
</tbody>
</table>
Fig. 10. Experimental waveforms of loop system before and after installing UPFC [Case (2)].
Fig. 11. Experimental waveforms of loop system before and after installing UPFC [Case (3)].

Fig. 12. Experimental waveforms of estimated and actual values of all node voltages [Case (1)].
Fig. 13. Experimental waveforms of estimated and actual voltages of node 1 and node 3 [Case (2)].

Fig. 14. Calculated node voltages before and after installing UPFC.

Fig. 15. Total line loss.

Fig. 16. RMS line-to-line node voltages.