Chapter 5. AlGaAs/GaAs Vertical-Cavity Surface-Emitting Lasers on Si Substrates

5.1 Introduction

The vertical-cavity surface-emitting lasers (VCSELs) on Si are the most promising devices for optical interconnections in future OEICs[1-9]. In addition, the residual thermal stress and dislocations in the active region and the threshold current can be reduced in the VCSELs on Si with the small active regions[1]. Therefore, the VCSEL structure also has the potential for the realization of reliable GaAs-based lasers on Si. There has been only one demonstration[1] of the VCSEL on Si fabricated by heteroepitaxial growth. For this VCSEL on Si, the pulsed I_{th} was ~125 mA at room-temperature, corresponding to the J_{th} of ~71 kA/cm^2. To date, however, cw operation has not been realized yet.

In this chapter, the low-threshold pulsed operation of AlGaAs/GaAs VCSEL on Si at room-temperature[10,11] was described. Furthermore, cw operation at low-temperature was also presented. This chapter is organized as follows: In section 5.2, room-temperature pulsed operation is described. Low-temperature cw operation is presented in section 5.3. This chapter is concluded in section 5.4.

5.2 Room-Temperature Pulsed Operation

5.2.1 Epitaxial Growth and Fabrication Process

The VCSEL structure was grown on Si substrate at 750 °C by the conventional two-step growth technique. Figure 5.1 shows the cross-sectional SEM micrograph of the AlGaAs/GaAs VCSEL on Si. The

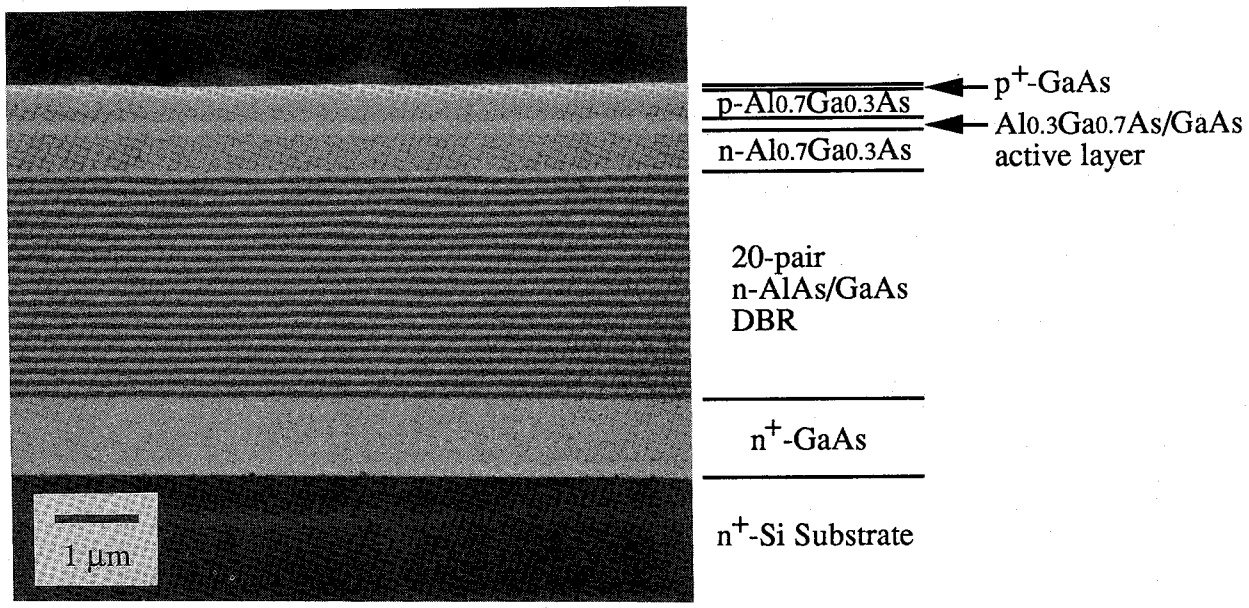
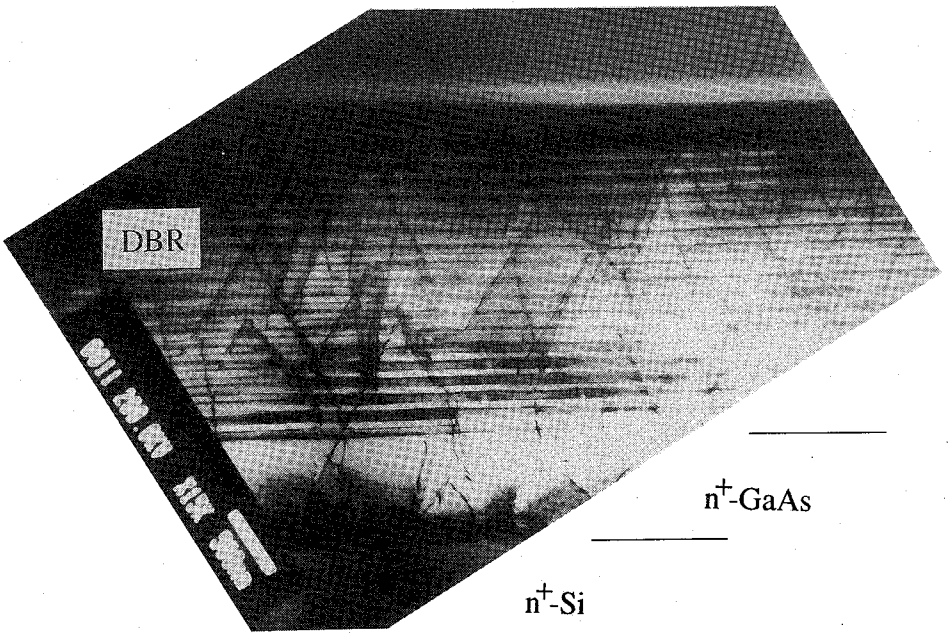


Fig. 5.1. Cross-sectional SEM micrograph of the AlGaAs/GaAs VCSEL on Si.

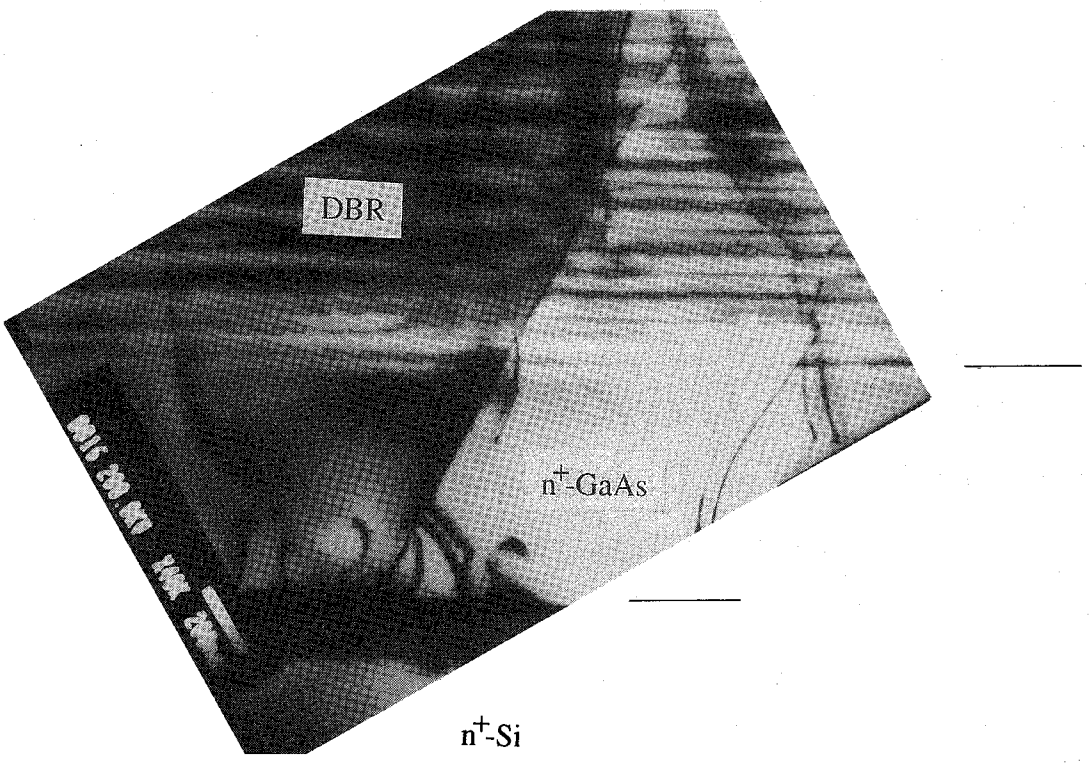
structure consisted of a 0.85-μm-thick thermal-cycle annealed n^+-GaAs buffer layer, a 20-pair of n^+-AlAs/n^+-GaAs (71 nm/59 nm) quarter-wave multilayer DBR, a 0.46-μm-thick n-$Al_{0.7}Ga_{0.3}As$ lower cladding layer, a 70-nm-thick undoped $Al_{0.3}Ga_{0.7}As$ lower confining layer, an undoped 9-nm-thick GaAs SQW active layer, a 70-nm-thick undoped $Al_{0.3}Ga_{0.7}As$ upper confining layer, a 0.34-μm-thick p-$Al_{0.7}Ga_{0.3}As$ upper cladding layer, and an 80-nm-thick p^+-GaAs contact layer. 50-nm-thick AuSb/150-nm-thick Au were used for the contact on the n^+-Si substrate. Nonalloyed 50-nm-thick AuZn/150-nm-thick Au of 40×40 μm^2, which was used for the top mirror and the electrical contact, was formed by the photoresist patterning and the lift-off technique. The devices were mounted, junction up, on a sample holder and tested under pulsed condition (0.1 μs pulses at 1MHz repetition rate) at room-temperature. Output power from the VCSEL was measured by detecting the light emitted around the edges of the AuZn/Au metallization. The DSD was also measured by electron-beam-induced current (EBIC) method using a SEM (Topcon ABT-55).

5.2.2 Characteristics of Reflectors

Figures 5.2(a) and 5.2(b) show the cross-sectional transmission electron microscopy (TEM) micrographs of the overall VCSEL on Si and near the GaAs/Si interface, respectively. Some threading dislocations, which originate at the GaAs/Si interface, can be effectively confined into the thermal-cycle annealed n^+-GaAs layer [Fig. 5.2(b)]. However, dislocation bending was not observed in the AlAs/GaAs DBR [Fig. 5.2(a)]. Although some previous studies[1,12,13] have indicated that the AlAs/GaAs DBR is effective in bending the dislocations due to interdiffusion-assisted dislocation motion in AlAs/GaAs[12] or crystal hardening of AlAs[14], Fig. 5.2(a) shows that



(a) overall VCSEL on Si



(b) near the GaAs/Si interface

Fig. 5.2. Cross-sectional TEM micrographs: (a) overall VCSEL on Si and (b) near the GaAs/Si interface.

many dislocations originating at the GaAs/Si interface propagate into the active layer. This VCSEL on Si, which was grown under the thermal cycle annealing and the AlAs/GaAs DBR, also showed the DSD of $2\text{-}3\times10^{7}$ cm^{-2}. This value is almost the same value for the sample without the AlAs/GaAs DBR. These results indicate that the AlAs/GaAs DBR is not effective in bending the threading dislocations because there is less mismatch (~0.14 %) in the lattice constant for the AlAs/GaAs layers.

The calculated and measured reflectivities of the 20-pair of AlAs/GaAs DBR on Si are shown in Fig. 5.3. The reflectivity of the DBR was measured with a monochromator and the reference reflectivity was supplied by a deposited aluminum mirror. The measured reflectivity was above 90 % at the wavelength region between 820 and 870 nm. The recorded maximum reflectivity was 93 % at 860 nm, which was slightly longer than the designed wavelength of 850 nm, presumably due to a small nonuniformity of the thickness during growth. As shown in Fig. 5.3, it is found that the measured peak reflectivity of 93 % is lower than the calculated reflectivity of 99.3 % at 860 nm. Figures 5.4(a) and 5.4(b) show the magnified cross-sectional SEM micrographs of the AlAs/GaAs DBRs grown on GaAs and Si substrates, respectively. The interfacial sharpness with uniform and smooth heterointerfaces is clearly seen in the DBR on GaAs. However, the DBR on Si shows quasiperiodic zigzag roughness and nonuniformity in the AlAs/GaAs layers[15]. Compared with Fig. 5.4(a), the thickness variations are estimated to be from -8 to +6 % for the AlAs layer and from -3 to +14 % for the GaAs layer in the DBR on Si as shown in Fig. 5.4(b). Additionally, Figure 5.5 shows the AFM image of the surface morphology for the VCSEL on Si. The microroughnesses consisting of hillocks and depressions with a different size were observed in the surface morphology. The surface

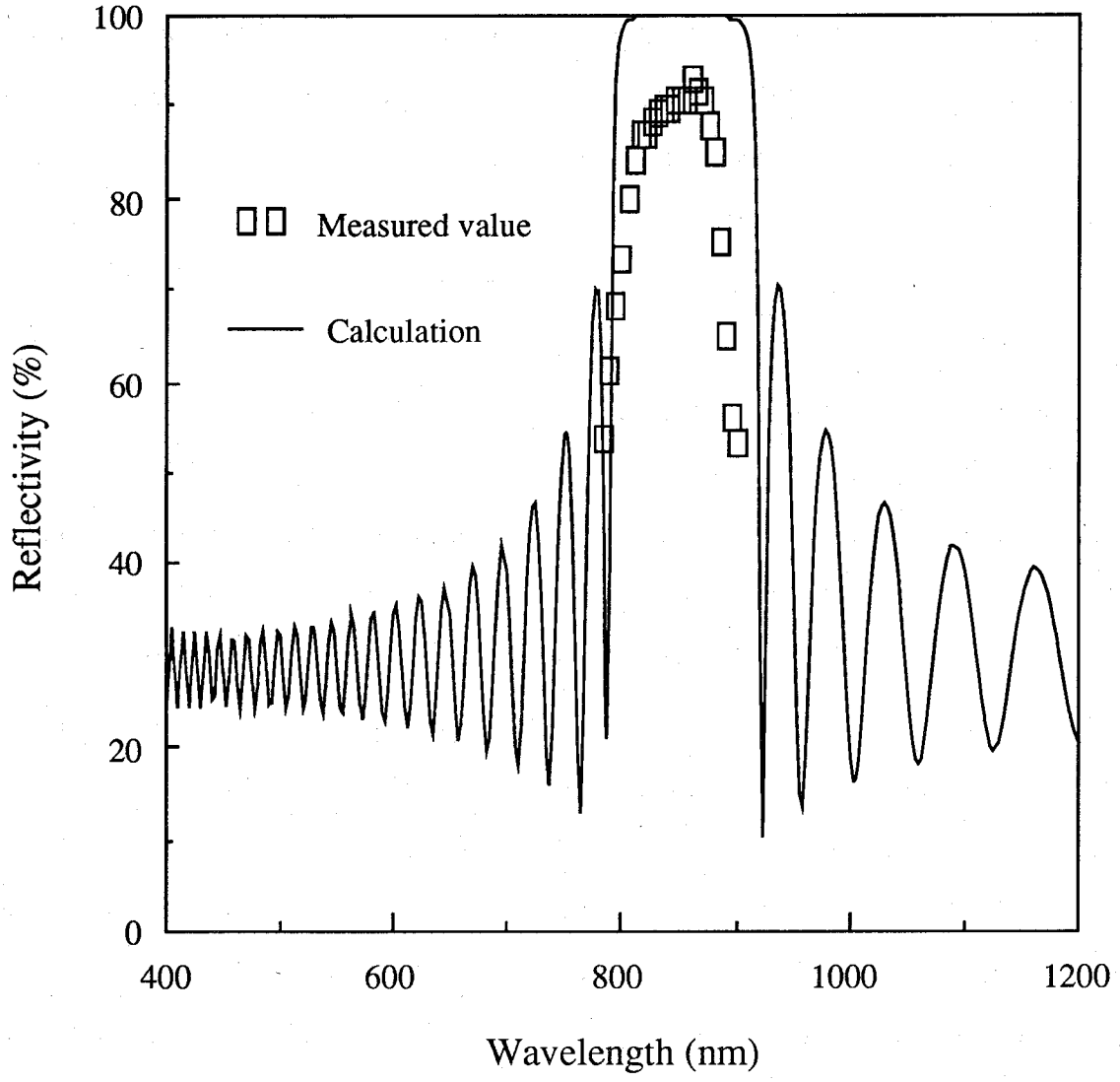
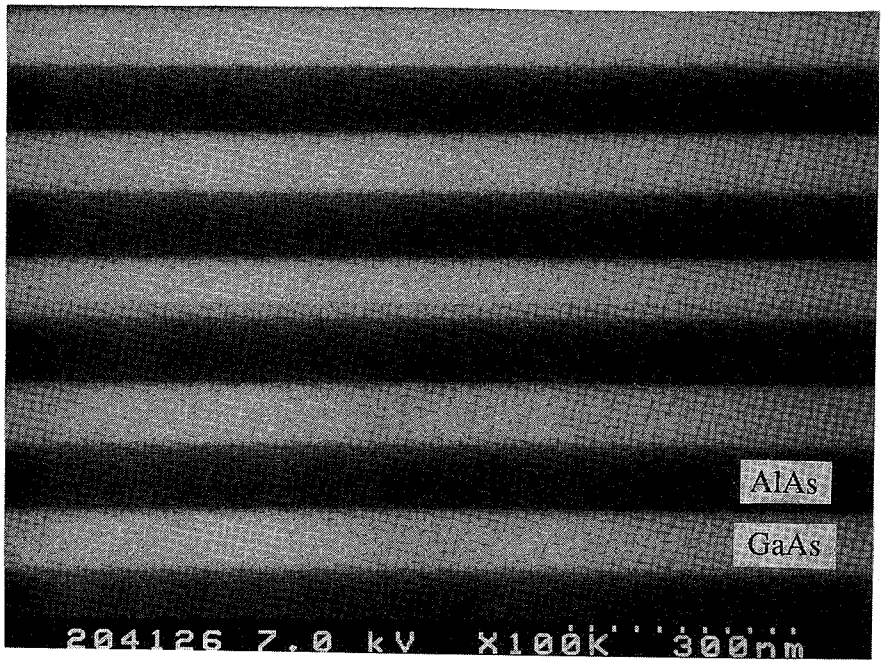
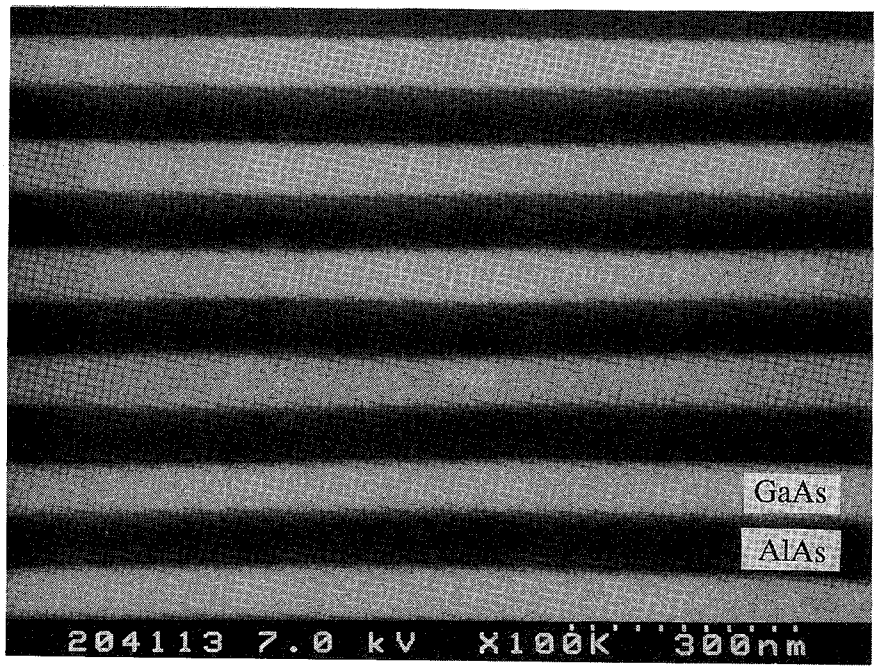


Fig. 5.3. Calculated and measured reflectivities of the 20-pair of the AlAs/GaAs DBR on Si.



(a) AlAs/GaAs DBR on GaAs sub.



(b) AlAs/GaAs DBR on Si sub.

Fig. 5.4. Magnified cross-sectional SEM micrographs of the AlAs/GaAs DBR on (a) GaAs and (b) Si substrates.

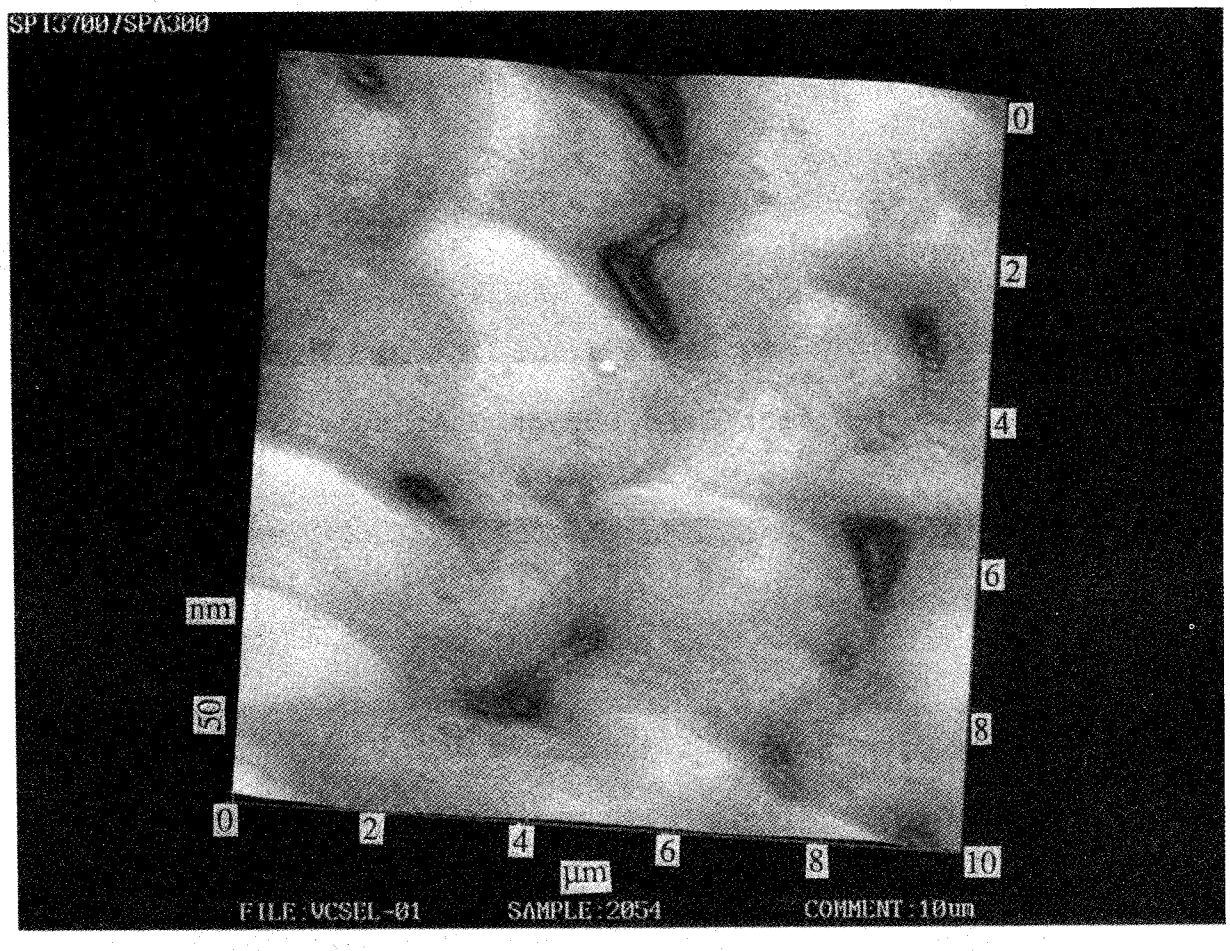


Fig. 5.5. AFM image of the surface morphology for the VCSEL on Si.

and interfacial roughnesses are probably due to the three-dimensional GaAs growth on Si at the initial growth stage. It has been theoretically demonstrated that the reflectivity spectrum and its peak value are very insensitive to small thickness variation (a few monolayers) in the DBR[16-18]. However, the large zigzag roughness and interfacial roughness (as shown in Figs. 5.4(b) and 5.5) introduce a large optical diffraction and scattering, resulting in the lower reflectivity of the DBR on Si.

In contrast, the top mirror has the reflectivity of 60 % for the alloyed and 96 % for the nonalloyed AuZn/Au. The higher reflectivity of the nonalloyed AuZn/Au seems to have been caused by a smooth morphology due to the lack of thermal annealing[19].

5.2.3 Lasing Characteristics

The turn-on voltage and the series resistance were 1.3 V and 26 Ω, respectively. These values are comparable to those of the conventional edge-emitting lasers on Si. These results indicate that the 20-pair of n^+-AlAs/GaAs DBR on Si hardly makes the series resistance high. Figure 5.6 shows an L-I characteristic of the VCSEL on Si under pulsed condition at room-temperature. This VCSEL exhibited the I_{th} of 79 mA, corresponding to the J_{th} of 4.9 kA/cm^2. Additionally, the peak emission wavelength was 840.03 nm and the FWHM was 0.28 nm. Compared with the previously reported results[1], this VCSEL on Si exhibits remarkable improvements such as a lower threshold and a narrower emission spectrum, which are probably due to relatively lower dislocation density and laser structure. However, this pulsed J_{th} of 4.9 kA/cm^2 is much higher than many reported results[2,20-24] of the VCSELs on GaAs substrates. A cw operation could not be achieved in this VCSEL because of a lower optical gain of the SQW active layer and a lower reflectivities of

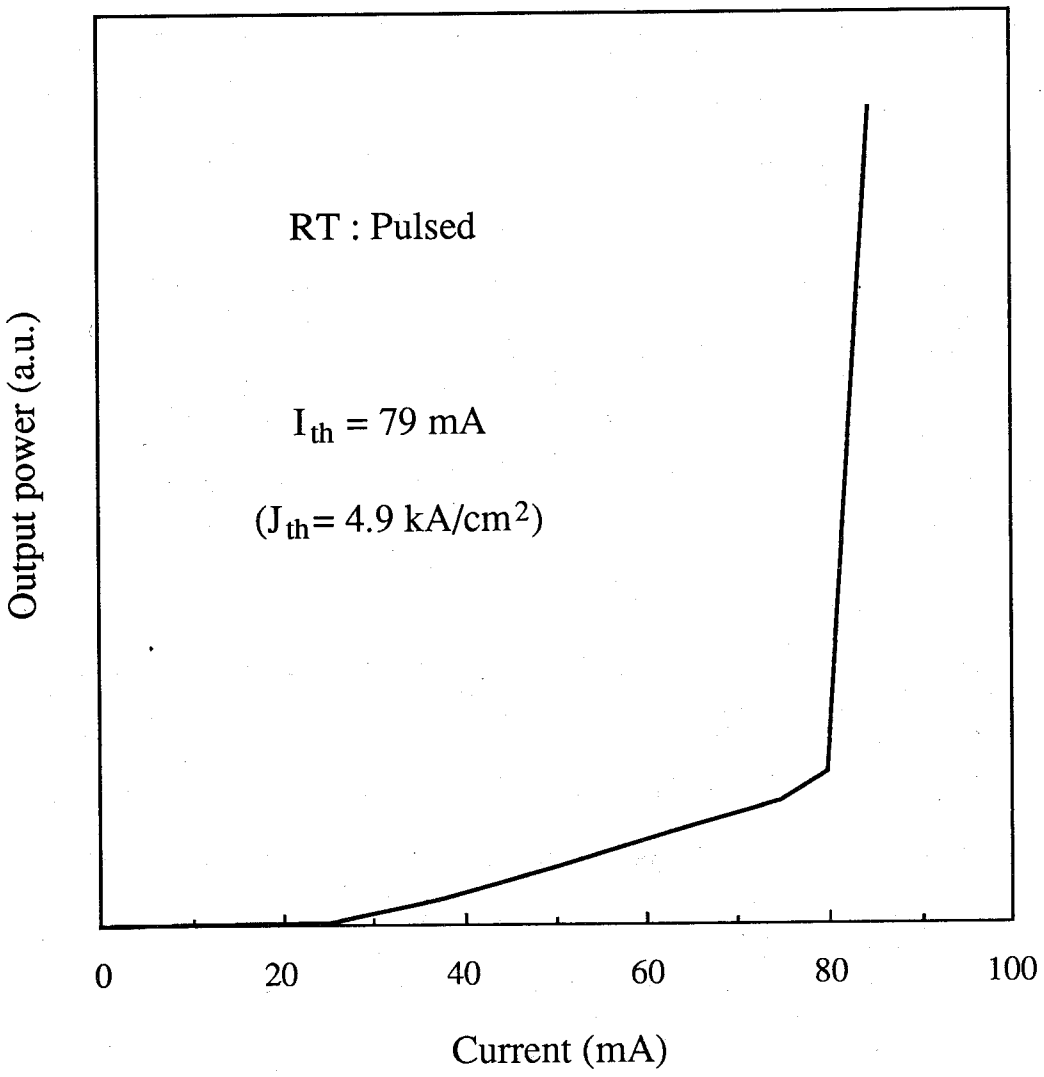


Fig. 5.6. L-I characteristic of the VCSEL on Si under pulsed condition at room-temperature.

reflectors.

5.3 Low-Temperature CW Operation

5.3.1 Epitaxial Growth and Fabrication Process

In order to achieve the cw operation, it is very important for the VCSEL on Si to increase the optical gain and the reflectivities of reflectors, because the VCSEL has a much shorter cavity length than that of the conventional edge-emitting laser and the mirror loss (1/Lln(1/R)) is very high. The higher reflectivity of the DBR on Si can be obtained by reducing the absorption losses of the n^+-GaAs layers in the DBR[1]. Therefore, the conventional AlAs/GaAs DBR was replaced with the AlAs/$Al_{0.1}Ga_{0.9}As$ DBR. Theoretically, the reflectivity increases by ~1 % for the AlAs/$Al_{0.1}Ga_{0.9}As$ DBR[1]. In contrast, the increasing optical gain is expected to be realized by use of MQW active layers structure due to the improvement of the gain flattening (saturation)[25-31].

The optimization of MQW active layers in the VCSEL, especially the number of quantum wells (N_w), has been discussed to achieve low threshold operation from the viewpoint of matched gain effect[29,31]. The threshold gain g_{th} of the VCSEL with internal loss and matched gain effect is given by[29,31]

$$\Gamma_r N_w L_w g_{th} = 1/2 \ln[1/(R_f R_r)] + \sum_{w,b}(\Gamma_r N_i L_i \alpha_{ai}) + (L-\sum_{w,b} N_i L_i)\alpha_c, \quad (5.1)$$

$$\Gamma_r = 1 + \sin(2\pi\sigma)/(2\pi\sigma), \ \sigma = 1/\lambda \sum_{w,b}(N_i L_i), \quad (5.2)$$

where L_w and L_b are the well thickness and barrier thickness, respectively. The L_b of 5.5 nm was used for the $Al_{0.3}Ga_{0.7}As$

barrier layer. R_f and R_r are the reflectivities of the front (top) and rear (bottom) side reflectors, respectively. Γ_r is the gain matching factor. α_{ai} and α_c are the absorption losses in the active and cladding layers, respectively. According to eq. (5.1), a large N_w in the cavity is desirable to increase the gain. However, from eq. (5.2), in order to achieve the matched gain (Γ_r>1), the total MQW thickness must be thinner than the $\lambda/2n$ (λ:wavelength, n:refractive index), which requires a reduction of N_w. For example, the N_w should be less than 14 if a 9-nm-thick GaAs quantum well is used as an active layer. Finally, from eq. (5.1), an optimum N_w is mainly determined by the reflectivities of reflectors.

From these viewpoints, an AlGaAs/GaAs VCSEL on Si with 10 GaAs quantum wells and a 23-pair of AlAs/$Al_{0.1}Ga_{0.9}As$ DBR was fabricated. Figure 5.7 shows a schematic cross-section of this VCSEL on Si. The laser structure comprised a 2.1-μm-thick thermal-cycle annealed n^+-GaAs buffer layer, a 23-pair of n^+-AlAs/n^+-$Al_{0.1}Ga_{0.9}As$ (71 nm/60 nm) quarter-wave multilayer DBR, a 0.29-μm-thick n-$Al_{0.7}Ga_{0.3}As$ lower cladding layer, a 51-nm-thick undoped $Al_{0.3}Ga_{0.7}As$ lower confining layer, ten undoped 9-nm-thick GaAs MQW (N_w=10) active layers separated by 5.5-nm-thick undoped $Al_{0.3}Ga_{0.7}As$ barrier layers, a 51-nm-thick undoped $Al_{0.3}Ga_{0.7}As$ upper confining layer, a 0.22-μm-thick p-$Al_{0.7}Ga_{0.3}As$ upper cladding layer, and a 34-nm-thick p^+-GaAs contact layer. After the growth, a laser device was fabricated as follows: A 0.1-μm-thick SiO_2 insulating layer was deposited on the p^+-GaAs contact layer and 50 μmϕ contact windows were opened by wet chemical etching of SiO_2. Next, 50-nm-thick Ti/60-nm-thick Au were evaporated on the p^+-GaAs layer as the p-side electrode except for the 20 μmϕ at the center of the 50 μmϕ contact window. A 70-nm-thick semitransparent Au was then evaporated on the p-side surface. A 50-nm-thick AuSb/150-nm-thick Au was used for the

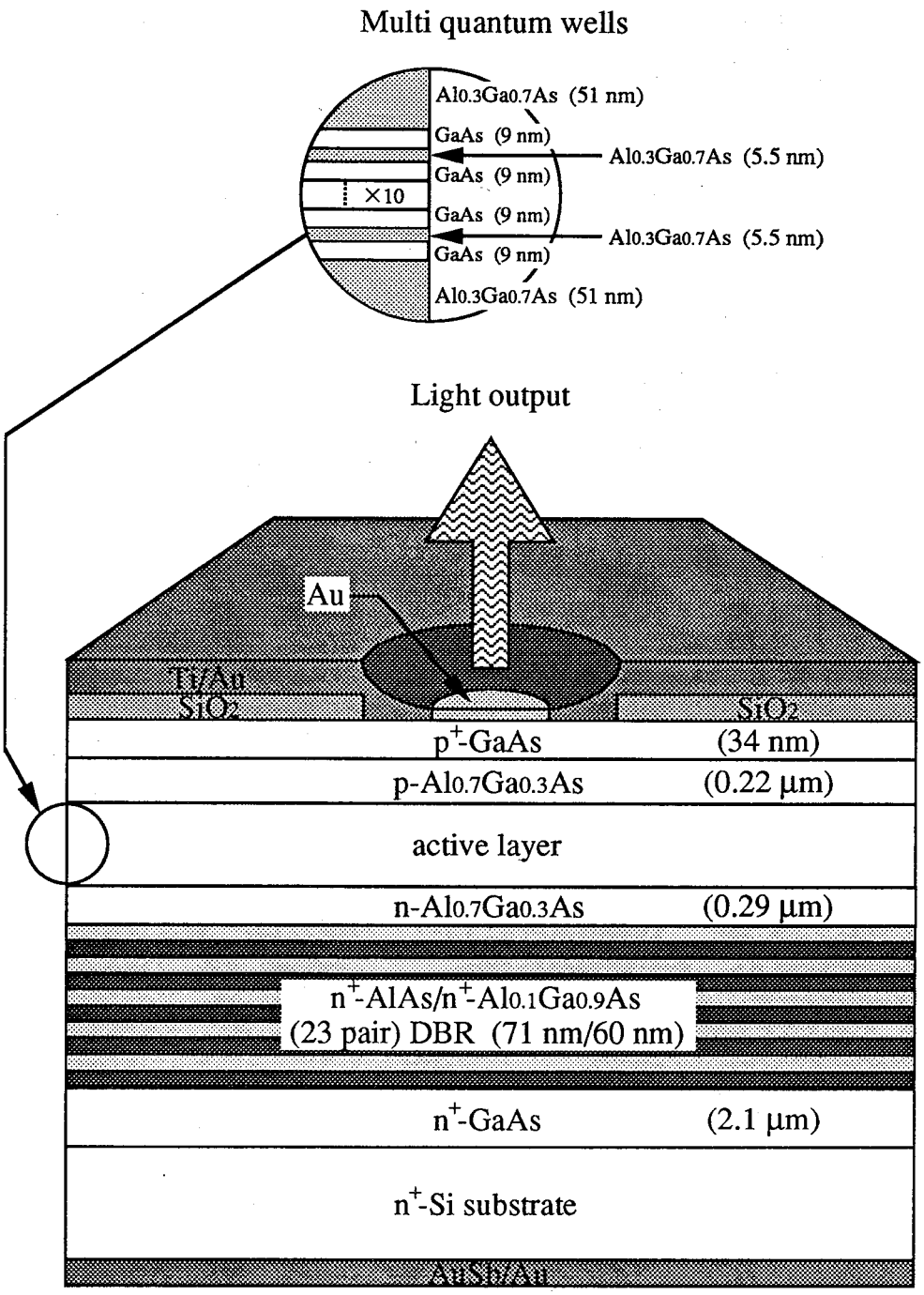


Fig. 5.7. Schematic cross-section of the VCSEL on Si with 23-pair of AlAs/$Al_{0.1}Ga_{0.9}As$ DBR and multi quantum wells active layers.

n-side electrode on the n^+-Si substrate. In this VCSEL on Si, the light output was measured by detecting the light emitted through the 20 μmϕ semitransparent Au.

The measured peak reflectivity of the 23-pair of AlAs/$Al_{0.1}Ga_{0.9}As$ DBR on Si was 94 % at 840 nm. Although a little increase of reflectivity was observed in comparison with the 20-pair of AlAs/GaAs DBR on Si, the reflectivity of 94 % still remains to be much lower than the calculated value of 99.4 % probably due to the large zigzag roughness and the interfacial roughness in the DBR on Si. The top mirror had the reflectivity of 93 % and transparency of 0.6 % for the semitransparent Au.

5.3.2 Lasing Characteristics

Figure 5.8 shows an L-I characteristic and emission spectrum of this VCSEL under cw operation at 100 K. The value of I_{th} was 73 mA, which corresponded to J_{th} of 3.7 kA/cm^2. The η_d was 0.8 %, which is much lower than that of the edge-emitting lasers on Si (for example, Fig. 3.13). This seems to have been caused by the large absorption in the semitransparent Au and the lateral current spreading due to the absence of current confinement structure such as mesa etching[20,32] and ion implantation[33,34]. The FWHM of this spectrum was 39.5 nm at $0.96\times I_{th}$ and 2.2 nm at $1.2\times I_{th}$. The relatively broad FWHM of 2.2 nm may be due to the generation of multi transverse-modes near the single fundamental mode[22]. The peak wavelength at $1.2\times I_{th}$ was 844 nm, which was near the wavelength achieving the peak reflectivity of the DBR. Figure 5.9 shows the polarization of this VCSEL for two perpendicular directions under cw operation at 100 K. It can be seen that the output light was scarcely polarized below I_{th} and was clearly polarized above I_{th}. It has been reported that there is no fundamental polarization

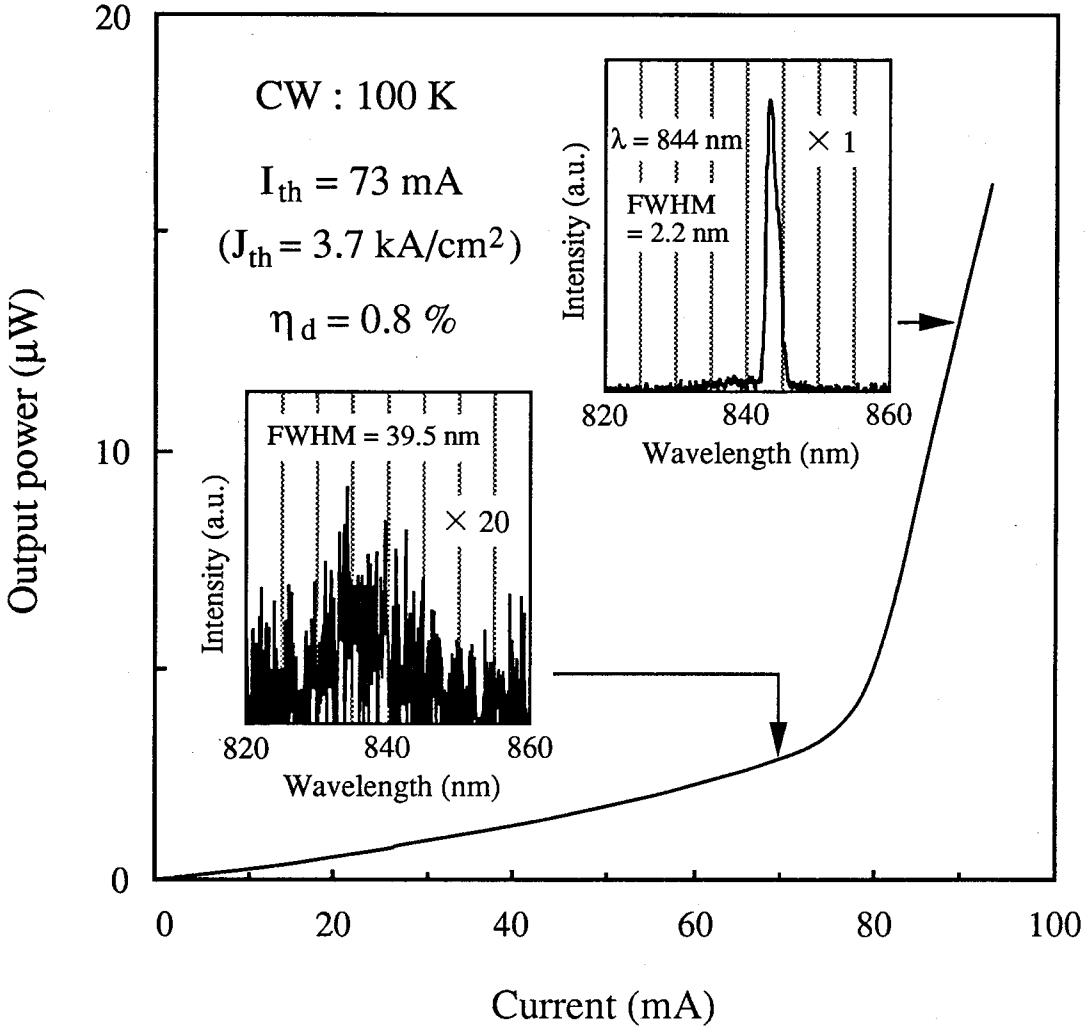


Fig. 5.8. L-I characteristic and emission spectrums of the VCSEL on Si ubder cw conditin at 100 K.

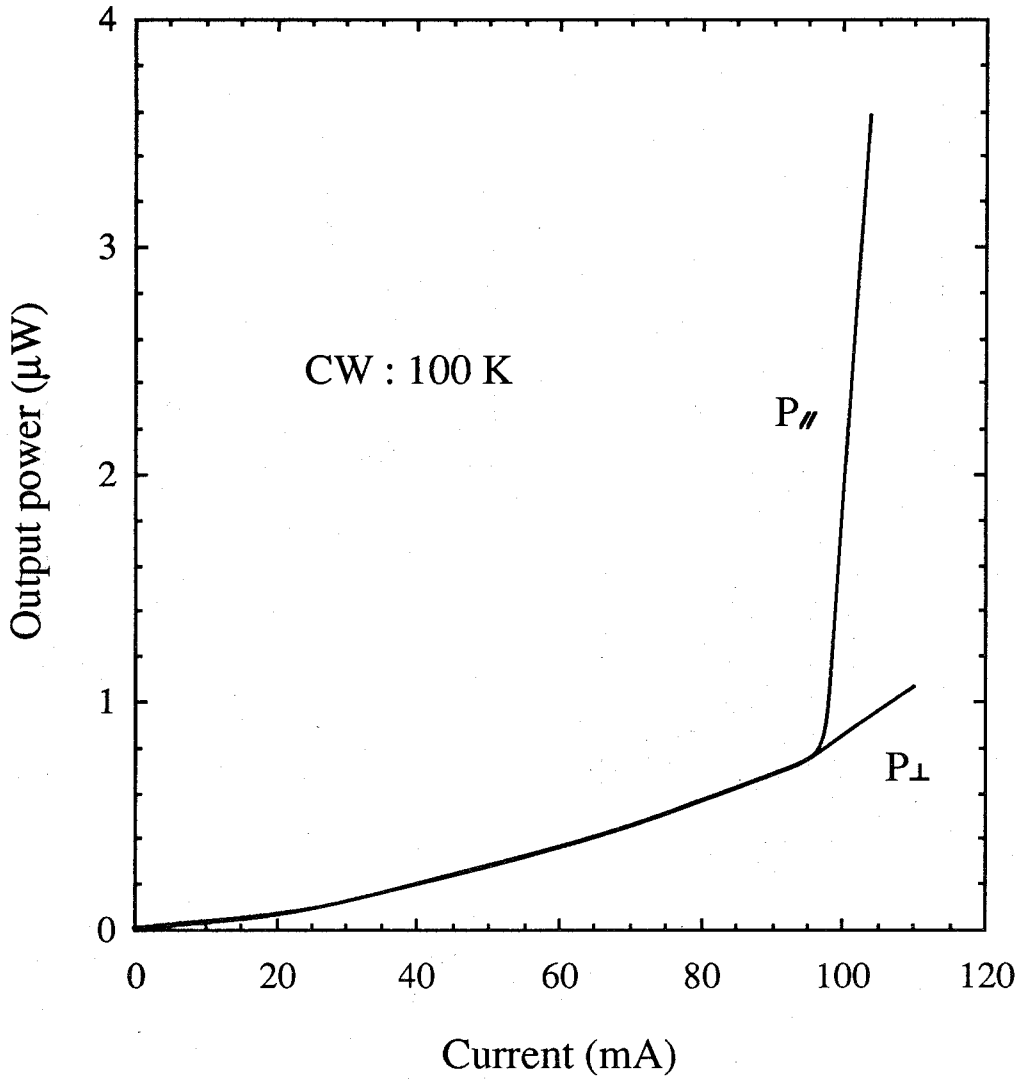


Fig. 5.9. Polarization of the VCSEL on Si for two perpendicular directions under cw condition at 100 K.

selection mechanism for the VCSELs on GaAs substrates with quantum well active layers in contrast to the edge-emitting lasers with quantum wells, and the polarization is probably due to some anisotropy introduced by the processing[35]. Additionally, it has been also reported that the polarization can be controlled by introducing stress[36,37]. These influences for the polarization characteristic observed in the VCSEL on Si are not yet understood. The L-I characteristics operated between 30 and 150 K were also shown in Fig. 5.10. It is found that the I_{th} increased with the increase of temperature. Up to 150 K, this VCSEL on Si could be operated under cw condition. The value of I_{th} was 82 mA (J_{th}=4.2 kA/cm^2) at 150 K. The successful cw operation up to 150 K was believed to have been mainly achieved by the increased gain due to increased N_w. The characteristic of the cw operation is expected to be more improved by the optimum N_w with increasing R_f and R_r from eq. (5.1).

However, this VCSEL on Si showed rapid degradation under cw condition at low-temperature and pulsed condition at room-temperature. The VCSEL degraded very rapidly only in ~1 min under cw condition at 100 K. Figure 5.11 shows a result from the APC aging test of the VCSEL on Si under room-temperature pulsed condition (0.2 μs pulses at 5 kHz repetition rate) at a constant output power of 210 μW. The inset in this figure shows an L-I characteristic of this VCSEL. The values of I_{th} and η_d were 104 mA and 1.8 %, respectively. The I_{th} of 104 mA corresponds to the J_{th} of 5.3 kA/cm^2. As shown in Fig. 5.11, the current increased gradually at a rate of ~30 mA/h in the first 170 min and then the VCSEL showed a rapid increase in current by ~114 mA/h. This rapid degradation under pulsed operation is believed to have been caused by rapid DLD growth due to high injected current density, which has

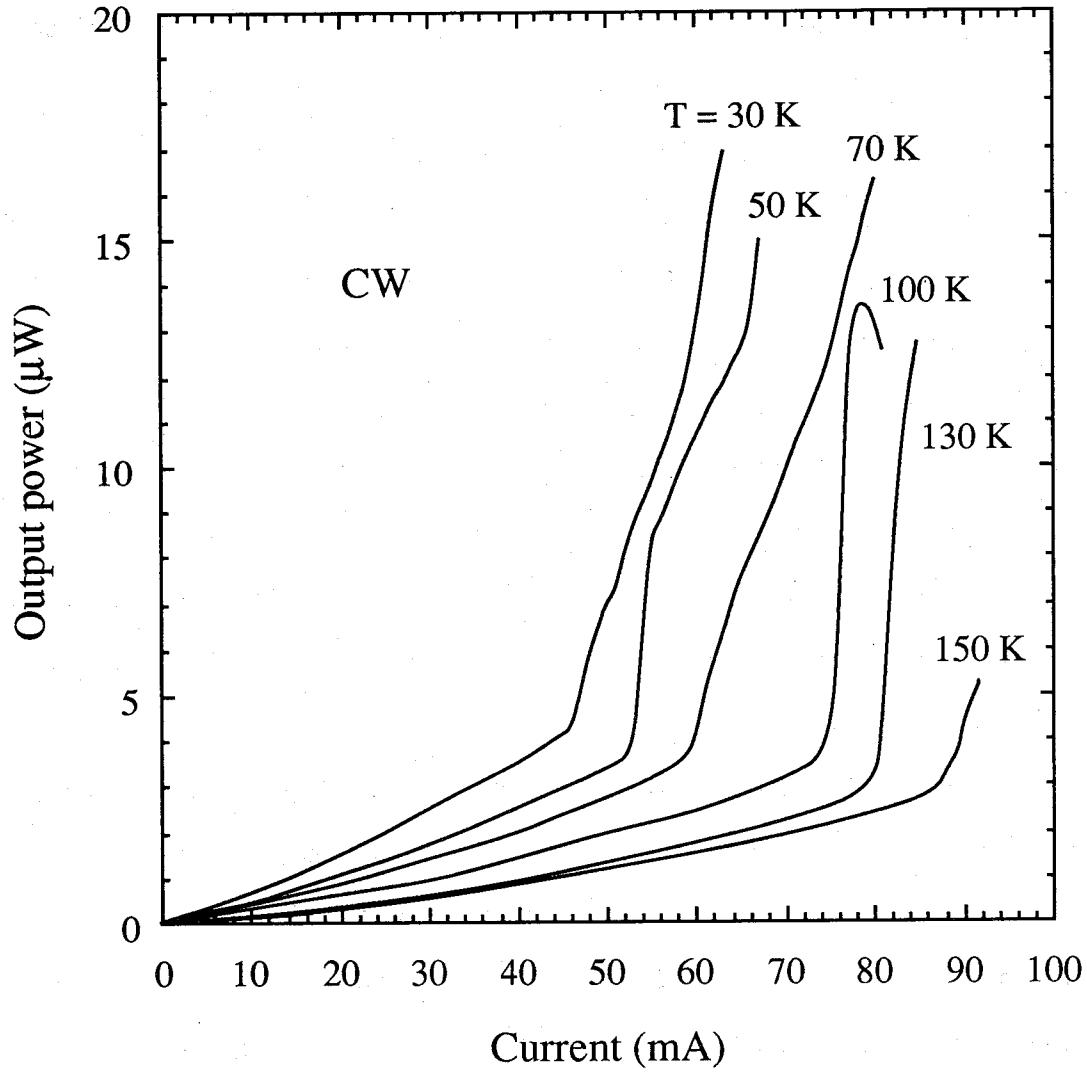


Fig. 5.10. L-I characteristics of the VCSEL on Si under cw condition between 30 and 150 K.

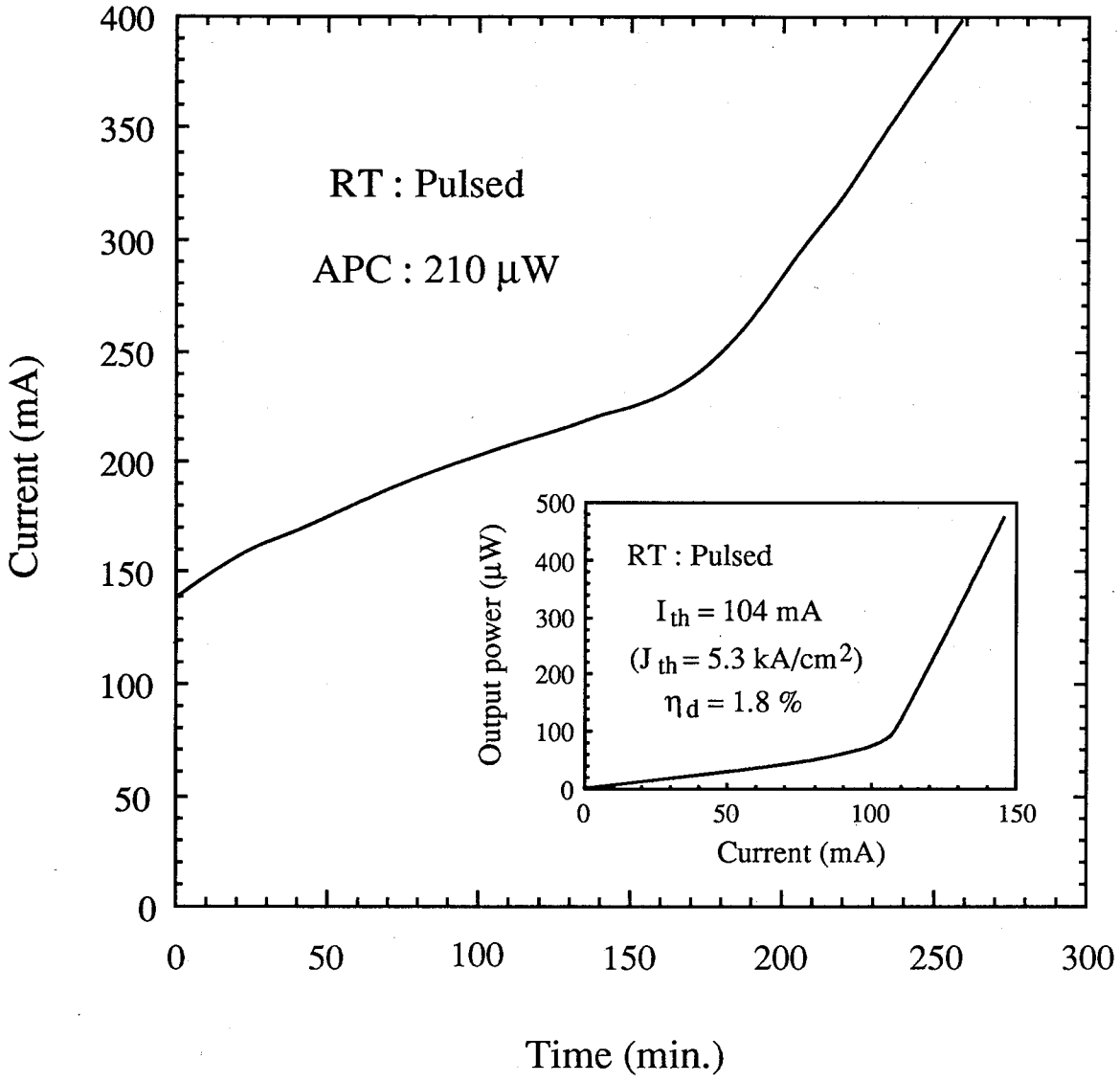


Fig. 5.11. Result from the APC aging test of the VCSEL on Si under pulsed condition at room-temperature. The inset shows an L-I characteristic of this VCSEL.

been shown in Figs. 2.10 and 2.11.

5.4 Conclusions

The room-temperature pulsed operation of the AlGaAs/GaAs VCSEL on Si with the 20-pair of AlAs/GaAs DBR and a SQW active layer was demonstrated. The measured peak reflectivity of the 20-pair of the AlAs/GaAs DBR was 93 % at 860 nm. A TEM observation showed that the AlAs/GaAs DBR is not effective in bending the threading dislocations because there is less mismatch in the lattice constant for the AlAs/GaAs layers. The I_{th} and J_{th} of this VCSEL were 79 mA and 4.9 kA/cm^2, respectively. Furthermore, low-temperature cw operation of the VCSEL on Si with the 23-pair of AlAs/$Al_{0.1}Ga_{0.9}As$ DBR and MQW (N_w=10) active layers was also demonstrated for the first time. Up to 150 K, the VCSEL could be operated under cw condition.

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Chapter 6. Summary

This dissertation has described the studies on GaAs-based light-emitting devices on Si substrates for future OEICs. At first, the observation and understanding of the rapid degradation mechanism of the AlGaAs/GaAs quantum well lasers grown on Si have been carried out. Then, the increasing lifetimes of these lasers have been achieved by both introducing InGaAs intermediate layers and replacing the conventional GaAs active layers with the InGaAs layers. Finally, the novel approaches for improving characteristics of the AlGaAs/GaAs light-emitting devices on Si have been presented. The demonstration of AlGaAs/GaAs VCSELs on Si for OEICs have been also described.

In chapter 1, the background and purpose of this research, and the current status of heteroepitaxial growth of GaAs/Si and device applications were presented.

The results obtained in this research are summarized as follows:

In chapter 2, the influences of DLDs on lasing characteristics and the dependence of the DLD growth velocity on the injected current density for an AlGaAs/GaAs quantum well laser on Si were described. The generation of <100> DLDs caused the decrease of η_i and the slow increase of driving current. At the subsequent rapid degradation stage, the expansion of DLDs caused the remarkable increase of αi and the decrease of β, and finally resulted in the rapid increase of driving current. Additionally, it was also found that the <100> and <110> DLDs growth velocities strongly depended on the injected current density.

In chapter 3, the increased lifetimes of AlGaAs/InGaAs SQW lasers on Si with InGaAs ILs were presented. Furthermore, the

differences of degradation mechanism between AlGaAs/GaAs and AlGaAs/InGaAs lasers on Si were also described. The observation of degree of polarization indicated that the AlGaAs/$In_{0.02}Ga_{0.98}As$ laser on Si with InGaAs IL had a stress-relieved active layer, while the AlGaAs/$In_{0.07}Ga_{0.93}As$ laser on Si with InGaAs IL had a compressive-stress induced active layer. The lifetime of the AlGaAs/$In_{0.02}Ga_{0.98}As$ laser increased to ~85 min under cw condition at room-temperature. The AlGaAs/$In_{0.07}Ga_{0.93}As$ laser also exhibited the increased lifetime of ~105 min. These improvements were caused by the reduction of threading dislocations by use of the InGaAs IL and the reduction of <100> DLD growth velocity due to the dislocation pinning in the InGaAs active layer. Furthermore, a drastic increased lifetime of ~24 h was realized for the post-growth annealed AlGaAs/$In_{0.07}Ga_{0.93}As$ laser, which resulted from the completely suppressed <100> DLD growth and slow <110> DLD growth.

In chapter 4, the improved characteristics of AlGaAs/GaAs light-emitting devices on Si with small active regions were described. The AlGaAs/GaAs quantum wire-like laser on Si with vertically-stacked quasi GaAs quantum wires was successfully fabricated. It was confirmed that the GaAs quantum wires of size (11-15 nm)×(83-127 nm) were grown on a V-grooved GaAs/Si substrate. Furthermore, the AlGaAs/GaAs quantum wire-like laser on Si with a p^+-GaAs current-blocking layer and quasi GaAs quantum wires of (20-21 nm)×(100-260 nm) exhibited extremely low-threshold current of 9.8 mA under pulsed condition at room-temperature. The AlGaAs/GaAs LED on Si with the self-formed GaAs islands active region was also fabricated. The GaAs island size and density could be controlled by the TMG flow rate. At the TMG flow rate of 10 sccm and the time of 6 s, for example, the islands showed the conical shape with the heights of 90-170 nm, the diameters of 600-750 nm and the density of

$1\text{-}2\times10^{7}$ cm^{-2}. The reliability of this LED was much superior to that of an LED on Si with a conventional GaAs quantum well active region, which resulted from the reduction of dislocation numbers and the suppressed DLD growth due to the reduction in the size of the active region. The dislocation numbers in these light-emitting devices on Si with the small active regions could be estimated to be reduced to ~1/100 of that of the devices on Si with the quantum well active regions.

In chapter 5, the AlGaAs/GaAs VCSELs on Si, which are the most promising devices for future OEICs, were presented. The room-temperature pulsed operation was realized for a VCSEL on Si with a 20-pair of AlAs/GaAs DBR and a SQW active layer. The I_{th} and J_{th} of this VCSEL were 79 mA and 4.9 kA/cm^2, respectively. Additionally, 150 K cw operation was achieved for a VCSEL on Si with a 23-pair of $AlAs/Al_{0.1}Ga_{0.9}As$ DBR and MQW (10 quantum wells) active layers.

With further improvements in crystallinity of GaAs/Si grown by heteroepitaxy and device structures, the characteristics such as reliability of the GaAs-based light-emitting devices on Si will be improved significantly. Consequently, the monolithic integration of GaAs-based optical I/O devices with Si-based ULSI chips will be realized in the near future. The results in this study are hopefully expected to give a helpful guidance for the realization of practical GaAs-based light-emitting devices on Si for future OEICs.