

1. Reliability Studies on MOCVD Grown AlGaN/GaN HEMT on Si Substrate

Chapter – I: Introduction

1.1 History of GaN

In 1932, Johnsonn et al. [1] prepared the first gallium nitride (GaN) compounds by reacting ammonia gas with metallic gallium at high temperatures. Almost four decades later in 1969/1970 optical properties of GaN were characterized by Maruska et al. [2] and Pankove et al. [3] where they determined the band gap to 3.39 eV at room temperature. In early 70's, Bloom [4] predicted GaN as a promising material for luminescent devices and laser applications due to its wide direct band energy. Following this in 1973, Ilegems and Montgomery [5] concluded that the presence of native defects in GaN leads to it n-type conductivity which were widely debated. In 1983, Yoshida et al. and Akasaki et al. [6, 7] groups reported, crystalline quality of GaN was improved by inserting AlN nucleation layer to accommodate lattice constant mismatch of sapphire substrate. The first p-n junction LED GaN fabrication in early 90's was reported by Akasaki et al. [8]. During the same period for the first time Khan et al. observed a two dimensional electron gas (2DEG) at the interface between AlGaN and GaN layers [9]. Since then, research on AlGaN/GaN based high electron mobility transistors (HEMTs) of improved performance towards novel applications like high frequency, high power, and high temperature operations were intensively pursued by number of groups [10 – 18]. In RF performance of the GaN HEMTs a recent overview by U. K. Mishra says 13.7 W/mm at 30 GHz, 10.5 W/mm at 40 GHz, and 2.4 W/mm at 60 GHz and the fastest GaN devices today at a cut-off frequency of 220 GHz and a maximum oscillation frequency of 400 GHz [19]. However, GaN based devices have shown a short term and a long term instabilities including current collapse of DC current-voltage (*I-V*) characteristics, and high leakage currents. This urges a

comprehensive reliability studies and it is one of the main purpose of this thesis. It is important to investigate the main cause of GaN HEMT degradation i.e electrical and optical characteristics through detailed investigations from material growth to device fabrication technology.

1.2 Group III-Nitrides

The aluminum nitride (AlN), gallium nitride (GaN), and indium nitride (InN) is the available semiconductor III-nitrides that has a big potential to be used in high power/temperature electronic and optoelectronic devices.

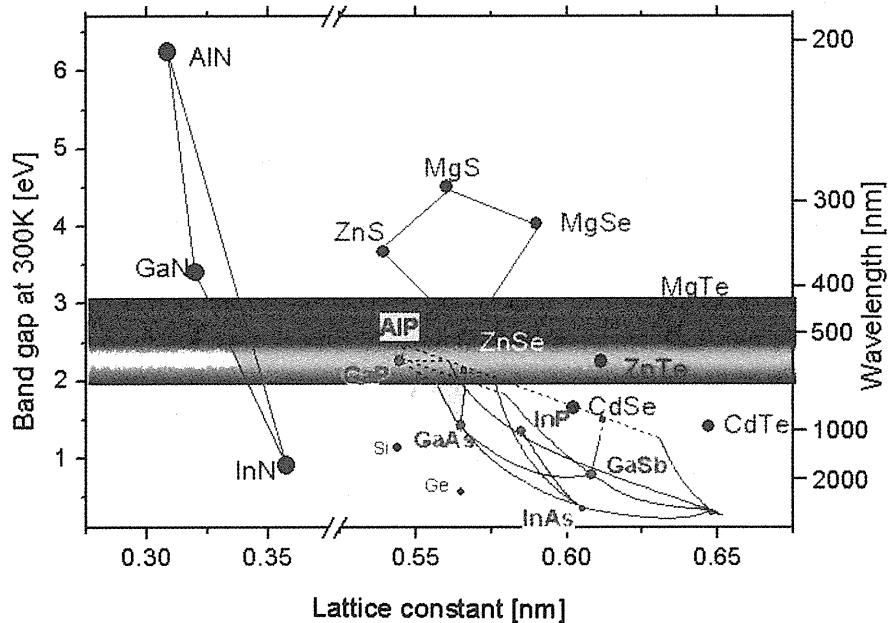


Fig. 1.1 Energy band gap of the most important semiconductors versus their lattice parameter

The energy band gap varies from 0.9 eV for InN through 3.4 eV for GaN to 6.2 eV for AlN as shown in Fig. 1.1. Group III-nitrides can crystallize in three possible crystal structures: wurzite (WZ) structure, zinc-blende and rocksalt structures. The GaN WZ structure has a hexagonal unit cell and is thermodynamically more stable than other structures such as zinc-blende or rocksalt structures [20]. The wurtzite structure has lack of inversion symmetry and displays piezoelectric effect. Ga-N bond is highly polarized

with the electrons located mostly near the nitrogen atom [21]. The most common growth direction of hexagonal GaN is normal to (0001) basal plane [22], where the atoms are arranged in bilayers consisting of two closely spaced hexagonal layers, one with the cations and the other with anions. The crystal surface of GaN can have either Ga-polarity (Ga atoms at the top) or N-polarity (N atoms at the top), depending on the nucleation or substrate on which is the GaN crystal grown [10] (See Fig. 1.2).

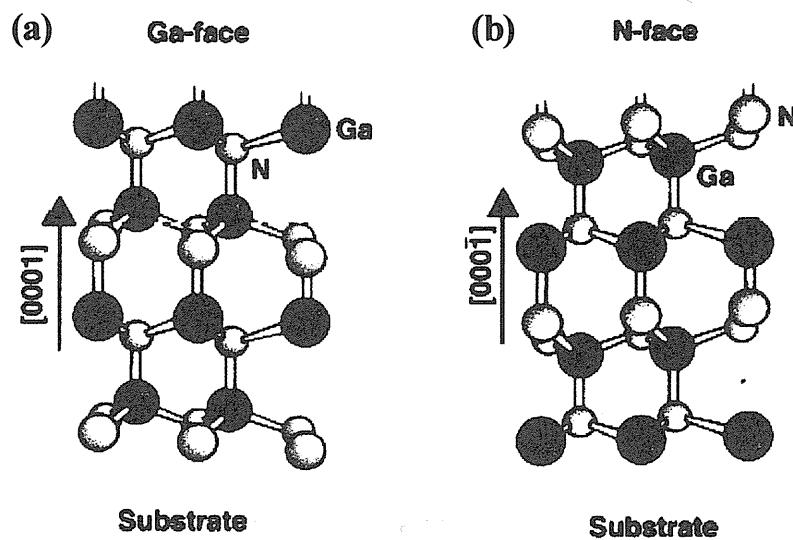


Fig. 1.2. Structure of (a) Ga-faced and (b) N-faced GaN with polarity and charges

The choice of the substrate, nucleation layer and the growth method will subsequently change the polarity of GaN. Polarity plays an important role by growth of heterostructure in the formation of defects and influencing the performance of final devices [23]. GaN has created much interest and investigation among the all other III-nitrides. GaN is an excellent candidate for device operation in high temperature and mordant environment due to its wide energy gap. A resume of these semiconductor parameters is given in Table 1.1 for the commonly used semiconductor technologies. From the data reported in Table 1.1, it is evident that GaN has the highest figure of merit for high power device applications.

Table 1.1 Semiconductors material properties figure of merit

Material Property	GaN	4H-SiC	GaAs	Si
Bandgap energy E_g (eV)	3.49	3.25	1.43	1.11
Breakdown electric field E_{br} (10^6 V/cm)	4	3.5	0.4	0.25
Saturated electric field E_{sat} (10^3 V/cm)	15	25	3	8
Electron Mobility μ^- (cm^2/Vs)	2000	700	8500	1350
Hole mobility μ^+ (cm^2/Vs)	300	120	330	450
Saturation electron velocity v_{sat} (10^7 cm/s)	2.5	2.1	1.3	1
Maximum drift velocity v_d (10^7 cm/s)	3	2	2	1
Thermal conductivity κ (W/cmK)	1.5	4.9	0.56	1.5
Maximum temperature T (°C)	700	600	300	300
Relative dielectric constant ϵ_r	9	10	12.5	11.9
Baliga figure of merit (BFOM = $\epsilon^* \mu^* E_{br}^3$)	24.6	3.1	9.6	1

1.3 Substrates for GaN

The best choice of a substrate for a GaN epitaxial growth and device is only gallium nitride itself. GaN substrate eliminates all problems associated with hetero-epitaxy. Homoepitaxy of GaN to GaN offers good control of polarity, dopant concentration, stress, zero or very low thermal expansion coefficient mismatch and lattice constant mismatch. The main disadvantages with GaN substrates are that they are very expensive and not available in large size. Hence the successful growth of GaN epitaxial layer on foreign substrates is inevitable. In choosing a foreign substrate for the growth of GaN epitaxial layer several factors to be considered like; lattice mismatch, thermal conductivity and cost. The physical properties of various available substrates are shown in Table. 1.2. The growth of GaN based devices on sapphire is not favorable for RF and high power device application due to its poor thermal conductivity. The most favorable GaN substrate for microwave applications is SiC, good in terms of thermal conductivity, low lattice mismatch but very expensive. Si promises advantages over other substrates also especially in possible integration with matured Si electronics.

Table. 1.2 Physical properties of available substrate for the growth of GaN

Substrate for GaN	SiC	Sapphire	Si
Lattice mismatch to GaN [%]	3.5	14.1	17
Thermal expansion [10^{-6} K^{-1}]	5	a: 7.5 c: 8.5	4.08
Thermal conductivity [W/cm.K]	4.9	0.2 ~ 0.5	1.5
Size [inch]	2 ~ 3	2 ~ 4	2 ~ 12
Cost	Very Expensive	Expensive	Low price
Output power	Very good	Moderate	Good
Overall rating	Good	Moderate	Very good

This is due to its availability in large area wafers (12 inches), cheaper than SiC/sapphire substrate, and has a moderate thermal conductivity. Disadvantage is the higher lattice mismatch and high thermal coefficients mismatch which causes strong tensile strain leading to cracks in the growth. But using a system of intermediate and buffer layers nowadays higher quality was achieved and crack free structures have been already grown [24, 25].

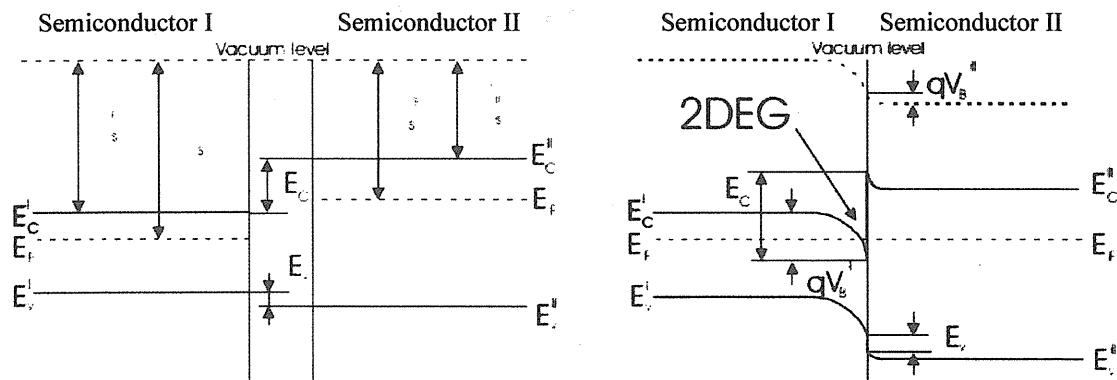


Fig. 1.3. Energy band diagram for wide (I) and narrow (II) band gap semiconductor

1.4 AlGaN/GaN high electron mobility transistors

AlGaN/GaN HEMTs are grown by metal organic chemical vapor deposition in crystal direction (0001) with gallium face surface. A thin AlGaN layer is deposited on top of GaN buffer layer. In general, a heterostructure or heterojunction is formed between two semiconductors with different energy band-gaps E_g , permitivities ϵ_s , work functions $q\phi_s$, and electron affinity χ_s . The energy band diagram of two different semiconductors is shown in Fig.1.3(a). When these two different semiconductors are in contact in the absence of external bias voltage, the equilibrium is reached by lining up the Fermi level and a discontinuity in conduction band and valence band is formed. The discontinuity in the conduction band creates a triangular quantum well, and near to the boundary at the bottom side, the two dimensional electron gas (2DEG) is formed as shown in Fig. 1.3(b).

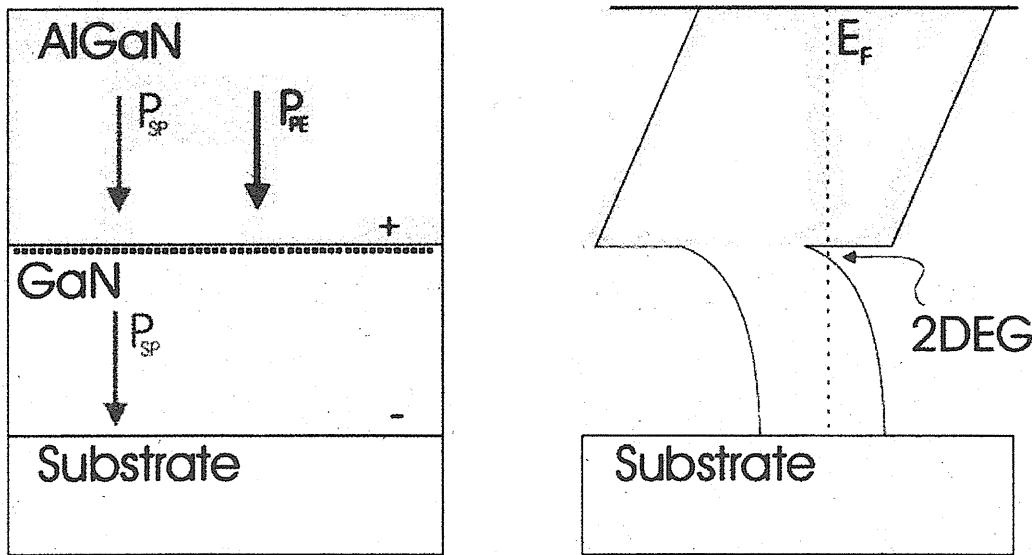


Fig. 1.4. AlGaN/GaN based structure with Ga-polarity. Polarization induced sheet charge density with the direction of the spontaneous and the piezoelectric polarization (left); electron accumulation and formation of 2DEG at the interface (right).

When the wide band gap semiconductor is highly doped then the electrons are separated from the donor atoms and collected as 2DEG channel in the quantum well under the

heterointerface. This separation of electrons drastically reduces the coulomb scattering and leads to a high mobility and a high saturation velocity in the channel [26].

The AlGaN/GaN heterostructure is created when the AlGaN barrier is grown on a relatively thick GaN layer. Due to the difference in band-gap energies, band bending occurs in the upper part of the GaN layer near to boundary and a two dimensional conductive channel is created by electrons. The lack of symmetry along the c-direction and the ionicity of the covalent bond in wurtzite GaN a large spontaneous polarization (P_{SP}) oriented along the hexagonal c-axis occur (Fig. 1.4.). The piezoelectric coefficients of III nitrides (P_{PE}) are almost an order of magnitude larger than in many of traditional III-V semiconductors. Hence, the polarization charge arises from two sources: the difference in spontaneous polarization between AlGaN and GaN and piezoelectric effect by strained AlGaN. The total polarization field of both spontaneous polarization and piezoelectric polarization induces charges in 2DEG at the AlGaN/GaN interface with the high sheet charge density of $\sim 10^{13} \text{ cm}^{-2}$ [27]. It was shown that there is a minimum AlGaN thickness necessary to induce charges in 2DEG and that the Al concentration in the AlGaN layer determines the charge sheet density in the 2DEG channel [28].

1.5 Applications of Gallium Nitride

In the recent decade, GaN is a semiconductor material with attractive physical characteristics for application in high frequency and high power devices as shown in Fig. 1.5. This shows GaN positioning itself as a next generation power semiconductor [29].

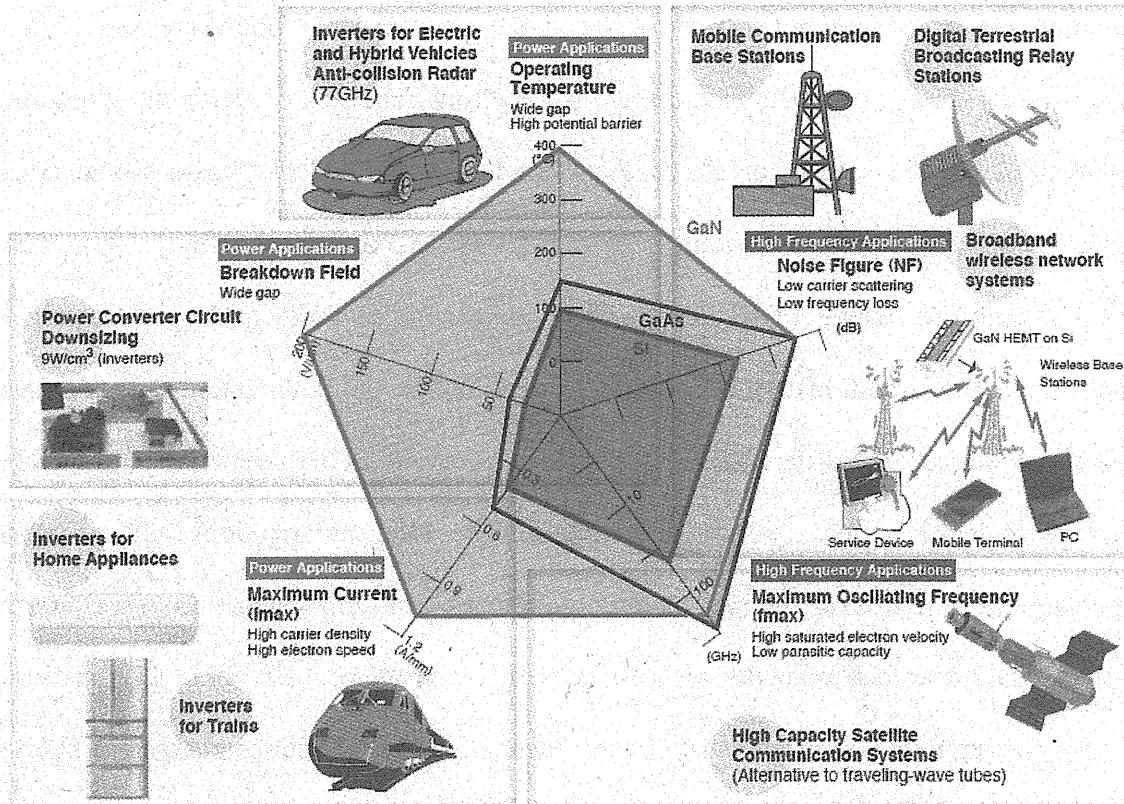


Fig. 1.5. Application areas of GaN based semiconductor

1.6 Reliability issues

In the recent years, GaN HEMTs have been subjected to various optimization processes, starting from the material properties, to the control of surface and buffer properties aimed improving device performance, breakdown voltage, reducing transient phenomenon, the current collapse problems and electrical degradation. Fig. 1.6 depicts critical areas in AlGaN/GaN HEMTs which are related to epitaxial growth quality and process as well. There are possibilities that Schottky and Ohmic contacts degrade and

imperfect passivation layer are responsible for parasitic charging effects which cause dispersion and lagging effects as shown in Fig. 1.6. see (a), (b), and (c).

In designing AlGaN/GaN HEMT device one should pay attention concerning the high electric field (~ 6 MV/cm) under the gate at the drain side which can cause degradation due to inverse piezoelectric effect and generate hot electrons (see (d) and (e) in Fig. 1.6). Localized native defects due to material growth condition, and dislocation mostly due to lattice mismatch between substrate and GaN see (f), (g) in the above fig can also acts as a point for degradation. During cooling down after material growth, resulting in large tensile strain due to the wafer bending. In worse case, thermal mismatch between GaN and substrate is large, even cracks can occur as described in Fig. 1.6. (h).

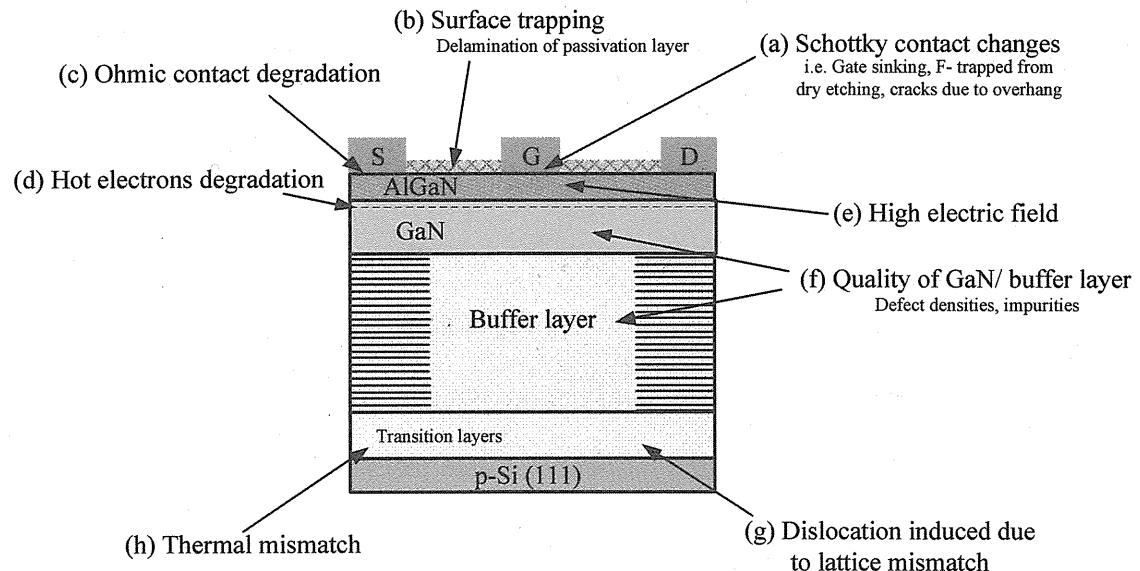


Fig. 1.6. Schematic representation of AlGaN/GaN HEMTs showing critical areas of device degradation

Presently there are two main streams of degradation mechanism explanations: inverse piezoelectric effect [30] and hot electron [31, 32].

1.6.1 Inverse piezoelectric effect

Joh and del Alamo [33] proposed a mechanism, as a result of applied high electric field, additional tensile strain generated in the AlGaN barrier due to the lattice

mismatch between the AlGaN barrier layer and GaN buffer which cause inverse piezoelectric effect. The total strain exceeds beyond crystal elasticity, and consequently crystallographic defects can be created. The electromechanical stress under the gate edge at the drain side during simulation reveals that the maximum electric field opens the possibility for electron injection and inverse piezoelectric effect [34]. Moreover several authors have reported that reduce in strain in the AlGaN barrier leads to improved device reliability [35-38].

1.6.2 Hot electron effect

By definition hot electrons are electrons with higher energy than the lattice thermal energy. They can get kinetic energy from the high electric field when the device is turned on. Hot electrons may be trapped on the device surface, in the AlGaN barrier or in the buffer giving rise to the reversible degradation and they can also generate traps thus promoting further charge trapping [31]. Some of the results discussed by various authors are addressed below

Kelvin probe experiments show the degradation involves surface of AlGaN changes the surface potential of gate-drain region, with accumulation of negative charge [39]. Jha et al. [40] have studied the influence of gate recess depth, formed by reactive ion etching, on hot electron degradation in GaN HEMTs. They concluded that a drastic increase in the interface trap density at the AlGaN/GaN heterointerface resulted from the hot electron stressing measurement. Another mechanism induces an early degradation of I_{DS} ; the larger the recess, the faster the degradation.

Valizadeh and Pavlidis [41] have studied adopting noise measurements to study the effect of DC and RF stress on AlGaN/GaN HEMTs: they concluded that hot electron trapping is responsible for the observed degradation in both DC and RF tests. Coffie et

al. [42] observed a negative activation energy for the degradation of output power in varying the junction temperature from -55 to 205 °C and concluded that hot carrier induced degradation is the dominant degradation mechanism. It should be stressed, however, that there is no agreement on this topic in the literature, and that many authors have reported thermally activated degradation of GaN HEMTs with positive activation energies $\sim 1.05 - 2.0$ eV.

1.7 Research objective and thesis outline

Although much technological advancement has been achieved in AlGaN/GaN HEMT performance, device reliability is still a bottle neck to its wide deployment. As of now there were only few reliability studies carried out on AlGaN/GaN HEMT on Si substrate. In this research study, we have carried out systematic reliability studies on AlGaN/GaN HEMT on Si with various buffer thicknesses to understand the device failure mechanisms. This thesis will be organized as following:

In Chapter 2, the details of MOCVD growth, HEMTs device fabrication process, HEMT device characterization and stress methodology of GaN HEMTs were discussed. In Chapter 3 degradation experiments and their results were discussed. First, comparison studies on AlGaN/GaN HEMT grown on thin and thick buffer thicknesses were carried out. Electroluminescence measurements were performed to detect the early degradation. In Chapter 4, DC step-stress experiments were carried out at different bias conditions for AlGaN/GaN HEMT grown on thick buffer was presented. Electrical and surface characterizations together with three terminal breakdown voltages were performed to get insight into respective degradation modes. Chapter 5 presents the relationship between the GaN stress and the threshold voltage shift. Finally Chapter 6 summarizes the conclusions of this dissertation.

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Chapter-II: Growth, device fabrication and characterization

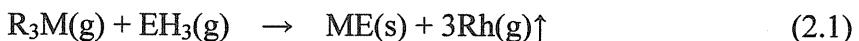
2.1 MOCVD growth method

Recently GaN and its alloys have led to the demonstration of very impressive results in electronic devices for high-power and high frequency applications due to their direct and wide band gap energy. In recent years, a remarkable progress in the development of GaN epitaxial growth techniques has been done. The most popular methods used for GaN epitaxial growth are Hydride vapor phase epitaxy (HVPE) [1-4], Molecular beam epitaxy (MBE) [5-11], and Metal organic chemical vapor deposition (MOCVD) [4-6, 12]. HVPE is a simple growth technique which offers high growth rate and quasi bulk GaN layers: it is one of the oldest techniques used for GaN growth. MBE can produce high-quality layers with good control of thickness, doping, composition and abrupt interface. Nevertheless, the disadvantages are very expensive, applicable for low temperature growth only and need ultra-high vacuum. The most widely embraced technique for the high quality growth of GaN in recent years is the MOCVD method. The MOCVD has produced the highest quality of GaN based devices till date.

Amano et al., is the first one to report on successful MOCVD growth of high quality III-N films by employing an RF-heated atmospheric pressure reactor [13]. Later, Nakamura et al., have described high quality GaN films produced in a two-flow atmospheric pressure MOCVD (AP-MOCVD) system [14]. Recently, low pressure MOCVD (LP-MOCVD) has also been used to grow high quality III-N films [15].

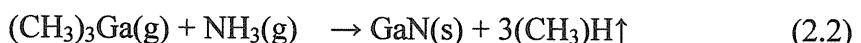
The detailed nature of chemical reactions occurring during the MOCVD growth of III-N films has begun to be elucidated [16]. The specific reaction kinetics and detailed thermo-dynamics are strong functions of the precursors and substrate employed, as well as the growth pressure, temperature, carrier gas, and reactor geometry.

Hydrodynamics can also play a strong role in the final results of growth experiments. This is especially true for the nitrides as a result of the high growth temperatures generally employed. The general reaction for III-V binary compounds growth described by the following equations [4,16]:

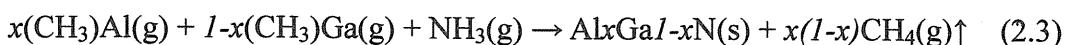


Where R is organic radical, typically CH_3 or C_2H_5 , M is a column III metal atoms, Ga, Al or In. and E is a column V atoms, in this case N.

The simple column III metal alkyls (methyl and ethyl derivatives) are most often the precursors selected for the growth of III-N compound semiconductors since they have reasonably high vapor pressures and can readily delivered using H_2 carrier gas and source temperatures conveniently near room-temperature. The most commonly used source for GaN is Trimethyl gallium (TMGa) and Ammonia (NH_3). An extremely important consideration in the growth of high quality epitaxial device structure is the purity of the sources.



Ternary alloys such as AlGaN and InGaN can be obtained by combining TMAI or TMIn simultaneously with TMGa as described in equation (2.3). Adjusting the gas-phase composition of the TMAI and TMGa or the TMIn and TMGa controls the solid composition.



However, the exact control of the composition of the film (x) obtained in such reactions strongly depends on the experimental conditions. Doping of GaN in MOCVD has been done by using Silicon [16-18], Germanium, Sulphur, Selenium, and Tin for n-type and Magnesium [19-20] and Zinc [7] for p-type.

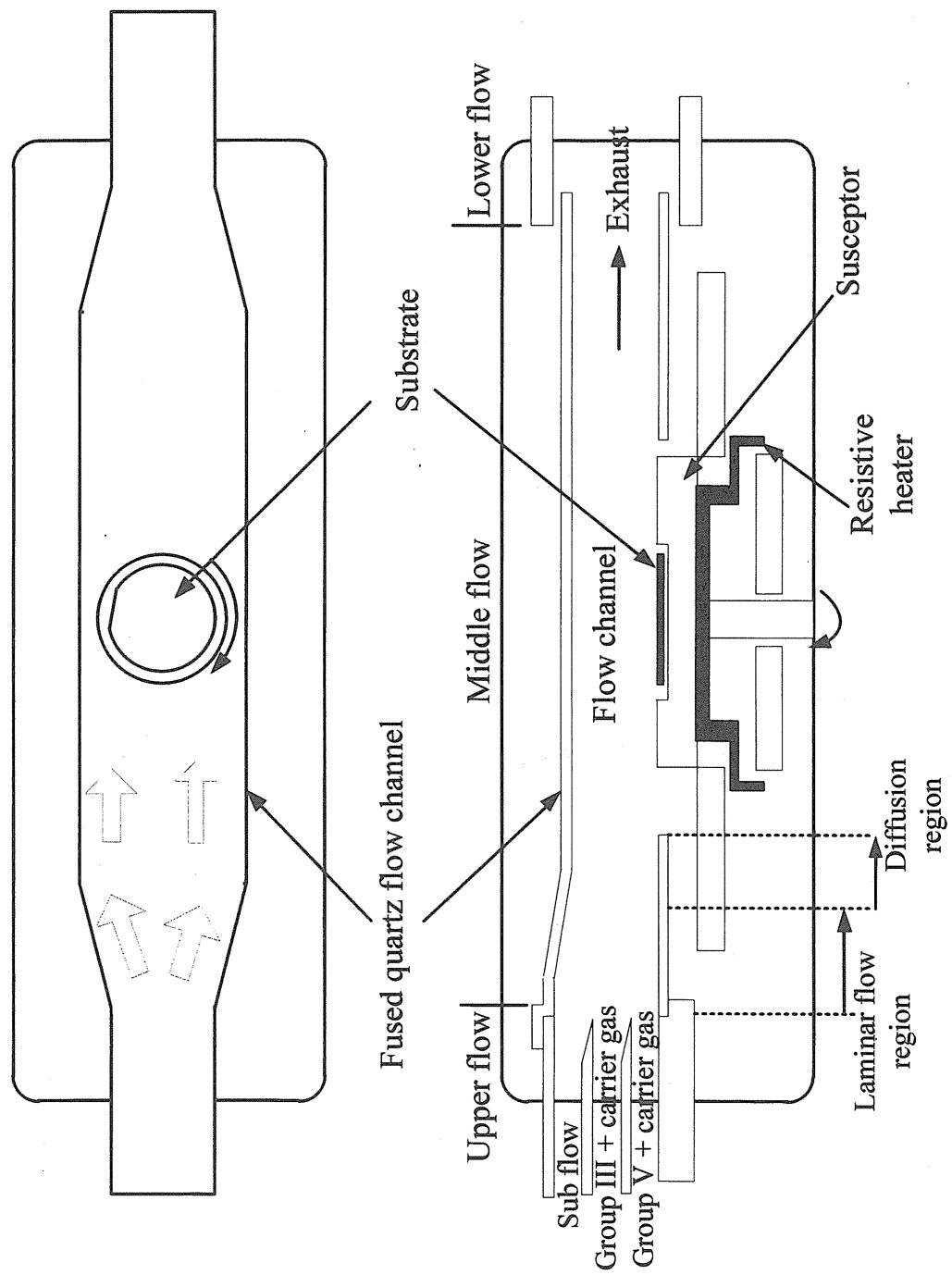


Fig. 2.1. Schematic drawing of the laminar flow channel of horizontal MOCVD reactor

Dopants can be transported to reactor through hydrides or organometallics. SiH₄ or Si₂H₆, Cp₂Mg are the most common n-type and p-type dopants of GaN. In our lab, Taiyo Nippon Sanso MOCVD growth machine was used which has a three-layer flat flow technology that yielded the growth with the acceptable quality. Figure 2.1 shows a laminar three-flow MOCVD reactor. The flow liner made of quartz glass is installed in a stainless steel chamber. A thin restricted gas flow liner is adopted in order to suppress thermal convection, which may cause the reduction of growth rate, uniformity, and film quality. In order to suppress undesirable gases reactions, the shape of the flow linear was carefully designed to achieve high velocity gas flow. In this MOCVD system, NH₃ and its carrier gas, mixture of group III element organometallics and their carrier gas and top flow inert gas are separately injected, as shown in Fig. 2.1. The upstream region of the flow liner has a three stage structure and through these regions the gases injected via the three nozzles that formed into laminar flows. Diffusion of the organometallics starts at the edge of the isolation plate and growth starts at a downstream region of the reactor. In this flow liner, the concentration of organometallics near the substrate gradually increases along the stream. The total gas flow and the flow balance of the three injected gases are very crucial since it can really affect the uniformity, growth rate, alloy composition, and dopant concentration. The wafer is heated by a carbon resistance heater up to 1200 °C. In order to avoid uncontrolled or unwanted dissociation of ammonia (NH₃) on other surfaces than the solution and corrosion of the furnace interior, electrically insulating ceramic PBM (Pyrolytic Boron Nitride) is used as the heater. The more stable material in direct contact to the melt is this pyrolytic boron nitride whereas other material like quartz glass, graphite, glassy carbon, silicon nitride, or aluminum nitride can be corroded by

the melt and thus can cause pollution in the solution with unwanted impurities.

2.2 Structural and optical characterization

This section describes the main methods to characterize the structural and optical properties of the sample. Though various characterization methods available we carried out X-Ray diffraction (XRD), Hall measurement, Raman spectroscopy, and Atomic Force Microscope (AFM). All these techniques present the advantage of being non destructive.

2.2.1 X-Ray diffraction

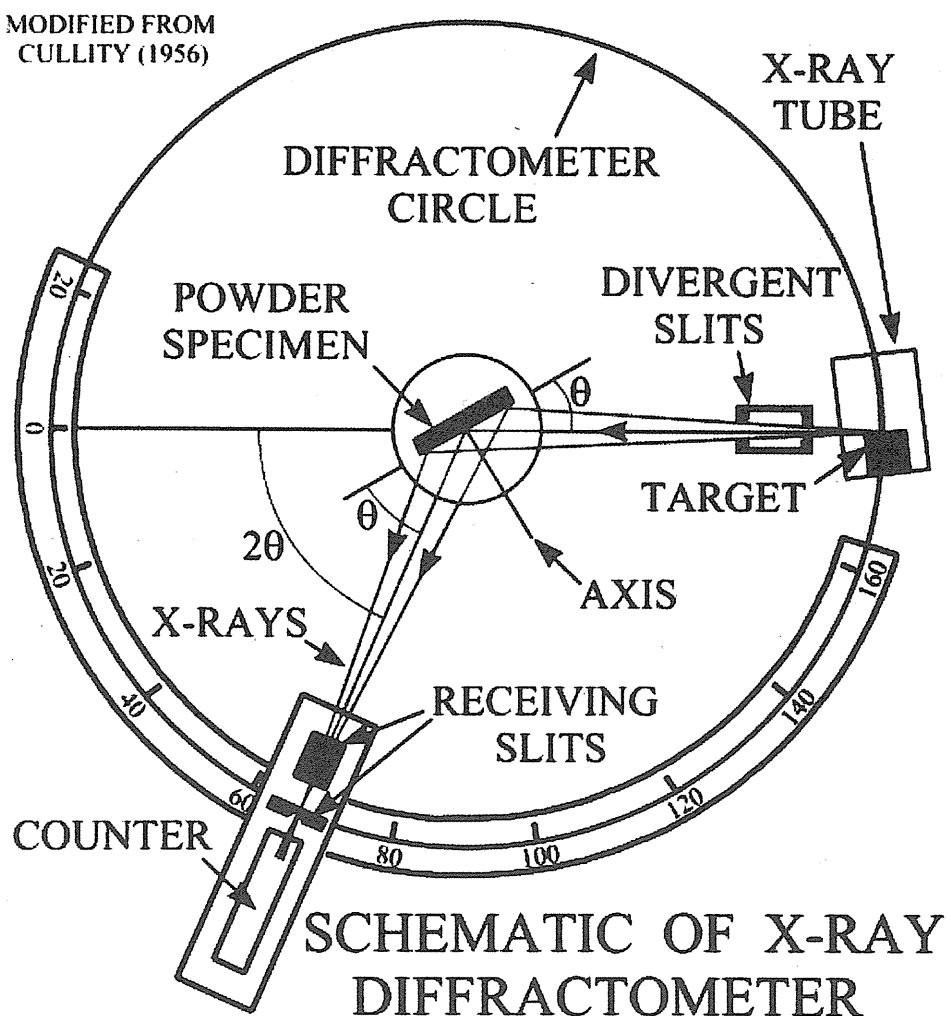


Fig. 2.2. Basic concept of an X-Ray diffractometer

The XRD has been widely used to probe the crystalline quality of the samples to verify their crystalline orientation, to identify the epitaxial relationships and to determine the lattice parameters. An X-ray beam impinges on the sample and is diffracted by a selected plane family [21]. The X-ray diffraction method is employed for measuring the threading dislocation density in GaN thin films. We use Philips X'pert X-ray diffractometer to study our MOCVD grown AlGaN/GaN epi-structure crystal quality from high-resolution X-ray rocking curve (HR-XRC). The ω -scan can directly influence by the line defect densities which in turn affects the FWHM line width. Figure 2.2 shows the pictorial representation of X-Ray diffraction unit.

2.2.2 Hall measurement

The importance of the Hall effect is supported by the need to determine accurately carrier density (n), electrical resistivity (R), and the mobility (μ) of the carriers in semiconductors. The Hall effect provides a relatively simple method for doing this, because of its simplicity, low cost, and fast turnaround time. It is an indispensable characterization technique in the semiconductor industry and in research laboratories.

The basic principle underlying the Hall Effect is the Lorentz force [22], which is a combinatory of two separate forces: the electric force and the magnetic force. When an electron moves along the electric field direction perpendicular to an applied magnetic field, it experiences a magnetic force $-qv \times B$ acting normal to both directions. The direction of its magnetic force can be determining by using the right hand rule convention. With an open hand, the fingers are pointed along the direction of the carrier velocity and curled into the direction of the magnetic field. The magnetic force direction on an electron is then determined by the opposite direction that the thumb is pointing.

The resulting Lorentz force F is therefore,

$$F = -q(E + VB) \quad (2.4)$$

Where, q is the elementary charge which is 1.602×10^{-19} C, E is the electric field, V is the particle velocity, and B is the magnetic field.

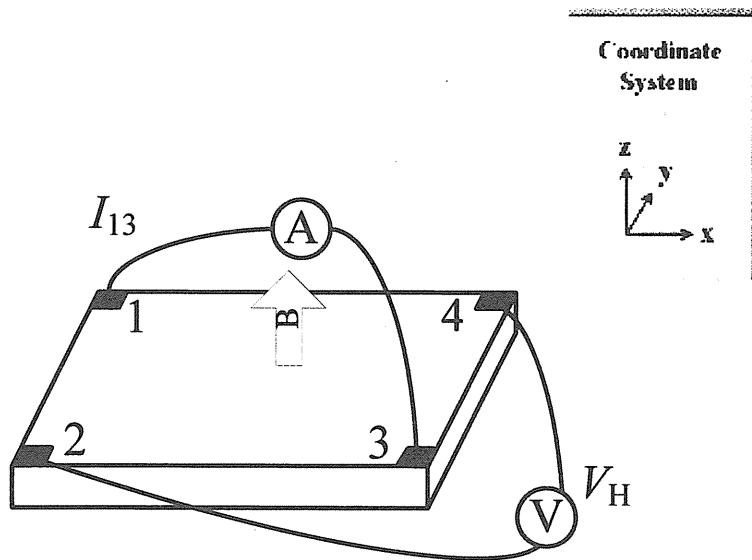


Fig. 2.3. Principle of Hall measurements

The Hall measurement consists of a series of voltage measurements with a constant current I and a constant magnetic field B applied perpendicular to the plane of the sample. The sample shown in Fig. 2.3 represents the Hall measurement method. To measure the Hall voltage V_H , a current I is forced through the opposing pair of contacts 1 and 3 and the Hall voltage $V_H (= V_{24})$ is measured across the remaining pair of contacts 2 and 4. Once the Hall voltage V_H is acquired, the sheet carrier density n_s can be calculated from the known values.

$$n_s = \frac{IB}{qV_H} \quad (2.5)$$

2.2.3 Raman Spectroscopy [23-25]

The scattering of light which is nothing but the redirection of light that takes place when an incident light ray encounters an obstacle, in our case scattering of material (Solid, liquid, gas). As this incident light ray interacts with the matter, the electron orbits with the constituent molecules are agitated periodically with the same frequency (ω) as the electric field of the incident ray. The agitation of electron cloud results in a periodic separation of charge within the molecules, which is called an induced dipole moment.

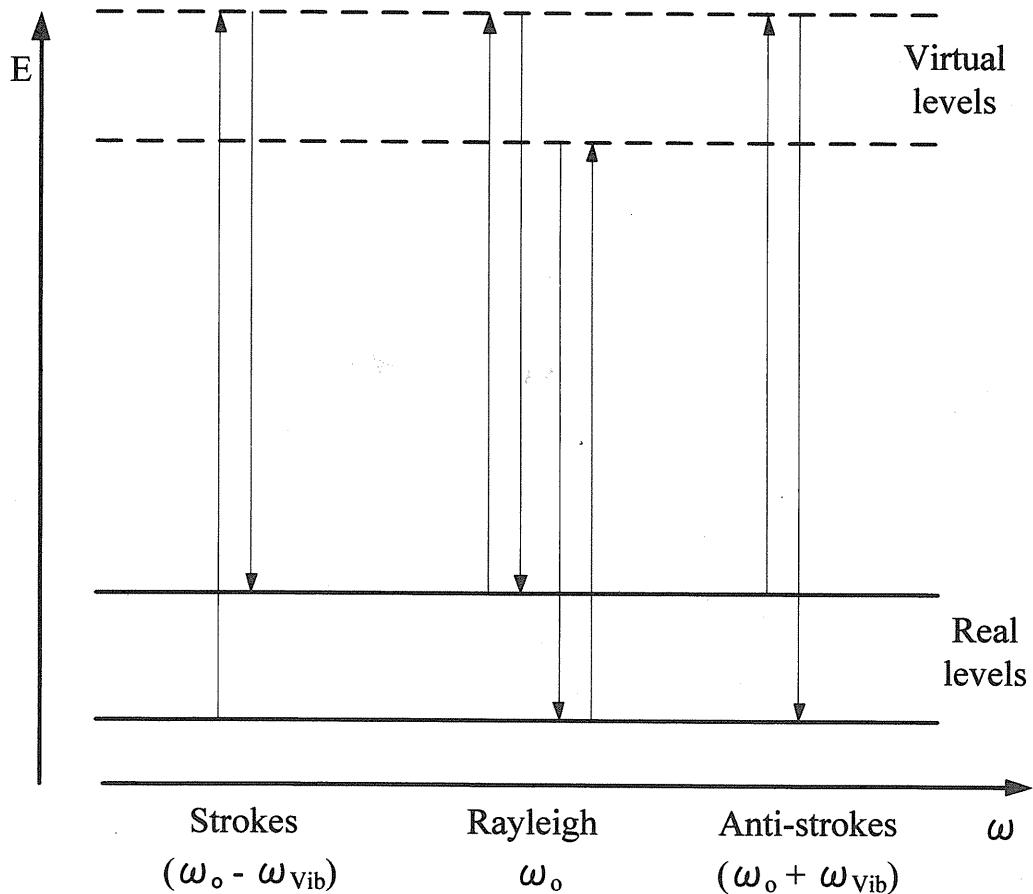


Fig. 2.4. Energy level diagram showing the state involved in Raman signal

In general, there are two types of scattering available i.e. elastic scattering and inelastic scattering. When the majority of light scattered is emitted at the identical

frequency (ω_0) of the incident light ray is called elastic scattering. Whereas additional light is scattered at different frequencies called inelastic frequency. The Fig. 2.4. shows the induced dipole moments are created at three distinct frequencies, namely ω_0 , $\omega_0 - \omega_{vib}$, and $\omega_0 + \omega_{vib}$, which results in scattering radiation at these same three frequencies. The first scattering frequency corresponds to the incident frequency, hence it is elastic scattering (Rayleigh), while the other two frequencies are shifted to lower or higher frequencies and are therefore inelastic scattering process.

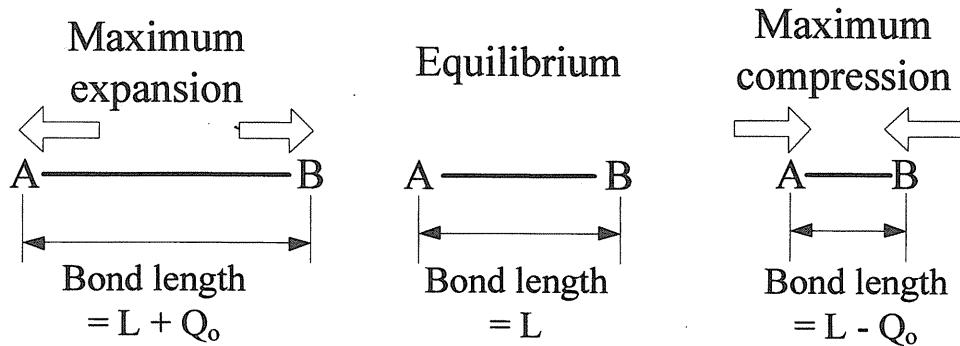


Fig. 2.5. Vibrational displacement of A-B about the equilibrium position

The scattering light in these cases is referred to as Raman scattering, with the down-shifted frequency referred to as Stokes scattering, and up-shifted frequency referred to as anti-stroke scattering. C. V. Raman was the first to describe this type of inelastic scattering, for which he was awarded the noble prize in physics in 1930. It has to be noted that the vibrational displacement of atoms corresponding to a particular vibrational mode results in a change in the polarizability and hence the necessary condition for Raman scattering is that the term $\frac{\partial\alpha}{\partial Q}$ must be non-zero.

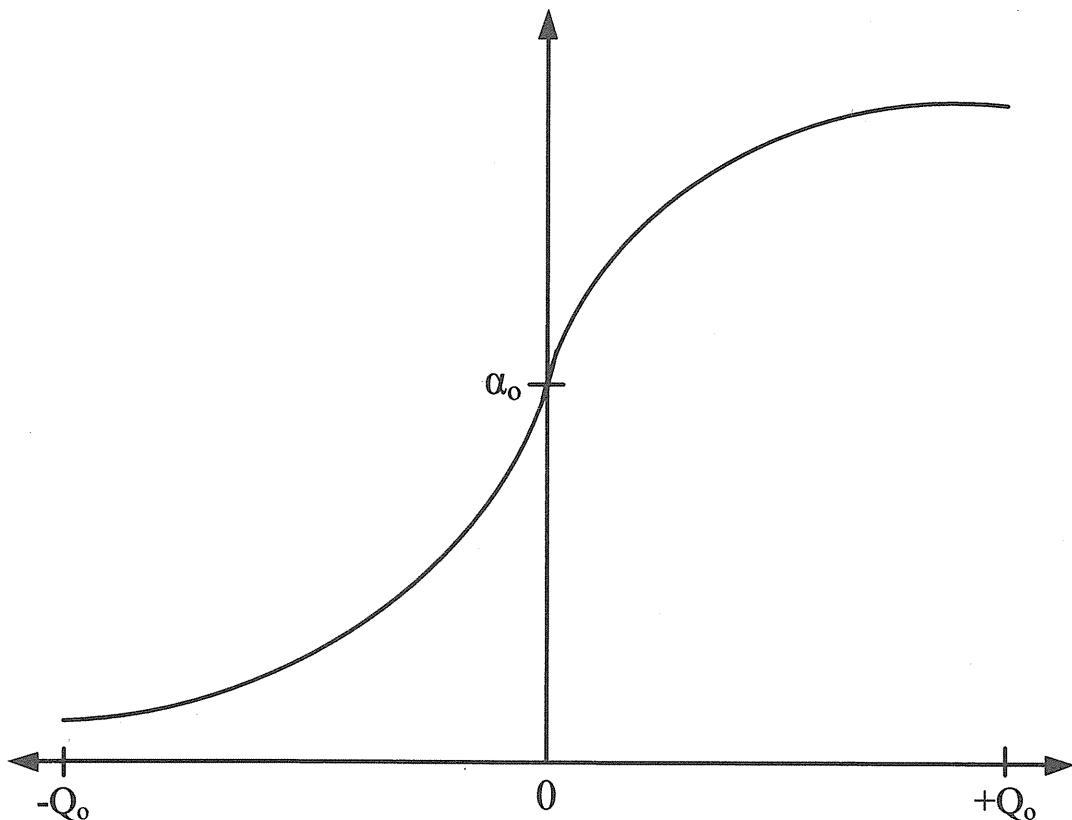


Fig. 2.6. Polarizability of A-B as a function of vibrational displacement about equilibrium

For example, let us consider a diatomic molecule A-B, with the maximum vibrational displacement Q_0 as shown in the Fig.2.5. When A-B is at maximum expansion, the electrons are more readily displaced by an electric field due to the greater separation from the other atom. Hence the polarizability is increased for maximum bond length. In contrast, when A-B is at maximum compression, the electrons from a given atom feel the effects of the other atom's nucleus and are therefore not agitated as much. Therefore, the polarizability is reduced for minimum bond length. It is apparent that the ability to agitate the electron cloud by an incident electric field will depend on the relative position of the atoms. It is apparent from the Fig.2.6 that the value of $\frac{\partial\alpha}{\partial Q}$ about the equilibrium position (at $dQ = 0$) is non-zero, hence the fundamental

vibrational mode of the diatomic molecule A-B would be Raman active and would generate inelastically scattered light at the two frequencies $\omega_0 - \omega_{vib}$, and $\omega_0 + \omega_{vib}$.

2.2.4 Atomic Force Microscope [26]

The atomic force microscope (AFM) is a combination of the principles of the scanning tunneling microscope (STM) and the stylus profilometer (SP). The SP has much in common with the STM. The tip in the STM and the stylus in the SP are both used to scan the surface, sense the variations of the sample, and generate three-dimensional images. The AFM consists of a cantilever with a sharp tip (probe) at its end that is used to scan the specimen surface. The cantilever is typically silicon or silicon nitride with a tip radius of curvature on the order of nanometers. When the tip is brought into proximity of a sample surface, force between the tip and the sample surface lead to a deflection of the cantilever according to Hooke's law.

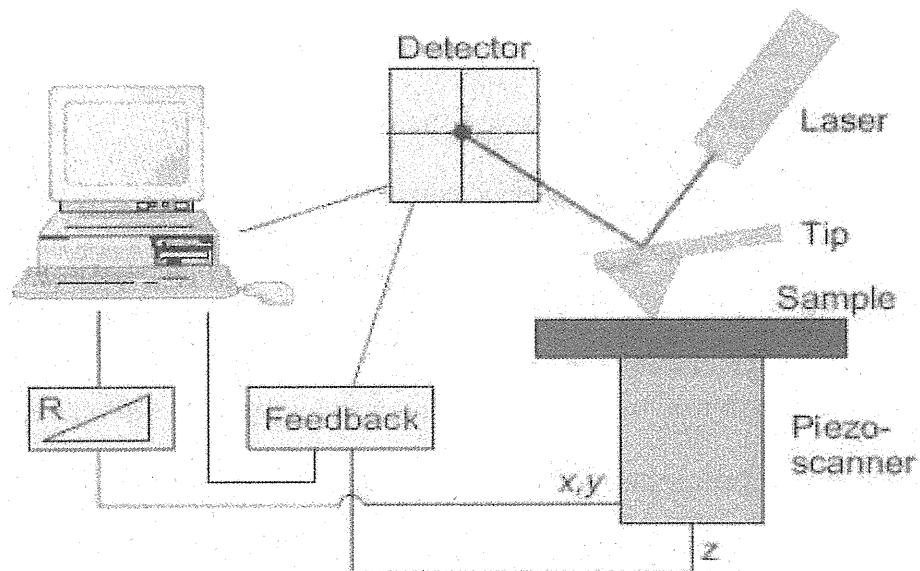


Fig. 2.7. Schematic representation of an AFM setup

Along with the force, additional quantities may simultaneously be measured through the

use of specialized types of probes. Typically, the deflection is measured using a laser spot reflected from the top surface of the cantilever into an array of photodiodes. Figure 2.7 shows the typical setup of AFM. The AFM can be operated in a number of modes, depending on the application. In general, possible imaging modes are divided into contact mode and non-contact mode where the cantilever is vibrated. In contact mode, the static tip deflection is used as a feedback signal. Because the measurement of a static signal is prone to noise and drift, low stiffness cantilevers are used to boost the deflection signal. However, close to the surface of the sample, attractive force can be quite strong, causing the tip to “snap-in” to the surface. Thus static mode AFM is almost always done in contact where the force is repulsive. In non-contact mode, the tip of the cantilever does not contact the sample surface. The cantilever is instead oscillated at either its resonant frequency or just above where the amplitude of oscillation is typically a few nanometers down to a few picometers [26]. The van der waals forces, which are strongest from 1 nm to 10 nm above the surface or any other long range force which extends above the surface acts to decrease the resonance frequency of the cantilever. This decrease in the resonant frequency combined with the feedback loop system maintains a constant oscillation amplitude or frequency by adjusting the average tip-to-sample distance. Measuring the tip-to-sample distance at each (x,y) data point allows the scanning software to construct a topographic image of the sample surface.

2.2.5 Electroluminescence spectroscopy

The creation of excess electron-hole pairs by photon absorption. Eventually, excess electrons and holes recombine, and in direct band gap materials the recombination process may result in the emission of a photon. The general property of light emission is referred to as luminescence. Electroluminescence is the process of

generating photon emission when the excitation of excess carriers is a result of an electric current caused by an applied electric field [27-30]. We will be mainly concerned with injection electroluminescence, the result of injecting carriers across a p-n junction. The light emitting diode and the p-n junction laser diode are examples of this phenomenon. In these devices electric energy, in the form of a current, is converted directly into photon energy. Electron and holes created by impact ionization can recombine radiatively, giving rise to the so called electroluminescence. EL spectroscopy is a sound diagnosis of impact ionization to probe both the localized and the energy distribution of carriers versus bias conditions.

2.3 AlGaN/GaN high electron mobility transistor fabrication process

The fabrication of HEMT is classified into five major divisions particularly structure design, mesa etching, device passivation, ohmic contact, and gate metallization. AlGaN/GaN epistructure grown on Si substrate with various buffer thicknesses were taken and diced into small pieces for the HEMT process. The Fig. 2.8. shows the schematic representation that involves various stages in the HEMT process.

2.3.1 Photolithography

Photolithography is the process of transferring geometric shapes on a mask to the surface of a silicon wafer. The steps involved in the photolithographic process are

- ◆ Surface preparation (wafer cleaning)
- ◆ Coating (Spin casting)
- ◆ Pre-bake (Soft bake)
- ◆ Alignment/ Exposure
- ◆ Development
- ◆ Post- bake (Hard bake)

◆ Post process cleaning

2.3.1.1 Surface preparation or Wafer Cleaning

The wafers are chemically cleaned to remove particulate matter on the surface as well as any traces of organic, ionic, and metallic impurities. Initially organic cleaning were done using ultrasonic bath and hot water bath. The sample was immersed in organic solvents acetone and propanal for 5 min on each. Then these samples were rinsed with de-ionized water and dried by blowing N₂. This cleaning will remove all the dirt and unwanted particle that affects the quality of the process.

2.3.1.2 Photoresist coating

A thin, uniform coating of photoresist (PR) at a specific, well controlled thickness is accomplished by the seemingly simple process of spin coating. The PR is poured onto the wafer/sample, which is then spun on a turntable at a high speed producing the desired film. Stringent requirement of thickness control, uniformity, and low defect density has to be given much attention in this process, where a large number of parameters can have significant impact on PR thickness uniformity and control. There is a choice between static dispense or dynamic dispense, spin speeds and times, and accelerations to each of the spin speeds. The volume of the resist dispensed, properties of the resist, and the substrate play an important role in the resist thickness uniformity. Further, practical aspects of the spin operation, such as exhaust, temperature, humidity control, and spinner cleanliness often have significant effects on the PR. In our case, after organic cleaning, a photoresist was applied using a spin coater. The spin coating was carefully done and the samples were baked in dry oven at 90 °C. There are two types of PR: positive and negative. In positive resist, the PR is exposed with the UV light wherever the underlying material is to be removed. In these resists, exposure to the

UV light changes the chemical structure of the resist so that it becomes more soluble in the developer. The exposed resist is then washed away by the developer solution, leaving windows of the bare underlying material. In other words, “whatever exposed, removed”. The mask, therefore, contains an exact copy of the pattern which is to remain on the wafer.

Negative resist behave in just the opposite manner. Exposure to the UV light causes the negative resist to become polymerized and more difficult to dissolve. Therefore, negative resist remains on the surface wherever it is exposed, and the developer solution removes only the exposed portions. Masks used for negative photoresist therefore, contains the inverse of the pattern to be transferred.

2.3.1.3 Soft-bake or Pre-bake process

After PR coating, the resulting film will contain 20 – 40 % by weight solvent. The soft-bake involves drying the photoresist after spin coat by removing this excess solvent. Reducing the solvent content is to stabilize the changing properties of the film with time. By baking the PR, majority of the solvent is removed and the film becomes stable at room temperature. The removing of solvent from a PR film give four major effects.

1. Film thickness is reduced
2. Post-exposure bake and development properties are changed
3. adhesion is improved, and
4. film becomes less tacky and thus less susceptible to particulate contamination

Typically pre-bake or soft-bake process leave between 3 to 8 percent residual solvent in the PR film, sufficiently small to keep the film stable during subsequent lithographic processing. There are several methods that can be used to bake PR. The most obvious

method is an oven bake.

2.3.1.4 Mask alignment and exposure

One of the most important steps in the photolithography process is mask alignment. A mask or photomask is a square glass plate with a patterned emulsion of metal film on one side. The mask is aligned with the wafer, so that the pattern can be transferred onto the wafer surface. Each mask after the first one must be aligned to the previous pattern. Once the mask has been accurately aligned with the pattern on the wafers surface, the photoresist is exposed through the pattern on the mask with a high intensity ultraviolet light.

2.3.1.5 Development

The last steps in the photolithographic process are development. Once exposed, the PR must be developed. Normally aqueous bases are used as a developer to remove the photoresist. Development is undoubtedly one of the most critical steps in the PR process. The characteristics of the resist developer interactions determine to a large extent the shape of the photoresist profile and more importantly the linewidth control.

2.3.1.6 Post-bake

The post-bake is used to harden the final resist image so that it will withstand the harsh environments of implantation or etching.

2.4 Fabrication process procedure

2.4.1 Mesa-isolation etching

Initially the samples are cleaned under ultrasonic vibration (45 cycles/min) by soaking in organic solvents namely acetone (CH_3COCH_3) and 2-proponal ($(\text{CH}_3)_2\text{CHOH}$, consecutively for 5 min each. This is followed by rinsing with the deionized water and dried using N_2 . The cleaned samples were then uniformly coated with the photoresist polymer solution (S1800) using a spin coater and then baked at 90°C in a dry oven for 20 min. the baked and cooled samples are then one by one set up appropriately under the isolation area aligned using mask aligner subjecting to optimal UV light exposure. This is followed by developing the exposed samples using the suitable developer solution (MF319). The post-bake was done at 90 °C for 30 min. Then immediately dry (plasma) etching was carried out inside a chamber by BCl_3 based reactive ion etching (RIE) under the following conditions: pressure = 3 Pa, power = 10 watts, reflection of the sample holder = 0, and BCl_3 flow rate = 10 sccm. The etching duration was 30 min, which approximately removes 200 nm until the underlying GaN buffer layer is reached.

2.4.2 Device passivation

After the mesa-isolation, organic cleaning was done again and additionally HCl cleaning was done for 1 min. The sample was then loaded into a evaporation chamber set up for depositing SiO_2 using electron beam evaporation technique. The thickness of SiO_2 deposited was 100 nm at a constant substrate temperature of 150 °C. The SiO_2 deposition was carried out at an evaporation rate of 0.4 ~ 0.6 Å/sec, with the chamber vacuum in the order of $6 \sim 9 \times 10^{-3}$ Pascal in order attain a uniform passivation film.

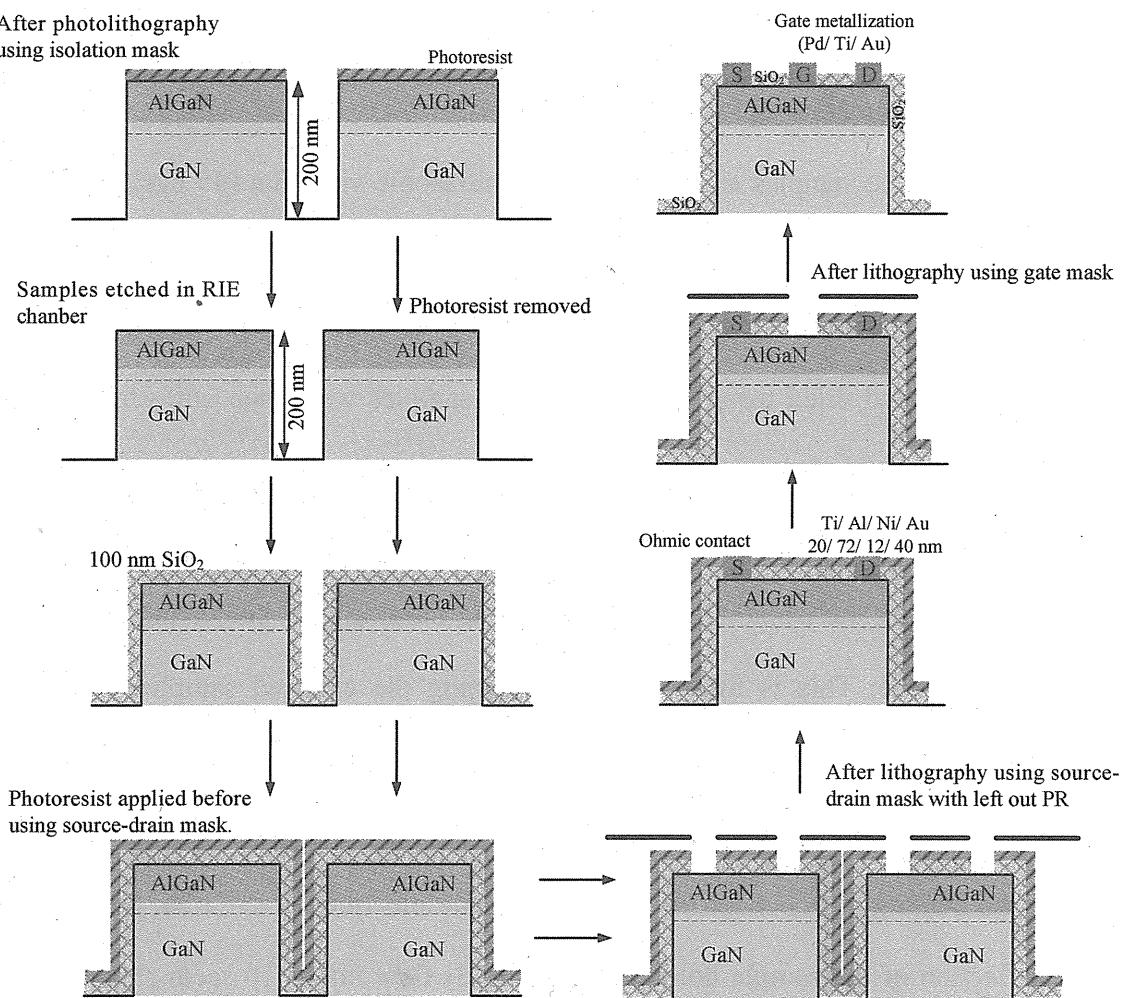


Fig. 2.8. The detailed flowchart of AlGaN/GaN HEMT process

2.4.3 Ohmic metal contact and alloying

These SiO_2 passivated samples are once again prepared for ohmic mask alignment following the same photolithography procedure as mentioned above. After post bake has done, wet etching were carried out using buffered HF solution ($\text{HF} - 2 \text{ ml} + \text{CH}_3\text{COOH} - 14 \text{ ml} + \text{NH}_4\text{F} - 40 \text{ ml}$) until for an optimum time (15 to 30 sec) in order to etch and remove SiO_2 passivation in the ohmic region alone. Again HCl cleaning were carried out before loading the samples into metallization chamber. The sample then has been loaded into metallization chamber for depositing Ohmic metal stack ($\text{Ti}/\text{Al}/\text{Ni}/\text{Au} - 15/72/12/40 \text{ nm}$) consecutively under optimal pressure. Once the

evaporation has been completed lift-off is done to remove the underlying patterned photoresist thereby defining the source and drain contact pads on the sample.

Rapid thermal annealing (RTA) was carried out on these samples for the formation of ohmic contact i.e source drain contact – metal alloying, radiation hardening, and recovering the electrical properties of the devices damaged by the earlier plasma assisted etching process. The annealing temperature for GaN-on-silicon substrate samples is 850 °C. The annealing was carried out for 30 seconds and then allowed to cool gradually until the room temperature is reached.

2.4.4 Schottky gate metallization

Again these samples went through another photolithography process finally for gate contacts. After gate finger formation, the SiO_2 was etched using buffer etchant followed by 1 min HCl cleaning. The samples were loaded immediately after HCl cleaning into the metallization chamber for depositing gate contact metal stack. The gate metal stacks used are Pd/ Ti/ Au - 40/ 20/ 60 nm.

2.5 Basic device characterization

The main parameters, some basic terms, important for evaluation of HEMT device will be described in this section. The basic geometrical parameters of HEMTs are gate width (W_g), gate length (L_g), source to drain spacing (L_{sd}), gate-source distance (L_{sg}), and gate-drain distance (L_{gd}). The drain current flowing through the device is directly proportional to the gate width. Dimension L_g is critical in determining the maximal frequency limits of the device. Therefore for low current, low noise application relatively small gate width devices are utilized and for power applications, large gate width devices are used.

A good power device is that which allows switching as large current as possible,

on and offing across as large load resistance as possible; to obtain the maximum output power across this load resistance. Therefore to sustain maximum current available from the device and the voltage swing is desired. In GaN based HEMTs due to the large values of the access resistance, the maximum drain current is not velocity limited but field limited hence the $n_s \cdot \mu$ product is more important than the $n_s \cdot V_{sat}$ product. The 2DEG channel provides the high carrier density and high carrier mobility as a consequence of the strong polarization field present in the GaN system.

A typical DC current- voltage ($I-V$) output characteristic of an AlGaN/GaN HEMT on Si substrate is shown in Fig. 2.8. The drain current is plotted against the drain voltage for various fixed gate voltages. We can divide the output characteristics into three main regions: linear region where the drain voltage is small and I_D is proportional to V_D ; the Non-linear region and the saturation region where the current remains essentially constant and is independent of V_D .

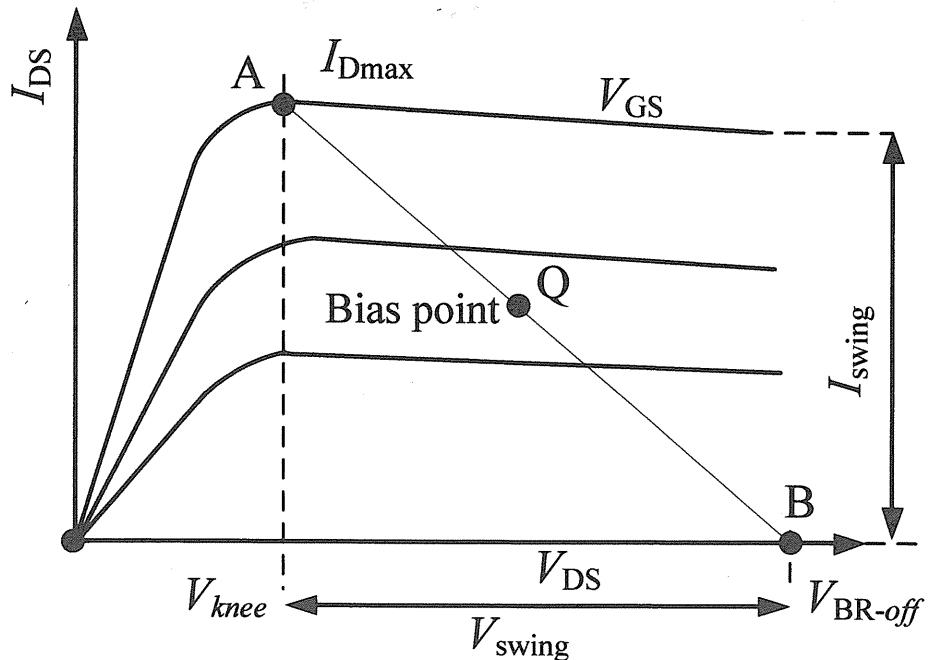


Fig. 2.9. Illustration of operation points on $I-V$ curves of microwave power amplifiers

The onset drain voltage in the non-linear region is referred to as knee voltage (V_{knee}) and the corresponding drain current density is maximum (I_{Dmax}). The I_D is typically depicted proportional to channel width W_g , so it is given in [mA/mm]. As the gate bias becomes more negative, both the saturation current and the corresponding saturation voltage decrease. The locus of $I_{Dsat} - V_{Dsat}$ is shown in the Fig. 2.8. In such devices both high current densities and high drain voltage are available and explain the large power capacity. The I_{Dmax} , V_{knee} , and the breakdown voltage can be measured to estimate the maximum output power in class-A operation.

$$P_{out} = \frac{I_{Dmax} (V_{BV,Off} - V_{knee})}{8} \quad (2.6)$$

Threshold voltage (V_{th}) is the gate source voltage necessary to stop the current in the device by totally depleting the 2DEG channel from mobile carriers.

$$V_{th} = V_{FB} + 2\psi_B + \frac{\sqrt{2\varepsilon_s q N_A (2\psi_B)}}{C_{ox}} \quad (2.7)$$

The ability of the gate to modulate the current flow between the source and the drain is expressed by the transconductance g_m defines as

$$g_m = \frac{\partial I_{Dsat}}{\partial V_{Dsat}} \quad (2.8)$$

2.6 Stress test methodology

In this thesis, we have focused on DC reliability studies on AlGaN/GaN HEMT on Si substrate. Figure 2.10 shows some typical approaches to stressing at fixed temperature, which shows the so called stress measurement approach, in which the parameter of interest such as voltage, current or RF power is stepped in some mode, either monotonically or with a recovery period in between. Stress recovery cyclic type

of experiments in which stress is followed by a recovery period is performed to study the degradation of the device and how it recovers from the degradation. In this type of experiment, a specific stress bias is applied in the stress phase, and this stress is removed in the recovery phase while the device is characterized.

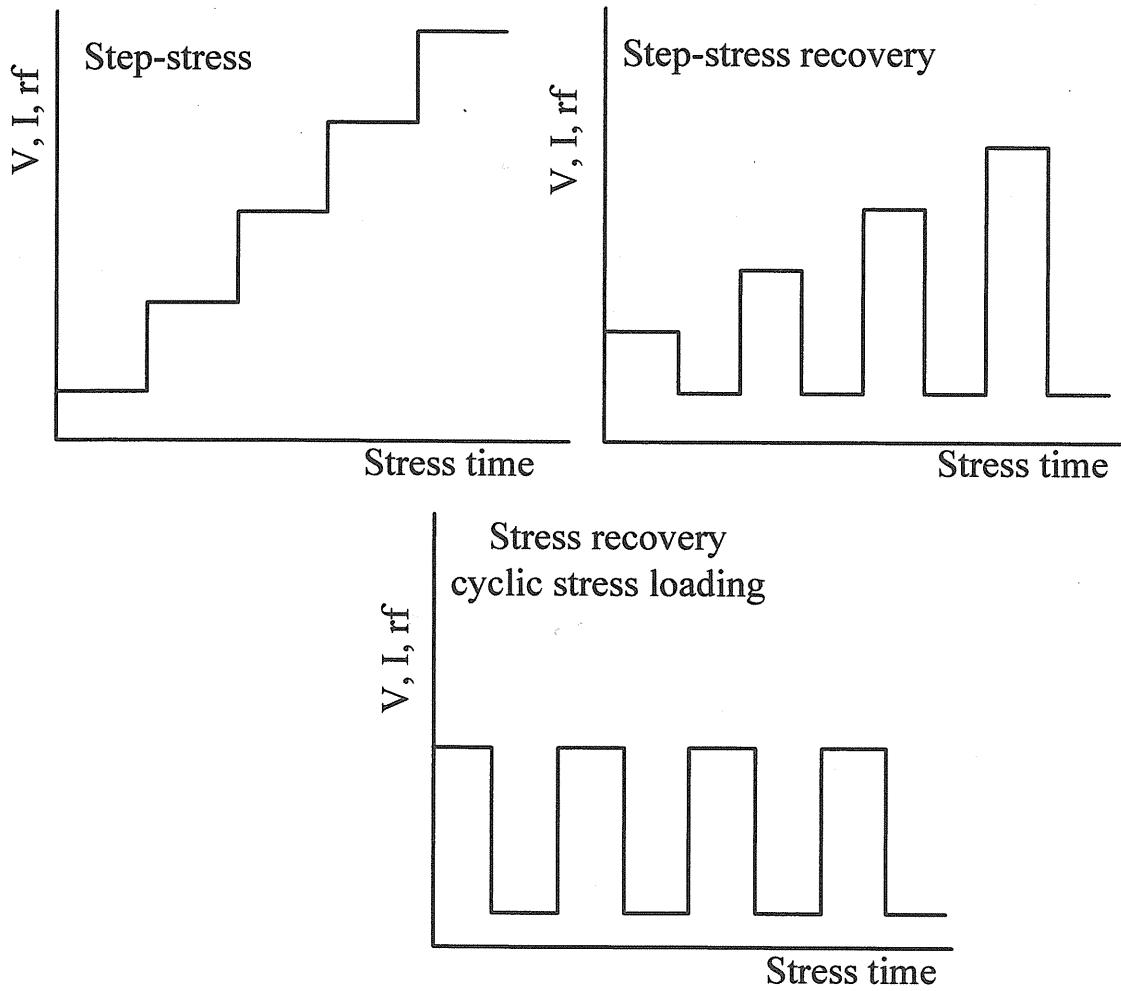


Fig. 2.10. Examples of typical time-dependence of stressing protocols for III-V electronic devices. The parameter is varied with time with voltage, current, RF power and others.

In step-stress experiment, the strength of the stress parameter either voltage or current is stepped up with the regular interval of smaller value to larger value in a single device. From this measurement, a great insight into physical degradation mechanism

can be addressed. Combining the above two method the step stress recovery experiments can also be studied. In this thesis we mainly focus on step-stress measurement. Under this step-stress measurement there are various stress condition available namely; Off-state bias stress, On-state bias stress, $V_{D\text{-stress}} = 0$ state, and high power state.

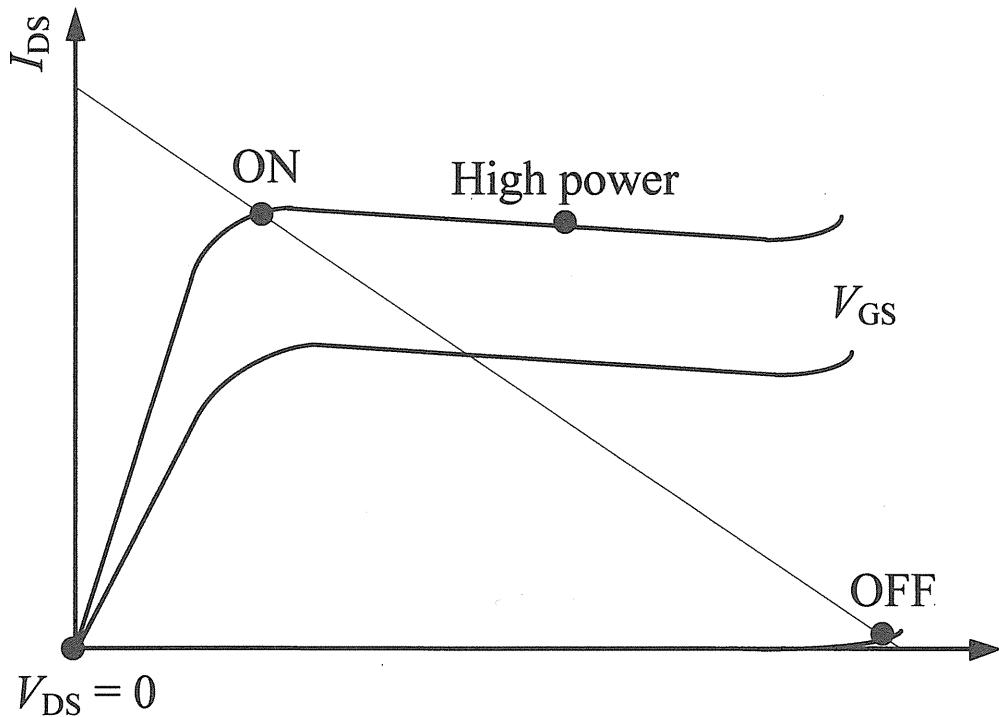


Fig. 2.11. Stress bias points: ON-state, high power state, OFF-state, and $V_{DS} = 0$ state.

The high power state is used study on the RF power amplifying operation in a more severe way. By investigating the both ends of the load line, ON state and OFF state, we can study where the most stressful point occurs. Also, $V_{D\text{-stress}} = 0$ state, wherein negative gate voltage is applied. In this condition, we can stress the both sides of the device simultaneously with a low current but a high voltage. All these conditions are shown in Fig. 2.11.

2.7 Summary

In this chapter we have discussed in detail on the growth technology and its various characterization technique. The device fabrication process and basic device characterization technique were also discussed and finally stress test methodology was introduced.

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Chapter-III: Reliability Studies on AlGaN/GaN HEMTs on Si with Different Buffer Thicknesses

3.1 Introduction

Material quality and reliability issues are the key points for the industrial application of GaN HEMTs that have demonstrated high power and RF power performance [1-3], but are subjected to various degradation mechanisms on operating at high electric field and/or high channel temperature [4-5]. Recently, the sudden increase of the gate leakage current on AlGaN/GaN HEMTs during electrical stress has been given much attention [6-14]. Joh and del Alamo [7] proposed a mechanism, where the electric field in the gate-drain region would increase the strain in the AlGaN/GaN heterojunction resulting in strain relaxation and crystallographic defect formation. It is widely accepted that the critical voltage does exist beyond which the gate contact of the AlGaN/GaN HEMT begins to degrade, showing a permanent increase in the gate leakage current which is irreversible. Electroluminescence microscopy can be very useful tool in detecting localized breakdown effects and evaluating degradation mechanisms in off-state bias stress [8, 14, 15-16]. In this chapter, reliability studies were carried out on AlGaN/GaN HEMTs on Si with different buffer thickness and their results were discussed.

3.2 Experiment

The AlGaN/GaN heterostructure with different buffer thickness (T_{Buf}) and GaN thickness (T_{GaN}) were grown on a 4" p-Si (111) substrate using a horizontal metal-organic chemical vapor deposition (MOCVD) system (SR 4000). The substrate was thermally cleaned at 1100 °C in H₂ flow. The growth started with the nucleation layer of 100 nm AlN, followed by 40 nm of AlGaN. To understand the device

degradation, wafer with different buffer thicknesses ($T_{Buf} = 1.25, 2.5, 4.0$, and $5.0 \mu\text{m}$) were grown. The intentionally doped GaN thickness varied from 0.5 to 1.5 μm and final 25 nm-thick $\text{Al}_{0.26}\text{Ga}_{0.74}\text{N}$ top layers were fixed for all the samples. All these layers were grown at a high temperature of 1130 °C, and these samples were free from cracks. Figure 3.1 shows the device structure of AlGaN/GaN HEMTs on Si with different buffer and GaN thicknesses that were used in our studies.

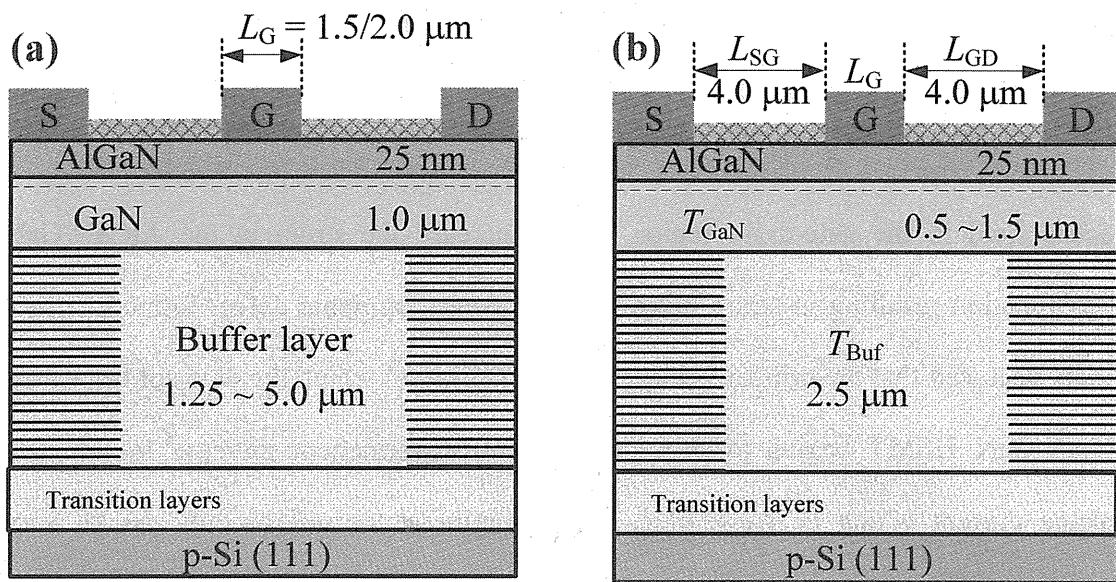


Fig. 3.1. Cross-sectional view of the SiO_2 passivated AlGaN/GaN HEMTs on Si (a) buffer layer thickness is varied and remaining kept constant and (b) varying the GaN thicknesses keeping the rest constant.

The device process started with mesa isolation by BCl_3 -based plasma reactive ion etching and passivated with SiO_2 deposited by electron beam evaporation with substrate temperature at 150 °C. Ohmic contacts were patterned with Ti/Al/Ni/Au (20/72/12/40 nm) metals followed by lamp annealing at 850 °C for 30 s in N_2 ambient. Gate metals Pd/Ti/Au (40/20/60 nm) were formed using conventional photolithography. All the metals except Al were deposited by electron beam evaporation, whereas Al was evaporated by the filament heating technique. The AlGaN/GaN HEMTs with device

dimensions of gate width (W_g) = 200 μm , gate length (L_g) = 1.5 μm , source-drain spacing (L_{sd}) = 9.5 μm , and gate-drain spacing (L_{gd}) = 4.0 μm were used for this study. The process condition and device parameters were kept the same throughout our study unless mentioned particularly.

Though several different step-stress measurements available, we have employed an OFF-state bias stress testing, where the gate-source bias voltage (V_{GS}) was kept constant at -10 V, which is well below the device threshold voltage. The drain stress voltage ($V_{D\text{-stress}}$) was increased from 5 to 45 V with 1 V step for a time interval of 60 seconds was carried out. Initially the comparison study on AlGaN/GaN HEMTs on Si on different buffer thickness ($T_{Buf} = 1.25, 2.5, 4.0$ and $5.0 \mu\text{m}$) with GaN thickness ($T_{GaN} = 1.0 \mu\text{m}$) were carried out. The dislocation densities were calculated using full width at half maximum (FWHM) values from X-Ray diffraction and Van der pauw Hall measurements were carried out at room temperature on these samples and reported in Table 3.1. Initially we chose two different buffer thickness i.e. $T_{Buf} = 1.25$ and $5.0 \mu\text{m}$, for our study and carried out the stress measurement with the above mentioned stress conditions.

3.3 Results and discussion

The figure 3.2 shows there is a continuous decrease in the $I_{D\text{max}}$ with an increase in drain resistance (R_D). The sub-threshold current slope shows a positive shift. Also, $g_{m\text{-peak}}$ shows a steady decrease with the shift in threshold voltage (V_{th}). The I_{GS} shows no significant change with the increase in step stress voltages.

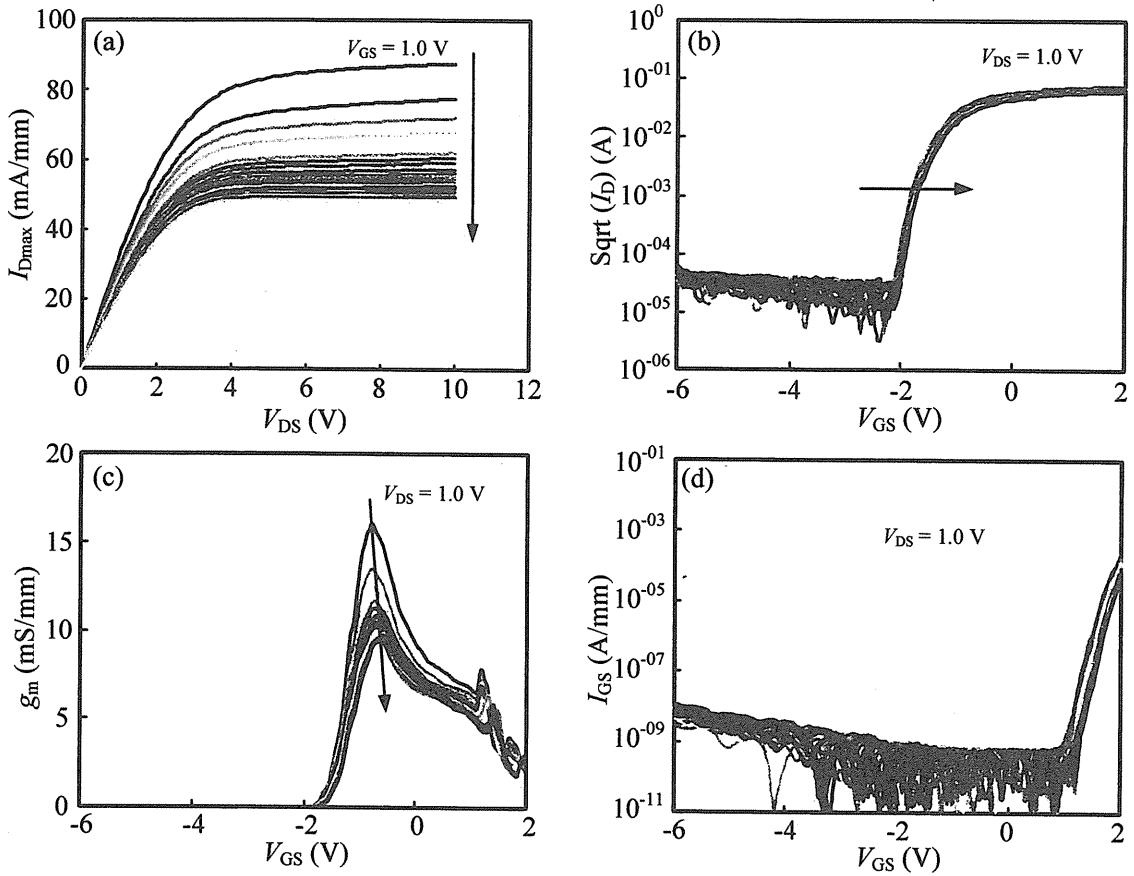


Fig. 3.2. Change in device characteristics at each step in the off-state bias stress condition was shown at $V_{G\text{-stress}} = -10 \text{ V}$; $V_{D\text{-stress}} = 5$ to 45 V ; step = 1 V and time period of 1 min . The (a) output characteristics, (b) sub-threshold characteristics, (c) transfer characteristics and (d) gate current characteristics for $T_{\text{Buf}} = 1.25 \mu\text{m}$ devices.

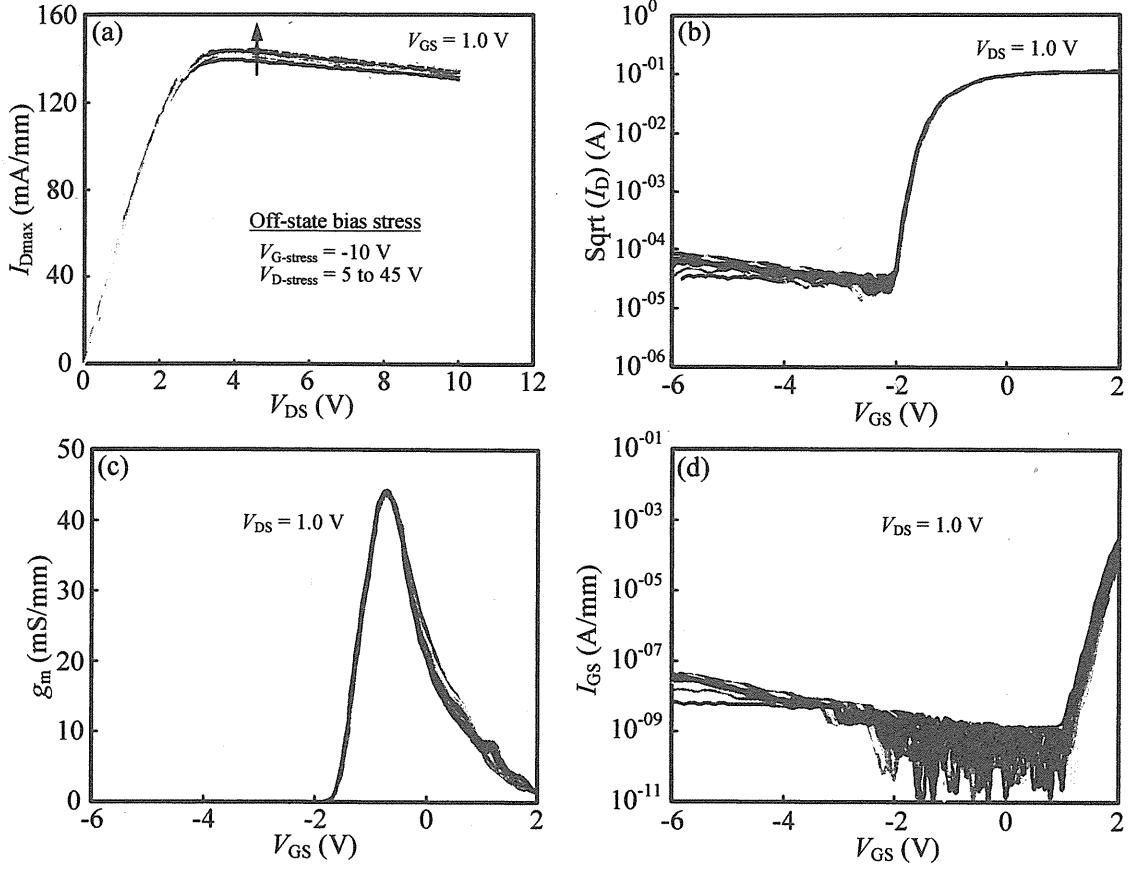


Fig. 3.3. The (a) output characteristics, (b) sub-threshold characteristics, (c) transfer characteristics and (d) gate current characteristics for AlGaN/GaN HEMTs on Si with thick buffer ($T_{\text{Buf}} = 5.0 \mu\text{m}$) devices.

The figure 3.3 shows, there is a small increase in the $I_{D\text{max}}$ with negligible change in R_D . There is no change observed in g_m -peak and V_{th} shift, sub-threshold drain current slope and I_{GS} doesn't show any significant changes either. This likely shows that increasing the T_{Buf} thickness the device shows a negligible degradation.

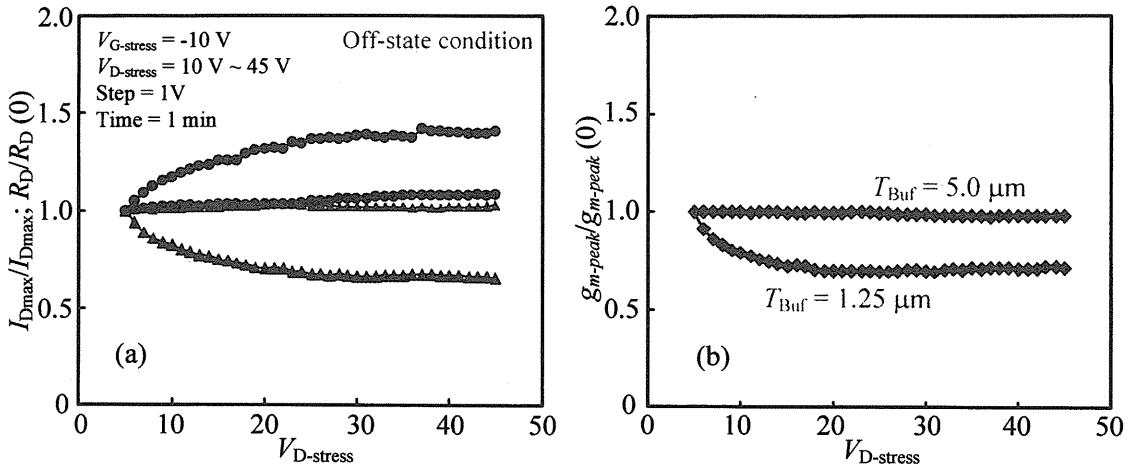


Fig. 3.4. Comparison of I_{Dmax} , R_D , and g_{m-peak} degradation of AlGaN/GaN HEMTs on Si with different buffer thickness.

Figure 3.4 shows the overall results of the step-stress test on AlGaN/GaN HEMTs with $T_{Buf} = 1.25$ and $5.0 \mu m$. The key figure of merit that was compared is I_{Dmax} , R_D , and g_{m-peak} . The Fig. 3.4 shows the change in output characteristics and transfer characteristics before and after each stress test. As it can be seen, drain current significantly decreases and R_D increases before and after stress for $T_{Buf} = 1.25 \mu m$. It is to be noted from Fig. 3.2 that a change observed in sub-threshold current slope, also steady decrease in g_{m-peak} observed. Whereas no such degradation were observed for $T_{Buf} = 5.0 \mu m$ in I_{Dmax} , R_D , g_{m-peak} and sub-threshold current slope. It has been reported by S. Demirtas et al., [12] that for AlGaN/GaN HEMT on Si there will be a steady decrease in the I_{Dmax} from the beginning of the stress test and the I_{Dmax} and R_D will show a mirror image behavior. They have proposed that this behavior is due to the presence of virgin defect that present in the GaN HEMT on Si substrate. From our finding we found that, there is a similar behavior in device operation trend as suggested by [12] for AlGaN/GaN HEMT on Si with thin buffer ($T_{Buf} = 1.25 \mu m$). Also to be noted that, the dislocation density was high for $T_{Buf} = 1.25 \mu m$ as shown in Table 3.1 confirms that it is

the defects that present in the virgin device causes this continuous decrease in $I_{D\max}$, R_D , and $g_m\text{-peak}$ for AlGaN/GaN HEMT on Si with $T_{Buf} = 1.25 \mu\text{m}$. Whereas, in the case of AlGaN/GaN HEMT on Si with thick buffer reduce in dislocation density reveals that the influence of virgin defects was reduced which results in good device performance. Since we did not observe any significant changes in the gate leakage current for $T_{Buf} = 1.25$ and $5.0 \mu\text{m}$ up to $V_{D\text{-stress}} = 45 \text{ V}$, we have carried out at higher $V_{D\text{-stress}}$ for two other buffer thickness ($T_{Buf} = 2.5$ and $4.0 \mu\text{m}$) devices.

Table. 3.1. Hall and XRD data listed for AlGaN/GaN HEMT grown on different buffer thickness

GaN/AlN SLS [pair]	T_{Buf} [μm]	i-GaN [μm]	Hall characteristics at 300K			Dislocation density [cm^{-2}]	
			sheet resistance [Ω/\square]	Sheet carrier concentration [cm^{-2}]	Mobility [cm^2/Vs]	screw	Edge
50	1.25	1.0	776	8.72×10^{12}	925	1.22×10^9	5.02×10^{10}
100	2.50	1.0	737	8.79×10^{12}	968	1.52×10^9	4.05×10^{10}
160	4.00	1.0	687	7.97×10^{12}	1150	1.71×10^9	2.79×10^{10}
200	5.00	1.0	1058	6.57×10^{12}	883	1.50×10^9	2.49×10^{10}

3.3.1 Critical voltage

The phenomenon of critical voltage is very importantly considered and widely discussed especially in reliability studies. The term critical voltage (V_{crit}) is defined as, at a specific drain-source voltage (V_{DS}) where one or both, namely, (i) gate leakage current ($I_{G\text{-off}}$) and (ii) sub-threshold voltage drain current (I_D), increase significantly and irreversible during DC stress under pinch-off conditions. Various authors have reported on this critical voltage phenomenon. Critical voltage between 20 to 30 V reported for AlGaN/GaN HEMT on SiC substrate [6, 7, 17], 70 to 80 V reported for AlGaN/GaN HEMT on sapphire substrate [18, 19], 25 to 70 V reported for AlGaN/GaN HEMT on Si substrate [12, 13]. In one case they have reported the V_{crit} delayed beyond

100 V on changing the gate metal stacks [20]. Hence, to observe this sudden increase in the gate leakage current during electrical stress, we have selected AlGaN/GaN HEMT with two different buffer thickness ($T_{\text{Buf}} = 2.5$ and $4.0 \mu\text{m}$).

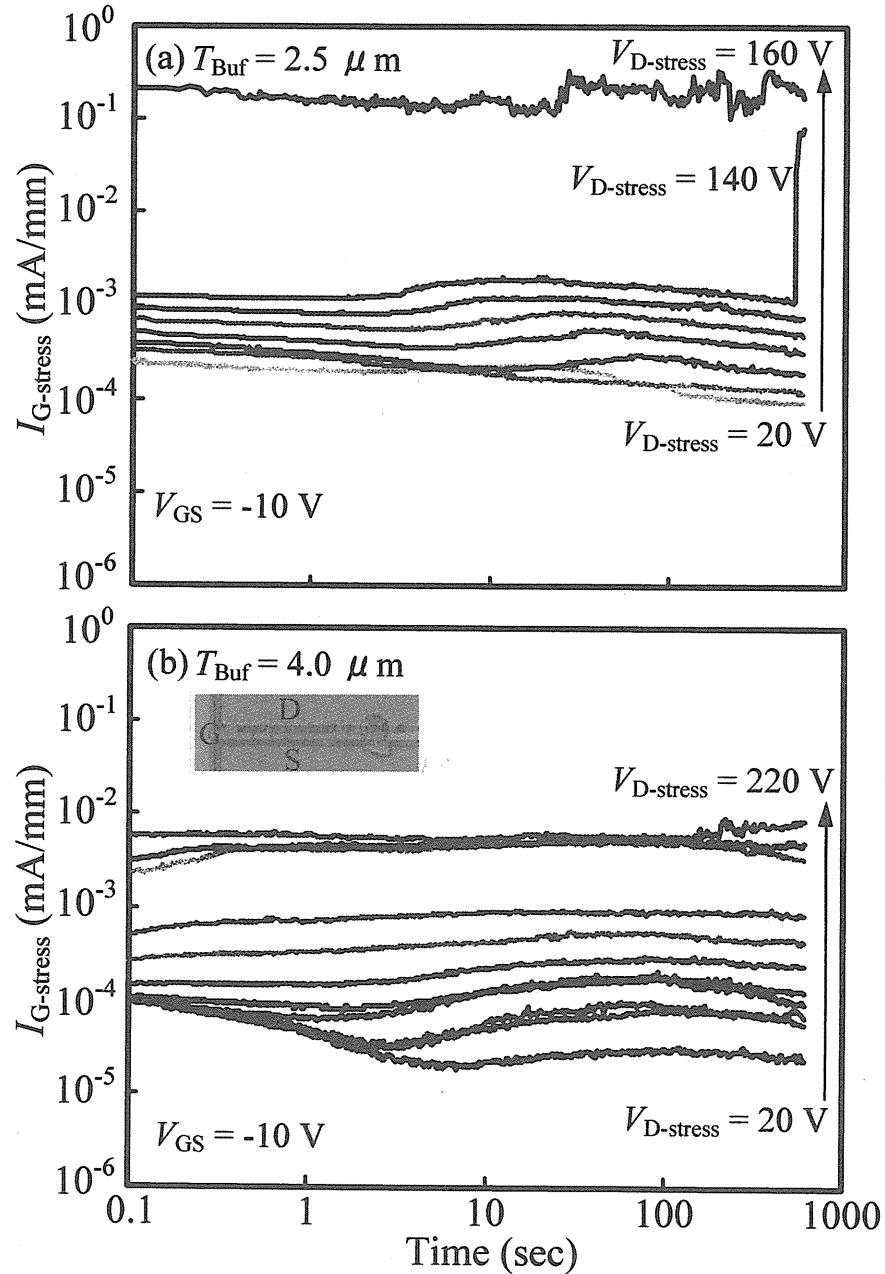


Fig. 3.5. Increase in $I_{\text{G-stres}}$ observed during continuous biasing of 600 s for increasing $V_{\text{D-stress}}$ at $V_{\text{GS}} = -10 \text{ V}$. Sudden increase in the $I_{\text{G-stres}}$ is observed for (a) $T_{\text{Buf}} = 2.5 \mu\text{m}$ at $V_{\text{D-stress}} = 140 \text{ V}$, (b) $T_{\text{Buf}} = 4.0 \mu\text{m}$ device burn out occurs at $V_{\text{D-stress}} = 230 \text{ V}$.

The $V_{\text{D-stress}}$ started at 20 V and gradually increased in steps of 20 V until the

occurrence of critical voltage. Each step voltage stressed for a time span of 600 s. In fewer cases, this step voltage changed from 20 to 10 V or much lower to obtain more sampling data which can identify a precise V_{crit} . For every buffer thickness, several devices from two different wafers were subjected to step-stress measurement. The substrate was grounded and the measurements were carried out in dark and at room temperature for all these measurements. Figure 3.5 shows the behavior of gate stress leakage current ($I_{G\text{-stress}}$) during continuous biasing with increasing $V_{D\text{-stress}}$ for both $T_{\text{Buf}} = 2.5$ and $4.0 \mu\text{m}$ devices. $I_{G\text{-stress}}$ was found to increase with increasing $V_{D\text{-stress}}$. It was reported that before failure occurs the gate stress leakage current should become unsteady and then resulting in permanent degradation [14]. This permanent increase in $I_{G\text{-stress}}$ during continuous biasing reflects a V_{crit} -like phenomenon. In the case of $T_{\text{Buf}} = 2.5 \mu\text{m}$ there found a slow increase in $I_{G\text{-stress}}$ with the increase in $V_{D\text{-stress}}$ and a sudden increase in $I_{G\text{-stress}}$ observed at $V_{D\text{-stress}} = 140 \text{ V}$ without any noise indication as shown in Fig. 3.5(a).

This sudden increase in $I_{G\text{-stress}}$ at $V_{D\text{-stress}} = 140 \text{ V}$ is a permanent increase that was observed well below the current compliance of the gate current which is irreversible. Moreover the device found recoverable up to the prior $V_{D\text{-stress}}$ i.e. $V_{D\text{-stress}} = 120 \text{ V}$. As discussed later, the device at this voltage still continues to operate as a transistor. This permanent increase in $I_{G\text{-stress}}$ was observed for all the devices with a broad distribution of $V_{D\text{-stress}}$ ranging from 140 to 180 V. Whereas for $T_{\text{Buf}} = 4.0 \mu\text{m}$, no such V_{crit} like phenomenon was observed, as shown in Fig. 3.5(b). At $V_{D\text{-stress}} = 230 \text{ V}$, the device burn out occurred confirming that the device had undergone breakdown phenomenon. It is to be noted that the $I_{G\text{-stress}}$ becomes unsteady before this device burn out occurs. The surface view using the microscope after this confirmed the device burn

out mark, as shown in the inset of Fig. 3.5(b). For devices having $T_{Buf} = 4.0 \mu\text{m}$, we did not observe the sudden increase in $I_{G-stress}$ during continuous biasing rather, this device undergoes breakdown accompanied by a burn out mark with a variation of $V_{D-stress}$ from 230 to 260V.

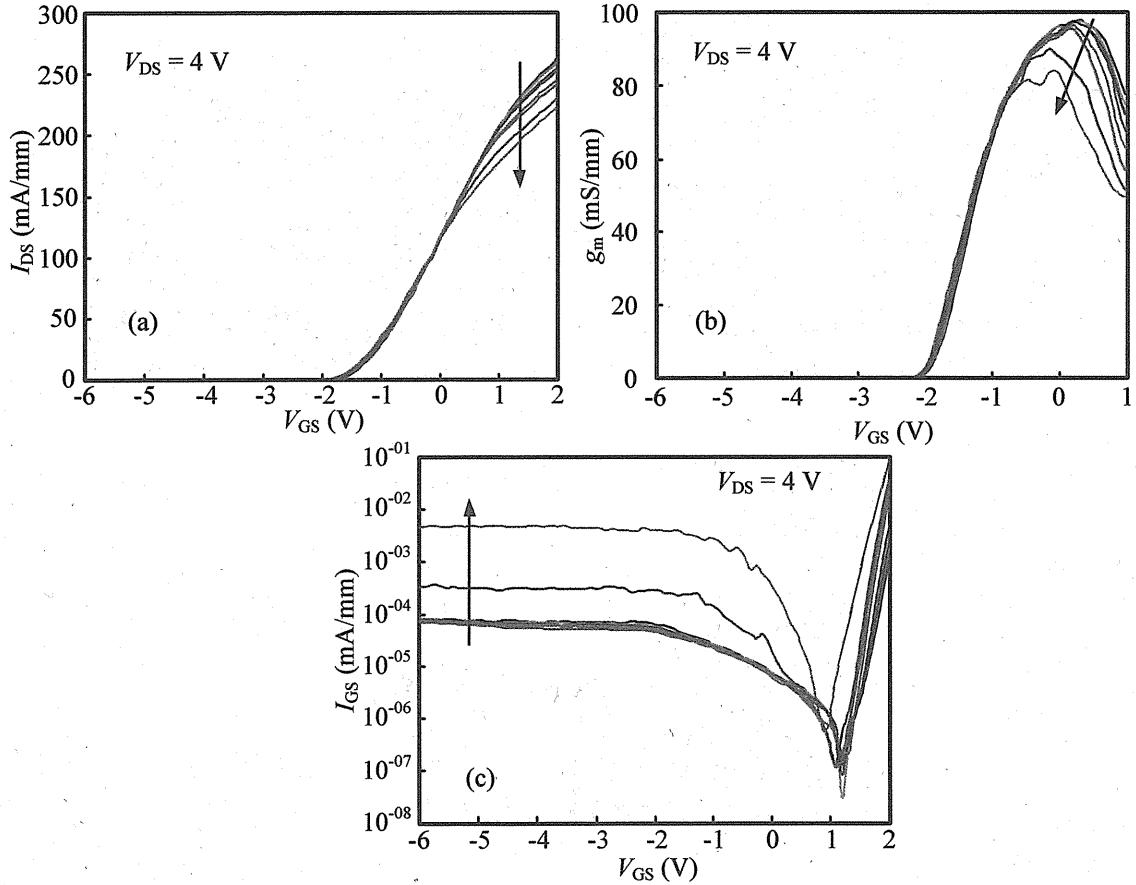


Fig. 3.6. The transfer characteristics measured after every step-stress off stress bias voltage for $T_{Buf} = 2.5 \mu\text{m}$.

We measured the transfer characteristics after every step-stress measurement. V_{DS} varied from 0 to 10 V in steps of 2 V in which V_{GS} swept from -6 to 2 V. Fig. 3.6 shows the transfer characteristics measured after each off-state bias stress voltages at $V_{DS} = 4 \text{ V}$ and $V_{GS} = -6$ to 2 V. There is a small decrease in I_{Dmax} and g_{m-peak} was observed and found a negligible change in the V_{th} shift as shown in Fig. 3.6(a) and (b) for $T_{Buf} = 2.5 \mu\text{m}$. The off-gate leakage current (I_{G-off}) measured at $V_{DS} = 4 \text{ V}$ and $V_{GS} =$

-5 V termed as $I_{G\text{-off}}$ is summarized from Fig. 3.6(c) for the entire step-stress measurement. The $I_{G\text{-off}}$ shows a sudden increase at $V_{D\text{-stress}} = 140$ V as shown in Fig. 3.7. This sudden increase in the $I_{G\text{-off}}$ at $V_{D\text{-stress}} = 140$ V is referred to a critical voltage in our case. For $T_{\text{Buf}} = 2.5 \mu\text{m}$, $I_{G\text{-off}}$ measured after $V_{D\text{-stress}} = 140$ V was observed to increase drastically compared with $I_{G\text{-off}}$ measured less than $V_{D\text{-stress}}$ of 140 V. After this sudden increase in $I_{G\text{-off}}$, the transistor characteristics measured show an ideal I_{DS} - V_{DS} curve with a pinch off voltage.

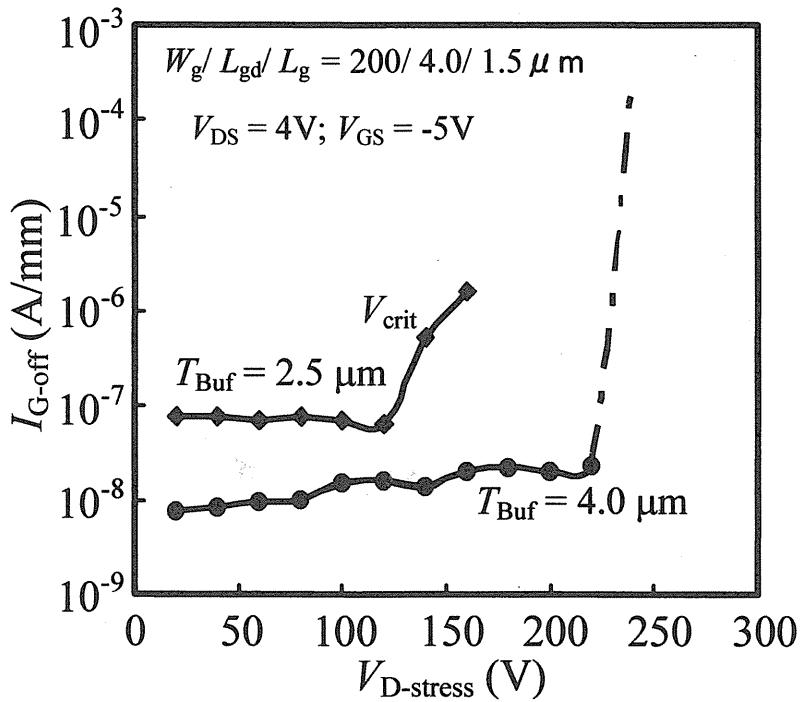
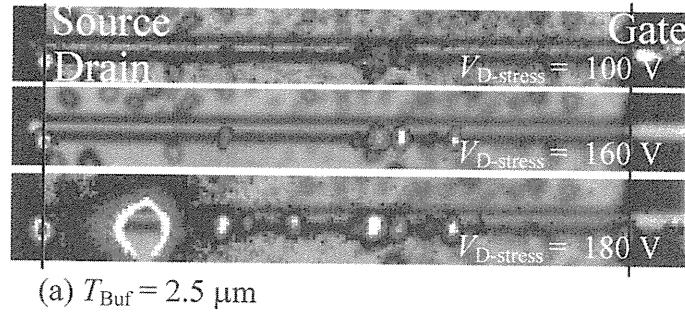


Fig. 3.7. change in $I_{G\text{-off}}$ observed at $V_{GS} = -5$ V and $V_{DS} = 4$ V. V_{crit} is observed for $T_{\text{Buf}} = 2.5 \mu\text{m}$ at $V_{D\text{-stress}} = 140$ V and no abrupt increase were observed for $T_{\text{Buf}} = 4.0 \mu\text{m}$ resulting in device burn out at $V_{D\text{-stress}} = 230$ V.

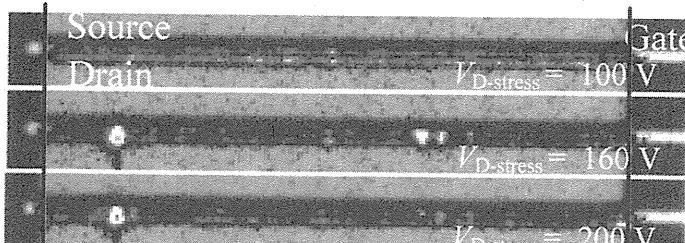
This confirmed that the normal FET operation of the device was not affected because of the sudden increase in $I_{G\text{-off}}$. In the case of $T_{\text{Buf}} = 4.0 \mu\text{m}$, there is no sudden increase in the $I_{G\text{-off}}$ observed even at higher $V_{D\text{-stress}}$. At 230 V, the device reaches the breakdown voltage limit and a burn out was noticed. Therefore, V_{crit} was observed only for HEMTs grown on $T_{\text{Buf}} = 2.5 \mu\text{m}$ and not for HEMTs grown on $T_{\text{Buf}} = 4.0 \mu\text{m}$.

3.3.2 Electroluminescence

Electroluminescence (EL) is an important tool where we can monitor the path of gate leakage current or strong electric field [8, 14]. EL in AlGaN/GaN HEMTs has been attributed to the intraband transition of hot carriers in the high-field region of the device, i.e., related to the lateral electric field strength [8]. The real-time electroluminescence was observed using the PHMOS instrument by Hamamatsu Photonics K. K., in which a silicon-intensified CCD (SI-CCD) camera has been installed [21]. In this system, the high sensitivity and low noise characteristics of the SI-CCD enabled us to observe the low-intensity emission with high position accuracy. For example, the Si-CCD slashes the detection time by 90% compared to a conventional cooled CCD camera. The detectable wavelength of the Si-CCD ranges from 0.3 to 1.1 mm, so that the electroluminescence due to the hot carrier in the AlGaN/GaN HEMT [14, 22, 23] is observable with PHMOS.



(a) $T_{\text{Buf}} = 2.5 \mu\text{m}$



(b) $T_{\text{Buf}} = 4.0 \mu\text{m}$

Fig. 3.8. Electroluminescence shows a spotty and uniform emission for $T_{\text{Buf}} = 2.5$ and $4.0 \mu\text{m}$, respectively.

Another feature of PHEMOS is that it has a probe inside, so that on-wafer devices as well as packaged ones can be measured easily.

During measurements, a movie of the electroluminescence with the 60 frames/s was captured while the AlGaN/GaN HEMT was biased at off-state condition for both the buffer thickness. The EL emissions for HEMTs grown on $T_{Buf} = 2.5$ and $4.0 \mu\text{m}$ were spotty and uniform, respectively as shown in Fig. 3.8. In the case of HEMTs grown on $T_{Buf} = 2.5 \mu\text{m}$, the EL emission spots began to appear at $V_{D\text{-stress}} = 100 \text{ V}$, as shown in Fig. 3.8(a) (frame 1). The emission spots observed at this voltage were weak and non-uniform. As the stress voltage increased, the EL emission intensity also increased and new spots were formed and visible altogether at a new region, as shown in Fig. 3.8(a) (frame 2). At the critical voltage of 180 V during continuous biasing, until the sudden increase in $I_{G\text{-stress}}$, there was no trace of new spots observed, but with the sudden increase in $I_{G\text{-stress}}$, an entirely new hot spot in a new region was observed as shown in Fig. 3.8(a) (frame 3). Whereas in the case of HEMTs grown on $T_{Buf} = 4.0 \mu\text{m}$, a weak and uniform emission throughout the gate-drain region was observed as shown in Fig. 3.8(b) (frame 1). With further increased $V_{D\text{-stress}}$, the emission was observed to be weak and uniform, as shown in Fig. 3.8(b) (frames 2 and 3). The HEMTs grown on $T_{Buf} = 2.5 \mu\text{m}$ show a critical voltage, i.e., a non-recoverable increase in gate leakage current. The generations of further leakage paths were identified as luminescent dots in the micro-EL images. The spotty emission that followed a new hot spot at the critical voltage was caused by large dislocation density ($3.6 \times 10^9 \text{ cm}^{-2}$) which increases the high electric field at the gate edge of the drain side resulting in non uniform emission. Whereas, for HEMTs grown on $T_{Buf} = 4.0 \mu\text{m}$, the distribution of the electric field is believed to be uniform even at high $V_{D\text{-stress}}$, and this, in turn, prevents the occurrence of

critical voltage.

3.4 Summary

In summary, we have studied the step-stress measurement under the off-state condition for different buffer thicknesses and found different failure modes. The AlGaN/GaN HEMT grown on $T_{\text{Buf}} = 1.25 \mu\text{m}$ shows a reduction in output and transfer characteristics which is believed to be due to the virgin defects present in the device. The AlGaN/GaN HEMT grown on $T_{\text{Buf}} = 2.5 \mu\text{m}$ shows the V_{crit} was observed above $V_{\text{D-stress}} = 100 \text{ V}$ for all its devices. Whereas we did not observe this V_{crit} for AlGaN/GaN HEMT grown on $T_{\text{Buf}} = 4.0 \mu\text{m}$ devices. On increasing $V_{\text{D-stress}}$, we did not observe the sudden increase in $I_{\text{G-stress}}$; rather, device burn out occurred at $V_{\text{D-stress}} = 230 \text{ V}$. The EL measured during continuous biasing shows weak and uniform emission throughout the gate edge of the drain side. It is believed that AlGaN/GaN HEMTs grown on a Si substrate with increasing buffer layer thickness dispels the existence of a non-uniform electric field at the gate-drain region and absence of V_{crit} .

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Chapter-IV: Origin and Appearance of Pits in the Gate-Drain Region of AlGaN/GaN HEMT Grown on Thick Buffer

4.1 Introduction

Several structural studies using transmission electron microscopy (TEM), scanning electron microscopy (SEM), and atomic force microscopy (AFM) obtained physical evidence suggesting that the defects are generated below the gate edge located in the AlGaN barrier layer [1-5]. Most of these studies reveal crystallographic defects such as pits and cracks at the drain side of the gate edge in spite of their low defect density. Apart from these defects generated in the AlGaN barrier layer, defects resulting in excess leakage through i-GaN due to imperfections and dislocation density during growth require more investigation [6-10].

In the previous chapter we discussed on the leakage current, critical voltage and electroluminescence for different buffer thickness and found the critical voltage was not observed in AlGaN/GaN HEMT on Si with thick buffer layers. In this chapter, we have carried out step-stress and cyclic stress measurements at various conditions exclusively on AlGaN/GaN HEMT grown on thick buffer. A Keyence 3D laser microscope which is an useful tool where it combines the capabilities of an optical microscope, profilometer and an SEM. This microscope uses laser light and white light source where both high end resolution and crisp optical image is observed. Atomic force microscope (AFM) was also used to study origin and the magnitude of the defects.

We chose AlGaN/GaN HEMT on Si with $T_{Buf} = 5.0 \mu\text{m}$ and carried out the step-stress measurement in 3 different conditions namely:

- (1) Off state ($V_{G\text{-stress}} = -10 \text{ V}$, $V_{D\text{-stress}} = 5 \text{ to } 45 \text{ V}$). (Discussed in chapter-3, Fig.3.2.)
- (2) $V_{D\text{-stress}} = 0 \text{ V}$ ($V_{G\text{-stress}} = -5 \text{ to } -45 \text{ V}$), and

(3) On-state ($V_{G\text{-stress}} = 0$ V, $V_{D\text{-stress}} = 5$ to 45 V) with 1 V step and time = 1 min.

Device dimensions: $W_g/L_g = 200/2.0$ μm and $L_{gd} = 3.0/4.0$ μm .

All our experiments were performed in the dark and at the room temperature.

The drain current-voltage ($I_{DS}-V_{DS}$) characteristics and transfer characteristics were measured after every step-stress measurement. Some of the parameters extracted are mentioned below.

$I_{D\text{max}}$: measured at $V_{GS} = 1.5$ V and $V_{DS} = 5$ V,

R_D extracted from the slope of I_D vs V_{DS} (for $V_{DS} < 1$ V) in the linear region.

$g_m\text{-peak}$ and $I_{G\text{-off}}$ measured at $V_{DS} = 1$ V and $V_{GS} = -6$ V were plotted.

4.2 Step-stress measurement

4.2.1 $V_{D\text{-stress}} = 0$ state bias stress

In the $V_{D\text{-stress}} = 0$ state bias stress measurement, we found that, there is a negligible variation observed in R_D and V_{knee} . Initially the $I_{D\text{max}}$ decreased at 5 V stress voltage and thereafter on increasing the stress voltage there observed an increase in the $I_{D\text{max}}$. Also, a small increase in the g_m -peak was observed, whereas no changes observed in sub-threshold slope, threshold voltage shift (V_{th}) and found a small decrease in the gate leakage current (I_{GS}).

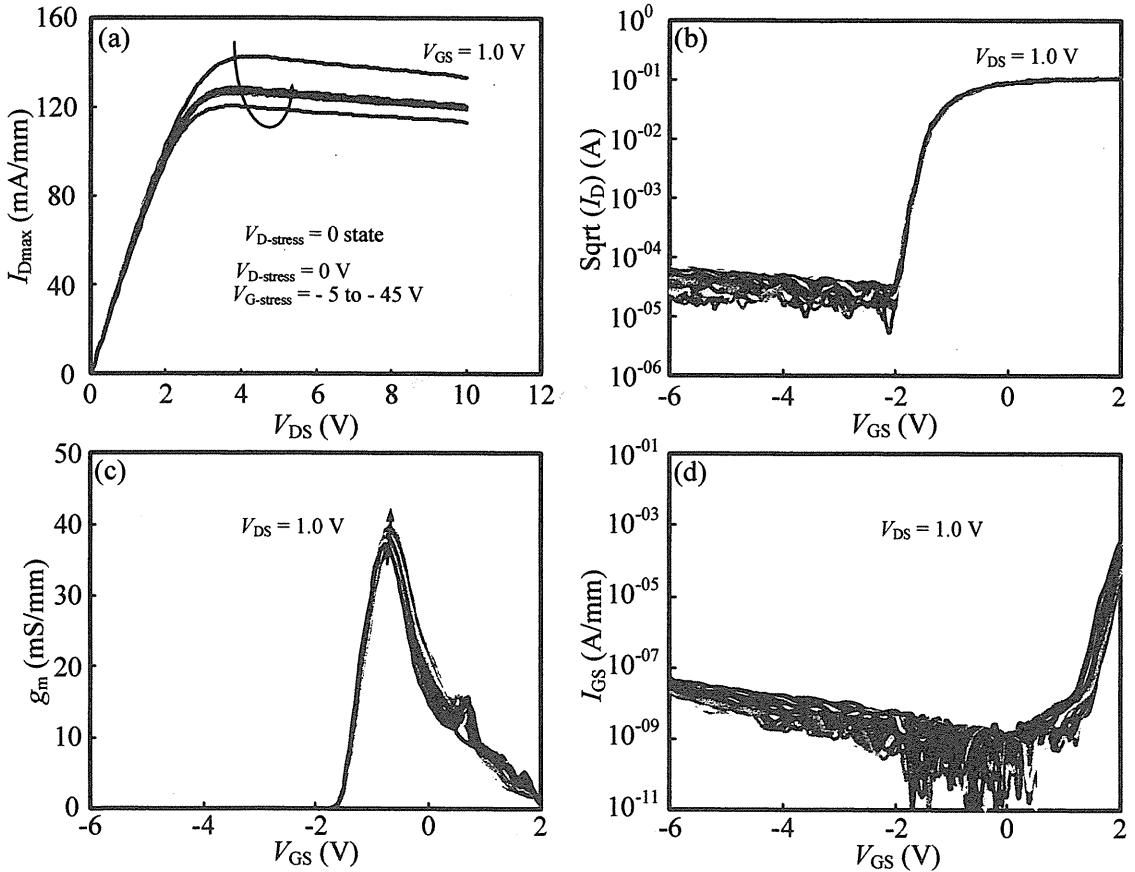


Fig. 4.1. Change in device characteristics at each step in the $V_{D\text{-stress}} = 0$ V bias stress condition. $V_{G\text{-stress}}$ was stepped from -5 to -45 V in 1 V step (1 min per step).

4.2.2 ON-state step-stress condition

In the ON-state bias stress measurement, we found that, there is no significant change observed at R_D and V_{knee} . There found a decrease in I_{Dmax} and $g_{m\text{-peak}}$. Whereas there is no change observed in sub-threshold slope, V_{th} and I_{GS} are shown in Fig. 4.2.

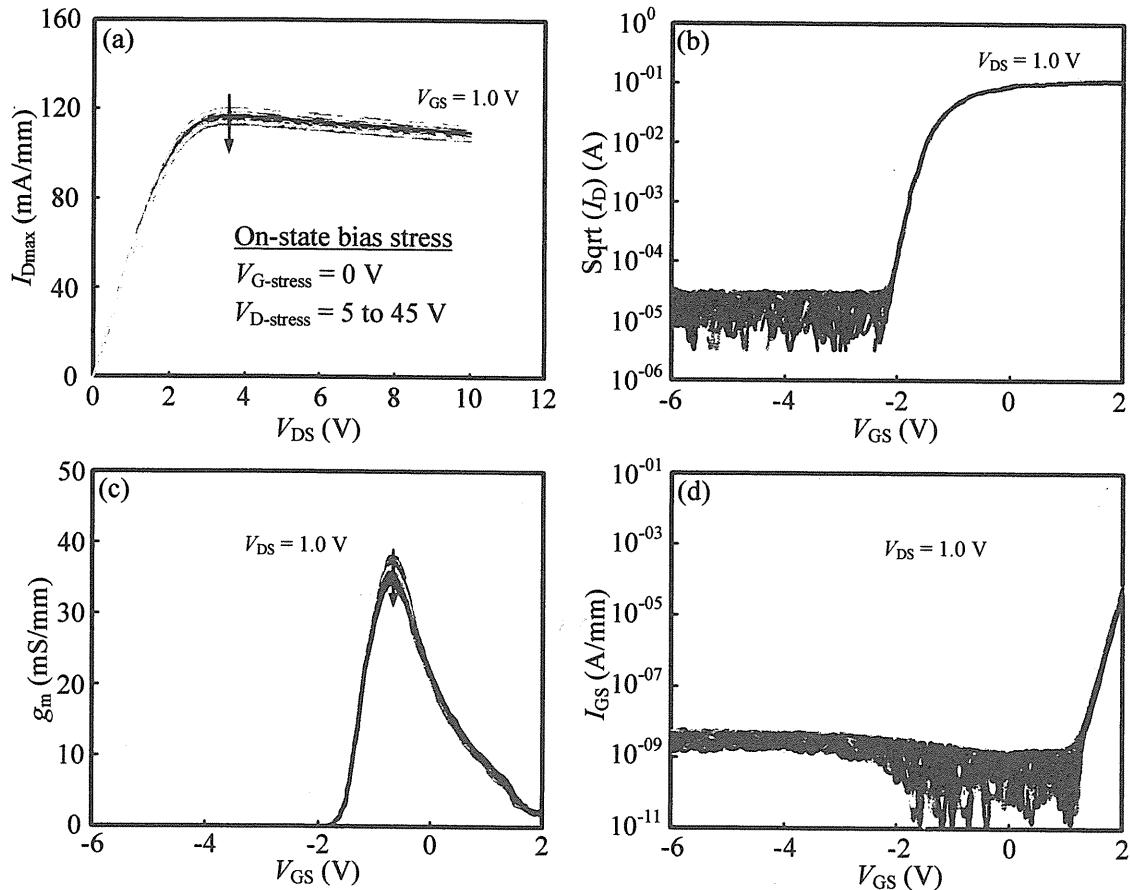


Fig. 4.2. Change in device characteristics at each step in the ON-state bias stress condition. $V_{D\text{-stress}}$ was stepped from 5 to 45 V in 1 V steps (1 min per step). From the upper-left corner (clockwise): (a) output characteristics, (b) sub-threshold characteristics, (c) transfer characteristics, and (d) gate current characteristics.

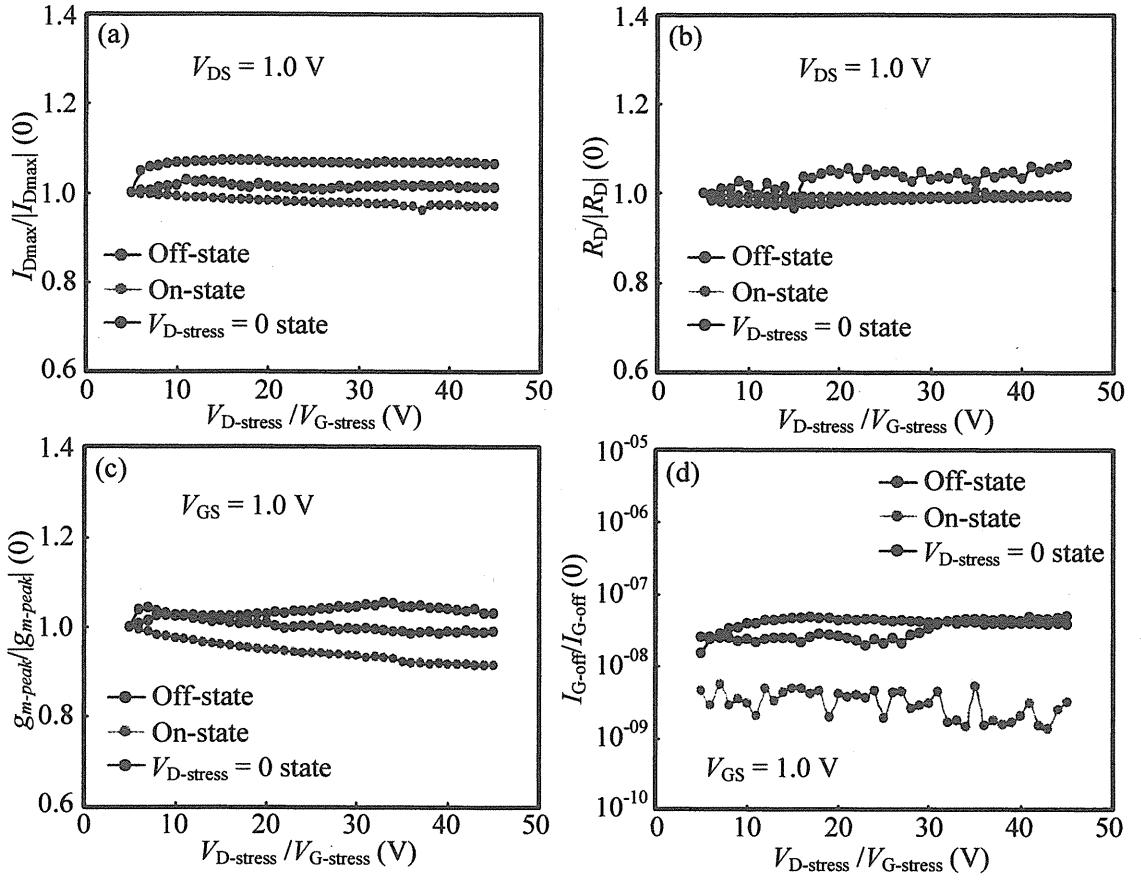


Fig. 4.3. Change in $I_{D\text{max}}$, R_D , $g_{m\text{-peak}}$ and $I_{G\text{-off}}$ at Off-state, On-state and $V_{D\text{-stress}} = 0$ V state.

Under these stress conditions ($-V_{G\text{-stress}}$ and $V_{D\text{-stress}} = 45$ V) neither the formation of pits across the source-drain region nor significant degradation on $I_{D\text{max}}$, R_D , $g_{m\text{-peak}}$ and $I_{G\text{-off}}$ were observed as shown in Fig. 4.3. This result motivated us to do the step-stress measurement for higher drain stress voltages.

4.3 Step-stress measurement at high drain bias stress

Off-state stress ($V_{G\text{-stress}} = -10$ V; $V_{D\text{-stress}}$ = 5 to 200 V; step = 5 V; time = 600 s)

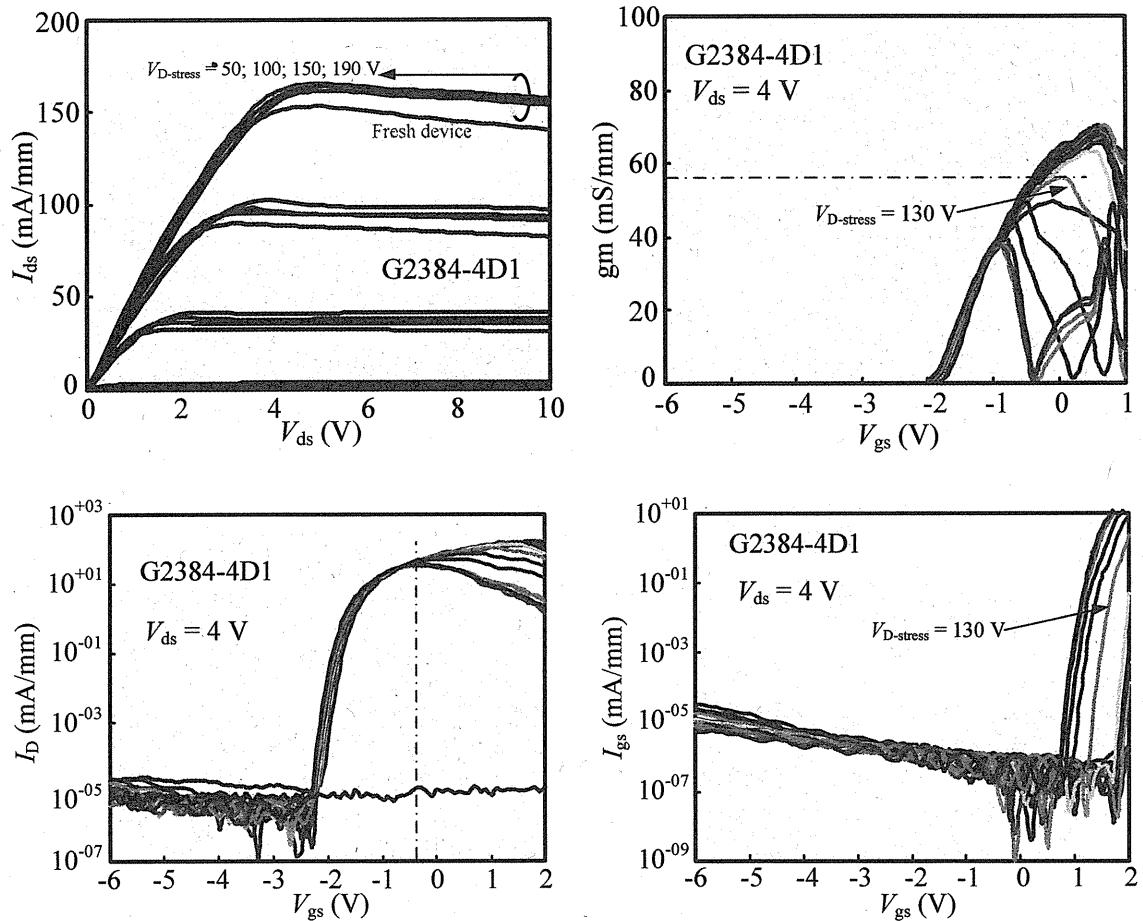


Fig. 4.4. shows the (a) output characteristics, (b) transfer characteristics, (c) sub-threshold characteristics, and (d) gate current characteristics at $V_{G\text{-stress}} = -10$ V; $V_{D\text{-stress}} = 5$ to 200 V; step = 5 V; time = 600 s for AlGaN/GaN HEMT grown on $T_{\text{Buf}} = 5.0$ μm .

The summary of output characteristics, transfer characteristics, sub-threshold characteristics and gate current characteristics are shown in Fig. 4.4. The I - V characteristics show an initial increase in the drain current than that of fresh device. But with the increase in $V_{D\text{-stress}}$ there is no further increase in the drain current observed. There observed a small increase in the drain resistance and shift in the knee voltage. The

transfer characteristics show that initially the $g_{m\text{-peak}}$ increased and there after it remained the same $g_{m\text{-peak}}$. At $V_{D\text{-stress}} = 130$ V a sudden decrease in $g_{m\text{-peak}}$ was observed which further decreased with the increase in $V_{D\text{-stress}}$. The sub-threshold characteristics reveals there found a negative shift in the sub-threshold slope and V_{th} . The gate current characteristics show there is a significant change in the turn-ON voltage observed at $V_{D\text{-stress}} = 130$ V but there is no much significant difference observed towards negative bias.

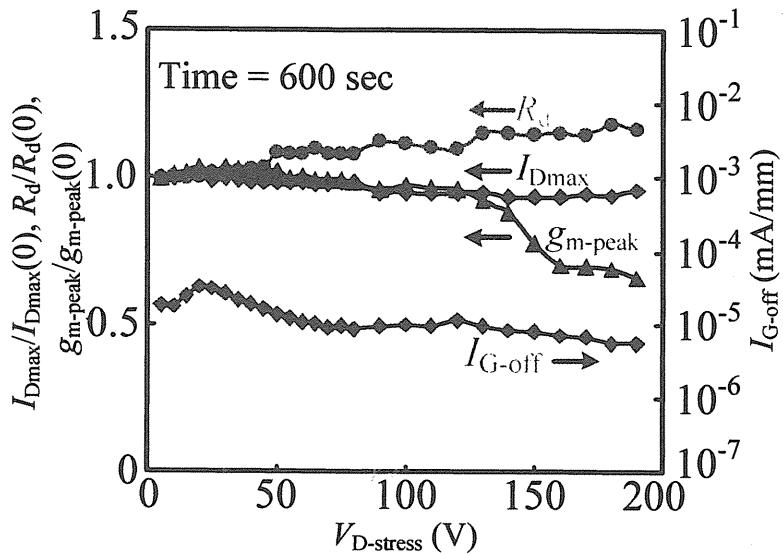


Fig. 4.5. Change in normalized $I_{D\text{max}}$, R_d , $g_{m\text{-peak}}$ and $I_{G\text{-off}}$ in step-stress measurement at OFF-state bias stress ($V_{D\text{-stress}} = 5\text{-}200$ V; 5 V step, 10 minutes per step).

Figure 4.5. shows the behavior of $I_{D\text{max}}$, R_d , $g_{m\text{-peak}}$ and $I_{G\text{-off}}$ after every step of off-state bias stress. The device undergoes a catastrophic failure at $V_{D\text{-stress}} = 200$ V without any signs of sudden increase in the $I_{G\text{-off}}$. The $I_{D\text{max}}$ and R_d shows a mirror image behavior and $g_{m\text{-peak}}$ shows no significant changes up to 130 V and beyond which, reduction in $g_{m\text{-peak}}$ was noted. Hence, it is clearly observed that for all our devices we did not show the critical voltage phenomenon for AlGaN/GaN HEMTs on Si with thick buffer. To understand the origin of degradation i.e. reduction in $g_{m\text{-peak}}$ around 130 V, the measurement was halted after 130 V and carried out the SEM in the gate-drain region.

We found cracks on the SiO_2 passivation layer in the gate-drain region. When the measurement was continued with further increase in $V_{\text{D-stress}}$, this crack developed into a crater. In addition, new cracks were seen in the gate-drain region.

Figure 4.6 shows the laser microscopic image of the spots formed at different location across the gate-drain region with the increased $V_{\text{D-stress}}$ for a time interval of 600 sec. These images were captured on the devices with SiO_2 passivation. The fresh device shows absolutely no spots or crack in either gate-source or gate-drain region as shown in Fig. 4.6.(frame1). From our measurement values it is evident that there is a degradation at $V_{\text{D-stress}} = 130$ V, hence after this stress voltage the microscopic images were recorded and found a spot observed at the gate-drain region as shown in Fig. 4.6.(frame 2). Similarly on increasing the stress voltages more spots were observed as shown in Fig. 4.6.(frame 3 & 4). In fewer cases some new spots were formed and already existing spots became enlarged on increasing the $V_{\text{D-stress}}$. Several such spots were generated before device breakdown occurred. The AFM images were carried out on these spots as shown in Fig. 4.7. AFM carried out at the cracked area revealed a heap of oxides among the SiO_2 passivation. No cracks or defects were spotted at the gate-source spacing throughout these measurements. To further understand the origin of spot, SiO_2 passivation was removed by wet etching to facilitate re-inspection by SEM and AFM. Figure 4.8 shows the AFM images taken after SiO_2 removal. It is apparent that the pits initially formed at the edge of the drain and migrate towards gate. Also few pits were generated in between gate-drain spacing and travels towards gate edge. It is evident that no pits were generated or formed at the gate edge. The AFM carried out on all these pits, showed a pit depth of 100 nm and in some cases a depth of 400 nm as shown in the Fig. 4.9. Thus, when the devices were stressed at a constant time with

increasing $V_{D\text{-stress}}$, it led to the formation of degradation in the form of pits.

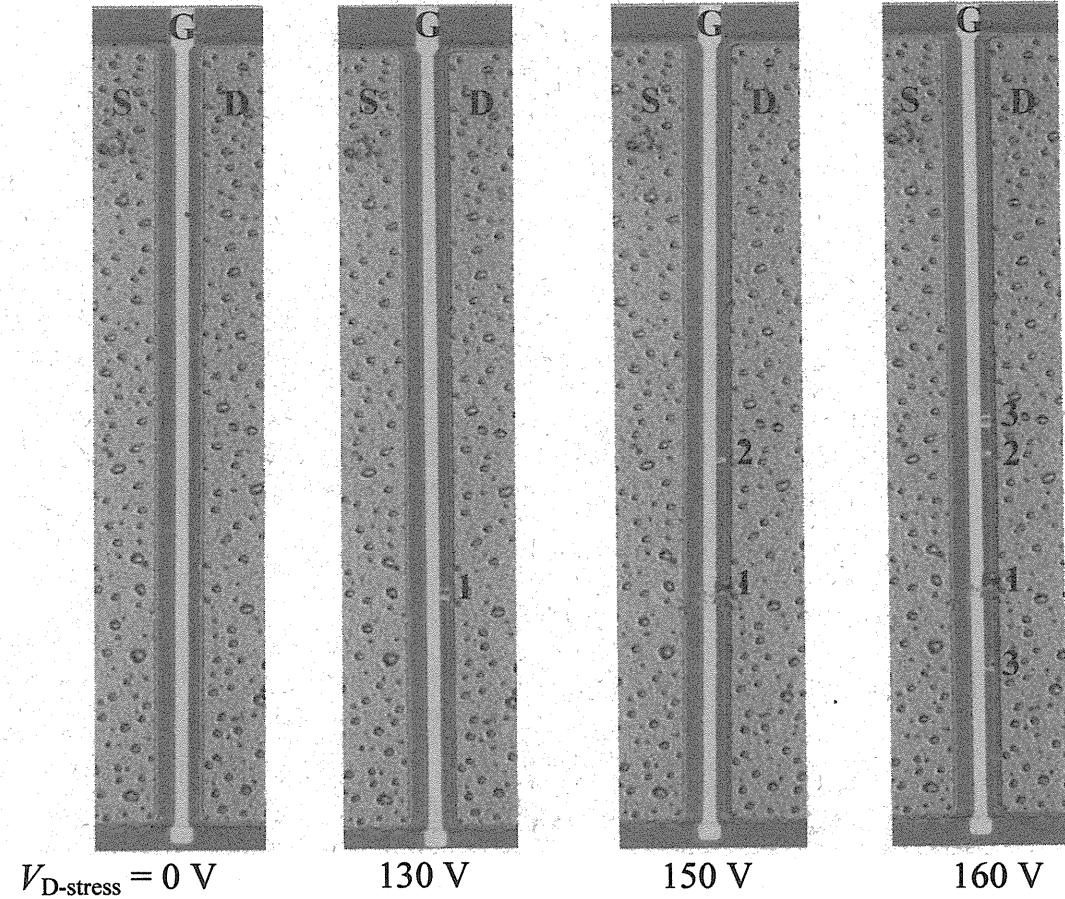


Fig. 4.6. SEM images show the evolution of spot under an off-state bias stress with increasing $V_{D\text{-stress}}$. On fresh device there is not spot observed (first frame). At $V_{D\text{-stress}} = 130 \text{ V}$ spot observed (second frame) and further new spots at different location (third & fourth frame) in the gate-drain region observed.

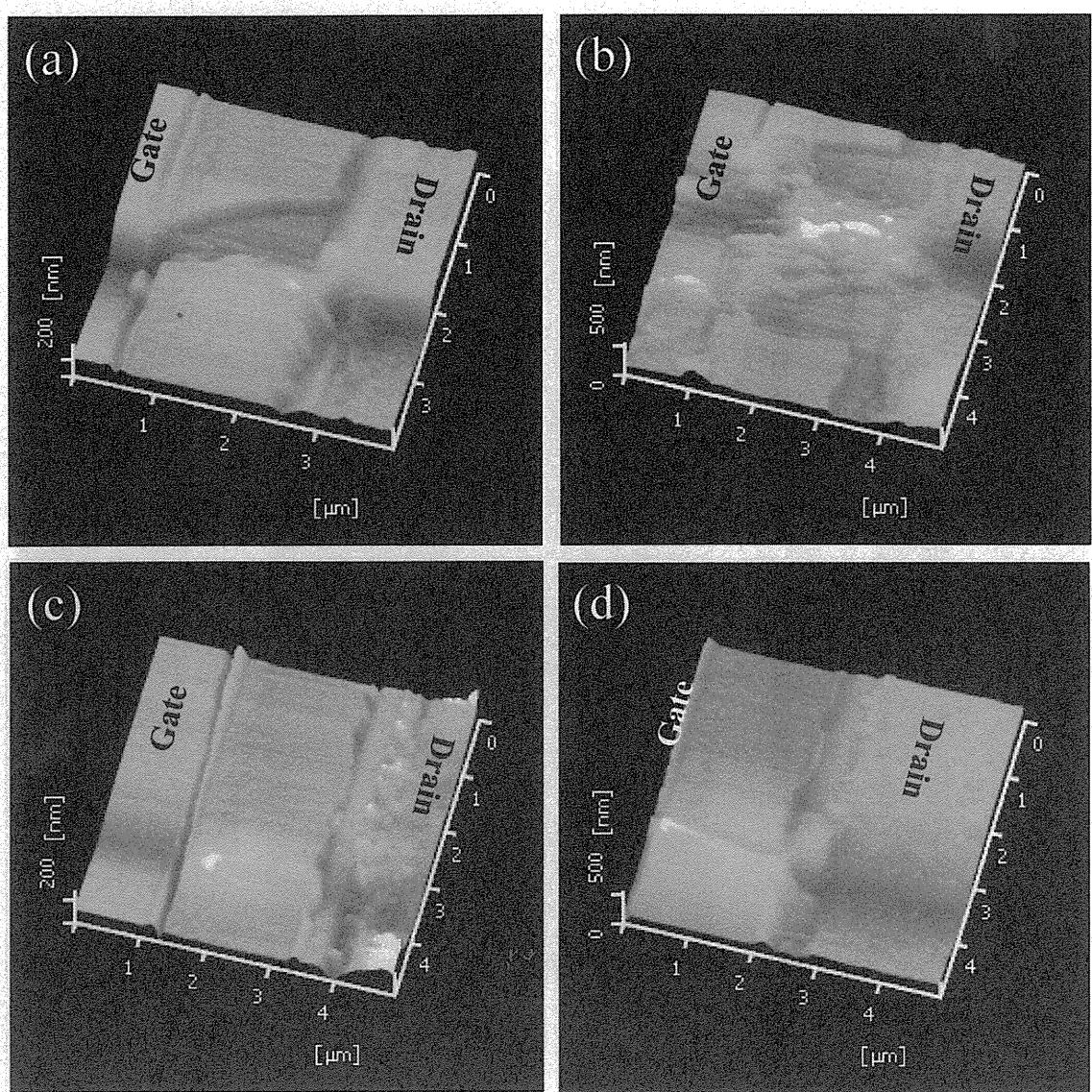


Fig. 4.7. AFM images taken with SiO_2 passivation ($V_{G\text{-stress}} = -10 \text{ V}$, $V_{D\text{-stress}} = 160 \text{ V}$).

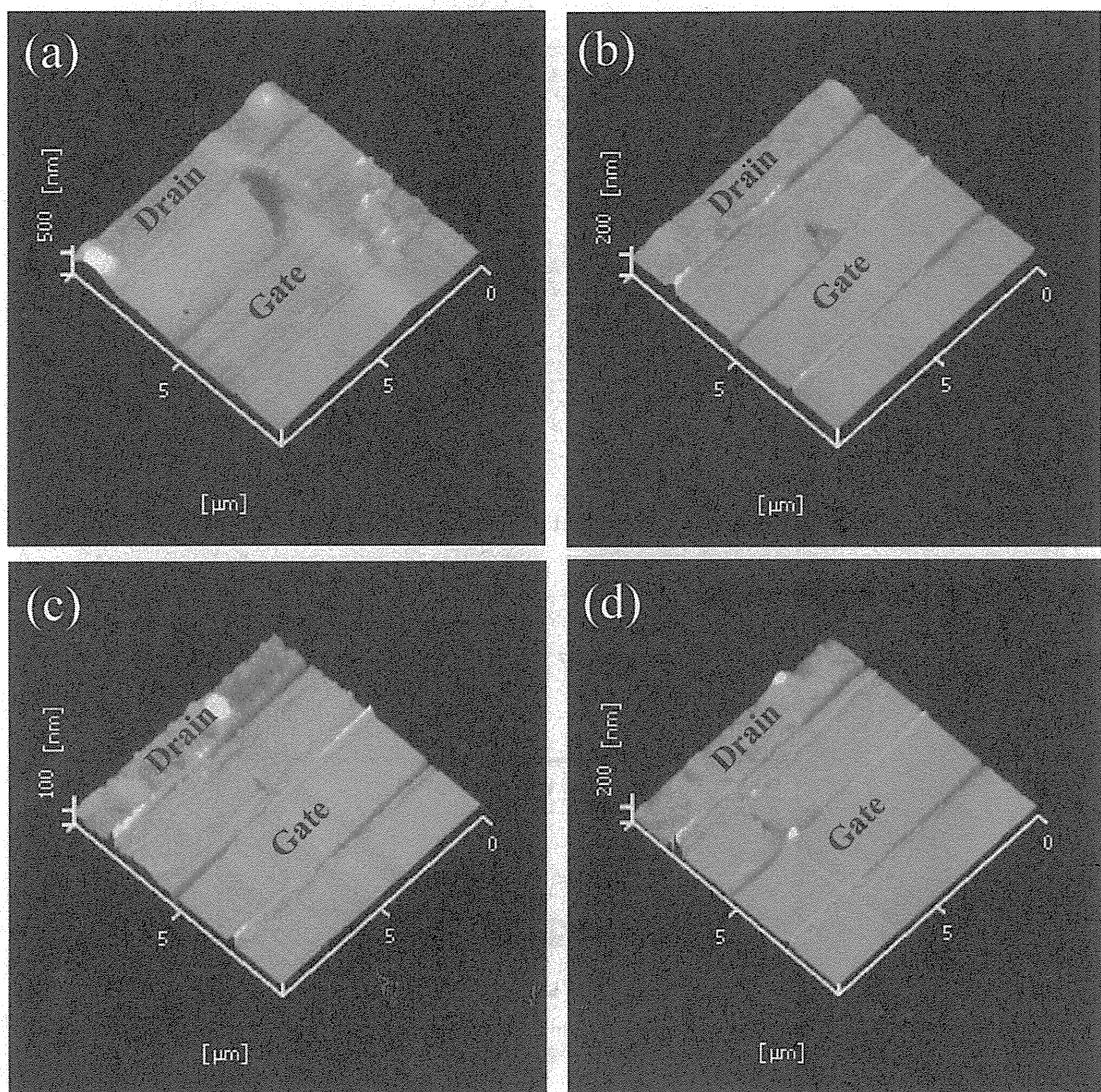


Fig. 4.8. AFM images taken after the removal of SiO_2 passivation. Pits were formed at gate-drain spacing and at drain edge were moved towards gate edge on increasing bias stress.

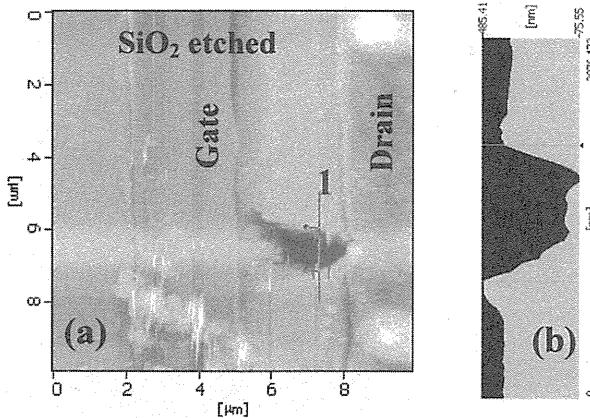


Fig. 4.9. AFM image depicts the (a) origin and traveling of pit, and (b) depth of the pit.

4.4 Cyclic stress measurement

4.4.1 $V_{G\text{-stress}} = -10 \text{ V}$ and $V_{D\text{-stress}} = 100 \text{ V}$

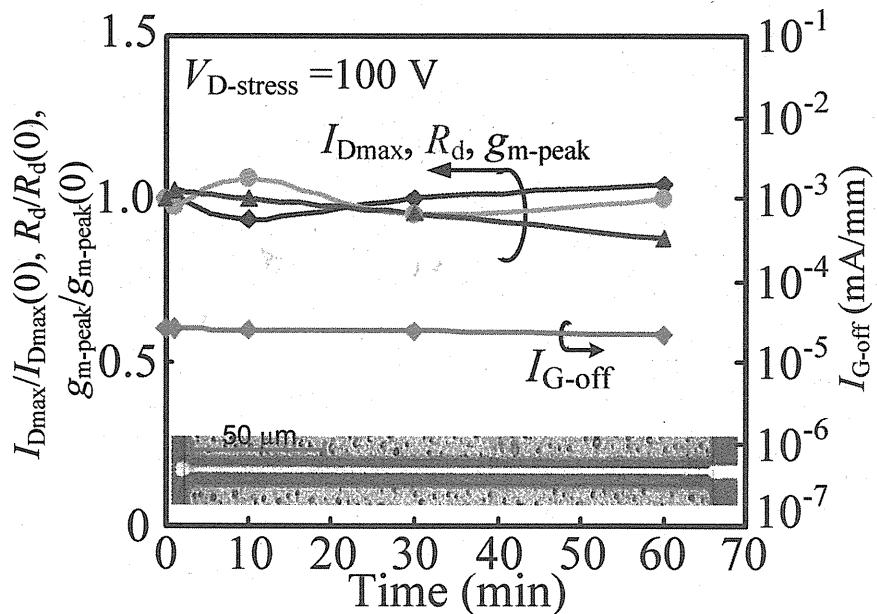


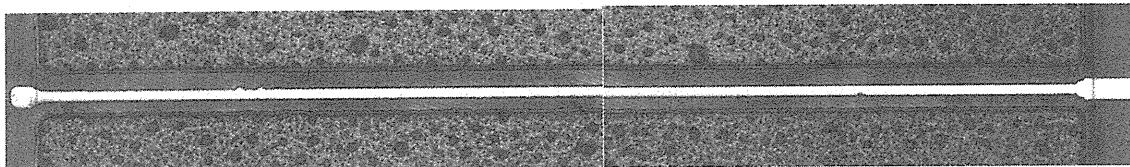
Fig. 4.10. Changes in $I_{D\text{max}}$, R_d , $g_{m\text{-peak}}$, and $I_{G\text{-off}}$ at constant voltage as the function of time reveals negligible degradation. The SEM images taken after 60 min reveal that there were no spots formed under constant voltage with increasing stress time (inset)

The devices were also stressed at constant $V_{D\text{-stress}} = 100 \text{ V}$ for different time periods (1, 10, 20, 30 and 60 mins). In this measurement, we did not observe any

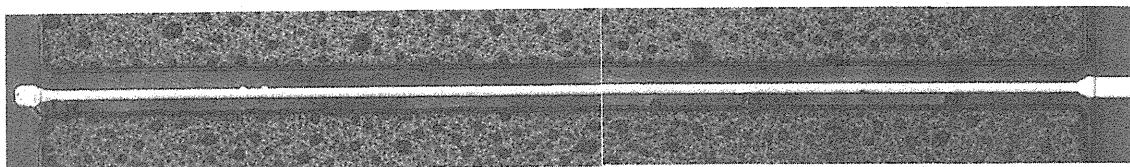
significant change in $I_{D\max}$, R_d and $I_{G\text{-off}}$ as shown in Fig. 4.10. Also no defective pits appeared in the gate-drain region at this $V_{D\text{-stress}} = 100$ V even after 60 mins of continuous stress as shown in Fig. 4.10 inset.

4.4.2 $V_{G\text{-stress}} = -10$ V and $V_{D\text{-stress}} = 150$ V

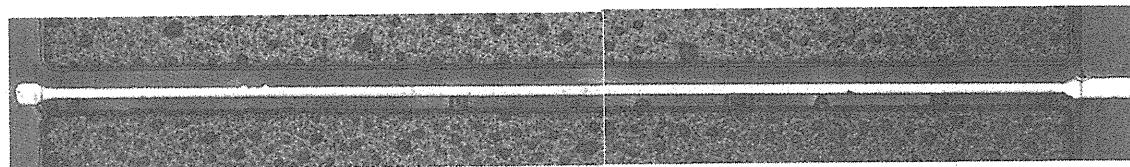
Frame1: after 1min stress time, shows one spot



Frame2: after 10min stress time, shows the appearance of new spots



Frame3: after 20min, apart from new spots some existing spots getting bigger



Frame4: after 30min, several spots observed found only at gate-drain region.

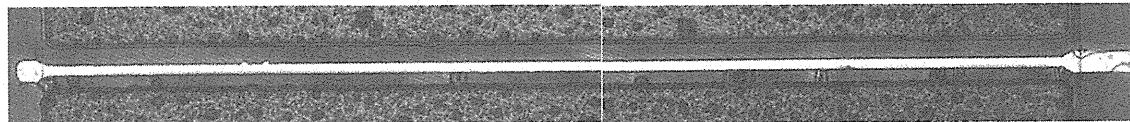


Fig. 4.11. The SEM images show spots generated from the beginning of the stress time at $V_{D\text{-stress}} = 150$ V. The number of spots was increased with increasing stress time.

For devices stressed at higher $V_{D\text{-stress}}$ of 150 V, the spots were formed from the beginning of stress time as shown in Fig. 4.11. The numbers of spots increased with the increase of stress time.

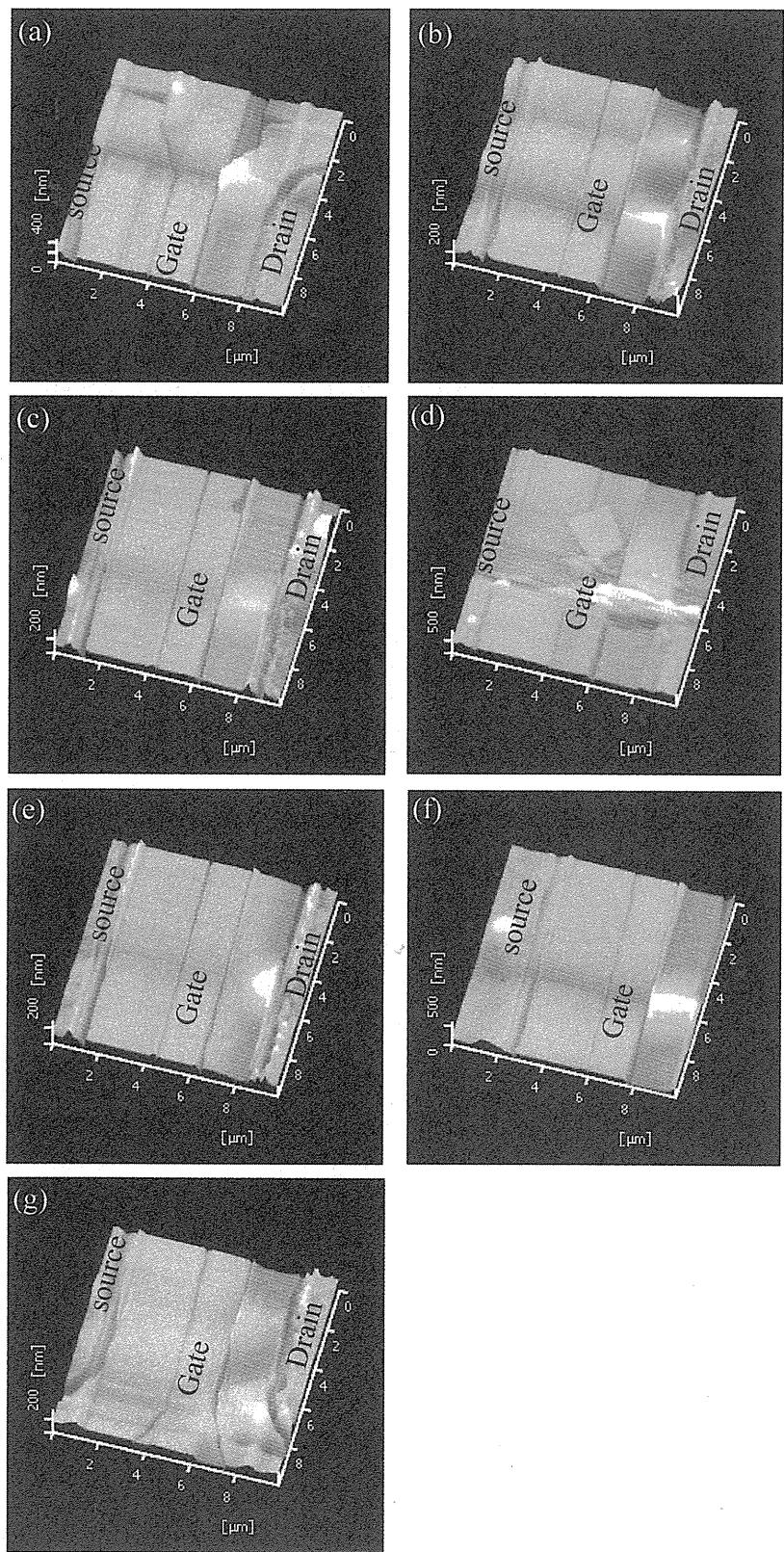


Fig. 4.12. AFM images taken with SiO_2 passivation reveals the heap of oxides at various places in gate-drain region.

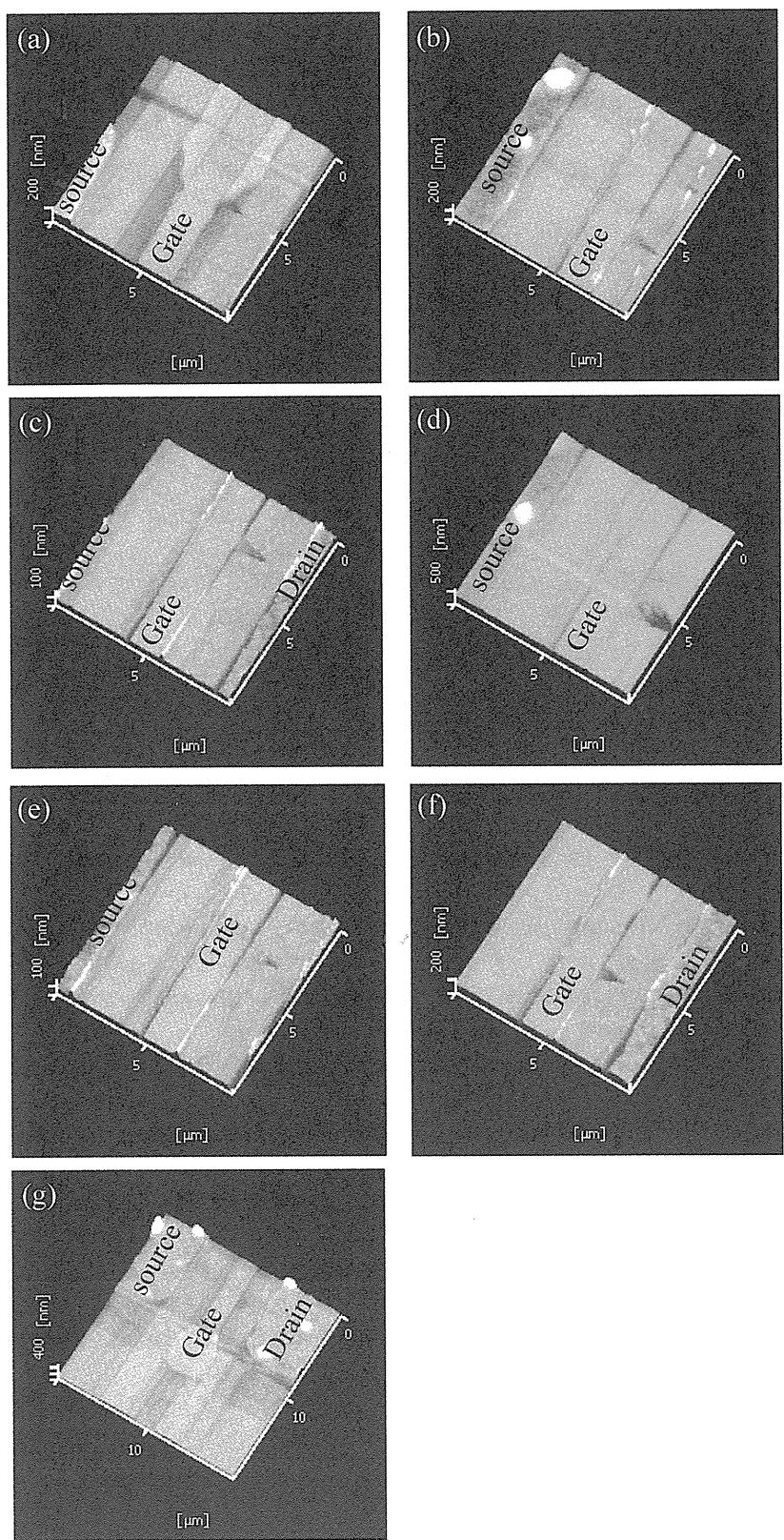


Fig. 4.13. AFM images taken without SiO_2 passivation reveals the pits formed in the middle of gate-drain spacing and traveled towards gate edge.

The AFM image taken with the SiO_2 passivation reveals the heap of oxides that present at various places in the gate-drain region shown in Fig. 4.12. No spots or defects were identified at gate-source region even at higher stress voltages. Figure 4.13 reveals the AFM images taken after the removal of SiO_2 passivation and reveals the pits were formed at the drain edge and in some cases middle of gate-drain region. These pits found traveling towards gate on increasing the stress time period.

Recently, few studies reveal the correlation between the structural defects and electrical degradation [2, 3]. The V-shaped pit defects were originated at $V_{\text{D-stress}} = 20 \text{ V}$ and the devices were highly degraded at $V_{\text{D-stress}} = 50 \text{ V}$. These pits were observed at the gate edge and reported to have a depth of 8 nm and width of 13 nm which results in sharp increase in the $I_{\text{G-off}}$. It was believed that high mechanical stress in the AlGaN layer due to the high-voltage stress results in the formation of these defects/pits which acted as the paths for the gate leakage current. In all these reports, for AlGaN/GaN devices grown on SiC or sapphire, no one has observed a pit depth beyond 12 nm in the gate-drain region during reliability stress measurement. However, in our case for AlGaN/GaN HEMTs grown on Si with thick buffer the pits were appeared at the drain edge for $V_{\text{D-stress}} = 130 \text{ V}$. Hence, we did not observe a sudden increase in the gate leakage current but a decrease in $g_{\text{m-peak}}$ was recorded at this stress voltage. Also on increasing the stress voltage we observed an increase in number of pit at the drain edge which results in further decrease of $g_{\text{m-peak}}$. The pit depth was found to be 100 nm and in fewer cases it went up to 400 nm for higher $V_{\text{D-stress}} = 130 \text{ V}$ and above. This means, the defective pits contributing to reliability degradation is caused not only by the top 25 nm AlGaN between gate and drain, but also by a part of i-GaN buffer. Also the pits originating at the drain edge seem to be migrating towards the gate edge on increasing

the $V_{D\text{-stress}}$. It is evident from our results that before gate degradation occur the pits were generated at the drain side which believed to be originating from the i-GaN layers.

4.5 Three-terminal breakdown characterization

The three-terminal breakdown measurements have been carried out by biasing the gate at a fixed voltage and increasing the drain voltage. The leakage currents were measured with the increase in drain voltage. The possible leakage currents measured are gate leakage current (I_{gate}), source leakage current (I_{source} or I_{buffer}) and substrate leakage current (I_{sub}). The drain leakage current (I_{drain}) is the sum of I_{gate} , I_{source} , and I_{sub} . The paths of this leakage current are shown in Fig. 4.14.

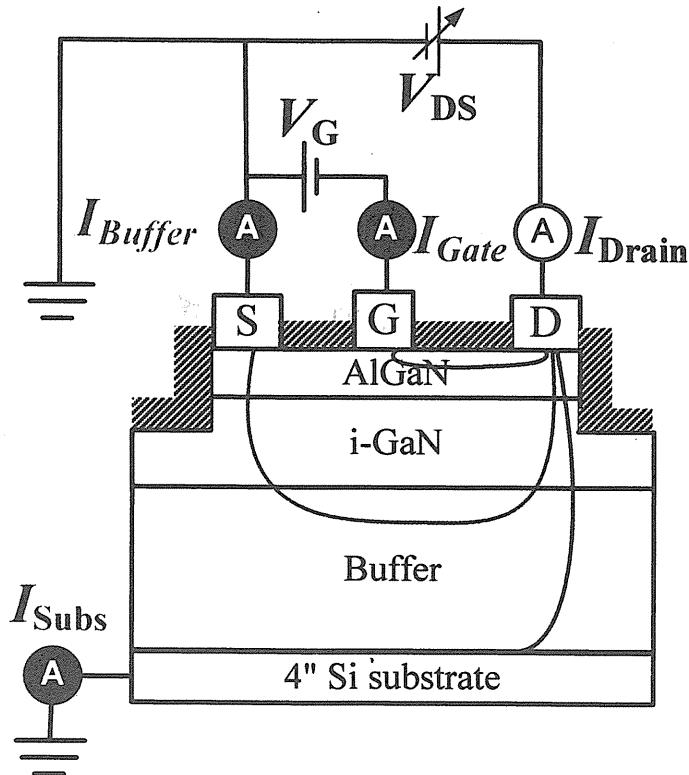


Fig. 4.14. shows the various leakage current pathways in 3-TBV for AlGaN/GaN HEMT on Si.

Three terminal off-breakdown voltage measurements were carried out by immersing the sample in an inert liquid Fluorinert (FC-40) to avoid any atmospheric influence in

the gate-drain region. Figure 4.15 shows the three terminal breakdown voltage (3TBV) for $W_g/L_{gd} = 200/4 \mu\text{m}$, where gate bias was maintained at a sub-threshold voltage of -5 V with Si substrate grounded. Our breakdown voltage is defined as the drain-source voltage at which the drain current of 1 mA/mm was observed. For all our devices an average 3TBV of 273 V was observed for $L_{gd} = 4.0 \mu\text{m}$. During the three terminal breakdown voltage measurements, the gate leakage current initially increases and then saturates till the breakdown occurs. Here it should be noted that the I_{source} and $I_{\text{substrate}}$ didn't show any significant change up to 130 V and thereafter beyond 130V there is a gradual increase in the I_{source} and $I_{\text{substrate}}$ leading to a final breakdown at 273 V. It is well understood in the case of AlGaN/GaN HEMTs on Si with thick buffer that I_{source} and $I_{\text{substrate}}$ influence the device breakdown in addition to I_{gate} .

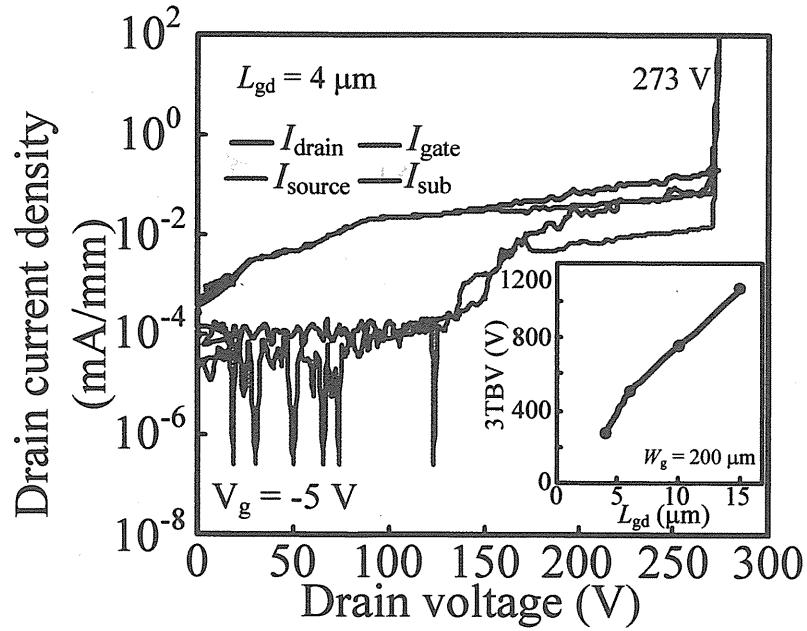


Fig. 4.15. Three-terminal breakdown voltage observed for AlGaN/GaN HEMT on Si with $W_g/L_{gd} = 200/4 \mu\text{m}$. The inset shows the linear increase in the breakdown voltage with increasing L_{gd} .

Recently, Meneghini et. al have reported a mechanism, where the breakdown is initiated by the increase in drain-source leakage current [11]. This is another indication

that the buffer leakage cannot be eliminated in the case of off-state device breakdown. Moreover this sudden increase in I_{source} and $I_{\text{substrate}}$ at 130 V corresponds to the beginning of defective pits at GaN region around $V_{\text{D-stress}} = 130$ V in microscope images. As we increase the L_{gd} , breakdown voltage increased linearly resulting a BV of 1060 V for $L_{\text{gd}} = 15 \mu\text{m}$ (Fig. 6 inset). In all these devices, gate-drain spacing varies from 4 to 15 μm shows that I_{source} and $I_{\text{substrate}}$ initiate for device breakdown.

4.6 Summary

We have studied the appearance of structural defect and its relation to electrical degradation and 3TBV. In the case of AlGaN/GaN HEMT on Si substrate several devices from the same wafer were step-stressed and showed no sudden increase in the $I_{\text{G-off}}$. Defective pits were formed in the gate-drain region at $V_{\text{D-stress}} = 130$ V and these defective pits increased in numbers with the increase in $V_{\text{D-stress}}$ with the pit depth of 100 nm and above. The 3TBV reveals that I_{source} and $I_{\text{substrate}}$ influence the device breakdown in addition to I_{gate} . From these results, it is evident that the defective pits contributing to reliability degradation is caused not only by the top 25 nm AlGaN between gate and drain, but also from a part of i-GaN buffer.

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Chapter-V: Influence of GaN Stress on Threshold Voltage Shift in AlGaN/GaN HEMTs on Si

5.1 Introduction

Though different substrates are available for the GaN epitaxial growth, the Si substrate is considered to be the most suitable because of its low cost and large-scale availability. The fundamental and key elements that has to be given attention for the growth of GaN on Si is understanding the strain involved epi-layers and forming a buffer layer made of strained superlattice structures (SLSs) to prevent large bowing and crack [1]. Large tensile stress in GaN grown on Si is undesirable because of the deterioration it causes to the crystal quality of the epitaxial layer [2]. It is widely understood that the built-in strain piezoelectric, together with the spontaneous polarization arising in the device heterostructure after growth, is responsible for the formation of two-dimensional electron gas (2DEG) at the AlGaN/GaN interface [3, 4]. Raman measurement is a useful method to evaluate the strain/stress in the GaN-on-Si [2-8]. Also, reliability becomes a bigger concern due to large lattice mismatch and thermal coefficient difference between Si and GaN [9-12]. When a high electric field is applied externally, the strain in the AlGaN layer would exceed the critical value and relaxes through defect formation leading to the deterioration of the AlGaN/GaN HEMT performance [13]. We have found that it is possible to grow crack-free epitaxial GaN films by varying the strained layer superlattice buffer thicknesses (T_{Buf}) [14]. This chapter discusses how the change in GaN epitaxy influences the strain that involved in it and influences over the device threshold voltage. We used Raman spectroscopy to study the strain and carried out electrical characterization to study the V_{th} shift. We found that there is a strong correlation between the GaN strain/stress and V_{th} shift.

5.2 Raman Analysis

Raman experiment requires a monochromatic light source, typically a laser, a spectrometer and a detector (nowadays most commonly a multichannel charge coupled device CCD). In general, the Raman signal intensity is orders of magnitude weaker than the elastic scattering intensity, hence stray light can be a considerable issue. While spectrometers are generally used to separate the elastic scattering and Raman scattering signals, the large mismatch in scattering intensity can enable the elastically scattered light to dominate the Raman light via stray light. Alternative concepts have been developed in recent years to be able to retain a high light throughput while achieving high stray light rejection, making the wider use of Raman systems possible, not only in research laboratories but also for growth and process monitoring in an industrial environment. Notch/ edge filters are being used in Raman systems to prevent elastically scattered laser light from entering the spectrometer. Often an optical microscope focuses the laser light on the material under the study and collects the scattered laser light (micro-Raman system), allowing Raman experiments with 1-2 μm spatial resolution. The high mechanical stability of such systems allows the recording of spatial maps of phonon properties over extended areas of a sample using motorized XY-stage.

The use of different laser excitation wavelengths in Raman experiments allows selective probing of phonon and therefore material properties, either averaged over a sample layer thickness or in a surface layer, for example, for optimizing metal contact formation to semiconductors. For GaN with a bandgap of 3.4eV, material properties averaged over the sample layer thickness can be probed under visible excitation wavelength (argon laser: 488 nm, 514 nm, and 532 nm), whereas surface properties can be studied using UV excitation wavelengths (HeCd laser: 325 nm) due to the absorption

of the UV laser light in the sample. In our case, for the micro-Raman spectrum measurement, a laser of 532.08 nm wavelength was used. Mostly Raman spectroscopy on (0001) surface has relevance for process and growth monitoring. The selection rules on the (0001) surface, for GaN with the E_2 and $A_1(LO)$ phonon mode at 567.5 cm^{-1} and 734.5 cm^{-1} , respectively, were clearly visible. The information on stress and crystalline quality can be extracted from the E_2 phonon frequency and line width.

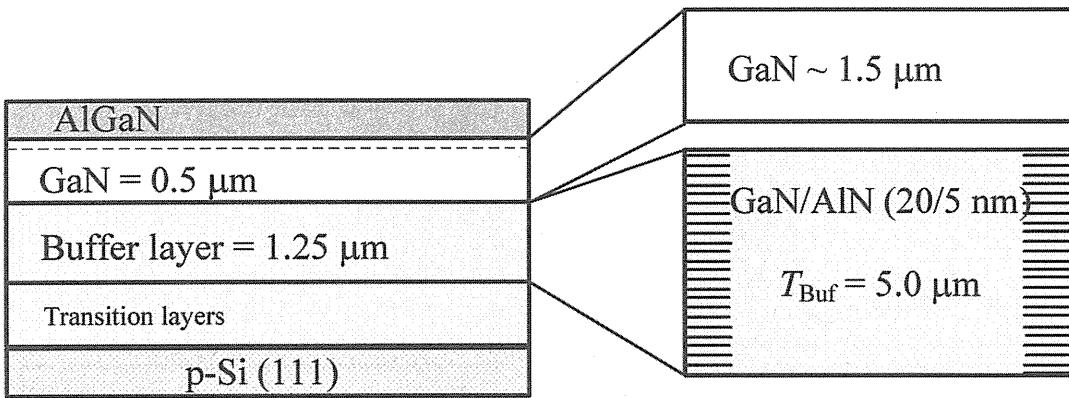


Fig. 3.1. Schematic representation AlGaN/GaN epi-structure with various buffer and GaN thicknesses.

5.3 Results and discussion

Raman spectra measurements were carried out for AlGaN/GaN epi-structure at different buffer and GaN thicknesses as shown in Fig. 3.1. For the micro-Raman spectrum measurement, a laser of 532.08 nm wavelength was used. Figure 3.2 shows the room-temperature Raman spectra of the E_2 (high) mode and $A_1(LO)$ line observed for a $T_{\text{Buf}} = 1.25, 2.5, 4.0,$ and $5.0\text{ }\mu\text{m}$ with various T_{GaN} thicknesses. The Si peak observed at 520.7 cm^{-1} which is found and also some other small peaks of Si were highlighted using star sign in all the shown figures. The E_2 (high) mode and $A_1(LO)$ peaks were identified and showed (Fig. 3.2. right side) with higher magnification.

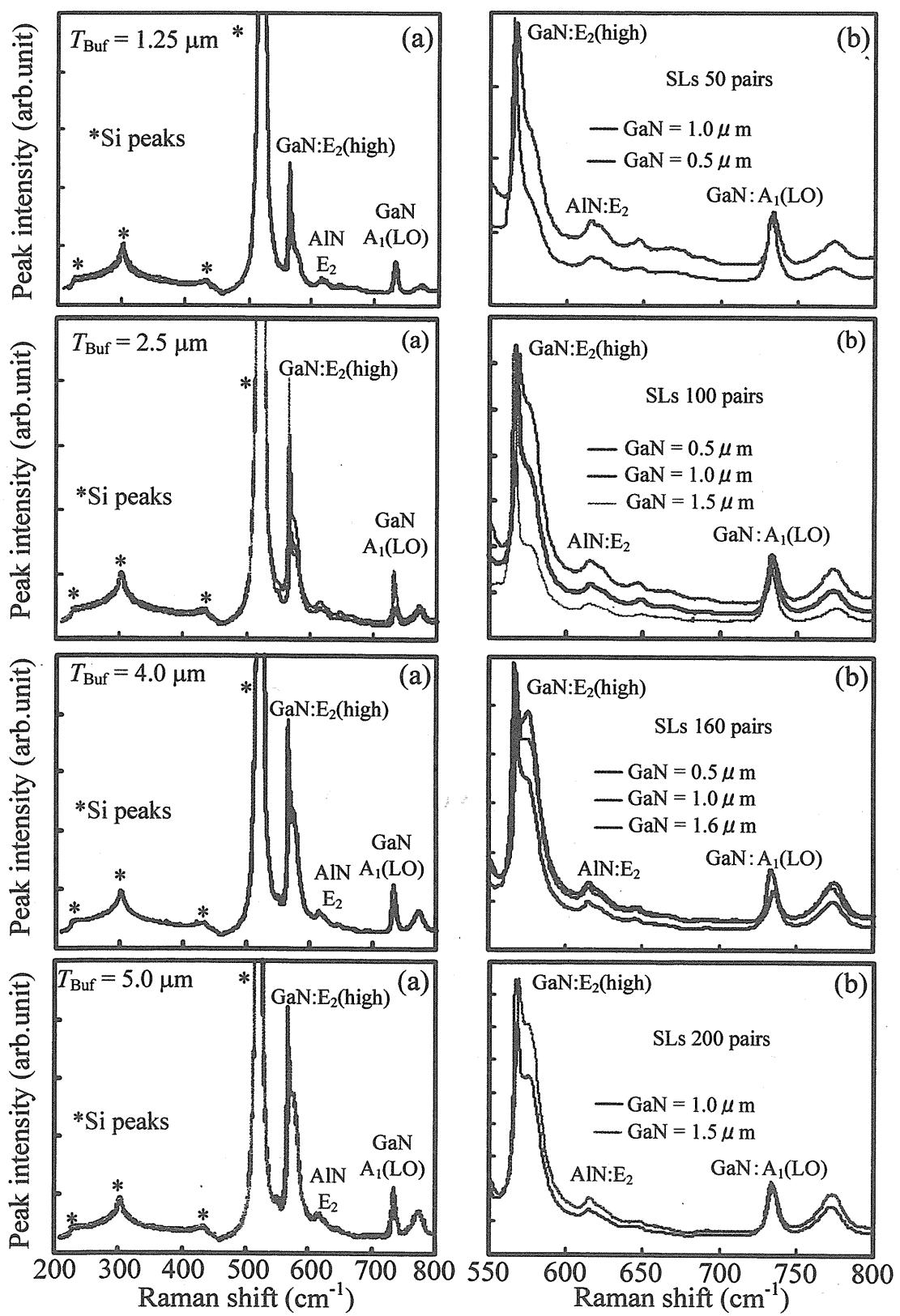


Fig. 3.2. Raman peak for various buffer thicknesses and various GaN thicknesses were also showed (Left side). The peak shift shown in a clear manner (right side).

From Fig. 3.2, it is clear that a satellite peak was found along with the E₂ (high) mode, which increases with the increase in T_{GaN} thicknesses. It is also to be noted that there is no much change in the peak intensity (except $T_{\text{Buf}} = 4.0 \mu\text{m}$, $T_{\text{GaN}} = 0.5 \mu\text{m}$) whereas there found a peak shift in each cases. To understand it further, we plotted the Raman spectra for 1 μm -thick GaN epilayers grown on Si (111) substrate with $T_{\text{Buf}} = 1.25, 2.5$, and 5.0 μm as shown in Fig. 3.3. For GaN with a band gap of 3.4 eV material properties averaged over the sample layer thickness can be probed under visible excitation wavelength [3, 15]. In general the E₂ (high) phonon peak is used to study the strain/stress present in the GaN layers. A typical unstrained GaN shows E₂ (high) phonon peak at 567.5 cm^{-1} [4, 6, 16].

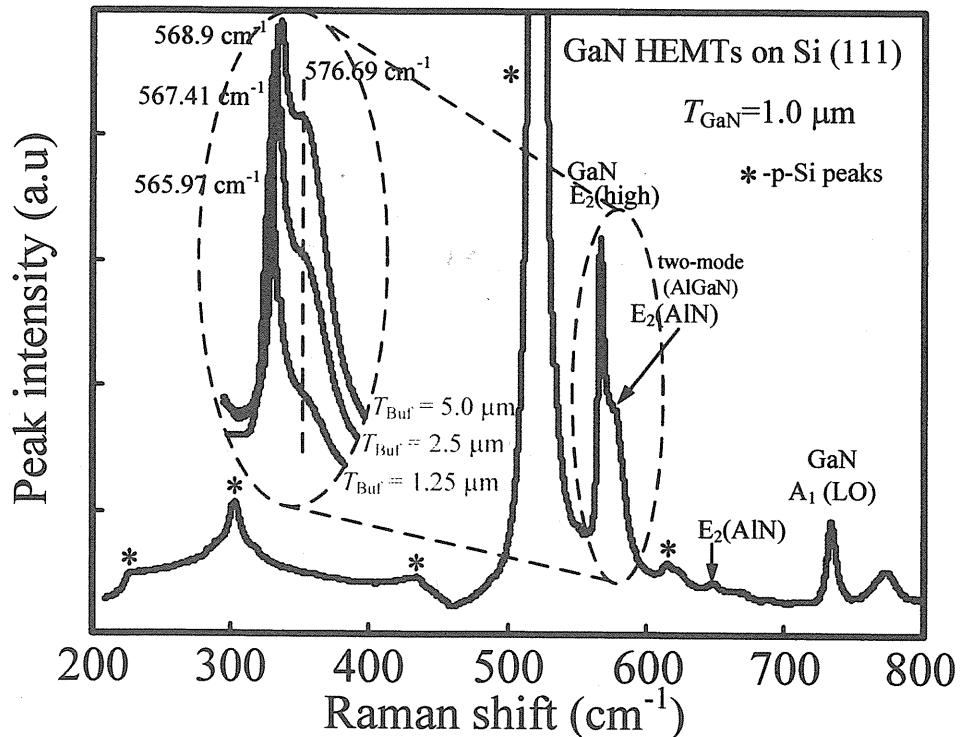


Fig. 3.3. Raman spectra obtained to find the E₂ (high) phonon peak shift with respect to buffer thickness. The inset shows the phonon peak shift for different buffer thicknesses.

We observed the phonon peak shift in GaN with the change in buffer thicknesses. The GaN E₂ (high) modes at 565.97, 567.41, and 568.9 cm^{-1} were recorded

for $T_{\text{Buf}} = 1.25, 2.5$, and $5.0 \mu\text{m}$, respectively (Fig.3.3 inset). A satellite peak was observed along with the E_2 (high) phonon peak is believed to be due to the presence of AlN (576.69 cm^{-1}) [17]. The satellite peak intensity increases with the increase in the amount of AlN that is present in the buffer layers.

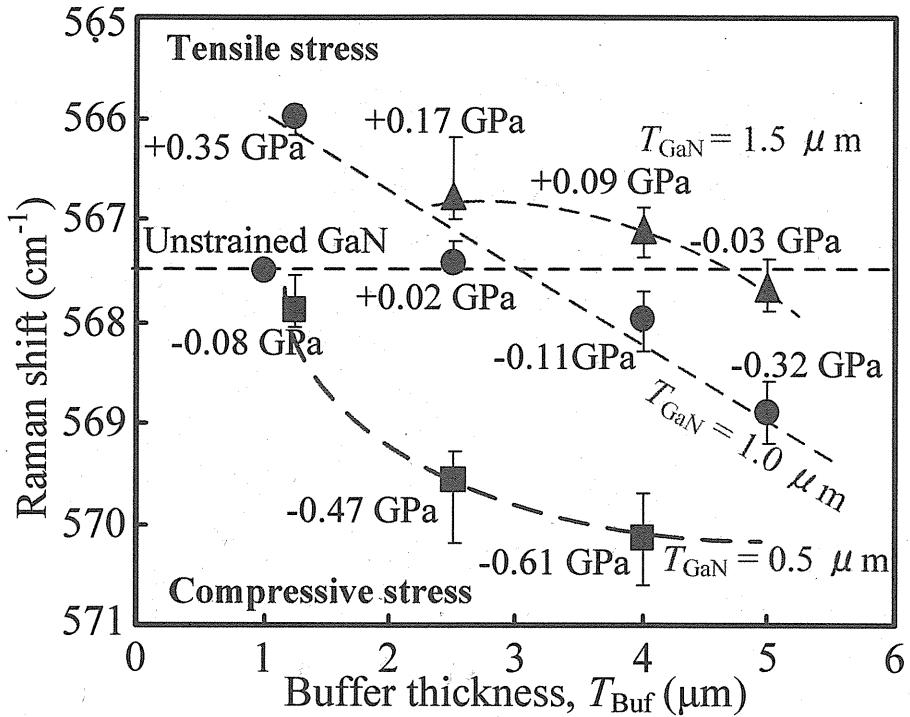


Fig. 3.4. The residual stress was calculated for the GaN E_2 (high) phonon peak shift using eq. (1) for various buffer and T_{GaN} thicknesses.

To understand the strain/stress that is present in the GaN epilayers, we calculated the amount of residual stress in the samples by using the measured phonon peak shifts of the E_2 (high) mode in the Raman spectra using the equation[4, 16, 18] below

$$\Delta\omega = \kappa_y \cdot \sigma_{xx} \quad (1)$$

where, $\Delta\omega$ is the difference in the measured peak position of the Raman peak and the theoretical peak position of an unstrained GaN (567.5 cm^{-1}). The strain coefficient (κ_y)

selected here is $4.3 \text{ cm}^{-1}\text{GPa}^{-1}$ [4, 18]. The GaN stress calculated using eq. (1) shows $+0.35$, $+0.02$, and -0.32 GPa for HEMTs with $T_{\text{Buf}} = 1.25, 2.5$, and $5.0 \mu\text{m}$, respectively. To further understand the change in GaN strain/stress, various epistructures were grown with different GaN and buffer thicknesses for this study as shown in Fig. 3.4. We found that GaN strain/stress changes from tensile to compressive with the change in T_{Buf} and T_{GaN} . Thus, changes in T_{Buf} and T_{GaN} play a key role in the strain modulation during the growth and the cooling down process.

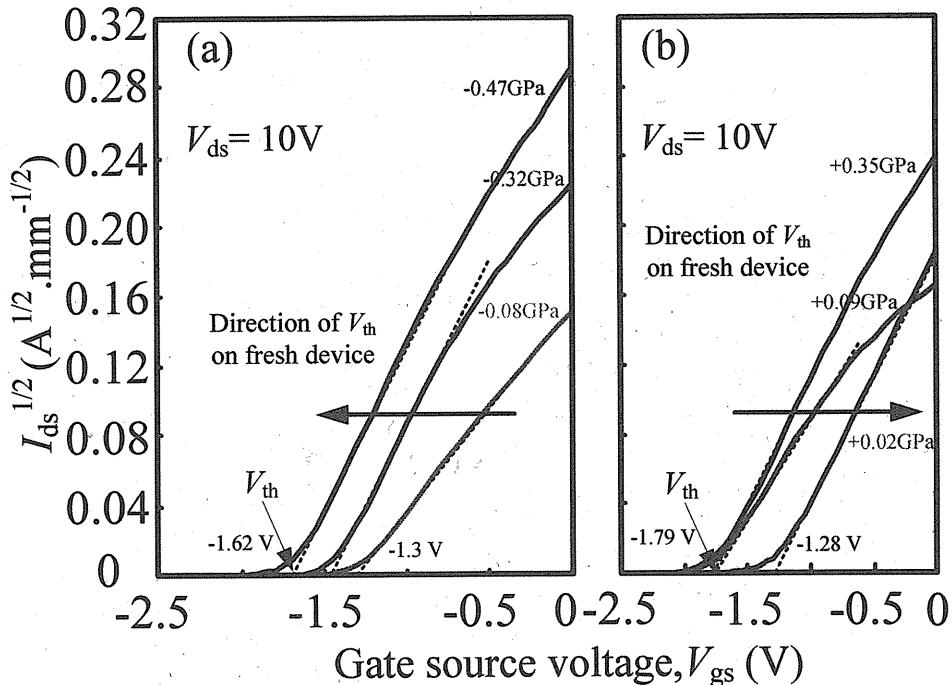


Fig. 3.5. Transfer characteristics of AlGaN/GaN HEMTs on Si with various GaN strain/stress devices.

The device fabrication process and its parameter were kept same as it is mentioned in chapter-3. The step-stress measurement was carried out at off-state bias stress ($V_{\text{G-stress}} = -10 \text{ V}$) under dark condition. The $V_{\text{D-stress}}$ ranging from 5 to 70 V with 5 V step was applied to HEMTs for duration of 600 s. In this measurement several devices were tested until a set of similar reliability data were observed. On completion of off-state bias stress, these devices were rested for 30 min before carrying out normal dc

I_{ds} - V_{ds} and transfer characteristics to obtain the device recovery rate. Threshold voltage (V_{th}) is the gate-source voltage at which the 2DEG channel is completely depleted from mobile carriers.

The transfer characteristics were measured on these different epilayers as shown in Fig. 3.5. The change in the V_{th} shift was observed with the change in the built-in GaN strain/stress present in the as-grown wafer. V_{th} of the device was determined from the linear region by applying a small drain bias ($V_{DS} \ll V_{GS}$), and plot of the square root of I_{ds} versus the V_{gs} as shown in Fig. 3.5. Figure 3.5(a) shows the negative V_{th} shift with the increase in compressive GaN strain/stress, whereas the positive V_{th} shift with the reduction in the tensile GaN strain/stress is shown in Fig. 3.5(b).

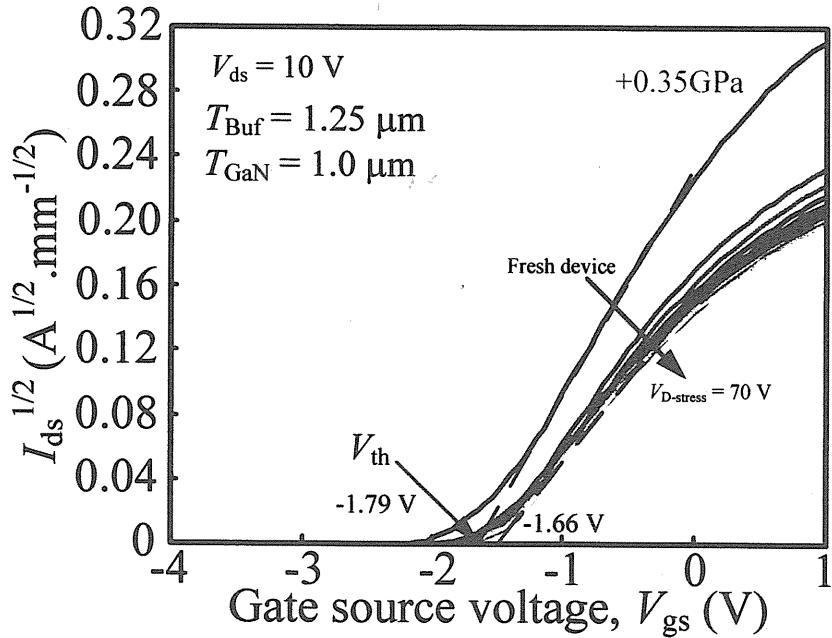


Fig. 3.6. AlGaN/GaN HEMTs on Si substrate with $T_{Buf} = 1.25 \mu m$ show $+0.35$ GPa GaN stress, the I_{ds} - V_{gs} characteristics were carried out on fresh devices, and after every $V_{D\text{-stress}}$, show that the V_{th} shifts positively.

It is believed that the built-in GaN strain/stress that present in the epilayers is influencing the change in the V_{th} shift. During off-state bias stress, there occurs a high

vertical electrostatic field, and additional strain/stress was generated in both the AlGaN and GaN regions. Figure 3.6. shows the transfer curves of AlGaN/GaN HEMT with $T_{Buf} = 1.25 \mu\text{m}$ measured before and after off-state bias stress. The I_{ds} - V_{gs} curves were acquired with the increase in $V_{D\text{-stress}}$ by sweeping the gate source voltage from negative to positive bias. The transfer characteristics show a reduction in the I_{ds} and change in the V_{th} shift with the increase in $V_{D\text{-stress}}$. Here, it should be noted that V_{th} shift towards positive bias. V_{th} for HEMTs on $T_{Buf} = 1.25 \mu\text{m}$ is found to be -1.79 V on a fresh device, and on increasing $V_{D\text{-stress}}$, V_{th} tends to shift positively and resulted in -1.66 V at $V_{D\text{-stress}} = 70 \text{ V}$. Hence, a positive V_{th} shift for HEMTs on $T_{Buf} = 1.25 \mu\text{m}$ devices were observed. Whereas for HEMTs on $T_{Buf} = 5.0 \mu\text{m}$, V_{th} shifts negatively from -1.60 to -1.84 V, and for HEMTs on $T_{Buf} = 2.5 \mu\text{m}$, V_{th} of -1.28 V was observed with negligible V_{th} shift. It is evident that GaN strain affects the electrostatics of AlGaN/GaN HEMTs through a combination of piezoelectric effect [19].

The changes in V_{th} shift with the increase in $V_{D\text{-stress}}$ for HEMTs with different epilayers are shown in Fig. 3.7. The figure shows the shift in V_{th} at $V_{D\text{-stress}} = 10, 30$, and 70 V with respect to a fresh device. It is evident that the AlGaN/GaN HEMT epilayers with tensile strain/stress show a positive V_{th} shift and those with compressive strain/stress show a negative V_{th} shift after the off-state bias stress. This suggests that there is a strong correlation between the type of strain/stress in GaN and the V_{th} shift. This difference in the polarity of the shift in threshold voltage strongly suggests that the nature of traps created during electrical stress is different for tensile strain/stress and compressive strain/stress that are present in GaN thicknesses. It has been reported that the device degradation occurs owing to the vertical electrostatic field that introduces additional tensile strain through the distortion of the crystal lattice in the AlGaN barrier,

resulting in an inverse piezoelectric effect [16].

We believe that a change in the GaN strain leads to a change in the 2DEG channel width, which in turn changes the 2DEG carrier densities with the increase in buffer thickness. In the past, our group established that dislocation densities were reduced on increasing T_{Buf} for the growth of GaN on Si [14].

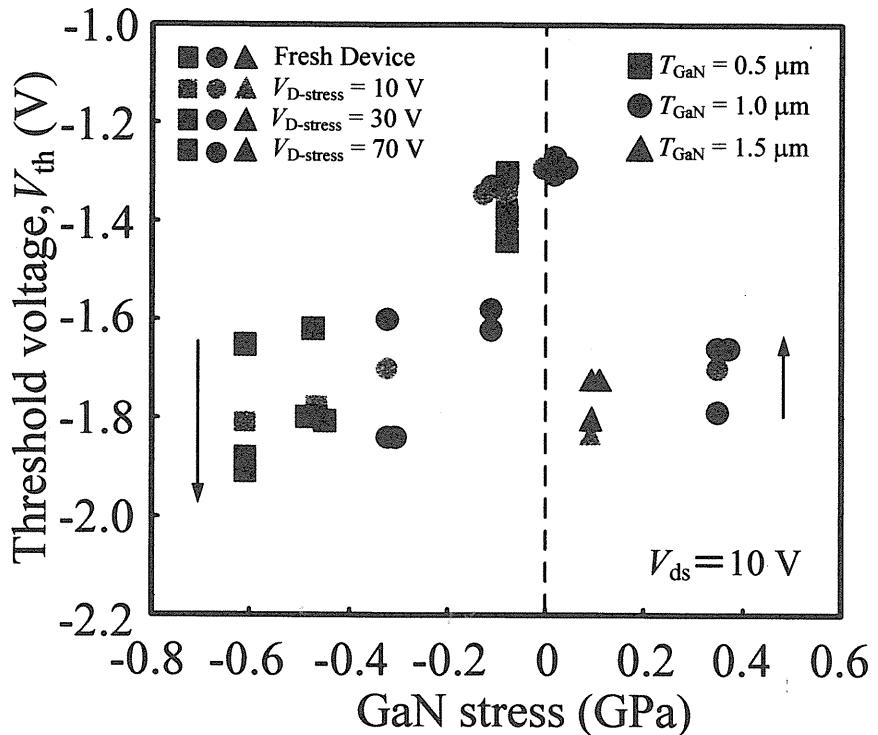


Fig. 3.7. GaN stress vs threshold voltage shift on off-state bias stress measured for various HEMT structures grown with different T_{Buf} and T_{GaN} thicknesses.

As discussed in [16], during off-state bias stress, an additional tensile strain/stress is created with the increase in vertical electrostatic field. In the case of HEMTs on $T_{\text{Buf}} = 1.25 \mu\text{m}$ devices, the GaN with a tensile strain/stress and large dislocation density produces acceptor-like trap states, which become negatively charged [20, 21]. This increases the trapping centers for electrons in the 2DEG channel resulting in the decrease of the electron concentration in the channel leading to a reduction in the I_{ds} and positive V_{th} shift. These trapped electrons were recovered fully by keeping the

device at rest for 30 min. In the case of HEMTs on $T_{\text{Buf}} = 5.0 \mu\text{m}$ devices, the dislocation densities were low and GaN show a compressive stress. For GaN with compressive stress it is believed that there is a reduction in the number of acceptor-like traps, causing more electrons to fill the 2DEG and leading to a more negative V_{th} shift. During off-state bias stress, we observed a negative V_{th} shift with reduction in I_{ds} similar to results reported by other authors in which they argue that electrons in the channel can achieve sufficient energy to be injected in the AlGaN, at the gate/AlGaN interface, and buffer [15]. After 30 mins recovery time, I_{ds} showed a partial recovery with the kink effect and V_{th} showed no recovery. Further studies are necessary to explain the mechanism behind the compressive GaN stress/strain and negative V_{th} shift. Whereas, in the case of $T_{\text{Buf}} = 2.5 \mu\text{m}$, GaN strain/stress found relaxed to that of the unstrained GaN, which operates the device within the elastic energy of the AlGaN/GaN HEMTs on high $V_{\text{D-stress}}$, results in a negligible V_{th} shift. We believe that the relaxed GaN strain/stress or less GaN strain/stress is responsible for the negligible I_{ds} degradation, and a negligible V_{th} shift results in a good and reliable performance.

5.4 Summary

We have evaluated the device reliability of AlGaN/GaN HEMTs on Si with various buffer and GaN thicknesses using off-state bias stress. The results illustrate the importance of GaN strain/stress for the degradation and reliability of AlGaN/GaN HEMTs. Raman spectra reveal the change in the GaN strain/stress with the change in buffer and GaN thicknesses. We found that there is a strong correlation between the V_{th} shift and GaN strain/stress. The GaN with minimum strain or relaxed strain results in less I_{ds} degradation with the negligible V_{th} shift during off-state bias stress.

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Chapter-VI: Conclusion

In this thesis a systematic study of electrical reliability of AlGaN/GaN high electron mobility transistors (HEMT) grown on silicon substrate with various buffer thicknesses (T_{Buf}) using MOCVD are discussed. An experimental framework for studying the reliability of GaN HEMTs has been developed. This framework extracts the important device parameters like I_{Dmax} , R_D , g_m -peak, I_{G-off} and V_{th} shift as the device undergoes degradation. In our experiments different stress methodology and stress conditions were carried out on GaN HEMTs with different buffer and GaN thicknesses. Also, electroluminescence, atomic force microscope, Keyence 3D laser microscope images and three terminal breakdown voltage measurements were carried out to understand the device failure mechanisms.

We have developed DC step-stress test at pinch off condition by increasing the drain-source voltage at room temperature. We define the critical voltage as the abrupt increase in the gate leakage current or the sub-threshold drain leakage current which is irreversible at that particular voltage. The main conclusions drawn from this study are discussed below.

For an AlGaN/GaN HEMT on Si grown with a $T_{Buf} = 1.25 \mu\text{m}$, the degradation in I_{Dmax} , R_D , and g_m -peak of the devices occurs from the beginning and it is believed to be due to the native defects present in the virgin device. In the case of AlGaN/GaN HEMT grown on $T_{Buf} = 2.5 \mu\text{m}$, the critical voltage was observed at higher drain bias stress above 100 V. These devices also show a decrease in $I-V$ and transfer characteristics but there is negligible shift in the threshold voltage observed. The electroluminescence reveals the bright spot at the sudden increase in the gate leakage current. This is believed to be due to the increase in high electric field at the gate edge of the drain side

resulting in non uniform emission. Whereas in the case of the AlGaN/GaN HEMT grown on $T_{Buf} = 4.0$ and $5.0 \mu\text{m}$, no critical voltage was observed. Also electroluminescence shows a uniform emission throughout the gate-drain region. There was no significant change in the I_{Dmax} , R_D , and $g_{m\text{-peak}}$ in the case of $T_{Buf} = 5.0 \mu\text{m}$ under off-state, ON-state and $V_{D\text{-stress}} = 0$ state condition up to $V_{D\text{-stress}} / -V_{G\text{-stress}} = 45 \text{ V}$.

The off-state bias stress carried out at higher drain bias reveals that AlGaN/GaN HEMT grown on $T_{Buf} = 5.0 \mu\text{m}$ results in pit formation at the drain edge instead of gate edge. Hence, no abrupt/sudden increase in the gate leakage current was observed. On the contrary, a $g_{m\text{-peak}}$ degradation at this $V_{D\text{-stress}} = 130 \text{ V}$ was observed for HEMTs grown on $T_{Buf} = 5.0 \mu\text{m}$. On further increase in stress voltage the number of pits and the pit depth increased. The pit depth of 100 nm increased as high as 400 nm . The three-terminal breakdown characteristics reveal that the source and substrate leakage current initiates the device breakdown along with the gate leakage current. This depicts that apart from AlGaN barrier the GaN buffer is also influencing the device degradation.

Further it was found that on increasing the buffer thickness the quality of GaN was improved. It is also found that on varying the buffer and GaN thicknesses the strain in the GaN changes. The GaN strain changed from tensile to compressive with the change in buffer and GaN thicknesses. This change in GaN strain reflects on the V_{th} shift of the device. The V_{th} shift tends to moves positive and negative for GaN with tensile and compressive strain, respectively. On applying electrical stress V_{th} tend to shift more positive and negative. However, GaN with minimum strain shows negligible V_{th} shift on fresh device and also after electrical bias stress.

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