1. Investigation of MIS-type GaN-based HEMT grown by MOCVD on Silicon (111) Substrate

Abstract

In this study, metal-organic chemical vapor disposition (MOCVD) grown GaN based metal-insulator/oxide-semiconductor high-electron-mobility transistors (MIS-HEMTs) on silicon (111) substrate are presented. In order to reduce the AlGaN/GaN heterostructure related traps, thicker super-lattice structures (SLS) were employed. A detailed XRC and Hall measurements of the AlGaN/GaN HEMT heterostructures grown using thicker SLS showed reduced edge dislocation densities and increased Hall mobilities. Trap characterization by frequency dependent conductance analyses (FDCA) showed a remarkable decrease in fast traps related to the AlGaN/GaN layers confirming improvements in the AlGaN/GaN heterostructures.

A process compatible Al_2O_3 based AlGaN/GaN MOS-HEMT was discussed. The device characteristics of MOS-HEMT compared with the normal HEMT shows reduced gate leakage and higher breakdown voltage (*BV*). The *BV* and power device figure-of-merit (FOM) for Al_2O_3/AlGaN/GaN MOS-HEMT was 431 V and 1.89 x 10^8 $V^2\Omega^{-1}cm^{-2}$ respectively. The trapping characteristics by FDCA on the MOS-HEMT showed the surface related slow traps (~ms) has been passivated by Al_2O_3 layer.

The importance of using a thin *in-situ* MOCVD grown AlN as a passivating layer for AlGaN/GaN MIS-HEMTs on Si was also discussed. The trapping analyses and device characterizations revealed that low growth temperature of AlN layer favor less defect AlN/AlGaN/GaN MIS-HEMT structures. Therefore, the AlGaN/GaN heterostructure related traps can be minimized by growing the AlGaN/GaN heterostructures on thick buffer layers and the surface related traps can be minimized by using a passivating material or a high~κ insulating material.

Introduction

1.1. Foreword

The beginning of 21st century has seen enormous progress and advancements in the solid state electronics and its applications in the areas of wireless and tele-communications, information technology as well as radar and satellite appliances. The progress in electronics industry although could always compete with the demands and requirements of the global market. These requirements may include aspects of ultra-high power, high efficiency, high linearity, high operating frequency and high-speed switching devices. To meet the broad necessity, the integrated circuit with as many transistors with sub-micron sizes should be closely packed. The Moore's law even predicted that the number of silicon transistors per chip has doubled ever since its invention in early 1970's as a progress of very-large-scale-integration (VLSI). These demands have made the researchers to push the operating power performance in the pioneer silicon and later Ge and GaAs based electronic devices closed to theoretical limits. SiC then widely believed to be a better candidate, although it appeared to be not truly microwave technology in terms of its relatively low carrier transport properties.

Further, these challenges also opened up wide band gap GaN based materials to be suitable alternative workhorse and promising candidates to compete or over-run the race with the predecessors. The advantages in Al_xGaN/GaN based devices includes cost effective, large bandgap (3.4 eV), high breakdown limit ($\geq$ 3 MV/cm), high electron mobility ($\geq$ 1300 cm^2/vs at 300 K) and very high carrier saturation velocity ($v_{sat} \cong 2 \times 10^7$ cm/s). The various applications of GaN based high power and high frequency devices are shown in fig. 1.1. These applications range from solid state lightings to space modules.

As shown in the figure 1.1 GaN based high power radio frequency (rf) amplifiers find applications in satellites, wireless base stations and radio communications. Further, they find importance in defense and military warfare utilities and space modules etc. GaN based high voltage devices are used for power transmission purposes and grids. Other potential applications include Monolithic Microwave Integrated Circuits (MMICs) and high power amplifiers.

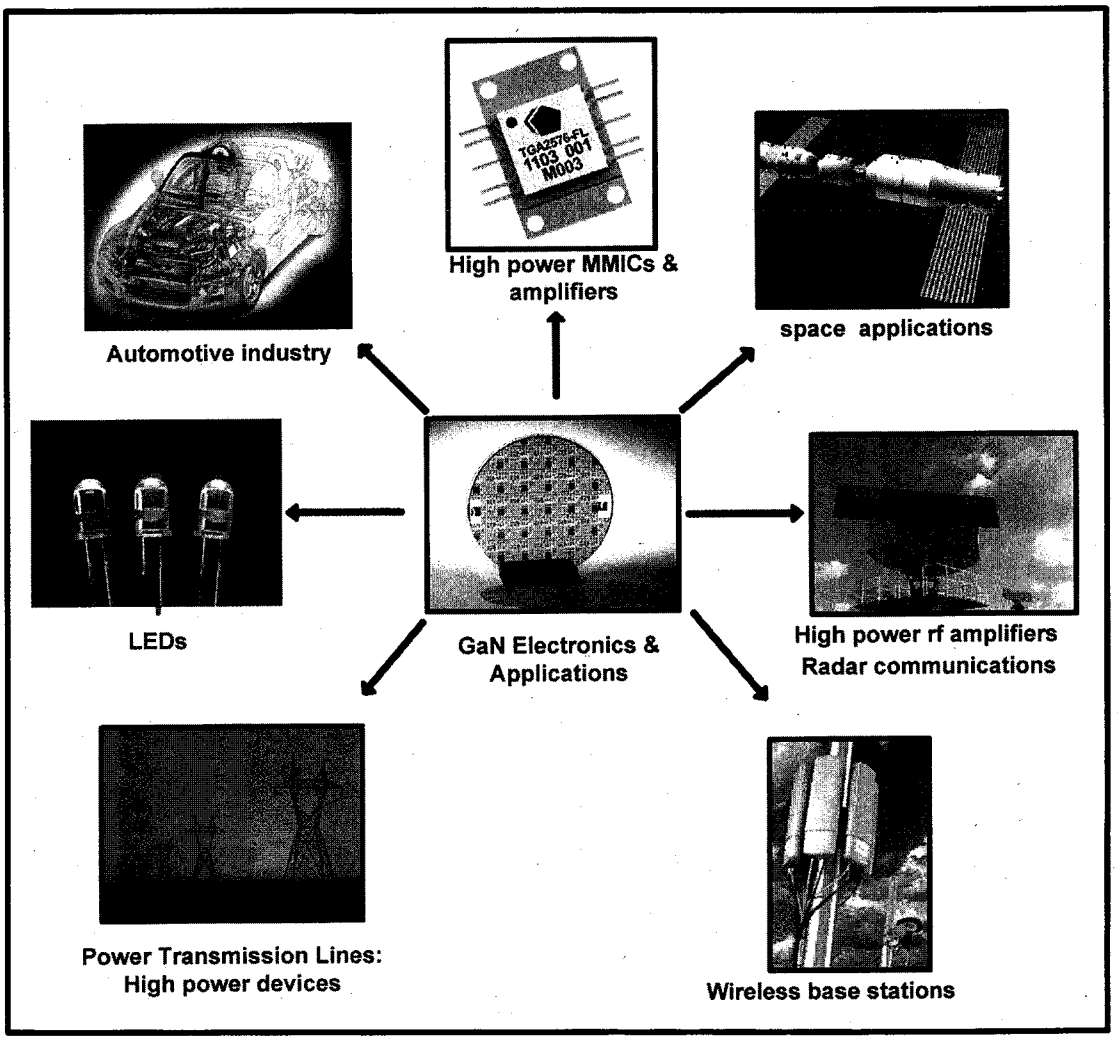

FIG. 1.1. Application areas of GaN based electronics.

Wurtzite AlN, GaN and InN have direct band gap energies of 6.2, 3.4 and 0.7 eV respectively for potential application in a broad spectrum of wavelength. Bandgap engineering and suitable alloy composition of the Nitrides makes them favorable candidates for blue-green and ultraviolet (UV) light emitting diodes (LEDs) [1-3], UV-lasers [4] and active photo detectors in the wavelength between visible and UV regions [5-6].

Other promising prospects of GaN devices are that, they offer high power, high frequency and high temperature electronics. Again the wide band gap makes the GaN materials more favourable for high temperature applications, since they go intrinsic at elevated temperatures compared to the counterparts like Si, Ge and GaAs. The critical breakdown field of the GaN is approximately the square of the band gap energy and it has been theoretically estimated to be ≥ 3 MV/cm which is ten folds higher than the small bandgap semiconductors like Si and GaAs with relatively low breakdown values of 0.3 and 0.4 MV/cm respevtively [7]. This simply means that GaN devices can be used for high power applications which can operate at elevated temperature. Therfore less cooling is required and involves cost effective process to dissipiate the heat generated. Alongside, GaN has excellent carrier transport properities such as good moblity and drift velocity which are highly desirable for high speed switiching devices and microwave rectifiers etc. The comparision of electronic properties of GaN with other leading semicondutor materials are presented in table. 1.1 [8-11]. With a high combined figure of merit (CFOM) value, it is unambiguously believed that GaN devices can deliver high power, high temperature and high frequency future needs.

Table. 1.1. Comparison of electronic properties of various semiconductors at 300 K.

Property	Si	GaAs	6H-SiC	4H-SiC	GaN
Bandgap E_g (eV)	1.12	1.43	2.86	3.02	3.39
Breakdown Field E_B (MV/cm)	0.3	0.4	2.4	2.2	3.0
Electron Mobility μ (cm^2/Vs)	1500	8500	800	460	2000
Drift Velocity $\upsilon_{s\text{-}max}$ (10^7 cm/s)	1.0	2.0	2.0	2.7	3.0
Thermal Conductivity χ (W/cmK)	1.5	0.5	4.9	4.9	1.5
Dielectric Constant ε	11.8	12.8	10	9.7	9.5
CFOM = $\chi.\varepsilon.\mu\,\upsilon_s\,E_B^2/(\chi.\varepsilon.\mu\,\upsilon_s.\,E_B^2)_{Si}$	1	7	295	222	290

(CFOM = Combined Figure of Merit for high temperature, high power and high frequency applications)

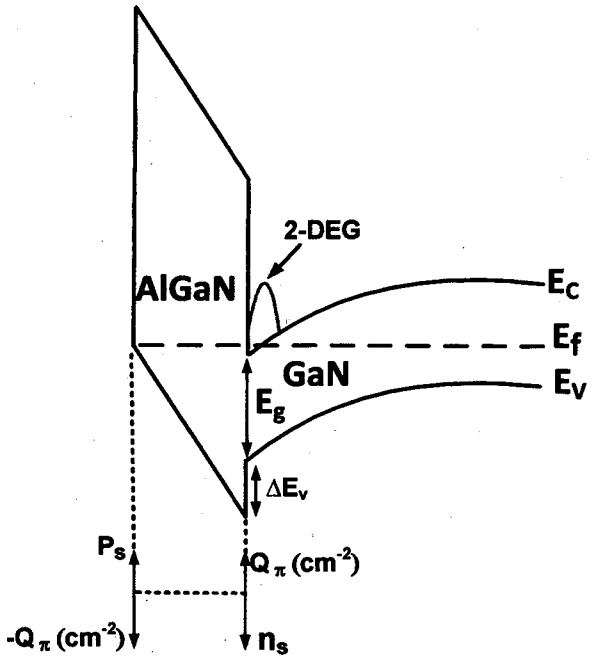

FIG. 1.2. Band diagram of AlGaN/GaN heterostructures with conduction band-discontinuity and formation of 2-DEG in the AlGaN/GaN quantum well.

The most amazing feature or property of Wurtzite III-nitrides is the Quantum well (see fig. 1.2) formed at the hetero-interface between GaN and AlGaN layers. A high concentration of two dimensional electron gas (2-DEG) is accumulated at the quantum well near the AlGaN/GaN hetero-interface due to large conduction band discontinuity and built-in piezoelectric (P_{Pe}) and spontaneous polarization (P_{Sp}) effects in AlGaN/GaN material system. This property makes the AlGaN/GaN heterostructure system more suitable for high power and high frequency electronics.

The maximum output power for the high power electronic device is given by the equation 1.1,

$$P_{max} = \frac{1}{8} V_{max} \cdot I_{max} \tag{1.1}$$

$$I_{max} = V.n_s.\upsilon_{sat} \tag{1.2}$$

Therefore for maximum output power (P_{max}), maximum current (I_{max}) and maximum voltage (V_{max}) are required. As given in equation 1.2, the drain current density can be pushed to the maximum by utilizing the advantages of P_{Pe} and P_{Se} polarization effects, as mentioned before and consequently increasing the sheet carrier concentration (n_s) [12]. This can be easily achieved by increasing the mole fraction of Al in the barrier layer without strain relaxation. Further, the v_{sat} of the carriers can also be improved by minimizing the gate width and the gate length extension. For this very reason, owing to the increased carrier concentration near the hetero-interface along with good mobility, the AlGaN/GaN heterostructure based field-effect transistors (FETs) are otherwise termed as AlGaN/GaN High-Electron-Mobility transistors (HEMTs).

1.2. Progress of GaN technology: Present status and issues

Extensive research has been made for the development of easily growable Si and GaAs smiconductors. While Si and GaAs reseach reached its peak and pushed to their theoretical limits, the growth of III-nitrides emerged its infant stage in the late 1960s. Although, GaN devices seems to be highly promising, at present it has its own challenges even after the first successful evoultion of AlGaN/GaN HEMTs [13]. One among the technological difficulty is the lack of large size ideal substrate to grow the GaN based devices. Even after forty years ever since its evolution, finding a better substrate suitable for the epitaxial growth of GaN is still challenging to meet all the requirements (see fig. 1.3). An ideal substrate candidate for the epitaxial growth of GaN is the one which satisfies or requires the following criterias [14-17],

- ✓ low cost availability of large sized substrates
- ✓ less lattice mismatch with bulk GaN
- ✓ low thermal expansion (TEC) when bulk GaN crystals are grown.

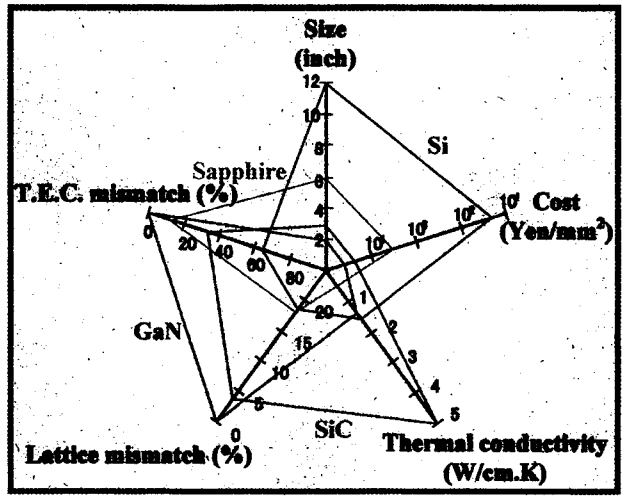

FIG.1.3. Schematic representation of various substrates available and their propertiesrelative with GaN.

As shown in the fig. 1.3, homo-epitaxial growth of GaN on free-standing GaN substrate has negligible lattice mismatch and low dislocation densities in the order of 10^6 cm^{-2} [18]. However, the limited availability of such substrate with large diameter is further hindered by its high cost. While 6H-SiC substrates are available in small size, yet their costs are too high for large scale commercial production of GaN wafers. While large size sapphire substrates are available at expensive costs, their poor thermal conductivity makes GaN devices difficult to dissipate heat generated during high power operations. Amano *et al.*, showed the growth of high quality GaN films on sapphire substrates using a low-temperature AlN buffer layer grown using metal organic vapor phase epitaxial growth [19].

On the other hand, availability of less expense and large scale Si substrates are the center of the attraction for GaN power electronics. However, the growth of high quality GaN on silicon substrates has its own challenges, such as high dislocation densities (10^9~10^{11} cm^{-2}) [19], cracks and deep pits [20-21] due to large lattice mismatch (17 %). Also, there is a large difference in thermal mismatch coefficients (~55%) between GaN and Si. These challenges have to be overcome in order to realize high quality GaN based optoelectronic and electronic devices on silicon substrates. To realize the mass production of GaN electronic devices on large sized wafers for high power and high frequency applications the epitaxial growth conditions of GaN on Si substrates has to be improved.

1.3. Scope of the Present Work: Background and motivation

Although, GaN HEMT technology finds extensive applications in the areas of high temperature, high power and high frequency, there are few serious issues which are

yet to be solved. One among the serious issues is the trap states at different locations existing in AlGaN/GaN HEMTs as shown in the figs. 1.4. (a) and (b) respectively. The location of these trap states can be identified as AlGaN surface, the AlGaN/GaN hetero-interface and the deep level buffer traps [22, 23]. The origin of these trap states can be due to various factors such as interruption of crystal periodicity, dangling bonds, interface roughness, dislocation, impurities and defects well known to exist in group III-nitrides.

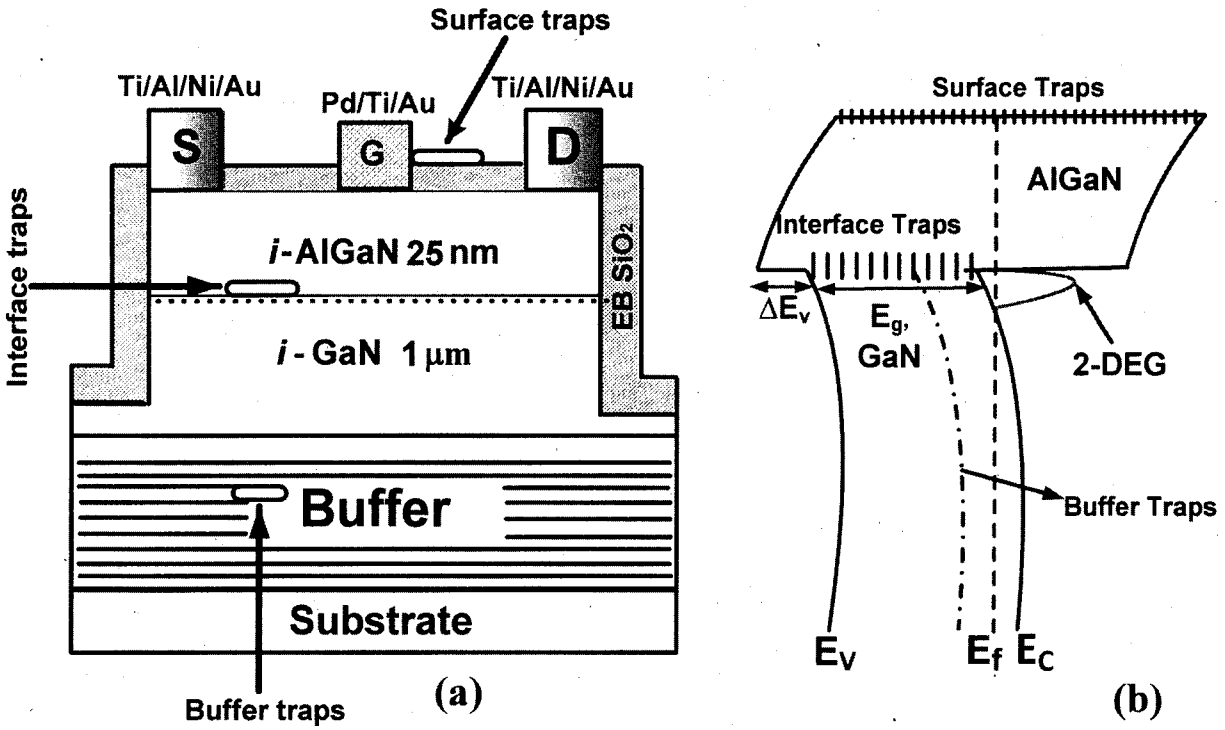

FIG. 1.4. (a) Schematic representation of typical AlGaN/GaN HEMT. (b) Corresponding energy band diagram with various traps and their location in the AlGaN/GaN HEMT heterostructure.

The trap is itself a serious problem and therefore can deteriorate the transistor performance in DC and RF conditions. The origin of the surface traps can sometimes be due to the device process such as plasma damages while mesa-etching and exposure of

semiconductor surface to acids and alkalis. The traps can act as trapping centers and can partially deplete the 2-DEG. The hetero-interface trap states can scatter the 2-DEG there by limiting the mobility of the carriers. The presence of surface traps can act as virtual gate depleting the channel electrons as well extending the depleting region [24]. Excess amount of these unwanted traps would eventually limit the maximum current available from a device during a microwave power measurement because of discharging of this virtual gate. As a result, there is current collapse in the AlGaN/GaN HEMTs. The presence of positive charges on the AlGaN surface induced by process damages such as nitrogen vacancies would in-turn enhance the Schottky leakage and limit the breakdown voltage [25]. Because of these problems, if the device is not good at DC operation, it is rather not going to be good at RF. Hence, the presence of the traps irrespective of its location is a serious pertinent problem that needs to be focused and improved.

1.4. Research goal and objectives

The main purpose and objective of this research is therefore

(i) to study the location and nature of these traps, and

(ii) to minimize the trap density.

a) To locate and minimize hetero-interface traps (D_{it}):

There can be considerable amount of hetero-interface traps (D_{it}) around the AlGaN layer adjacent to the GaN channel as shown in figs. 1.4. (a) and (b) respectively. These traps can be electrically active and have specific time constant for trapping and detrapping of carriers. The exact origin of this hetero-interface trap has not yet been fully understood. However these can represent material imperfections such as impurities, dislocations, point defects etc. Even the small lattice mismatch (~2.2 %) between GaN

channel and AlGaN barrier layer can cause the existence of hetero-interface traps. The presence of these traps can seriously deteriorate the carrier reduction and mobilities. These traps cannot be quantitatively identified by conventional capacitance-voltage (*CV*) techniques. Further, the most commonly used Terman method cannot be extended to the AlGaN/GaN heterostructures and hence suitable measurements are needed for the qualitative examination and quantitative estimation of these traps. Hence, in this work frequency dependent conductance analyses which can simultaneously estimate both the hetero-interface traps and surface traps will be employed.

b) To locate and minimize surface-related traps:

There are also AlGaN surface-related traps present in the AlGaN/GaN based HEMTs. The origin of these surface states can be due to process such as exposure of AlGaN surface to alkalis and acids while processing. Further, the nitrogen vacancies, ionized impurities and the dangling bonds caused during the plasma based mesa-etching can mostly cause the existence of surface states. The surface related trap states have time constants in the order of ~ ms.

The presence of these surface related traps can eventually form virtual gate and can partially deplete the 2-DEG which can cause the drain current slump. This can seriously deteriorate the performance of AlGaN/GaN HEMT operation in DC and RF conditions [24, 25]. Hence there is a serious necessary to identify and minimize the surface states for effective high power and high frequency operations. While quantitative analysis of the surface states is itself a challenging issue, the next obstacle to overcome is the reduction of surface traps. The ultimate solution is the realization of AlGaN/GaN based MOS/MIS-HEMTs. Utilization of a good quality oxide/insulator layer would in-

turn alleviate or minimize the existence of surface-related slow traps. On the other hand, if the interface formed between the oxide/insulator and the AlGaN is not of best quality, it can also limit MOS-devices from efficient operation. Therefore, choosing a good insulator/oxide and appropriate deposition condition is very essential for AlGaN/GaN based MOS-HEMTs. Apart from the surface and hetero-interface traps there can be buffer related traps which can also affect the performance of HEMTs if present in large volume. These buffer traps can be identified using deep level transient spectroscopy techniques [26].

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Chapter 2

MOCVD Growth of AlGaN/GaN HEMT structures on 4-inch silicon substrates

2.1. Introduction

Most of the III-V Nitrides and its related compounds are either grown using MOCVD or molecular beam epitaxial (MBE) method. The most widely used technique for the high quality growth of GaN is the MOCVD. The advantages of MOCVD grown nitrides are i) faster growth than MBE, few microns of epilayers can be grown per hour, ii) multi-wafer capability easily achievable (4 to 6 wafers can be grown), iii) higher growth temperature, which favors highly thermodynamically stable product and iv) quality of epitaxial layer (atomically sharp interface) is always better than the MBE [1-5]. However, few disadvantages may include difficulty in monitoring the growth rate exactly since no *in-situ* RHEED measurements are possible due to high pressure. Also, post growth cooling can sometimes introduces structural defects.

The advantage of MBE includes the ability to monitor the growth by *in-situ* RHEED measurements, low temperature growth and the possibilities to use plasma or laser assisted growth. Nevertheless, the disadvantages are need ultra-high vaccum, low growth rate and very expensive. Other less commonly used technique for the growth of III-V semiconductors are liquid phase epitaxy (LPE) and hydride vapor pressure epitaxy (HVPE) [6-9] which produce reasonable quality GaN epitaxial films with no sharp atomic interfaces.

Overall, the MOCVD technique has produced the highest quality GaN based devices till date. Because of the economy and flexibility of the process, the quality of the

materials produced, and the scalability of the technology, MOCVD has come to dominate the heteroepitaxial growth of III-V semiconductors.

2.2. MOCVD growth of AlGaN/GaN HEMT structures

The general reaction for MOCVD grown III-V binary or ternary nitrides is based on the pure gas phase chemical reaction between highly volatile organometallic chemical precursors with nitride source. The vapor phase chemical reaction lead to the highly stable III-V nitride compound with highly volatile by-products. The general chemical reaction [10-11] between organometallic III-precursor and NH_3 gas is given by equation 2.1,

$$R_3M_{(g)} + NH_{3(g)} \rightarrow MN + 3RH \qquad (2.1)$$

where R is alkyl group like CH_3 or C_2H_5 and M is group III metal atoms like Al, Ga or In. The MOCVD growth of GaN is widely done by introducing the metal-alkyl precursor Trimethyl Gallium (TMG) and ammonia (NH_3) into the reaction chamber with the substrate heated at elevated temperature (≥ 1000 °C). The reaction is represented by the equation 2.2,

$$(CH_3)Ga_{(g)} + NH_{3(g)} \rightarrow GaN_{(s)} + 3CH_{4(g)}\uparrow \qquad (2.2)$$

Similarly, heterostructures involving ternary compounds such as $Al_xGa_{1-x}N$ or $In_xGa_{1-x}N$ can be grown by the reaction of respective metal-alkyls and ammonia as given in the equation 2.3,

$$x(CH_3)Al_{(g)} + 1\text{-}x(CH_3)Ga_{(g)} + NH_{3(g)} \rightarrow Al_xGa_{1-x}N_{(s)} + x\,(1\text{-}x)CH_{4(g)}\uparrow \qquad (2.3)$$

In this MOCVD process, growth can take place as high as 1000-1200 °C. The growth can be optimized based on the substrate used that is SiC, sapphire or Si where the nucleation layers can be varied depending on the substrate's property. For example, two

pretreatment steps are essential for the growth of high quality GaN films on sapphire substrates, a high temperature nitridation of the sapphire surface followed by the deposition of buffer layer [12]. The nitridation of the sapphire was found to result in the formation of relaxed AlN layer, which acts subsequently as a buffer layer. Some of the substrate property and its consequences in the MOCVD GaN epitaxial growth are; (i) Lateral lattice constant (a) mismatch will lead to high dislocation density, (ii) Vertical lattice constant (c) mismatch can lead to anti-phase boundaries and inversion domain boundaries, (iii) Co-efficient of thermal expansion mismatch will lead to thermally induced stress and cracks in epitaxial layer and (iv) Low thermal conductivity can make poor heat conduction which is unfavorable for high power devices.

Alongside with the substrate properties, the growth of high quality MOCVD epitaxial films also depends on the temperature and III-V flux ratio. If the temperature is too high it might result in desorption and nitrogen vacancies whereas, the low temperature growth can result in impurities incorporation and structural defects. Similarly, III-V flux ratio when too high, there will be low surface mobility for the III-metallic atoms leading to structural defects. On the other hand, too low III-V flux ratio will ultimately result in nitrogen vacancies and auto background doping. Therefore, for good MOCVD grown epitaxial layer the III-V flux ratio and temperature should be optimized in addition to finding a better substrate candidate. The MOCVD growth will always result in polarizing *c*-plane of GaN which is preferable for III-V electronic devices. Thus, the state-of-the-art MOCVD GaN based HEMT technology relies in less-defect AlGaN/GaN epilayers. The MOCVD growth of GaN on free standing GaN, sapphire and SiC are considered to be expensive ones and well established.

2.3. Present challenges in MOCVD growth of AlGaN/GaN structures on silicon

Silicon can be a promising substrate for the MOCVD growth of GaN due substrate's large size availability (upto 12″), low cost and large thermal conductivity. However, there is large lattice mismatch (~17 %) and difference in thermal expansion coefficient (~55%) for GaN on Si that leads to a high defect density like pits and cracks. Figure 2.1 (a) and (b) shows the schematic representation of how cracks or deep pits are formed and how cracks and pits free epilayers are grown using SLS. The thermal expansion of GaN is much larger than that of Si, so the epi-wafer becomes concave shape, and a tensile stress is applied to the GaN epilayer, mostly resulting in cracks. The formation of deep pits is believed to be due to the melt-back etching of Gallium atoms into Si substrate, while the cracks are due to the tensile stress [13-14].

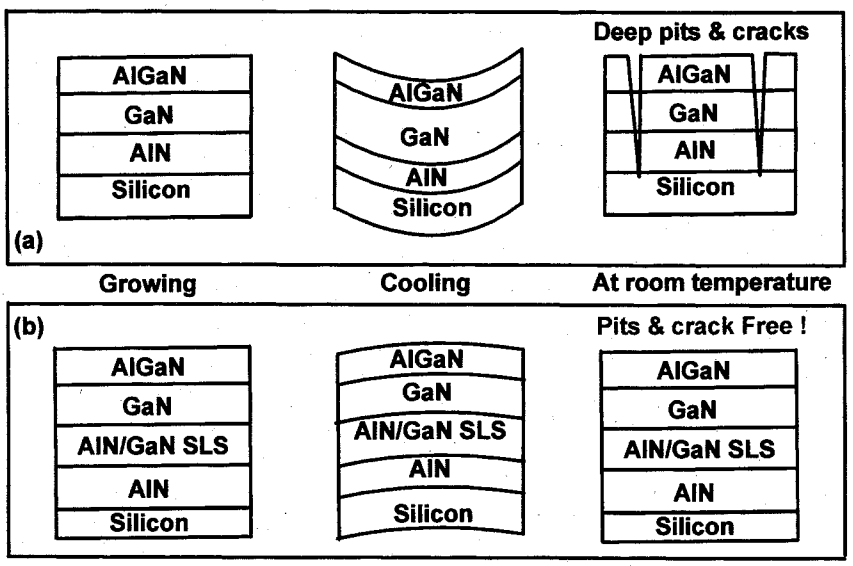

FIG. 2.1. (a) Schematic representation of cracks and pits formation during the MOCVD growth of AlGaN/GaN/Si HEMT. (b) Pits and crack free AlGaN/GaN/Si HEMT structures using AlN/GaN based super lattice structures (SLS).

The presence of these pits tends to degrade the optical and electrical properties such as increased sheet carrier density and decreased carrier mobilities in GaN devices

[15]. The deep pits are clearly visible on the AlGaN surface as shown in fig. 2.2 (a) optical microscopic view and in fig. 2.2. (b) AFM view. Apart from these pits and cracks, there can be large concentration of treading edge dislocations owing to the aforementioned lattice mismatch for GaN on Si. GaN epitaxial layer on Si can have dislocation densities of the order of 10^{8}-10^{11} cm^{-2} depending on the growth and buffer layers involved [16].

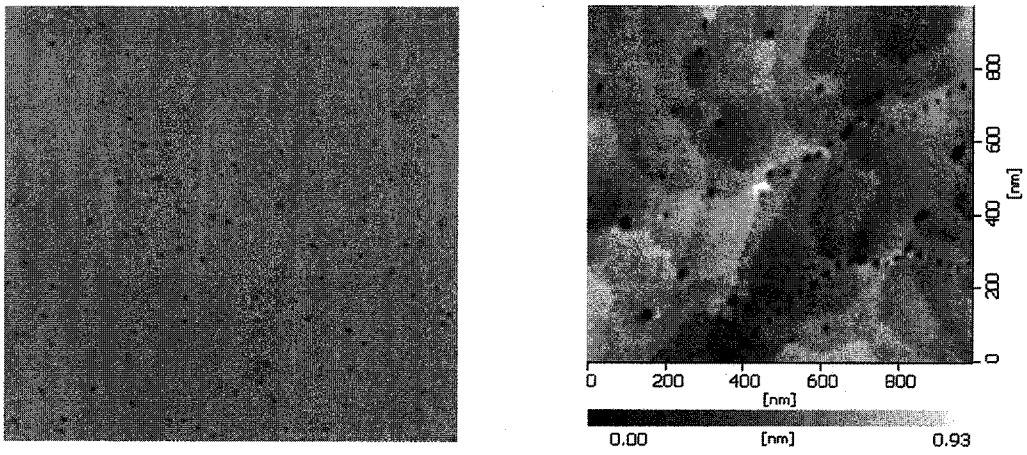

FIG. 2.2. (a) Optical microscopic view of pits in AlGaN surface. (b) AFM view of pits on the AlGaN surface.

Furthermore, the deep pits can increase the leakage currents in the GaN based HEMT devices, which in turn can limit the breakdown voltage, hampering the high power operations [13]. Therefore, these deep pits have to be eliminated in order to increase the transport properties of the GaN HEMT structures and to enhance the high power applications. This can be done by careful design of the nucleation layer for GaN on Si with high resistive buffer layers. As mentioned, the origin of deep pits is found to be the silicon surface (~a) and the pits extend vertically through the buffer layers (~b) and

to the GaN/AlGaN heterostructure (~c) as shown in figs. 2.3 (a) and (b) respectively. Whenever the dislocations reach the surface it ends in a pit. This makes it possible for AFM to record dislocations due to equilibrium between surface tension and line tension.

Further, the presence of these pits and cracks can seriously affect the device characteristics such as Schottky gate leakage and current collàpse. Various transport mechanisms such as conduction through dislocation states by hopping and tunneling assisted by the dislocation states are accounted for the gate leakage. However, the formations of these kinds of deep pits and cracks can be eliminated by canceling the tensile stress in the GaN layer by using thick multipairs of GaN/AlN super lattice structure.

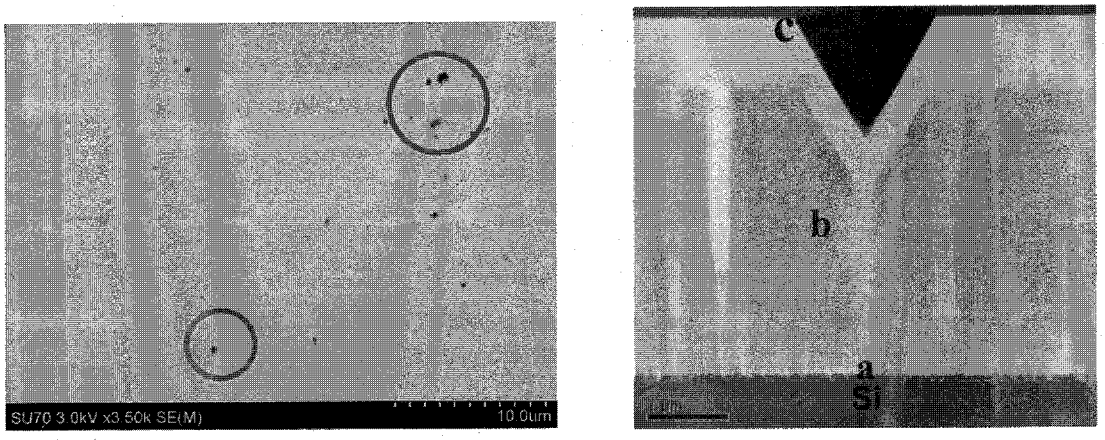

FIG. 2.3. (a) SEM micrograph of pits present on the AlGaN surface. (b) Cross-sectional TEM image showing the origin of deep pit from Si substrate.

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Chapter 3

Characterization and HEMT fabrication on MOCVD grown AlGaN/GaN heterostructures on Si (111) with thick buffer layers

3.1. Introduction

The epilayer design serves as the key factor for the device characteristics such as the drain current density, the channel conductance, leakage and breakdown voltage mechanisms. Therefore, proper design of the AlGaN/GaN heterostructure is crucial for the subsequent fabrication process [1-3]. In this study, the AlGaN/GaN heterostructures involved were all grown by Taiyo Nippon Sanso SR-4000 MOCVD system. The HEMT structures were grown on 4" p-type Si substrate by using various (AlN/GaN) buffer layers thickness (T_{buff}). The thickness ratio of the AlN/GaN multipairs was 1:4. The T_{buff} was between 1.25 to 5 μm in order to study the influence buffer layers on the heterostructures and their device characterisistics. The growth of these graded buffer layers is to overcome the large lattice mismatch with the Si substrate and to lower the defects arising due to it.

The AlGaN barrier thickness and Al composition for the hetero structures were fixed as 25 nm and 26 % respectively. The unintentionally doped GaN channel layer was also fixed as 1 μm for the heterostructures. All the heterostructures layers including the buffers were grown at high temperature (≥ 1000 °C).

3.2. Characterization of MOCVD grown AlGaN/GaN HEMT structures on Si (111) with thick buffer layers

The as grown MOCVD AlGaN/GaN heterostructures were subjected to material and carrier characterization prior to the device fabrication.

3.2.1. HR-XRC characterization method

The crystal quality of MOCVD grown GaN layer with increasing T_{buff} were analyzed by measuring (004) and (100) crystallographic reflections HR-XRC measurements using Philips X`pert x-ray diffractometer. Screw and edge dislocation components in GaN layers can be calculated by using the full-width at half-maximum (FWHM) values of 004 and 100 planes respectively. The densities of line defect can directly influence the ω-scan which in turn affects the FWHM line width. Any increase of screw and mixed component of the dislocation density will increase the tilt component in *c*-plane GaN, and hence increase the FWHM line width of symmetric reflection in (004) diffraction peak. The threading edge dislocation densities can be derived from the FWHM values by scanning the symmetric reflection in (100) diffraction peak. Increase in FWHM value will reveal the edge dislocation component of *c*-plane GaN layer [4-5]. The screw and edge dislocation components are given according to the equations 3.1 and 3.2,

$$(D_{screw}) = \frac{\alpha_{004}^{2}}{4.35.c_{screw}^{2}} \tag{3.1}$$

$$(D_{edge}) = \frac{\alpha_{100}^{2}}{4.35.c_{edge}^{2}} \tag{3.2}$$

In these equations, α is the FWHM (in radian) at respective reflection and *c* is the Burger's constant. The values of c for screw and edge components are 0.5185 and 0.3189 A° respectively. The calculated screw dislocation density for AlGaN/GaN heterostructures with various T_{tot} was around ~1.5 x 10^9 cm^{-2}. Meanwhile, the FWHM value corresponding to 100 reflection decreased significantly as the buffer thickness increased. And the calculated edge dislocation density ($D_{D\text{-}edge}$) was found to decrease considerably with increasing T_{tot}. Furthermore, it was found that increasing the T_{buff},

reduced the edge dislocation densities while increasing the GaN layer thickness reduced the screw dislocation densities. Hence, growing thick GaN layers using thick buffers is an effective way to reduce both edge and screw dislocation densities.

The Hall effect can be measured by inducing a magnetic field perpendicular to the current flow direction in a semiconductor [6-10]. The summary of the HR-XRC results and Hall measurements for AlGaN/GaN HEMT heterostructures are presented in the table. 3.1.

Table 3.1. Summary of XRC and Hall measurement results for AlGaN/GaN HEMT heterostructures grown with increasing buffer thickness

Thickness in μm		**XRC results FWHM (arcsec)**		**Hall measurements @ 300 K**			**Hall measurements @ 77 K**		
T_{tot}	T_{buff}	(004)	(100)	N_s x 10^{13} (cm^{-2})	μ_H (cm^2/Vs)	R_{sh} (Ω/□)	N_s x 10^{13} (cm^{-2})	μ_H (cm^2/Vs)	R_{sh} (Ω/□)
2.25	1.25	779	3073.8	0.83	923	809	0.92	2950	230
3.5	2.50	869.8	2769.9	0.83	983	769	0.91	3450	188
5.0	4.0	921.5	2289.6	0.87	1100	649	0.93	4240	158
6.0	5.0	868.1	2163.3	0.70	980	978	0.78	4245	191

It was observed that increasing the T_{buff} resulted in considerable decrease in $D_{D\text{-}edge}$ and improved carrier mobilities at (77 K). A plot of $D_{D\text{-}edge}$ and μ_H against T_{tot} is shown in fig. 3.1. As seen, the $D_{D\text{-}edge}$ were found to decrease with increasing T_{tot} and was low (≅ 52 %) for the heterostructures with thicker T_{tot} that is with increasing buffer thickness [11]. The μ_H was enhanced by 50 % for AlGaN/GaN HEMT heterostructures grown on thick T_{buff}~5 μm, compared to heterostructures grown on thin T_{buff} ~1.25 μm.

However, there is very less percent (~5%) of reduction in edge dislocation density between buffer thickness of 4 and 5 μm. Therefore, for AlGaN/GaN/Si heterostructures with i-GaN thickness of 1 μm, the critical buffer thickness can be around 4 μm based on HR-XRC and hall measurements.

The increase in μ_H is also attributed to good quality AlGaN/GaN heterostructures relatively with a smoother hetero-interface resulted by increasing the T_{buff}. A high concentration of dislocations/defects at the hetero-interface can ultimately limit the μ_H due to interface roughness scattering. The increases in carrier mobilities are often expressed in terms of increase in the epilayers thickness, reduced dislocations, defects and interface roughness [12-16]. Moreover, Jena *et al.* [17] have also showed the dependence of mobility and dislocation density with an extremely good approximation by the expression $\mu^{2D} \propto n_s^{3/2}/N_{dis}$. In this expression, μ^{2D} is the two dimensional electron gas (2-DEG) mobility, n_s and N_{dis} are 2-DEG concentration and dislocation densities respectively.

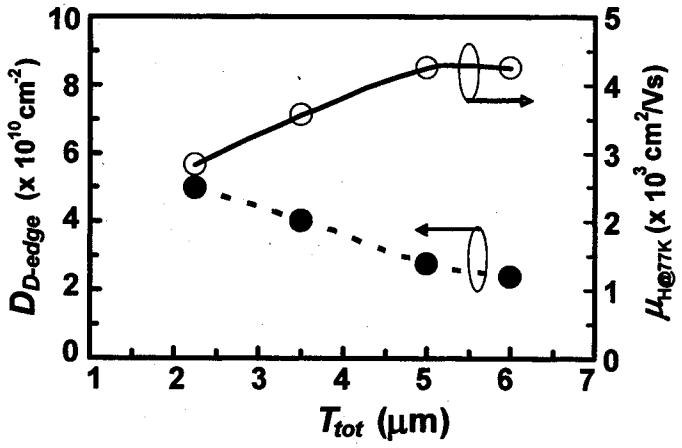

FIG. 3.1. Plot of calculated edge dislocation densites from XRC results and measured carrier moblities versus total epilayer thickness for AlGaN/GaN HEMT heterostructures grown with increasing buffer layers thickness.

In the case of AlGaN/GaN heterostructures a large *in-built* piezoelectric [18-21] and spontaneous polarizations [21-22] results in high concentration of charge carriers also called as 2-Dimensional Electron Gas (2-DEG) at the heterointerface as discussed in chapter 1. This makes them favorable candidates for high frequency characteristics. The 2-DEG concentration can be modulated by varying the composition of Al in the barrier layer [23-26] and hence sometimes termed as modulation-doped FET (MOD-FETs). The wide band gap of GaN (3.4 eV), makes AlGaN/GaN hetero-system more special, as they can be utilized for high power applications as well.

Transmission line model (TLM) was used to measure the contact resistance of the ohmic contacts of the AlGaN/GaN HEMTs. TLM is the technique that is widely used to access the electrical properties and the quality of Ohmic contacts by employing four probes method [27-28].

3.3. Analyses of trapping characteristics in AlGaN/GaN HEMT structures on Si

3.3.1. Traps in AlGaN/GaN HEMT structures

In semiconductors, any defect which disrupts the periodicity of the crystal lattice will also result in the semiconductor band structure. A localized defect existing in the semiconductor can act as a "trapping center" for mobile charges in the region of defect. The occupancy of the trap centers is governed by the capture and emission process for both electrons and holes. In the case of hole-capture and emission processes, the trap levels behave as generation and recombination centers. However, the samples used in this study all are n-type so the analyses are focused mainly on electron-capture and emission processes. Moreover, trapping centers in AlGaN/GaN HEMTs are very much responsible for current collapse [29]. The presence of these traps limits the HEMT performance in

high-speed power switching devices depending on the location, concentration, cross-section and energy. On comprehensive literature survey, possible locations of the traps are, a) the interface between the substrate (Si or SiC or sapphire), b) the buffer layers, c) the GaN channel layer, d) the AlGaN/GaN hetero-interface and e) the free AlGaN surface.

3.3.2. Frequency dependent conductance technique for AlGaN/GaN structures

The trap centers existing in the interface between substrate-nucleation layers and buffer layers are regarded as deep traps and are identified vastly by deep-level transient spectroscopy technique [30-32]. In addition, there are considerable amount of traps located in the AlGaN/GaN active device structure. These traps could not be successfully characterized by the conventional high-low frequency *C-V* and Terman techniques due to limitations and associated errors in case of hetero-structures. This made frequency dependent conductance method to be extended for hetero-structures, which was initially developed for Si/SiO_2 MOS-devices by Nicollian and Goetzberger (also called *NG* method [33-34]). Later, conductance technique was proved to be an effective tool to diagnose the trapping effects in AlGaN/GaN HEMT structures on the consideration that the AlGaN barrier acting as a loosy-dielectric layer [35-36]. In addition, two kinds of traps, namely fast and slow traps were identified based on their time constants by this method [37-39]. The slower traps are mainly surface related and are present along the access region between the gate and drain electrode. Further, they can be minimized by using a passivating material. Recently, a variety of such materials like Al_2O_3, HfO_2 SiN, AlN, etc. and their post deposition annealing conditions have considerably reduced the slow surface related traps [37-40]. However, these passivating films had no effects on the fast traps. This shows that the location of the fast traps can be in close proximity to the

AlGaN/GaN hetero-interface near the channel. The AlGaN/GaN hetero-interface traps usually have shorter time constant (~μs) for trapping/detrapping process. Apparently, location of these fast traps in the hetero-interface near channel has also been confirmed by techniques like backgating current deep level transient spectroscopy (DLTS) [41], frequency dependent conductance analyses [42] and noise spectral studies [43]. Unfortunately, not many reports are available for minimizing these AlGaN/GaN hetero-interface traps and/or interface roughness in AlGaN/GaN/Si HEMT heterostructures by improving the hetero-epitaxial growth conditions.

3.3.3. Trapping characteristics of AlGaN/GaN HEMT structures grown with thick buffer layers

It is our imperative attention to characterize the AlGaN/GaN HEMTs grown using thick buffer layers (T_{buff}) by conductance method to establish growth standards for GaN on silicon. SBD were fabricated on same AlGaN/GaN HEMT epilayers that were used for the HR-XRC and Hall measurements. The thickness of the undoped AlGaN barrier layer and Al composition were fixed as 25 nm and 26 % respectively. The undoped GaN layer thickness (T_{GaN}) for all the heterostructures was 1 μm. In order to investigate the AlGaN/GaN hetero-interface trapping effects, an increasing sequence (1.25 – 5 μm) of GaN/AlN T_{buff} (20/5 nm) was used. All these layers were grown at high temperature. The total epilayer thickness (T_{tot}) given by ($T_{tot}=T_{GaN} + T_{buff}$) will be used in further discussions. AlGaN/GaN SBDs of uniform area 7.07 x 10^{-4} cm^{-2} were used for the conductance measurements. Capacitance voltage (C-V) and conductance voltage (G-V) measurements were performed between frequency ranges (1 kHz -5 MHz) by sweeping the gate bias (V_g) using Agilent B1505 power device analyzer. The amplitude of ac signal

was fixed as 20 mV and the measurement period was long, so that small signal conditions were maintained.

The normalized *C-V* curves measured at 100 kHz showed a sharp transition from accumulation to depletion region for all devices as shown in fig. 3.2. As seen, a small negative shift in threshold voltage ($\Delta V_{th} \sim 0.12\ V$) was observed on increasing the T_{tot}. This is explained in terms of AlGaN/GaN heterostructures grown on thicker buffer layers can increase the 2-DEG carrier density ($N_{D\text{-}2DEG}$). Then a higher voltage would be required to pinch off the channel [44]. This was also confirmed from the extracted $N_{D\text{-}2DEG}$ versus depth profile (W in nm) with increasing T_{Tot} as shown in fig. 3.3. In other words, the reduced carrier scattering effects can be a major contributing factor for the increase in carrier density with thicker T_{Tot}. About one order difference in $N_{D\text{-}2DEG}$ (i.e. 2.2 x 10^{19}~ 2.0 x 10^{20}) cm^{-3} was observed for AlGaN/GaN HEMT hetero-structures grown with thin and thick buffer layers respectively.

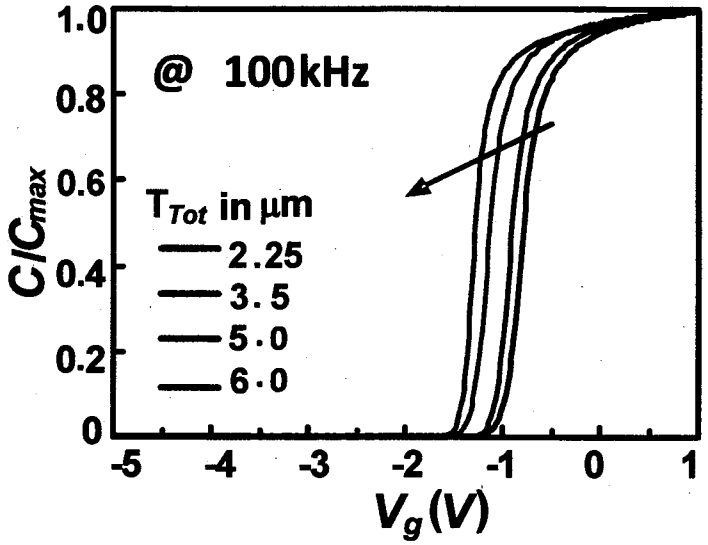

FIG. 3.2. Normalized *C-V* curves of AlGaN/GaN HEMT heterostructures grown with increasing epilayer thickness (T_{tot}).

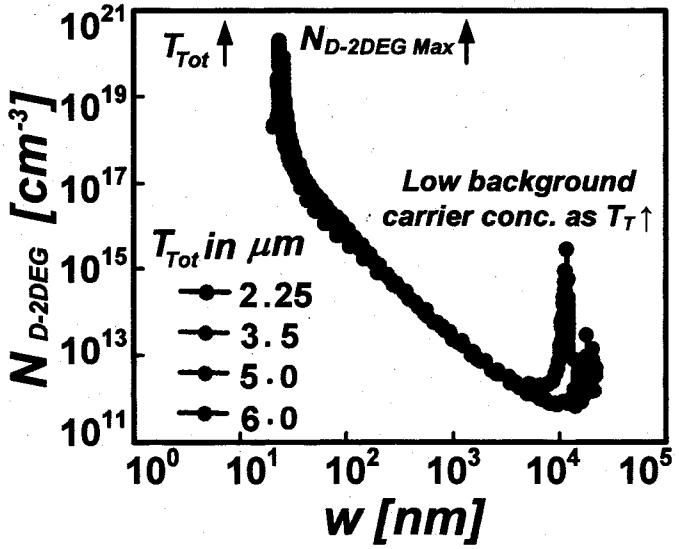

FIG. 3.3. Extracted 2-DEG carrier density versus depth profile for AlGaN/GaN HEMT heterostructures grown with an increasing T_{tot}.

A plot of measured $N_{D\text{-}2DEG}$ and V_{th} as a function of T_{tot} are also shown in fig. 3. 4. An exponential function of $N_{D\text{-}2DEG}$ against T_{tot} showed a good fit with maximum accuracy for AlGaN/GaN HEMT heterostructures which also accompanied a V_{th} shift. In addition, the background carrier concentration was found to be low for AlGaN/GaN HEMT heterostructures grown with thicker T_{buff}, which is advantageous because of low buffer leakage.

A decrease in trapping effects near the hetero-interface can be one of the possible explanations for both increase in carrier concentration and mobility, because these traps can also act as scattering centers. Furthermore, the trap centers can be associated with charged line defects, since a low V_{th} of (-0.9 V) due to partial depletion of the 2-DEG electrons was observed in the case of AlGaN/GaN HEMT structure grown using thin buffer layers, which obviously showed low carrier density and had maximum edge

dislocation densities. It is noteworthy to mention that the charged line defects are known to exist in GaN based devices and may provide acceptor traps and form negatively charged Columbic scattering centers [45-47].

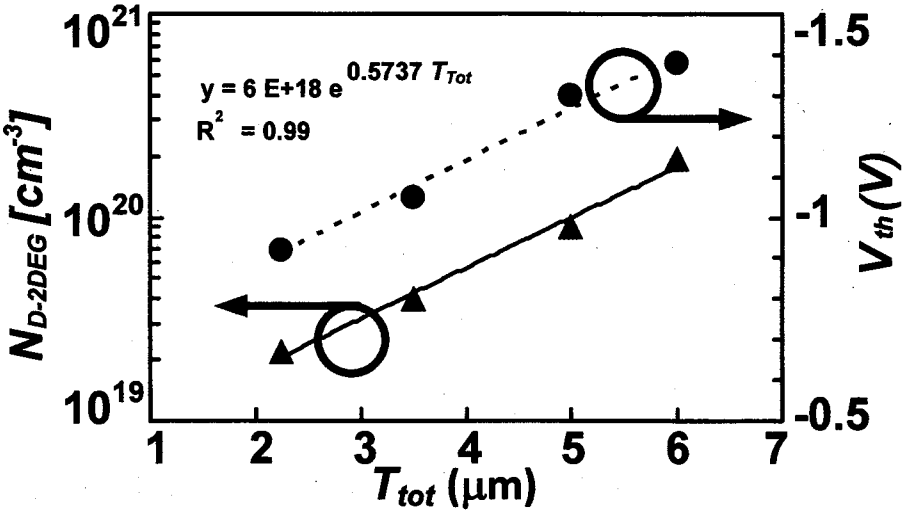

FIG. 3.4. Plot of 2-DEG carrier densities and threshold voltage for AlGaN/GaN HEMT heterostructures grown with an increasing T_{tot}.

In order to evaluate the hetero-interface trapping effects quantitatively, the equivalent parallel conductance/angular frequency (G_p/ω) values near the depletion region were fitted according to the equation [35-38],

$$\frac{Gp}{\omega} = \frac{qD_T}{2\omega\tau_t} \text{x ln } [1+(\omega\tau_t)^2], \tag{3.1}$$

where D_T and τ_t are the trap densities and trap time constants which are parameters evaluated by fitting the experimental G_p/ω values.

As shown in fig. 3.5 (a), typical G_p/ω fitting curves against ω for selected gate voltages near the depletion region ($V_g < V_{th}$) showed an excellent agreement with the experimental G_p/ω results. Both surface related slow traps as well as AlGaN/GaN hetero-interface traps were identified and evaluated. Figure 3.5 (b) shows only the contribution

of hetero-interface traps to the G_p/ω fitting curves and were found to be two orders of magnitude lower than the surface traps. The densities of slow traps (D_{st}) were in the order ~ 0.5 x 10^{12} $cm^{-2}eV^{-1}$ with slow trap time constant (τ_{st}) range between (0.3 – 1 ms). Nevertheless, these D_{st} values are lower for AlGaN/GaN HEMTs without a gate insulating layer [37-38].

On the other hand, the evaluated hetero-interface trap time constants (τ_{it}) increased with an increasing T_{tot} and were in the range of (0.6 – 10 μs). Furthermore, the τ_{it} of these devices showed exactly an exponential dependence on the gate bias ($\tau_{it} \propto \exp V_g$) near the depletion region ~$V_g \leq V_{th}$ as shown in fig. 3.6. This confirms the presence of continuum of hetero-interface trap states near the AlGaN/GaN layers. Also, these electrically active traps may represent material imperfections such as impurities or point defects, dislocations, etc. that are capable to capture and emit charge carriers with a specific time constant. A decrease in hetero-trap state density (D_{it}) probably associated with the edge dislocation densities were eventually reflected in conductance analyses too.

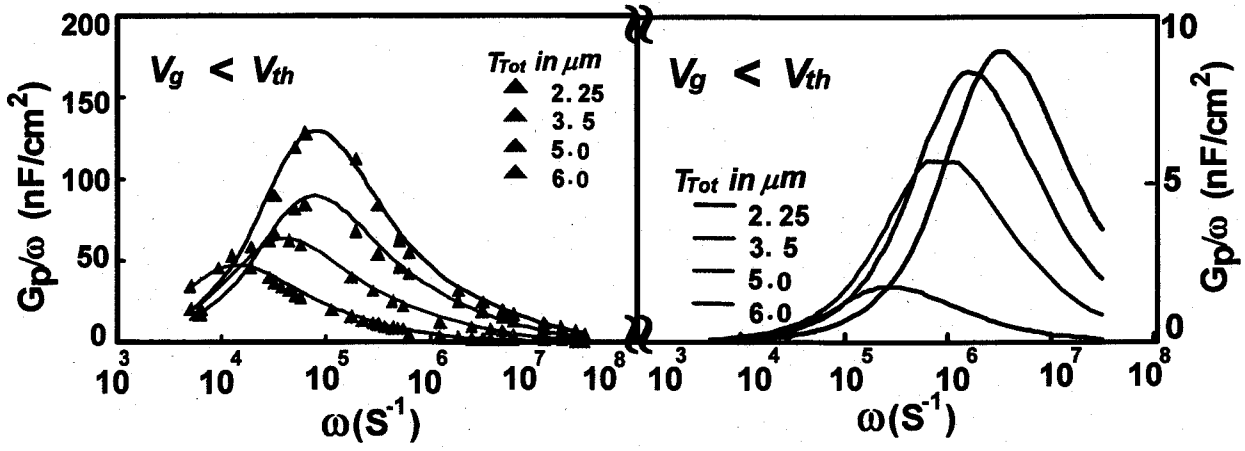

FIG. 3.5. (a) Parallel conductance as a function of angular frequency at selected gate voltages near depletion for AlGaN/GaN HEMT structures grown with an increasing T_{tot}. (b) Contribution of hetero-interface trap states to the measured parallel conductance.

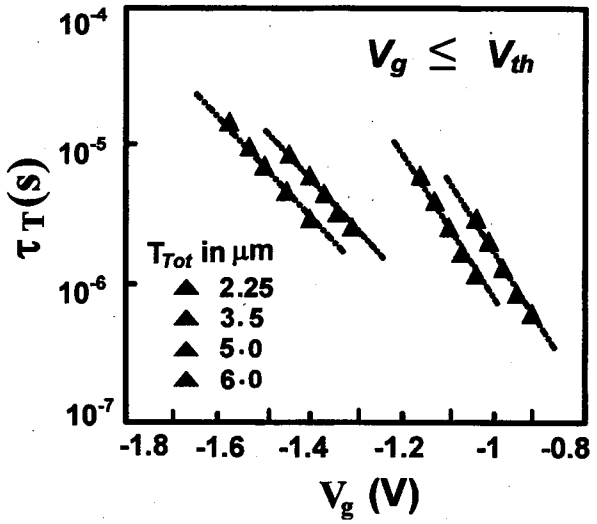

FIG. 3.6. Hetero-interface trap time constants as a funciton of gate voltages in the vicinity of depletion region for AlGaN/GaN HEMT heterostructures grown with an increasing T_{tot}.

The hetero-interface traps, otherwise termed as fast traps as a function of epilayer thickness were exclusively studied by conductance technique and are shown in fig. 3.7. The extracted AlGaN/GaN hetero-interface state density (D_{it}) versus the gate voltages ($V_g \leq V_{th}$) normalized to the V_{th} showed a decreasing trend with respect to the increase in T_{tot}.

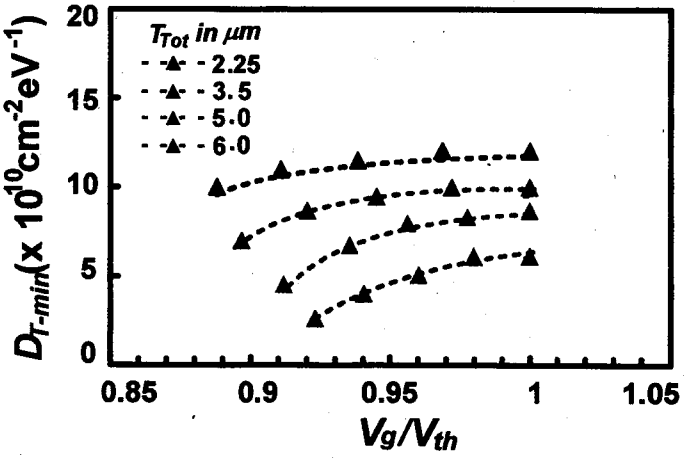

FIG. 3.7. Hetero-interface state density versus the gate voltages normalized to the threshold voltage for AlGaN/GaN HEMT heterostrucutures grown with an increasing T_{tot}.

Furthermore, the comparison chart of previous and present $D_{it\text{-}min}$ results versus T_{tot} exclusively with similar kind of traps evaluated from conductance analyses is also shown in fig. 3.8. The $D_{it\text{-}min}$ is the minimum value of hetero-interface state density that can be extracted near the depletion region. The τ_{it} in this study and in the references was well within the comparable range between (0.1 -10 μs). In addition, the composition in Al_xGaN layer was x ≥ 20 % and the barrier layer thickness considered was also reasonable. A $D_{it\text{-}min}$ value of 2.5 x 10^{10} $cm^{-2}eV^{-1}$ was observed for AlGaN/GaN heterostructures grown with T_{tot} ~6 μm. In contrast, the $D_{it\text{-}min}$ value for similar AlGaN/GaN heterostructures with thin T_{tot} ~2.25 μm was 1 x 10^{11} $cm^{-2}eV^{-1}$. However, this value is low when compared to heterostructures ($T_{tot} \leq 3$ μm) grown without the multipairs of AlN/GaN buffer layers [37].

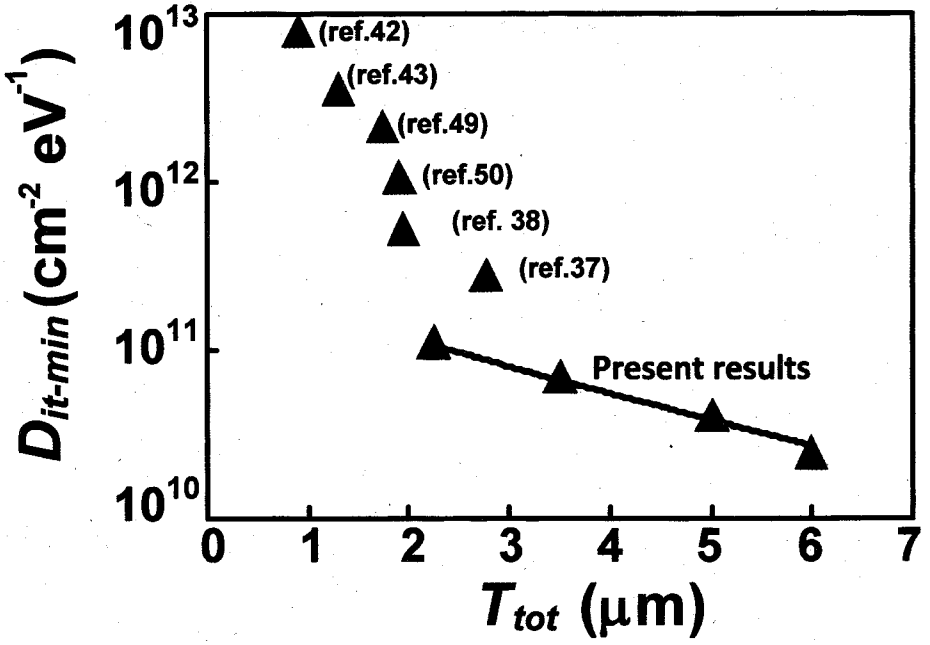

FIG. 3.8. A comparision chart of $D_{it\text{-}min}$ for AlGaN/GaN HEMT heterostructures from conductance analyses versus T_{tot}. The AlGaN/GaN HEMT heterostructures in this work

were all grown using thick AlN/GaN multilayers. The solid line represents the exponential fitting for $D_{it\text{-}min}$ versus T_{tot}.

A significant decrease in $D_{it\text{-}min}$ by nearly an order was evident with an exponential dependence on T_{tot}. From the slope of $D_{it\text{-}min}$ against T_{tot}, it was found that the interface traps concentration decreased by a factor of $\cong 2 \times 10^{10}$ $cm^{-2}eV^{-1}$ per unit increase in T_{tot} (in μm). Ultimately, the reduced $D_{D\text{-}edge}$ and $D_{it\text{-}min}$ with an increasing T_{tot} further suggests that dislocations or extended line defects can be a factor that influences the AlGaN/GaN hetero-interface traps. The presence of extended defects due to dislocations mostly located at the AlGaN/GaN hetero-interface was also confirmed by Fourier Transform (FT-DLTS) technique [48]. A decrease in 2-DEG density for AlGaN/GaN HEMT structures with respect to thin T_{buff} confirms that the hetero-interface traps are acceptor like.

3.4. Summary

The hetero-interface trapping characteristics of MOCVD grown AlGaN/GaN HEMT heterostructures on silicon substrate with increasing buffer thickness were extensively studied. A low $D_{it\text{-}min}$ value of 2.5×10^{10} $cm^{-2}eV^{-1}$ was observed for AlGaN/GaN heterostructure grown using thick buffer layers, T_{buff} ~5 μm. On contrast, similar heterostructures grown using thin T_{buff} ~1.25 μm showed a $D_{it\text{-}min}$ value of 1.0×10^{11} cm^{-2} eV^{-1}. The HR-XRC and Van der Pauw-Hall measurements also confirms that increasing the T_{buff} improves the AlGaN/GaN HEMT heterostructures and its interface properties as evident from reduced edge dislocations and enhanced $N_{D\text{-}2DEG}$ and carrier mobilities respectively. A good quality MOCVD AlGaN/GaN HEMT heterostructures were grown using thick T_{buff} with reduced $D_{D\text{-}edge}$ as well as smoother interface with low $D_{it\text{-}min}$ values as evident from increased $N_{D\text{-}2DEG}$ and carrier transport properties.

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Chapter 4

AlGaN/GaN based metal - oxide - semiconductor high-electron-mobility transistors (MOS-HEMTs)

4.1. Introduction

Although, Schottky gate for GaN HEMTs finds tremendous attention towards high-frequency device applications, it is difficult to utilize them for high-power applications. The drawbacks of Schottky gate invariably of the metal used (Ni or Pt or Pd); include a high gate leakage current, small gate voltage swing (GVS) accompanied by a very low breakdown voltage. An introduction of a thin insulator/oxide (dielectric) layer between the barrier layer and the metal gate would in-turn overcome the drawbacks aforementioned. In general, a native oxide can offer a good interface quality with the semiconductor as in the case of SiO_2/Si MOS-devices. However, in the case of compound semiconductors like GaAs and GaN, the unavailability of native oxide (Ga_2O_3) or the suitable deposition condition make it hard to develop a high quality GaN based MOS-devices. This prompts the use of other dielectric materials such as SiO_2, Si_3N_4, SiO_xN, Al_2O_3, Sc_2O_3, ZrO_2, NiO and HfO_2 for GaN MOS-devices [1-10].

4.2. Oxide, insulator deposition methods

As mentioned earlier, the quality of the oxide layer mainly affects the GaN MOS-devices. Considerable amount of interface charges if present in the semiconductor/oxide interface, can adversely affect the device characteristics. As the interface charges can act as both virtual gate and parallel conduction path for gate leakage. In addition, the interface charges can partially deplete the channel electrons and cause current collapse when operated under rf conditions. There are many deposition techniques available for

the deposition of dielectric layer depending upon the nature of the dielectric films to be deposited. Some of the conventional methods for the deposition of dielectric layers are

(i) Electron Beam (EB) evaporation [1-11],

(ii) Sputtering [12-16],

(iii) Chemical Vapor Deposition (CVD) [17-20],

(iv) Metal Organic Chemical Vapor Deposition (MOCVD) [21-24],

(v) Atomic Layer Deposition (ALD) [25-28],

(vi) Liquid Phase Deposition (LPD) and other techniques [29-38].

Besides these techniques, unconventional methods such as plasma oxidation of AlGaN layer are also available to introduce dielectric layer. Of all the dielectrics/oxides available high~κ dielectric such as Al_2O_3 is highly preferred because of its large band gap (~9 eV), high dielectric constant (~9) and high breakdown field (upto 30 $MVcm^{-1}$), high thermal stability, and a good interface quality with GaN. Furthermore, the use of high- κ Al_2O_3 based AlGaN/GaN MIS transistors can result in superior performance such as low gate leakage current, large GVS, and improved input-output linearity compared to the Schottky gate transistors.

4.3. Fabrication of thermally oxidized Al_2O_3/AlGaN/GaN MOS-HEMTs

The AlGaN/GaN heterostructures were grown on 4 in. *p*-Si (111) substrate using Taiyo Nippon Sanso SR-4000 MOCVD system. For the given structure the Al concentration and thickness of AlGaN layer was fixed as 26% and 25 nm respectively. A Hall mobility of 1520 cm^2/Vs, a sheet resistance of 413 Ω/cm^2 and a sheet carrier concentration of 9.94×10^{12} cm^{-2} were recorded for the sample using Van der Pauw Hall measurements. The device fabrication started with mesa isolation using BCl_3 plasma

based Reactive Ion etching (RIE). The devices were passivated using electron beam evaporated SiO_2. Ohmic patterns were performed using photolithography followed by metallization of Ti/Al/Ni/Au (15/80/12/40 nm). The Ohmic contacts were annealed at 850°C using infra-red lamp annealing for 30s in N_2 ambient. Gate lithography was performed to define Al_2O_3 layer under the Schottky gate. A 10 nm pure Al layer was deposited by filament heating at the patterned gate region. The samples were transferred to the oxidative annealing chamber where Al layer was oxidized/annealed at 600°C for 15 minutes at a constant oxygen flow rate of 4.5 ml/min and at atmospheric pressure. Finally, gate and contact metals Pd/Ti/Au (40/20/60 nm) was deposited followed by lift off. Figure 4.1 shows the cross-sectional schematic representation of a fabricated Al_2O_3/AlGaN/GaN MOS-HEMT. By this method, the oxide impurities especially near the gate electrode can be eliminated and hence can expect lower gate leakage current.

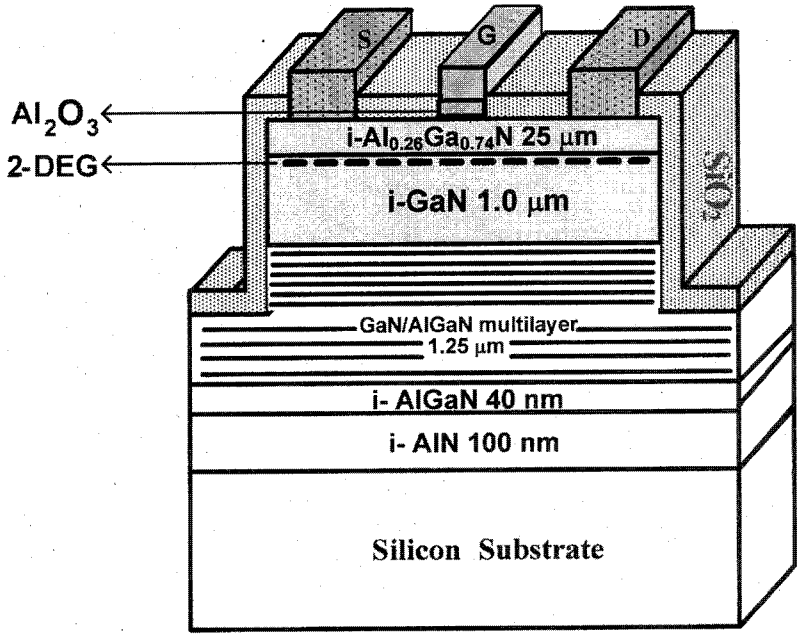

FIG. 4.1. Cross-sectional schematic representation of Al_2O_3/AlGaN/GaN MOS-HEMT.

4. 4. Surface and compositional analyses of oxidized Al layer

4.4.1. X-ray photoelectron spectroscopy (XPS) analyses

XPS analyses were carried out to confirm that as deposited pure Aluminum layer has been partially or fully converted into the respective oxide layer. XPS measurements were recorded using SSX-100 with AlKα monochromator source. The oxidized Al layer was scanned and it consists of Al2*p* peak at a higher binding energy of 75.7 eV as shown in fig.4.2. The alumina surface was precisely etched up to the AlGaN surface and XPS measurements were carried out. An Al2*p* peak at binding energy of 74.5 eV corresponding to Al-N bond in AlGaN barrier layer was observed. On the other hand, we did not observe any metallic Al2*p* peak at low binding energy between 65 to 73 eV, neither in alumina surface nor in the AlGaN barrier layer. This also confirmed the absence of metallic Al-Al bond under the gate electrode.

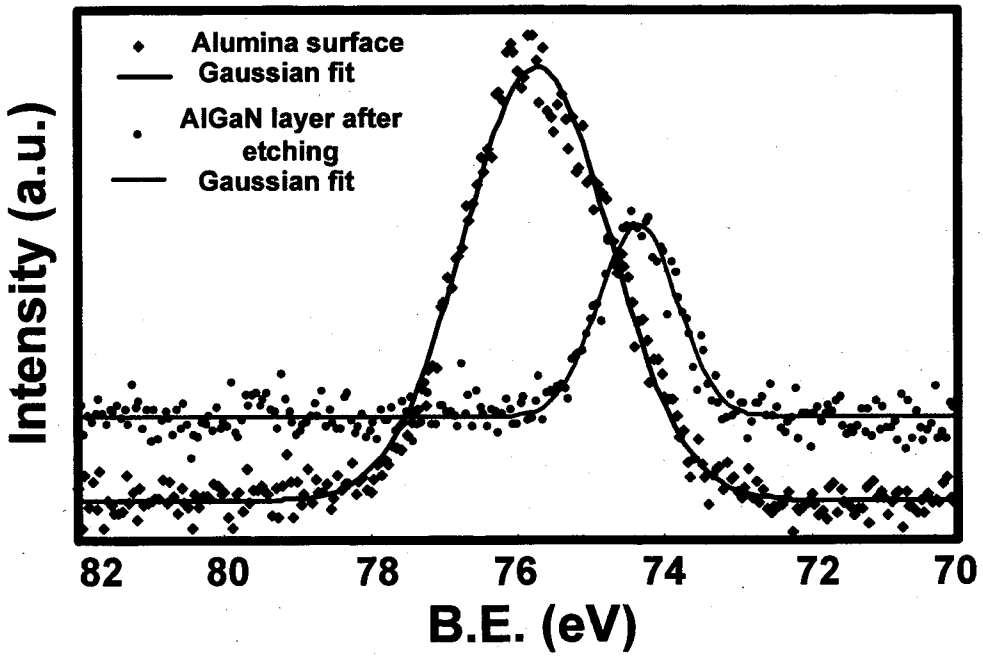

FIG. 4. 2. Core level Al2*p* signal from Al_2O_3 surface and AlGaN layer.

The O1*s* peak was observed at a binding energy of 532.8 eV as shown in fig. 4.3. The higher binding energies of Al2*p* and O1*s* indicate nearly stoichiometric alumina layer. Since the alumina exists in several forms, we could not distinguish the exact phase in which it exists. Similar binding energy was also reported in other report [39].

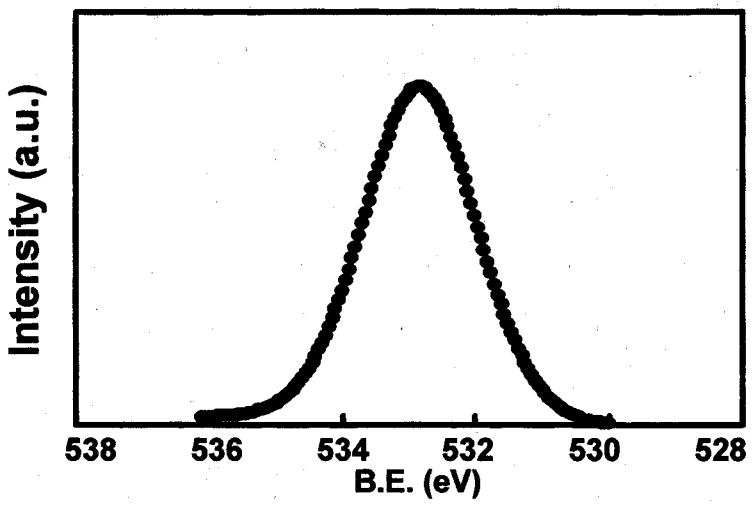

FIG. 4.3. Core level O 1s signal from Al_2O_3 surface.

4.5. Device characteristics

4.5.1. Transfer characteristics

The transfer and log plot of I_{ds}-V_{gs} characteristics are shown in fig. 4.4. The peak transconductance ($g_{m\,max}$) for conventional HEMT and MOS-HEMT (@ V_{DS} = 4 V) and with similar device dimensions were 124 and 121 mS/mm respectively. This is reasonable because in MOS-HEMT, an additional 10 nm oxide layer can increase the gate to channel separation. As a result, a small decrease in transconductance and a moderate increase in the V_{th} could be expected in MOS-HEMTs with high ~k gate dielectrics [40]. The decrease in $I_{DS\,max}$ and g_{mmax} is due to the presence of the Al_2O_3 layer in MOS-HEMT. The MOS-HEMT also exhibited high on/off ratio of the order of 10^4 compared to the normal HEMTs.

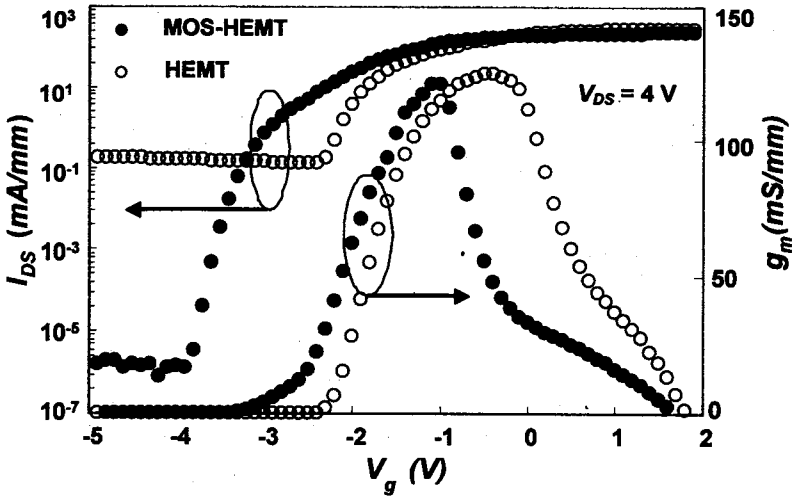

FIG. 4.4. Transfer characteristics of HEMT and Al_2O_3 based MOS-HEMT.

4.5.2. Three terminal leakage and breakdown measurements

Three terminal (*off-state*) breakdown measurements were carried out by maintaining a constant V_g of -5 V with increasing V_{DS} voltage. Since the V_g was -5 V the 2DEG channel is closed and the leakage current emanating from the substrate, the buffer and gate of HEMT and MOS-HEMT were sweeped. It is notable from figs. 4.5 (a) and (b) that for HEMT the breakdown voltage (*BV*) was 256 V whereas the *B-V* for MOS-HEMT was 431 V. This reflects on the gate leakage (I_g) which contributes to the *BV* [40].

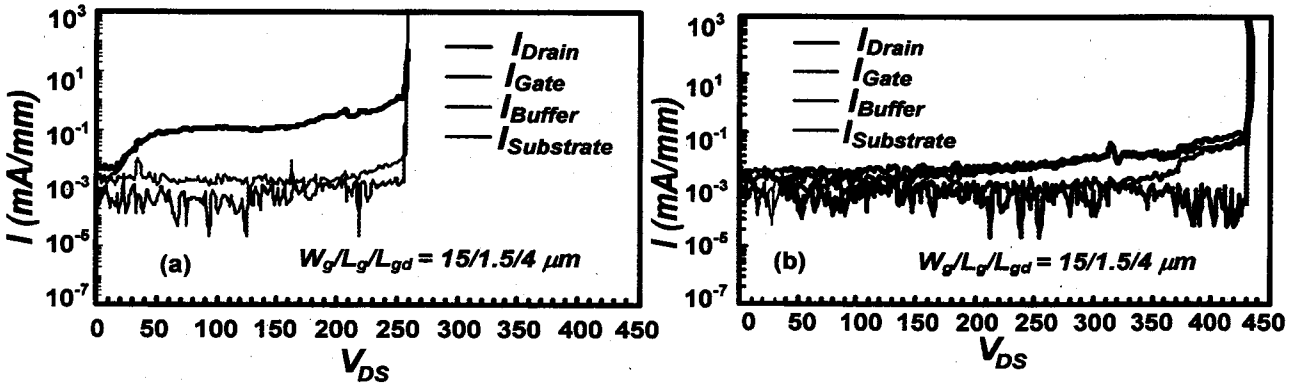

FIG. 4.5. Three-terminal (*off-state*) breakdown measurements for (a) AlGaN/GaN HEMT and (b) Al_2O_3 based MOS-HEMT.

4.6. Analyses of trapping effects in Al_2O_3/AlGaN/GaN MOS-HEMT structures by frequency dependent conductance technique

Frequency dependent conductance measurements of AlGaN/GaN MOS-HEMT were performed to evaluate the interface trap density (D_T) and trap state time (τ_T). Figure 4.6 shows the plot of parallel conductance (G_p/ω) as a function of frequency for selected gate voltages near V_{th} using equation 3.1. The experimental G_p/ω values agreed well with the theoretical fitting values and only fast traps ($\sim\mu s$) were evaluated in the case of Al_2O_3/AlGaN/GaN MOS-HEMT, unlike the AlGaN/GaN HEMTs which exhibited both surface related slow traps and fast traps as discussed briefly in chapter 3. This also suggests that the surface traps are passivated by the oxidative annealing of pure Al layer at elevated temperature.

The values of D_T and τ_T are extracted by fitting the experimental G_p/ω. We evaluated a maximum D_T of 6.7 x 10^{12} $cm^{-2}eV^{-1}$ with a τ_T of 46 μs and a minimum D_T of 2.2 x 10^{12} $cm^{-2}eV^{-1}$ with a τ_T of 1.3 μs. The τ_T as a function of V_g in the vicinity of V_{th} as shown in fig. 4.7. The τ_T shows an exponential increase versus V_g near threshold voltage.

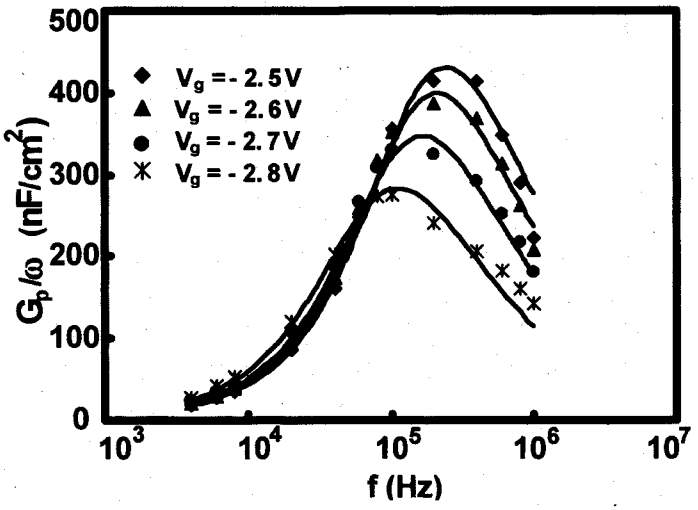

FIG. 4.6. Frequency dependent parallel conductance as a function of radial frequency

for selected gate voltages near V_{th}.

The trap state energy can be evaluated using the equation,

$$E_T = \mathrm{kTln}\,(\sigma_T N_c \upsilon_T)\ \tau_T \qquad (4.1)$$

where k is the Boltzman constant, T is the absolute temperature, σ_T is the capture cross section. N_c and υ_T are the density of states in conduction band and average thermal velocity. The values of the parameters are considered according to Ref. 3. The D_T as a function of their energy is shown in fig. 4.7 (b: Inset).

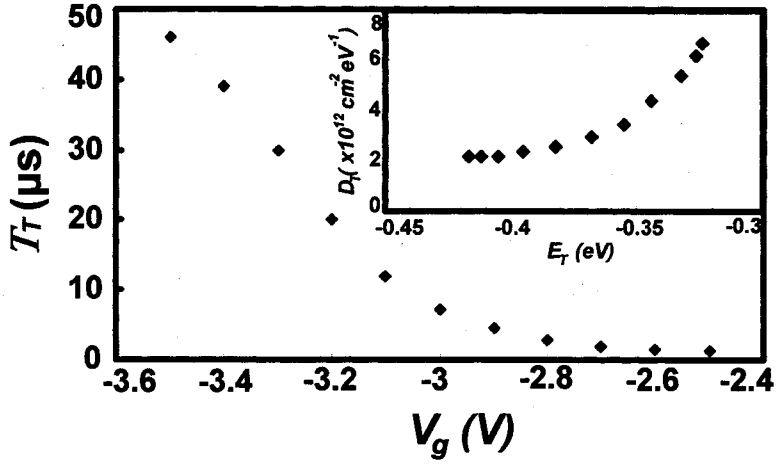

FIG. 4.7. Trap state time as a function of gate voltage of Al_2O_3 based MOS-HEMT. (Inset) Trap state density (D_T) as a function of trap state energy (E_T).

4.7. Summary

A process compatible synthetic route for Al_2O_3 based AlGaN/GaN MOS-HEMT has been developed. The approach is based on oxidative annealing of thin Al layer deposited prior to Schottky gate metallization. The MOS-HEMT exhibits good pinch off features with $I_{ds.\,max}$ and $g_{m\text{-}max}$ of 421 mA/mm and 121 mS/mm. A high BV of 431 V and figure of merit (FOM) of 1.89 x 10^8 $V^2\,\Omega^{-1}\,cm^{-2}$ for ($L_{gd} \leq 4\mu m$) was observed for Al_2O_3 based MOS-HEMT. Frequency dependent conductance measurements yielded a single

continuum of fast trap states. A minimum trap density (D_T) and trap transient time (T_T) of 2.2 x 10^{12} $cm^{-2}eV^{-1}$ and 1.3 μs respectively was observed. The surface traps were absent for the Al_2O_3 based MOS-HEMT due to the effective passivation as well as high temperature annealing.

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Chapter 5

In-situ MOCVD grown AlN/AlGaN/GaN MIS-HEMTs

5.1. Introduction

To suppress the gate leakage and to improve breakdown voltage and a larger gate voltage swing, a variety of gate insulators have been used for AlGaN/GaN MIS-HEMTs [1-4]. However, these insulators are deposited *ex-situ* which can introduce additional growth and process related defects. On the other hand, *in-situ* MOCVD grown thin AlN insulating layer would be advantageous over existing *ex-situ* deposited insulators for its reduced AlN/AlGaN lattice mismatch, high dielectric constant, and large band gap.

Ultra thin AlN layers grown on GaN have also been of great interest recently for a number of applications [5, 6]. For better device performance, lower gate leakage and to prevent tensile strain-induced cracking of AlN layer, low temperature (LT) growth of AlN layer is preferred for MIS-HEMTs [7,8]. Therefore it is worthwhile to study the behavior of trap states existing in AlN/AlGaN/GaN MIS heterostructures (MISHs).

5.2. AlN/AlGaN/GaN MIS-HEMT fabrication

The AlN/AlGaN/GaN MISHs were grown using Taiyo Nippon Sanso, SR 4000 MOCVD system. The MISHs consists of (from the top) 2 nm AlN layer grown at 1030 °C, 25 nm $Al_{0.26}Ga_{0.74}N$ layer, 1 nm AlN spacer interface layer, 1 μm GaN layer, 1.25 μm super lattice structure (SLS) and AlGaN/AlN buffer layer grown over 4 inch p-type Si substrate. The device fabrication started with mesa isolation using BCl_3 plasma based Reactive Ion etching (RIE) [9]. The devices were passivated using electron beam evaporated 100 nm SiO_2. Ohmic patterns were made directly on the AlN layer using conventional photolithography followed by metallization of Ti/Al/Ni/Au (15/80/12/40

nm). The Ohmic contacts were annealed at 850°C using infra-red lamp annealing for 30s in N_2 ambient. Finally, gate metals Pd/Ti/Au (40/20/60 nm) were deposited on the AlN layer followed by lift-off procedure as shown in fig. 5.1.

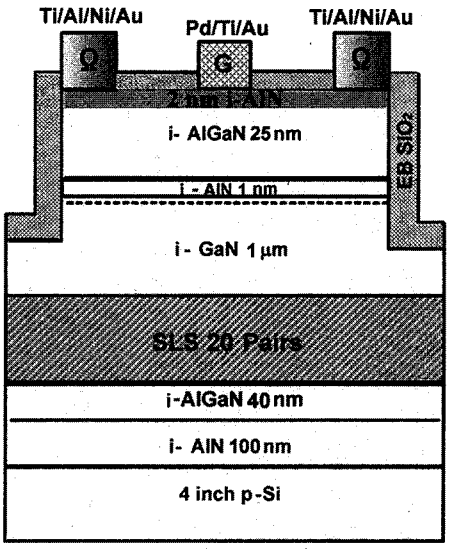

FIG. 5.1. Cross sectional view of MOCVD grown AlN/AlGaN/GaN MIS-HEMT.

5.3. Analyses of trapping effects in *in-situ* MOCVD grown AlN/AlGaN/GaN MIS-HEMT structures on silicon substrate

5.3.1. Frequency dependent conductance technique for AlN/AlGaN/GaN MIS-HEMT structures

As discussed briefly in chapter 3, there are various possibilities that a charged carrier can be trapped by the trapping centers present in various epitaxial layers from the substrate to the barrier layer in AlGaN/GaN HEMT. It is widely accepted that the AlN layer is known to contain defect charges or trapping centers [10-13]. Frequency dependent conductance measurements to evaluate the trap state time (τ_T) and trap state density (D_T). Conductance technique for the measurement of trap states in MIS capacitors is generally accepted as the most accurate technique in existence [14-17]. A device V_{th} of

-1.7 V was observed for these MIS-diodes from capacitance-voltage (C-V) measurements. Traps due to the insulating and barrier layers in a MIS structure can be explicitly studied by selectively chosen voltages near the V_{th}. The G_p/ω values were plotted against ω for selected gate voltages near the vicinity of V_{th}. The G_p/ω-ω plot for in-situ MOCVD grown AlN/AlGaN/GaN MIS-diode at V_g = -1.2, -1.6 and -1.8 V are shown in figs. 5.2 to 5.4 respectively.

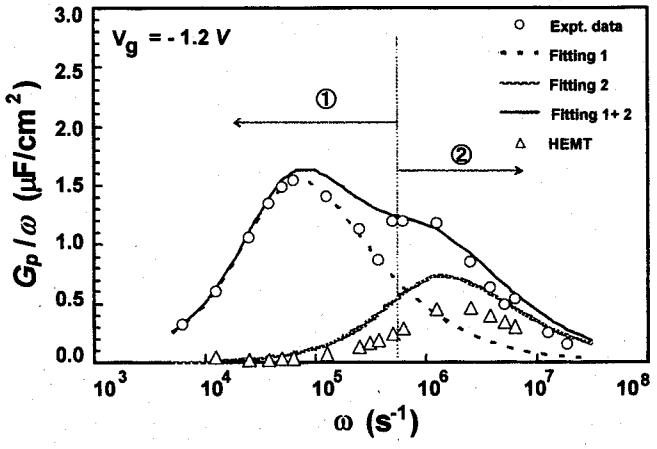

FIG. 5.2. G_p/ω as a function of ω for *in-situ* MOCVD grown AlN/AlGaN/GaN MIS-diode at V_g=-1.2 V. The open triangles represent G_p/ω as a function of ω for AlGaN/GaN HEMT SBD without the insulating AlN layer.

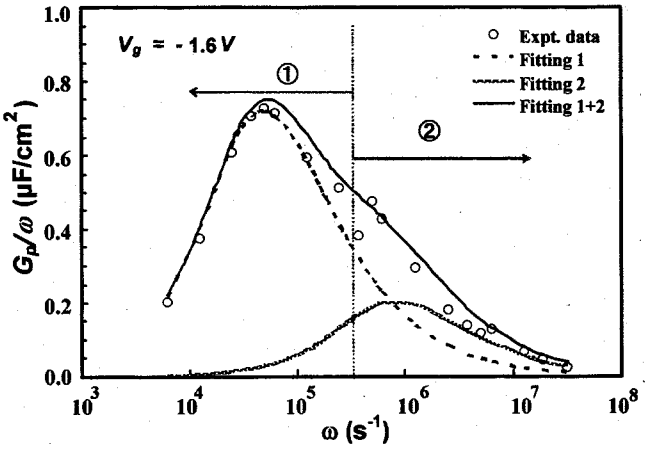

FIG. 5.3. G_p/ω as a function of ω for *in-situ* MOCVD grown AlN/AlGaN/GaN MIS-diode at V_g=-1.6 V.

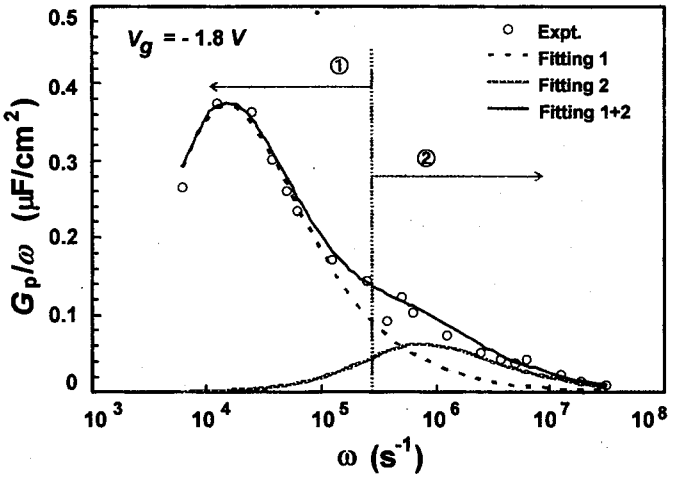

FIG. 5.4. G_p/ω as a function of ω for in-situ MOCVD grown AlN/AlGaN/GaN MIS-diode at V_g=-1.8 V.

Conventional curve fitting method [17, 18] could not explain the experimental G_p/ω dispersions of AlN based MIS-diodes. Alternatively, the experimental G_p/ω values were resolved into two fitting curves for all gate voltages near V_{th} using a curve fitting model. In the low frequency region (≤ 50 kHz) indicated as region ① in figs. 5.2 to 5.4, the experimental G_p/ω values can be fitted into a single G_p/ω curve. On the other hand, in the high frequency region indicated as region ②, two G_p/ω curves were necessary to fit the experimental G_p/ω values. Similar fitting results were observed even at higher bias voltages (as shown in fig. 5.3 and 5.4), while the peak position in region ① moved largely toward low frequency with an increasing τ_T value. This shows the gate voltage dependency on τ_T for the AlN insulated MIS-diode. The fitting model clearly indicates the existence of two types of trap states and their correlation, as evident from the cross over point between regions ① and ② respectively.

The interpretation is that the main G_p/ω peak exhibited in the lower frequency region could be due to trap states existing in insulating AlN layer which includes the traps at the AlN/AlGaN interface. The smaller G_p/ω peak observed relatively in the high frequency region corresponds to the bulk traps caused by the AlGaN barrier layer and AlGaN/GaN interface (hereinafter referred to as the AlGaN barrier layer). Further, the fitting curve (1+2) of the proposed model represents the combined contribution of trap states due to the insulating AlN and AlGaN barrier layers, which agrees well with the experimental G_p/ω values. To validate this, conductance measurements were performed on reference AlGaN/GaN Schottky barrier diodes (SBD) with similar epilayers except, without the AlN insulating layer. The open triangles in fig. 5.2, represent the G_p/ω values against ω for AlGaN/GaN heterostructures. The AlGaN/GaN SBD showed a single Gp/ω peak in same frequency region, as that of smaller G_p/ω peak exhibited in AlN/AlGaN/GaN MIS-diode (referred as fitting curve 2 in figs. 5.2 to 5.4).

Furthermore, to extend the arguments based on this model, conductance analyses was performed on another in-situ MOCVD grown AlN/AlGaN/GaN MISHs with 5 nm AlN insulating layer. Interestingly, the experimental G_p/ω values were also resolved into two fitting curves, exactly in the same frequency ranges as obtained for AlN/AlGaN/GaN MISHs with 2 nm AlN as insulating layer. Two G_p/ω peaks in the AlN based MISHs could be the result of smooth interface between the in-situ grown AlN layer and the AlGaN barrier layer as observed from our experimental results and fitting model. In contrast, the conductance analyses of any of the AlGaN/GaN MISHs with ex-situ grown insulators could not be explicitly resolved into two trap states caused due to the insulator and barrier layers respectively. The trap parameters were also extracted for these AlN

based MIS-diodes [19]. The τ_T due to insulating AlN layer in MISHs was between (27-300) μs. On the other hand, the τ_T due to AlGaN barrier layer in the MISHs was in the range of (1~3) μs.

The plot of trap state density as a function of its energy level is shown in fig. 5.5. A D_T of (4 x 10^{12} ~ 20 x 10^{12}) cm^{-2} eV^{-1} due to the AlN insulating layer was located deeply at E_T (0.4 ~ 0.52 eV). The AlGaN barrier layer exhibited D_T of (1 x 10^{11} ~ 10 x 10^{12}) cm^{-2} eV^{-1} distributed at shallow energy levels E_T (0.32 ~ 0.34 eV). Recently, excess traps at energy levels of 0.22 and 0.38 eV below the conduction band were reported for HfAlO and AlO based AlGaN/GaN MISHs respectively [20, 21].

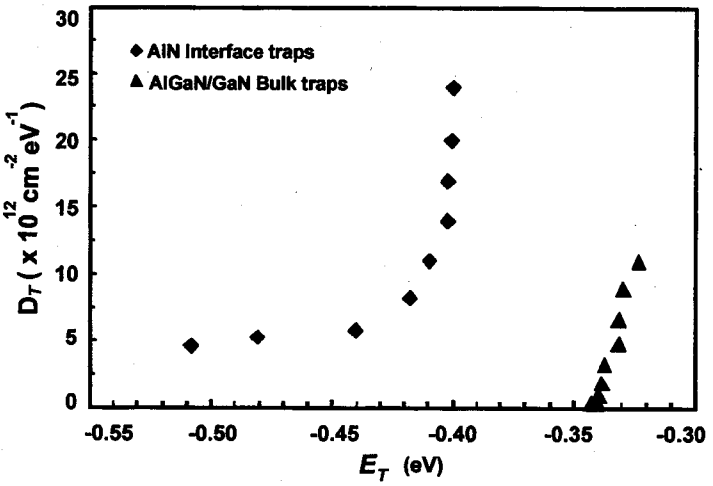

FIG. 5.5. Trap state density as a function of trap state energy of in-situ MOCVD grown AlN/AlGaN/GaN MIS-diode due to AlN insulating and AlGaN barrier layers.

5.4. Effect of AlN growth temperature on trap densities of *in-situ* MOCVD grown AlN/AlGaN/GaN MIS-HEMTs on silicon substrate

In order to effectively use AlN layer as an insulating layer for AlGaN/GaN MIS-HEMT hetero-structure, optimization of the growth of AlN is essential. However, detailed studies on trapping and device properties of *in-situ* MOCVD grown AlN/AlGaN/GaN

MIS-HFETs as a variation of AlN layer T_G are necessary to understand the potential utilization of AlN layer in GaN based MIS-devices. Therefore, two different growth temperatures 600 and 700 °C were chosen to study the trapping characteristics of AlN/AlGaN/GaN MIS-HEMTs. For better understanding the AlN/AlGaN/GaN based MISHs with AlN layer at grown at 600 °C and 700 °C are referred as MIS-(diodes/HFETs) A and B respectively.

5.4.1. Trapping characteristics

Two curves could be fit to the asymmetric experimental G_p/ω values at V_{th}, for MIS-diodes A and B. For comparison, the fitting results of MIS-diodes are shown in figs. 5.6 (a) and (b) respectively. The fitting curves 1 and 2 correspond to the $D_{T\text{-}AlN}$ and the $D_{T\text{-}AlGaN}$ respectively. Both $D_{T\text{-}AlN}$ and $D_{T\text{-}AlGaN}$ can be quantified from the G_p/ω peak magnitude, while the τ_T can be located from the peak position of G_p/ω. By comparing the fitting results of MIS-diodes, we observed both $D_{T\text{-}AlN}$ and $D_{T\text{-}AlGaN}$ of MIS-diode A is one order lower in magnitude than B.

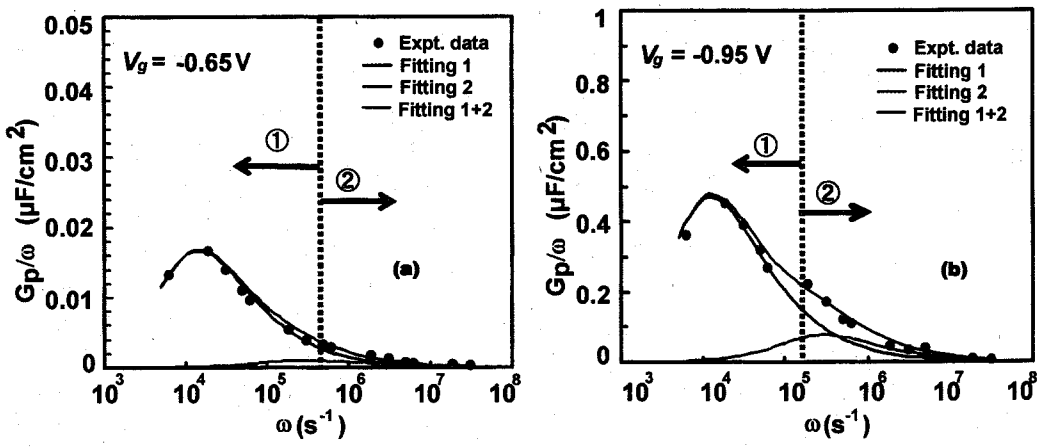

FIG. 5.6. G_p/ω as a function of ω for AlN/AlGaN MIS-HFETs with AlN layer (a) T_G ~ 600 °C and (b) T_G ~700 °C.

In the fitting process for $V_g \leq V_{th}$, similar trend was observed for both the MIS-diodes. Moreover, the fitting curve (1+2) at the cross over region (denoted by a dashed line in fig 5.6 (a) and (b) was relatively broader than the experimental G_p/ω values in the case of MIS-diode B compared to A. This phenomenon was also observed for AlN/AlGaN/GaN MISHs grown relatively at high temperature $T_G \geq 1000$ °C [9]. This is due to the asymmetric behavior of experimental G_p/ω values caused by a high $D_{T\text{-}AlGaN}$ for MIS-diodes with AlN layers grown at high temperatures. Nevertheless, these *in-situ* AlN/AlGaN/GaN MISHs exhibited two trap states with distinct time constants irrespective of their AlN layer T_G.

The AlN trap time constant ($\tau_{T\text{-}AlN}$) and AlGaN trap time constant ($\tau_{T\text{-}AlGaN}$) evaluated are plotted against the V_g for MIS-diodes as shown in figs. 5.7 (a) and (b). In the case of MIS-diode A, both $\tau_{T\text{-}AlN}$ and $\tau_{T\text{-}AlGaN}$ showed better dependencies on V_g than MIS-diode B. An exponential dependency of τ_T on V_g manifests uniformities in the trap states of MIS-diode A than B. A broader conductance curve and a deviation from exponential dependence ($\tau_T \propto V_g$) can be observed if surface potential fluctuation due to some non-uniformity in the oxide (Insulator) and/or interface traps exits [18]. The $\tau_{T\text{-}AlN}$ values for MIS-diodes A and B was in the range of (14 μs – 0.3 ms) and (0.1 – 0.2 ms). On the other hand, $\tau_{T\text{-}AlGaN}$ for MIS-diodes A and B were between (2 – 6 μs) and (5 – 8 μs) respectively. These $\tau_{T\text{-}AlN}$ and $\tau_{T\text{-}AlGaN}$ are consistent with the τ_T ranges generally reported for AlN related traps [26], and AlGaN related bulk traps [20].

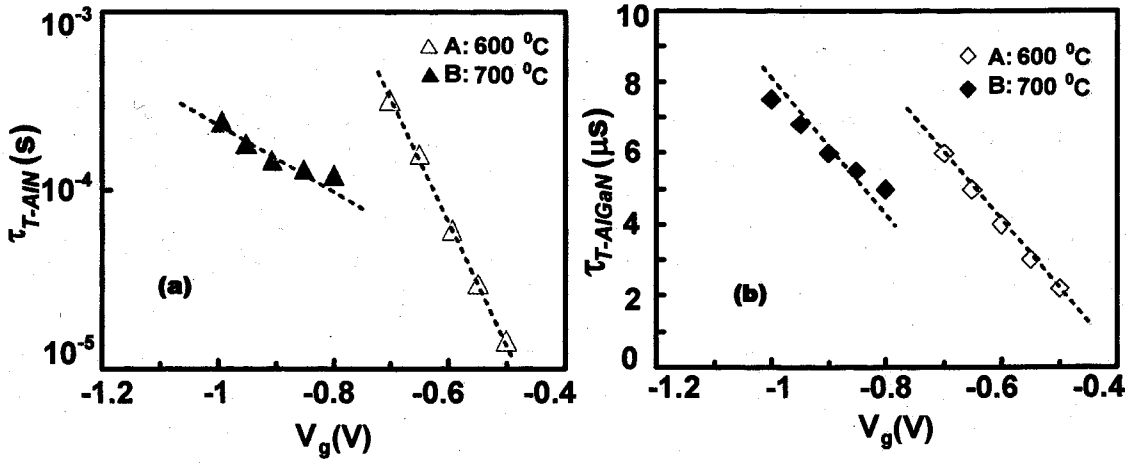

FIG. 5.7. Trap time constants of (a) AlN traps and (b) AlGaN bulk traps in *in-situ* MOCVD grown AlN/AlGaN/GaN MIS-HFETs with AlN layer grown at 600 and 700 °C.

The trap state energy level (E_T) is proportional to the τ_T, and therefore it can be deduced using the equation 4.1. Furthermore, the $D_{T\text{-}AlN}$ and $D_{T\text{-}AlGaN}$ as a function of corresponding E_T for MIS-diodes A and B are shown in figs. 5.8 (a) and (b). The minimum $D_{T\text{-}AlN}$ and $D_{T\text{-}AlGaN}$ values measured for MIS-diode A were 1.1 x 10^{11} and 1.2 x 10^{10} $cm^{-2}eV^{-1}$. Their corresponding energy levels were -0.47 and -0.36 eV below the conduction band. In contrast, the minimum $D_{T\text{-}AlN}$ and $D_{T\text{-}AlGaN}$ values observed for B at similar energy levels were 3.4 x 10^{12} and 5 x 10^{11} $cm^{-2}eV^{-1}$ respectively. By comparing the $D_{T\text{-}AlN}$ and $D_{T\text{-}AlGaN}$ at their respective E_T, it was observed unambiguously that $D_{T\text{-}AlN}$ and $D_{T\text{-}AlGaN}$ of MIS-diode A was one order of magnitude lower than B. This signifies that low T_G can favour a better AlN layer over AlGaN with reduced trap densities.

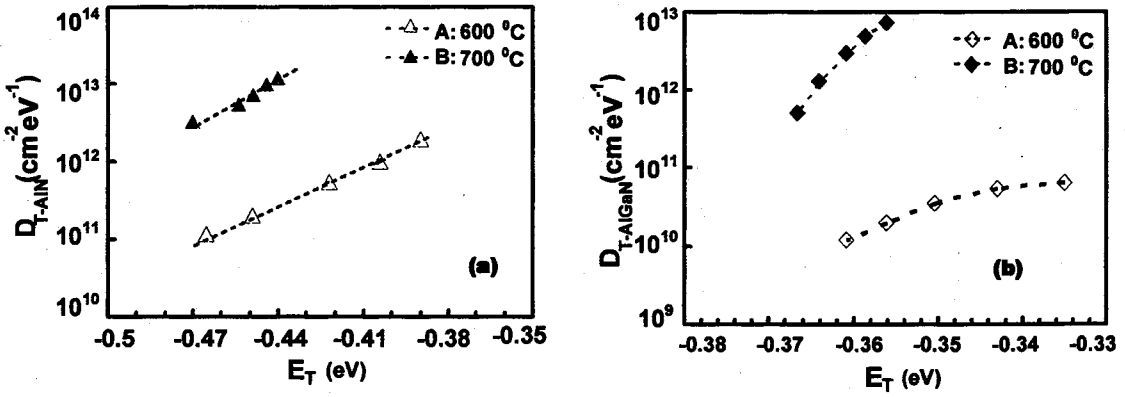

FIG. 5.8. The density of (a) AlN traps and (b) AlGaN bulk traps as a function of their energy levels below the conduction band of *in-situ* MOCVD grown AlN/AlGaN/GaN MIS-HFETs with AlN layer grown at 600 and 700 °C.

5.6. Summary

In summary, the experimental and the fitting results from extensive conductance studies on *in-situ* MOCVD grown AlN/AlGaN/GaN MISHs significantly shows the existence of two types of trap states and their correlation. Frequency dependent conductance analyses were performed on three different AlN based MIS-heterostructures with AlN growth temperatures. We observed the conductance dispersions in the cross over region can be caused by the AlN/AlGaN interface due to *in-situ* deposition of AlN insulating layer compared to the other existing *ex-situ* grown insulators. A $D_{T\text{-}mins}$ of 4.5 x10^{12} and 1 x 10^{11} cm^{-2} eV^{-1} at energy positions E_T (0.52 and 0.33 eV) below the conduction band were observed corresponding to the trap states of AlN insulating and AlGaN barrier layers respectively for AlN MISHs grown at 1030 °C.

Further, the trapping properties of *in-situ* MOCVD grown AlN/AlGaN/GaN MIS-HFETs with AlN layers grown at 600 and 700 °C has been quantitatively analyzed by frequency dependent conductance technique in order to identify the suitable growth condition for AlN layer. The AlN and AlGaN related traps were identified for both the

devices and were one order of magnitude lower for MIS-FET with AlN layer grown at 600 °C. They exhibited a lower $D_{T\text{-}AlN}$ and $D_{T\text{-}AlGaN}$ values of 1.1 x 10^{11} and 1.2 x 10^{10} $cm^{-2}eV^{-1}$ with characteristic energy levels at -0.47 and -0.36 eV below the conduction band.

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Chapter 6

Conclusions and future work

6.1. Conclusions

The results discussed in this dissertation were mainly focused on the importance of realizing high quality AlGaN/GaN based devices MIS-type on less expensive and large diameter silicon substrate. The results of the works lead to the location and reduction of hetero-interface and surface traps existing in the AlGaN/GaN based MIS-type devices on Si which were comprehensively and conclusively discussed with in each chapter. The conclusions drawn are mainly on the basis of extensive investigations performed within the scope of the work that lead to this dissertation. The summary of the results discussed according to individual chapters are as follows,

From this study, it was concluded that AlGaN/GaN hetero-interface states and (i) hetero-interface traps do exist near the AlGaN/GaN heterostructure interface and it was minimized my growing thicker buffer layers for AlGaN/GaN on Si, (ii) Further, a high~κ Al_2O_3 layer effectively passivates the surface traps existing in the AlGaN layer, and (iii) for using AlN as insulator for AlGaN/GaN MIS-type devices low temperature growth of AlN layer results in lower trap density due to AlN layer.

6.2. Future Work

It is well established that current collapse is a serious trap related phenomena that adversely affects the effective functioning of any GaN based high-power and high-frequency devices. The location and magnitude of these traps can be evaluated using existing techniques. Therefore the development of high quality *state-of-the-art* AlGaN/GaN devices on large size Si wafers (8 ~16 “) relies on the fact to minimize the

traps. This can be achieved by AlGaN/GaN MOS-HEMTs that can meet the requirements of near-future high-power, high-frequency and high-speed switching devices.

Therefore the objective of future work is to use AlGaN/GaN/Si HEMT heterostructure grown using thick buffer layers and to fabricate high quality high-κ material based AlGaN/GaN MOS-HEMT with negligible traps and associated current collapse for high-power and high-frequency potential applications.

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