1. Studies on MOCVD Grown AlGaN/GaN HEMTs on 4-in Si substrate for High Power Device Applications

Chapter 1
Introduction

Gallium Nitride has received tremendous attention ever since the first High-Electron-Mobility Transistor (HEMT) was demonstrated in 1993 [1]. Since then many advancements and device scaling have been reported securing an irreplaceable status for GaN based devices in the high power electronic device applications. What is important and interesting in an AlGaN/GaN HEMT is the formation of two-dimensional electron gas (2DEG) at the interface of an AlGaN/GaN heterostructure which causes high electron mobility and carrier density of $1x10^{13}$ cm^{-2} due to its piezoelectric and spontaneous polarization phenomenon. Further, these devices offer high saturation velocity, high speed and large current operation. The high breakdown field of GaN (E_c = 3 MV/cm) which is approximately three times greater than Si or GaAs makes promising candidate for high power device applications.

For power semiconductor switching applications, high breakdown voltage and lower specific ON-resistance (R_{ON}) are essential to minimize the power loss. AlGaN/GaN HEMTs are an excellent choice as they have high sheet carrier density and higher critical breakdown field. In order to achieve a high breakdown, there are many approaches reported namely field plate at gate, large gate-drain length (L_{gd}), *C*-doped buffer, *Fe*-doped buffer and Si substrate removal. These approaches have their own demerits namely, the field plate and substrate removal methods complicate the device process, *C* and *Fe* doping in the buffer creates deep levels and large L_{gd} causes large R_{ON}. Therefore our approach is based on growing a GaN with less dislocations by growing thick buffers between Si and GaN channel. This article deals with the growth of thick GaN on Si, breakdown mechanism and the challenges before GaN on Si.

1.1. MOCVD growth for GaN

Metal-organic chemical vapour deposition (MOCVD) is the most commonly used technique for the growth of GaN based devices. The growth quality and device characteristics obtained by MOCVD have superior performances than the GaN grown by molecular beam epitaxy (MBE). For example, the dislocation density (N_{dis}) of GaN grown by MOCVD is lower (of the order of $1x10^9$ cm^{-2}) compared to GaN grown by MBE which is of the order of $5x10^9$ cm^{-2}. The lower growth temperatures used in the MBE process might be the reason for high dislocation density. This leads to the fact that mobilities in MBE grown GaN are generally lower than those in MOCVD grown GaN [2]. Optical devices such as light-emitting diodes and laser diodes can work with such a high dislocation density, but electronic devices especially for power device applications, such high density of dislocations hamper the device performance. Therefore it is necessary to grow high quality GaN with reduced dislocations and imperfections using MOCVD.

1.2. Substrates for GaN devices

The substrates that are widely used for the growth of AlGaN/GaN HEMTs are SiC, sapphire and silicon. Inspite of the large mismatch in the lattice and thermal expansion co-efficient, Si is undoubtedly the substrate of choice as it favours large scale production at a reduced cost. Until now, only Si offers a large size (6-inches diameter) wafer growth. The table 1 given below lists the characteristics of using the Si substrate compared to SiC and sapphire for the growth of GaN.

Over the past several years, our group was involved optimizing the growth of AlGaN/GaN HEMTs on Si substrate. It was our group which first speculated the location of breakdown for AlGaN/GaN HEMTs grown on Si. In 2005 *Arulkumaran et. al.*, reported that GaN/AlN/Si junction is weaker than the AlGaN/GaN junction causing a low breakdown [3]. Since then, improving the quality of buffer and strengthening the AlN/Si junction have become the priorities of our research.

Table: 1 Substrates commonly used for the growth of GaN and the comparison of their properties.

Substrate characteristics	6H-SiC	c-sapphire	Si (111)
Lattice mismatch to GaN [%]	3.5	16.1	17.0
Thermal expansion [10^{-6} K^{-1}]	5.0	a: 7.5	4.08
(GaN : a ~ 5.5)		c: 8.5	
Thermal conductivity [W/cm·K]	4.9	0.3 ~ 0.5	1.5
Cost (per 3 inch)	US$ 2500	US$ 800	US$ 50
Size [inch]	2 ~ 3	2 ~ 4	3 ~ 6

All the HEMT device structures mentioned in this report were grown by Taiyo Nippon Sanso (SR4000) horizontal MOCVD reactor using 4-inches *p*-Si (111) substrate. The resistivity of the *p*-Si substrate is 1 – 3 Ω·cm. Trimethylgallium (TMG), trimethylaluminium (TMA) and Ammonia (NH_3) were used as Ga, Al and N sources respectively for the MOCVD growth.

1.3 Outline of the Report

This report is organized into 4 chapters. This Chapter-1 outlines the introduction for GaN devices and its growth on various substrates. Chapter-2 summarizes the experimental results out of using thin gate dielectrics at the Schottky gate terminal of the High Electron Mobility Transistors (HEMTs). The different thin gate dielectrics namely oxidized Al [4-6], MOCVD grown AlN were used and its device characteristics are discussed. Chapter-3 discusses the approach adapted to increase the breakdown of AlGaN/GaN HEMTs. By growing thick epi-layers of AlGaN/GaN HEMTs, the breakdown were improved and various leakage currents affecting the breakdown were discussed [7-8]. Chapter-4 describes the existing challenges before GaN on Si [9-10]. The appearance of deep-pits on the growth completed wafer poses a major challenge for the MOCVD

growth on Si [9-10]. Deep-pits of various densities are used for the HEMT device process and the characteristics are studied by electrical and optical measurements. The summary of the results are listed in Chapter-5.

References:

[1]. M. Asif Khan, A. Bhattarai, J. N. Kuznia, and D. T. Olson, Appl. Phys. Lett., **63** (1993) 1214.

[2]. D. C. Look and J. R. Sizelove, Phys. Rev. Lett., **82** (1999) 1237

[3]. S. Arulkumaran, T. Egawa, S. Matsui, and H. Ishikawa, Appl. Phys. Letts., **86** (2005) 123503.

[4]. S. L. Selvaraj and T. Egawa, Appl. Phys. Lett., **89** (2006) 193508.

[5]. S. L. Selvaraj and T. Egawa, J. Electrochem. Soc., **156** (2009) H690.

[6]. S. L. Selvaraj, T. Ito, Y. Terada and T. Egawa, Appl. Phys. Lett., **90** (2007) 173506.

[7]. S. L. Selvaraj, T. Suzue and T. Egawa, Electron. Dev. Lett., **30** (2009) 587.

[8]. S. L. Selvaraj, T. Suzue and T. Egawa, 67th IEEE Device Research Conference Digest (2009) pp.283.

[9]. S. L. Selvaraj, T. Suzue and T. Egawa, Appl. Phys. Express **2** (2009) 111005.

[10]. S. L. Selvaraj, A. Watanabe and T. Egawa, Appl. Phys. Lett., **98** (2011) 252105.

Chapter 2

Thin gate insulators for AlGaN/GaN HEMTs on Si

In this chapter, AlGaN/GaN HEMTs with different gate dielectrics were discussed along with their device performance. The thin insulators experimented in this chapter are thin Al which oxidizes into thin aluminum oxide and MOCVD grown AlN.

2.1. Thin 3 nm Al at the Schottky

There is a need to enhance the drain current density and output power of AlGaN/GaN HEMTs for making it attractive for high power device applications. Background doping, δ-doping, increasing the barrier height are common methods to increase the electron concentration at the 2DEG channel. It is our objective to increase the drain current density by adding 3 nm Al prior to gate metal deposition. Recently Nanjo *et al.*[4] have studied the effect of 3 nm e-beam evaporated Al layer prior to the gate (Ni/Au) metal on AlGaN/GaN HEMTs. In this letter, the effect of 3 nm Al layer in the gate metal of the HEMT (Al-gated HEMTs) was studied and reported. As e-beam Al evaporation is not recommended, [5] in the current study we used filament heating method to evaporate Al under high vacuum conditions. The dc, capacitance-voltage (*CV*) and breakdown voltage (*BV*) characteristics of the Al-gated HEMTs in comparison with Pd-gated HEMTs are presented with necessary explanation.

The AlGaN/GaN HEMTs were grown on 4 inch p-Si (111) substrate by metal organic chemical vapour deposition (MOCVD) system using Taiyo Nippon Sanso SR-4000. The HEMT structure growth and electrical parameters were published earlier [7,8]. The device process started with mesa isolation by BCl_3 plasma based reactive ion etching (RIE) [9] and passivated with SiO_2 deposited by electron beam evaporation with substrate temperature at 150 °C. Ohmic contacts were patterned with Ti/Al/Ni/Au (20/72/12/40 nm) metals followed by lamp annealing at 850 °C for 30 s

in N_2 ambient. Gate metals Al/Pd/Ti/Au (3/40/20/60 nm) were formed using conventional photolithography. All the metals except Al were deposited by electron beam evaporation method whereas Al was evaporated by filament heating technique. For comparison, a separate HEMT was fabricated without Al metal and will be referred to as Pd-gated HEMTs. The dimensions of the fabricated HEMTs are: source-drain spacing (L_{sd}) = 10 μm; gate width (W_g) = 15 μm; gate length (L_g) = 2.0 μm and source-gate spacing (L_{sg}) = 3.0 μm. *C-V* measurements were carried out at 1MHz using HP4845 LCR meter. The dc I_{DS}-V_{DS} and *BV* characteristics on the 15μm and 200 μm device dimensions respectively were studied using Agilent 4156c semiconductor parameter analyzer.

Figure 2.1(a) shows good pinch-off *I-V* characteristics for the HEMTs over a drain bias (V_{DS}) of 0 to 20 V with an increase in the $I_{DS\,max}$ for Al-gated HEMTs. A maximum drain current density ($I_{D\,max}$) of 616, 730 mA/mm and peak transconductance ($g_{m\,max}$) of 173 and 151 mS/mm were observed for the Pd-gated and Al-gated HEMTs respectively. Any increase in I_{DS} is expected when the 3 nm Al metal forms a defect free contact with AlGaN cap layer depriving or minimizing the interface states in the region. Threshold voltages ($V_{th\text{-}IV}$) from *I-V* measurements were -2.5 and -3.1 V for Pd-gated and Al-gated HEMTs respectively.

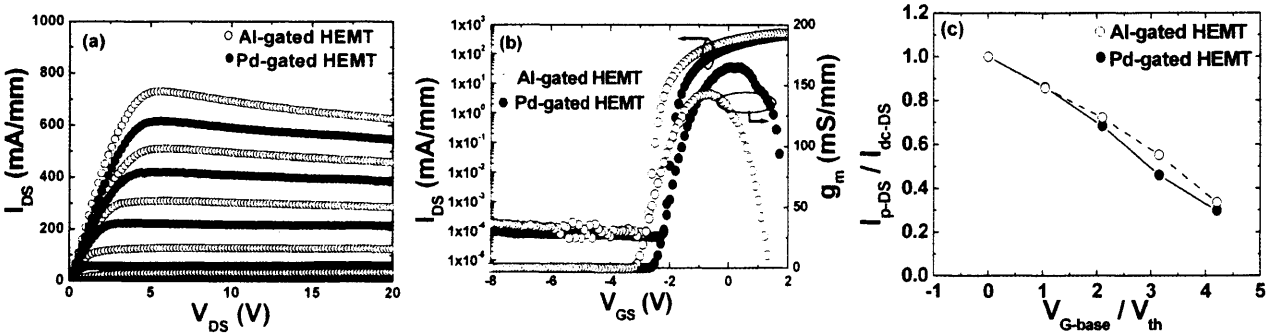


Fig. 2.1. (a) DC-*IV* measurements for W_g = 15μm HEMTs; (b): I_{DS}, g_m for the Pd-gated and Al-gated HEMTs; (c): Pulse current normalized to the dc current ($I_{dc\text{-}DS}$) at zero gate bias *vs* the gate voltage ($V_{G\text{-}base}$) normalized to threshold voltage.

Due to the increase of Schottky-gate channel separation, decrease of $g_{m\,max}$ and negative V_{th} shift has been observed for Al-gated HEMTs. Moreover, the increase of barrier thickness leads

to the increase of sheet carrier concentration due to strengthened polarization effect [10]. Similar increase of sheet carrier density and a subsequent enhancement of $I_{DS\,max}$ was also observed by Kordos *et al.*, [11] by depositing 12 nm SiO_2. If the 3 nm Al deposited forms an oxide layer as observed by Nanjo *et al.*, [4] then the decrease of g_m is inevitable due to increase in the Schottky-channel gap [12].The increase of 2DEG carrier density and negative shift of threshold voltage for Al-gated HEMTs were also confirmed by *C-V* measurements.

To study the effect of Al metal over current collapse phenomenon, pulsed *I-V* measurements were carried by applying a pulsed bias of 1 μs duration with 50% duty cycle [13]. The amplitude of the pulsed bias swept from 0 V to $V_{G\text{-base}}$ which is less than the threshold voltage (V_{th}). For comparison, a plot of pulse current normalized to the dc current at V_g = 0V versus the gate voltage ($V_{G\text{-base}}$) normalized to the threshold voltage is shown in Fig 1(c). It is found that the Al-gated HEMTs does not show any additional current collapse over Pd-gated HEMTs. Two terminal gate leakage current measurements carried on the 200 μm HEMTs as in Fig.2 shows that the Pd-gated HEMTs have less gate leakage than Al-gated HEMTs. Because of low leakage current, higher OFF-state breakdown voltage of Pd-gated HEMTs were exhibited [8]. The Al-gated HEMTs found to have higher ON-state breakdown voltage when compared to Pd-gated HEMTs [inset of Fig. 2.2]. This proves that the *BV* characteristics of the devices were not degraded due to the presence of Al in the gate metal.

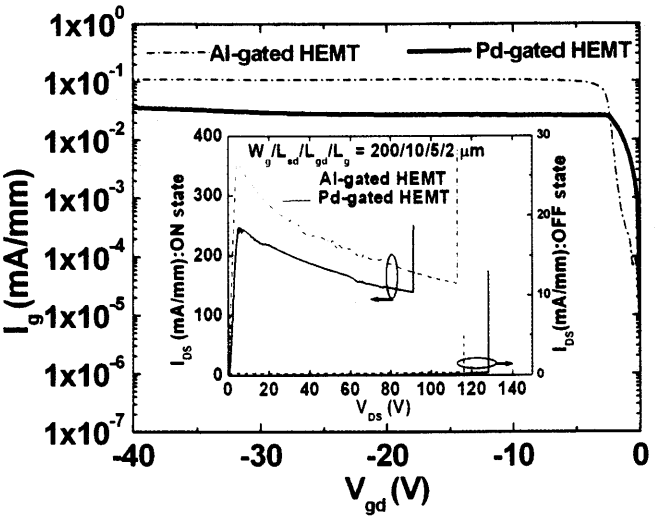


Fig. 2.2. Two terminal gate leakage *I-V* measurements of Pd-gated and Al-gated HEMTs (W_g = 200 μm); Inset: Three terminal ON-state and OFF state BV_{gd} characteristics.

The presence of Al layer in the gate metal shows a difference in the capacitance measured

at zero bias. Further the carrier concentration *vs* depth profile [Fig. 2.3] illustrates that 2DEG channel is formed at 21 and 25 nm for HEMTs without and with 3 nm Al respectively. Therefore we confirm that the depth of the 2DEG channel is shifted additionally by 4 nm for Al-gated HEMTs. This makes it clear that 3 nm Al deposited does not become part of the gate metal composition, but oxidized resulting in the increase of 2DEG depth from the virtual gate metal Pd/Ti/Au. Using the capacitance value at zero bias [Inset of Fig. 2.3], theoretically [14,15]. the thickness of the oxide layer was calculated to be 3.75 nm which is close to the actual thickness (3 nm) of the Al layer deposited and also the variation of the 2DEG position from *C-V* (4 nm). The threshold voltage measured from *CV* ($V_{th\text{-}CV}$) also confirms a shift for Al-gated HEMTs (Table 1.) due to increased Schottky-channel separation. Similar results have been observed for SiO_2/AlGaN/GaN MOS-HEMTs [14].

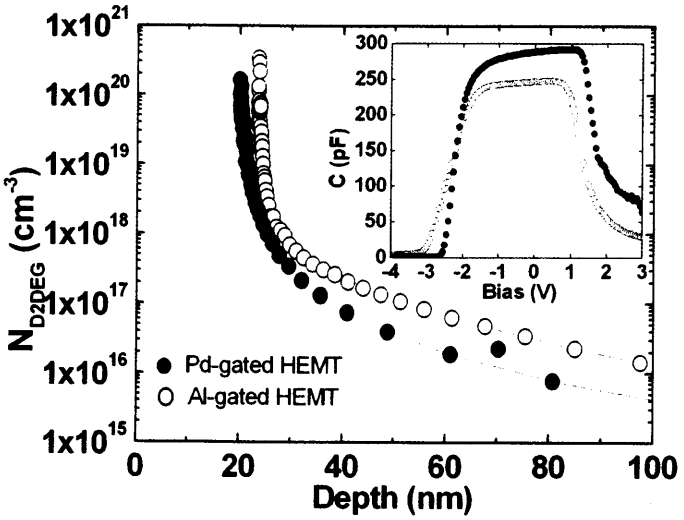


Fig. 2.3. 2DEG carrier concentration *vs* depth profile; Inset: *C-V* measurements of the HEMTs.

Considering the fact that Al was deposited under ultrahigh vacuum conditions, the source of oxygen for the formation of Al-O is questionable. As Al is highly reactive to oxygen, large number of oxygen atoms that are present in the AlGaN cap layer [16]. forms Al-O when it comes in contact with a thin 3 nm Al layer in the gate. It is these oxide interface states present in the AlGaN cap layer that initiates the formation of Al-O between the gate and the AlGaN. Similar Al-O formation at the interface has been found in the literature [4,17]. Therefore at this UHV condition, the out diffusion of oxygen atoms from the bulk AlGaN layer was the possible cause for oxide formation in the gate area depriving the defect states with increased Schottky-channel separation.

Table I. Device parameters of SiO_2 passivated Pd-gated and Al-gated AlGaN/GaN HEMTs on 4 inch Silicon

Parameters	Pd-gated HEMT	Al-gated HEMT
$I_{DS\,max}$ (mA/mm)	616	730
$g_{m\,max}$ (mS/mm)	173	151
N_{D2DEG} (x 10^{20} cm^{-3})	1.6	3.5
Depth of 2DEG (nm)	21	25
$V_{th\text{-}IV}$ (V)	-2.5	-3.1
$V_{th\text{-}CV}$ (V)	-2.5	-3.0
BV:ON (V) *Wg* = 200 μm	91	113
BV:OFF (V) *W*g = 200 μm	128	116

The chemical composition of the deposited gate metal layers were analyzed by studying the depth profile of AES to confirm the presence of Al-O. The intensity peaks for the gate metals namely Au, Ti and Pd were observed as shown in Fig. 2.4. Oxygen peaks were observed around 1600 s for Al-gated HEMTs, and the same was absent for the Pd-gated HEMTs [Fig. 2.4(a)]. For Al-gated HEMTs, the designated peaks for Al were partially observed in the same region as that of oxide and becomes significant after 1700 s which is due to the 26% Al composition in the AlGaN cap layer. This confirms that the 3 nm Al layer has partially transformed into a thin oxide layer between the Pd gate and the AlGaN cap layer. Further the oxide layer was identified to be Al_2O_3 by recording the XPS spectra. A designated XPS peak (spectrum not shown) at 74.6 eV confirms [18]. the oxide as Al_2O_3 at the Schottky.

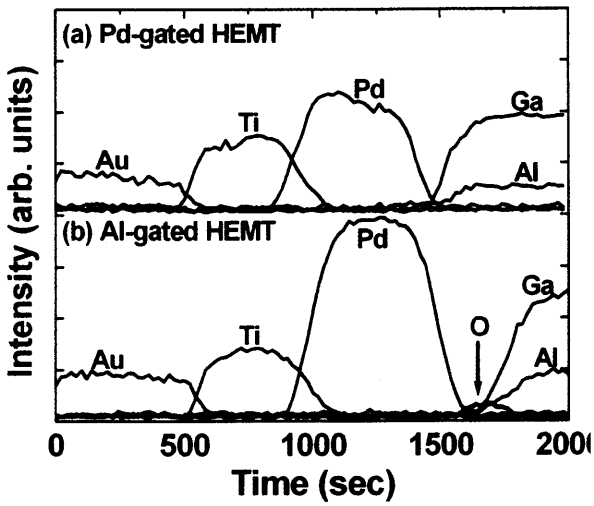


Fig. 2.4. AES depth profile over 1μm gate area for (a) Pd-gated HEMTs and (b) Al-gated HEMTs.

2.2. Plasma Oxidized Al as gate dielectric

The presence of an insulator or oxide layer at the gate dielectric permits the application of high positive gate voltages to further increase the sheet electron density in the 2DEG channel and thus yielding maximum device current. In the past, different insulators like SiO_2, SiNx, SiON, TiO_2, HfO_2 etc were studied for application as a gate dielectric in the designing of MISFET, MOSFET etc. Among these insulators, SiO_2 has been widely used as a gate dielectric and for passivating GaN based devices. Though SiO_2 does not have an immediate rival for replacement in near future, SiO_2 has serious limitations in controlling the gate leakage and current collapse. Scaling of gate oxide insulating materials is facing a critical fundamental limit in the case of SiO_2 as tunneling and gate leakage phenomena causing circuit failures and device degradation. Therefore alternate insulating materials like AlN [19], Al_2O_3 as gate dielectrics for GaN based devices are an important subject of investigation.

There is a wide application of ultrathin Al_2O_3 as a gate dielectric [15,20-23] and for device passivation [24]. Due to its high dielectric constant (ε = 9), Al_2O_3 is a highly desirable gate dielectric with a high band gap (around 9 eV). Further Al_2O_3 has high breakdown field (5-10 MV/cm), high thermal stability (up to 1000°C) and remains stable under typical processing conditions [25]. A good quality of α–Alumina (Al_2O_3) has a combination of interesting properties such as great hardness, high wear resistance and chemical inertness [26]. This promotes the application of Al_2O_3 as an excellent passivation material as well as a gate dielectric for GaN based MOS devices. Different techniques are possible for the growth of good quality Al_2O_3. Of these, a simple method to obtain Al_2O_3 is by evaporating a thin aluminum metal followed by plasma oxidation [27]. Kuiper et al., [28] have reported the formation of Al_2O_3 by plasma oxidizing a thin Al layer. A more detailed analysis of AlGaN/GaN MOSHFETs using 4 nm Al_2O_3 as gate dielectric was done by Kordos et al., [29,30].

In the previous section (2.1) it was described [31] that presence of a thin Al layer between the Schottky gate metal and AlGaN barrier, removes oxide interface states at AlGaN to form an aluminum based oxide (AlO). This un-intentionally formed AlO on top of AlGaN layer motivated us to try for an intentionally oxidized Al layer by O_2 plasma. Further our interest is to explore a simple method of forming an aluminum oxide (Al_2O_3) at the Schottky contact as an effective gate dielectric. Hence this report analyses the HEMT device characteristics of three different treatments at the Schottky gate terminal namely (i) a regular Schottky contact of Pd/Ti/Au, (ii) 3nm Al/Pd/Ti/Au and (iii) 3nm Al/O_2 plasma oxidation / Pd/Ti/Au.

The AlGaN/GaN HEMT structures were grown on 4 in. semi insulating Si (111) substrate using Taiyo Nippon Sanso SR-4000 metal-organic chemical vapor deposition (MOCVD) horizontal growth chamber. The Aluminum concentration for 20 nm AlGaN barrier layer was fixed at 26%. Van der Pauw Hall measurements on the sample yielded a hall mobility of 1576 cm^2/Vs, sheet resistance of 356 Ω/square and sheet carrier concentration of 1.2 x 10^{13} cm^{-2}. Inclusion of a thin 1nm AlN spacer layer causes an increase in the hall mobility as it shields the electrons in the 2DEG channel from alloy and interface scattering.

The device process started with a mesa isolation by BCl_3 plasma based reactive ion etching, followed by 100 nm electron beam evaporated SiO_2 as passivation layer. Using conventional lithography source/drain Ohmic contacts (Ti/Al/Ni/Au : 15/72/12/40 nm) were made on to the devices and annealed at 850°C for 30 seconds while flowing Nitrogen gas. After the gate lithography, the 100nm SiO_2 in the gate opening was wet-etched; further cleaned with 1 min HCl and the process continued with three different treatments at the gate opening as listed below:

(i) Making a final metal contact of Pd/Ti/Au (HEMTs) – a conventional method of making a Schottky gate contact

(ii) 3nm deposition of Al under high vacuum, continued with gate metal deposition of Pd/Ti/Au

(Al-based MOS-HEMTs). Here the samples_were not exposed to atmosphere as the metals namely Al/Pd/Ti/Au (3/40/20/60 nm) were evaporated continuously. These devices are named Al-based MOS-HEMTs.

(iii) 3 nm deposition of Al under high vacuum at an evaporation rate of 0.05 Å/sec. After the Al evaporation, the samples were quickly transferred to plasma oxidation chamber for O_2 plasma oxidation (10 watt power/3 Pa for 5 minutes). After the plasma treatment, samples were cleaned with HCl (1 min) before returning to the metallization chamber for gate metal evaporation. These devices are named as plasma treated MOS-HEMTs.

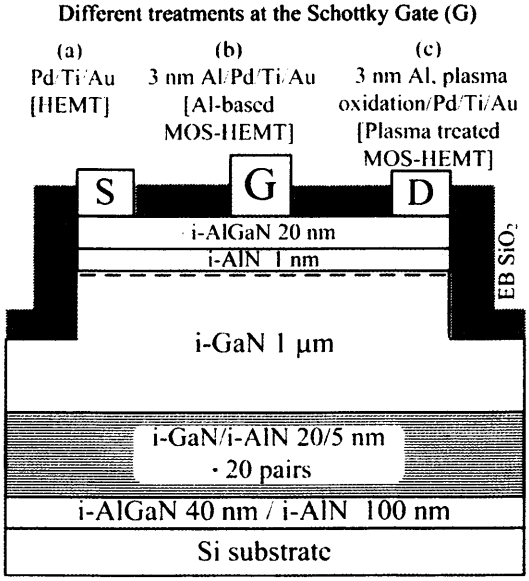


Fig. 2.5. SiO_2 passivated AlGaN/GaN HEMT structures with different treatments at the Schottky contact.

For all the above samples, before metal deposition they are cleaned with HCl for 1 min and rinsed with de-ionized water to have a defect free surface. In the above process, the deposition of Aluminum under very high vacuum is necessary in order to suppress the gate leakage. Therefore the Al was evaporated at the chamber pressure of $8x10^{-5}$ Pa. The device characteristics of Al based MOS-HEMTs and the plasma treated MOS-HEMTs are compared to conventional HEMTs. (Table I). For an easy understanding and comparison, the processed devices are better identified in figure 2.5.

The dimensions of the fabricated HEMTs are as follows: source-drain spacing (L_{sd}) = 8 μm, gate width (W_g) = 15 μm, gate length (L_g) = 1.5 μm, and source-gate spacing (L_{sg}) = 3.0 μm. Capacitance-voltage (C-V) measurements were carried out at 1 MHz using HP4845 LCR meter. The static I_{DS}-V_{DS} measurements were measured using Agilent 4156c semiconductor parameter

analyzer.

Figure 2.6 shows the polarized 2DEG density of electrons forming an electron channel respectively at 19, 23 and 24 nm for HEMTs, Al based MOS-HEMTs and plasma treated MOS-HEMTs. The depth of 19 nm was observed for HEMTs in the absence of any oxide or insulating layer between Schottky contact and AlGaN. But the Schottky contact – 2DEG channel separation is increased for Al based and plasma treated MOS-HEMTs. This means there is an additional increase in the barrier layer due to the presence of an insulating oxide layer. The out diffusion of oxide inter-states present at the AlGaN cap layer into 3 nm Al layer facilitates the formation of AlO or Al_2O_3[16]. In the previous section we confirmed the presence of an aluminum based oxide at the Schottky for Al-gated HEMTs [31] by Auger Electron Spectrum. The oxide layer was identified as Al_2O_3 by recording the x-ray photoelectron spectrum (XPS) shown in figure 2.7 with a peak at 74.6 eV assigned for Al_2O_3 [32]. This formation of an oxide insulating layer at the Schottky contact increases the 2DEG channel depth to 23-24 nm for the MOS-HEMTs.

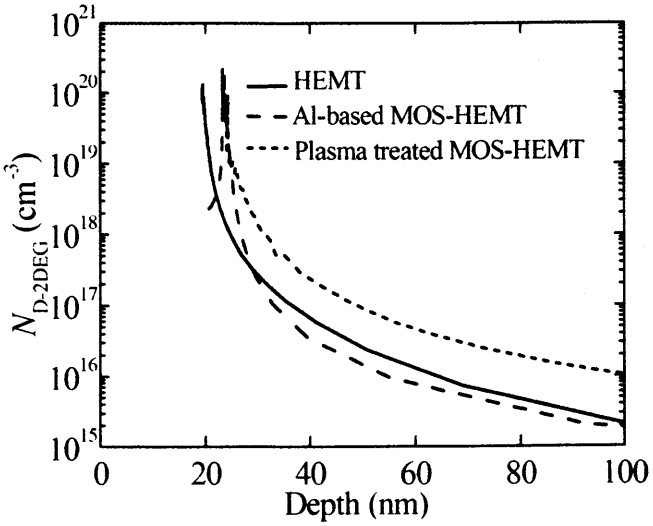


Fig. 2.6. 2DEG depth profile of the fabricated HEMT, MOS-HEMTs from *C-V* measurements.

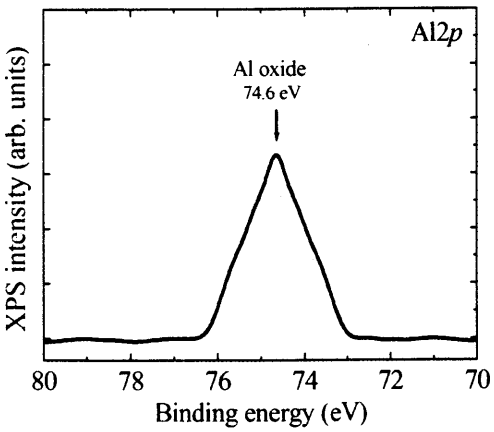


Fig. 2.7. *XPS* Al2*p* spectra for plasma oxidized Al at the Schottky contact.

To study the interface quality of this newly formed oxide and semiconductor (Al_2O_3/AlGaN interface), high frequency (1 MHz) *C-V* measurements were performed on the

MOS-HEMTs. Capacitance was measured by continuously sweeping the voltage (+4 V to -6V to +4 V) as shown in Fig. 2.8. The hysteresis was not observed for Al-based MOS-HEMT, signifying a low interface defect states between Al_2O_3 and AlGaN. On the contrary a considerable hysteresis voltage (V_{hys} = 0.2 V) was observed for MOS-HEMTs with plasma oxidized Aluminum at the Schottky contact. From this we observe that Al_2O_3 formation by natural diffusion of oxide states at the AlGaN into 3 nm Al forms a good interface compared to plasma treated Aluminum. Therefore the 2DEG carrier concentration is maximum for Al based MOS-HEMTs (2.4 x 10^{20} cm^{-3}) and a decrease is observed for plasma treated MOS-HEMTs (0.9 x 10^{20} cm^{-3}) which is probably due to plasma damage causing an increased defective states at the Al_2O_3/AlGaN interface.

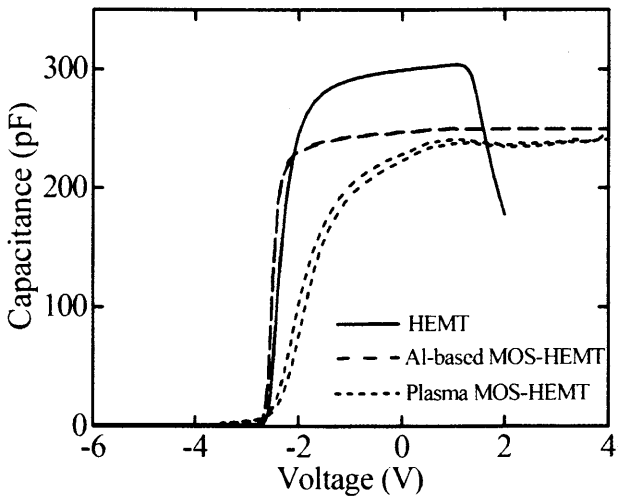


Fig. 2.8. *C-V* characteristics measured at 1 MHz for Schottky, Al-based and Plasma treated MOS diodes.

With the formation of the 2DEG channel at a depth of 23-24 nm from the gate for the MOS-HEMTs, the AlGaN and oxide layers are considered to contribute two capacitance's connected in series. Therefore the total capacitance is given by the equation [33],

$$\frac{1}{C_{MOSHEMT}} = \frac{1}{C_{OX}} + \frac{1}{C_{HEMT}} \qquad (1)$$

Here the oxide capacitance C_{ox} is inversely proportional to its thickness d_{ox}, hence with increasing oxide thickness layer the oxide capacitance decreases as per equation

$$C_{OX} = \frac{\varepsilon_o \varepsilon_{ox} A}{d_{ox}} \qquad (2)$$

where the dielectric constant of the oxide (Al_2O_3) ε_{ox} = 9 and ε_o is the vacuum permittivity. A Schottky diode of radius 150 μm is available at the same HEMT mask. Using *C-V* measurements on the MOS diode of area 7.07×10^{-4} cm^{-2}, the zero bias capacitance are respectively 299 pF and 249 pF for Pd-contact Schottky diodes and Al-based MOS diodes. Thus the thickness of the oxide layer formed was calculated using the above equation as 3.8 nm which is close to the total depth of the 2DEG channel observed experimentally for Al-based MOS-HEMTs (23 nm). Similarly, the thickness of the O_2 plasma oxidized Al layer was calculated to be 4.6 nm, forming the 2DEG channel at a depth of 24 nm for plasma treated MOS-HEMTs.

Table II. Device characteristics of the HEMTs, Al-based MOS-HEMTs, and plasma treated MOS-HEMTs.

Device parameters	HEMT	Al-based MOS-HEMTs	Plasma treated MOS-HEMTs
$n_{sC\text{-}V}$ (x $10^{13}cm^{-2}$)	2.0	5.2	1.1
$\mu_H . n_{sC\text{-}V}$ ($x10^{16}V^{-1}s^{-1}$)	3.2	8.2	1.7
2DEG depth (nm)	19	23	24
$N_{d\text{-}2DEG}$ ($10^{20}cm^{-3}$)	1.3×10^{20}	2.4×10^{20}	0.9×10^{20}
I_{DSmax} for V_G=+2.5 V (mA/mm)	714	900 (1086 for V_g = +3.5 V)	540 (662 for V_g = +3.5 V)
$g_{m\ max}$ (mS/mm)	151	209	150
R_s (Ω.mm)	1.8	1.1	3.9
V_{th} from *I-V* (v)	-2.4	-2.6	-2.0
I_{gleak} (mA/mm) @ -40V	1.2×10^{-1}	1.9×10^{-2}	1.1×10^{-2}
Forward ON voltage V_{ON}	0.9	1.6	2.3

The static I_{DS}-V_{DS} characteristics of the HEMTs and MOS-HEMTs are shown in Figure. 2.10. The HEMTs show proper operation as a FET for V_G up to +1.5 V, but significant gate leakage current observed for V_G higher than +2.5 V as shown in figure 2.9(a). On the other hand Al based and plasma treated MOS-HEMTs have an I_{DS}-V_{DS} curve free from gate leakage for gate bias as high as +3.5 V. Though there is an increase in the $I_{DS\text{-}max}$ for Al based MOS-HEMTs, the drain current density decreases for plasma treated MOS-HEMTs which is due to the plasma damage. The maximum drain current density obtained for the plasma treated MOS-HEMTs are low in

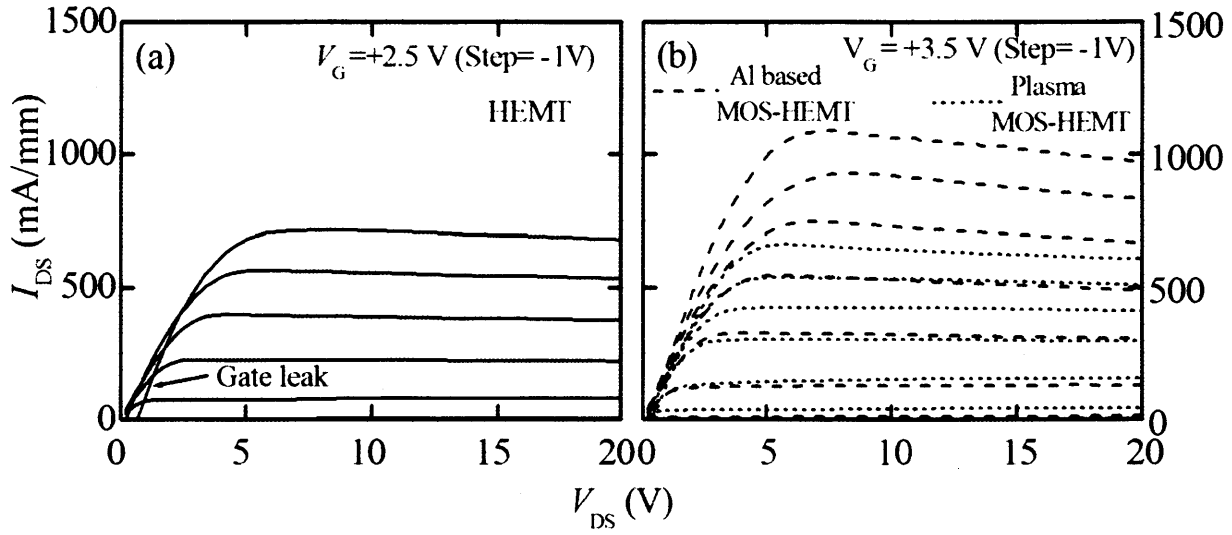


Fig. 2.9. Static I_{DS}-V_{DS} characteristics of HEMT, MOS-HEMTs with device dimensions W_g/L_g = 15/1.5μm.

accordance with the product value of $\mu_H.n_{sC\text{-}V}$ where $n_{sC\text{-}V}$ is the integrated carrier concentration from *C-V* measured 2DEG profile. Further a comparatively high source resistance of 3.9 Ω.mm for plasma treated MOS-HEMTs is an indication that the plasma damage hampers the mobility of charge carriers in the cap layer.

Here we observe that insertion of thin oxidized Al has brought a significant improvement in applying a high gate voltage (+3.5 V) for a good I_{DS}-V_{DS} characteristics without gate leakage. Further aluminum based oxide effectively increases the gate voltage operation needed for transistor operation at high gate voltage. The fabricated devices were tested for drain current collapse (results

not shown) and we found a reduction in the drain current collapse because of the O_2 plasma oxidized Al layer for MOS-HEMTs. A homogeneous and good quality of Al_2O_3 as an insulating layer at the Schottky contact is needed to completely eliminate drain current dispersion.

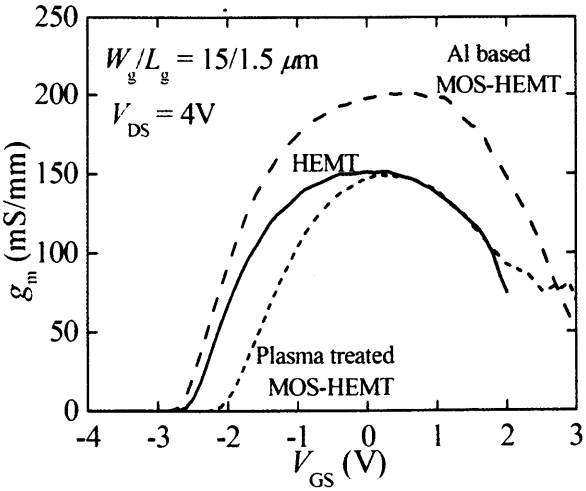


Fig. 2.10. Transconductance (g_m) measurements for the HEMT, MOS-HEMTs.

The transconductance measured on these HEMTs are shown in figure 2.10. The Al based MOS-HEMTs have a high transconductance maximum ($g_{m\text{-}max}$) of 209 mS/mm. The HEMTs and plasma treated MOS-HEMTs have an identical $g_{m\text{-}max}$ around 150 mS/mm. The HEMTs and the Al-based MOS-HEMTs have device threshold voltage -2.4 and -2.6V respectively. A small negative shift in the threshold voltage for Al-based MOS-HEMTs with respect to HEMTs is due to increase in the Schottky contact - channel separation. However, the plasma treated MOS-HEMTs have a positive shift in the threshold voltage

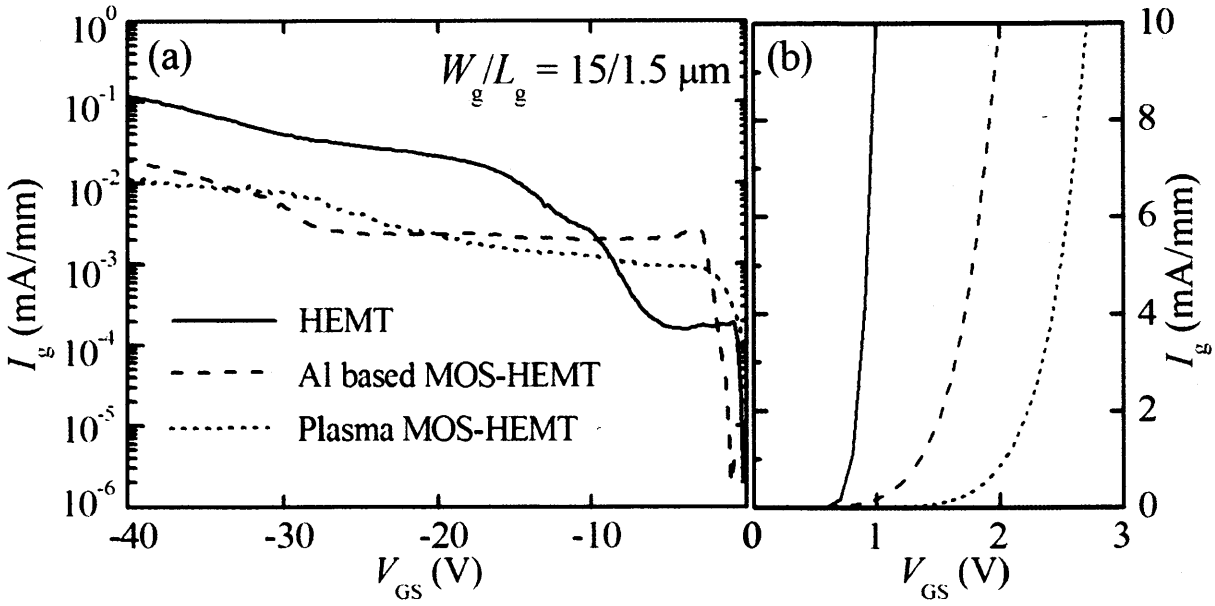


Fig. 2.11. (a) Two terminal gate leakage measurements and (b) forward *I-V* characteristics.

in spite of an increase in the Schottky contact - 2DEG channel separation. This is because of a decrease in the polarized 2DEG channel concentration caused by the damage during plasma oxidation.

Two terminal gate leakage currents were measured between the gate and drain terminals of the HEMTs and MOS-HEMTs (W_g=15 μm). Figure 2.11 (a) shows the gate leakage observed for Al based MOS-HEMTs and plasma treated MOS-HEMTs are an order less than conventional HEMTs. The chamber pressure during the deposition of Al is very important with regard to suppressing the gate leakage. Depositing Al at high vacuum is necessary to reduce the gate leakage. Kotani *et al.* [34] have reported a thin Aluminum layer deposition followed by O_2 plasma yielded (Al turned into Al_2O_3) two orders of magnitude reduction in the gate leakage. Suppressing the gate leakage is very important to attain a high breakdown in the devices. Further there is an increase in the forward ON voltage (V_{ON}) for the MOS-HEMTs as can be seen in figure 2.11 (b) confirming the presence of Al based oxide dielectric at the Schottky contact.

2.3. MOCVD grown AlN capped MIS-HEMTs

In the previous two sections, the gate dielectrics used were ex-situ grown. In this section gate insulator using in-situ grown AlN and its device characteristics are described. Aluminum Nitride (AlN) with a large band gap of 6.2 eV and reduced mismatch to GaN is suitable for the application as gate insulator and passivation for AlGaN/GaN high-electron-mobility Transistors (HEMTs) [35]. AlN passivation reduces the surface states which are responsible for the current collapse under large signal RF modulation. The AlN/AlGaN metal-insulator-semiconductor FETs (MISFET) offers the possibility of utilizing devices with a very wide band gap material under the gate thus yielding a reduced gate leakage and high breakdown. Further AlN based MISFETs would be preferred for high-temperature operations, because an additional insulator could provide higher

potential barrier between the Schottky and the channel, which suppresses the thermionic emission, tunneling at high temperature and keeps the gate voltage swing reasonably large for proper operation. In literature MISFETs using AlN cap layer over AlGaN/GaN on sapphire are widely reported [36-38] as the lattice mismatch of the AlN growth on sapphire is less. On the other hand the AlN based MISFETs on silicon are very difficult to achieve due to increased lattice mismatch between AlN and silicon. For reduced mismatch and good morphology of AlN on silicon, metal-organic chemical vapour deposition (MOCVD) technique could be utilized with properly controlled growth mechanism in an oxygen-free environment. AlN based metal-insulator-semiconductor high-electron-mobility transistor (MIS-HEMT) on 4 in. silicon and its device characteristics are discussed here.

The MIS-HEMT structure shown in Fig. 2.12 was grown using Taiyo Nippon Sanso, SR 4000 horizontal metal organic chemical vapour deposition (MOCVD) set up. The morphology of the MOCVD grown AlN films were investigated by x-ray diffraction (results not shown), atomic force microscopy (AFM) and electrical resistivity by Van der Pauw Hall-effect measurements. To compare the device characteristics, a separate structure was grown without the 2nm *i*-AlN cap layer and subjected to HEMT device processing simultaneously. The devices were passivated with 100 nm SiO_2 followed by source, drain and gate contacts patterned using lithography. The dimensions of the fabricated HEMTs / MIS-HEMTs are: source-drain spacing (L_{sd}) = 8 μm; gate width (W_g) = 15 μm; gate length (L_g) = 2.0 μm and source-gate spacing (L_{sg}) = 3.0 μm.

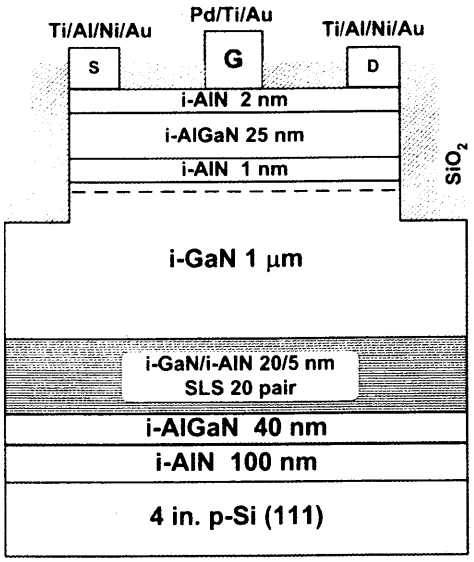


Fig. 2.12. Schematic diagram of the 100 nm SiO_2 passivated AlN/AlGaN/GaN MIS-HEMT.

Table III. Device parameters of SiO2 passivated AlGaN/GaN HEMTs and AlN/AlGaN/GaN MISHEMTs on 4 in. Si.

Device parameters	HEMT	MIS-HEMT
R_{MS} roughness (nm)	0.21	1.03
P-V (nm)	5.06	9.52
R_c (Ω.mm) TLM	2.6	5.1
n_s (x10^{13} cm^{-2})	0.87	1.37
2DEG Mobility (cm^2/Vs) @300 K	1863	1032
R_{sh} (Ω / □) Hall effect	384	441
N_{D2DEG} (x 10^{20} cm^{-3})	0.6	1.6
Depth of 2DEG (nm)	22	20
$I_{DS\,max}$ (mA/mm)	541	361
$g_{m\,max}$ (mS/mm)	134	152
$V_{th\text{-}IV}$ (V)	-2.6	-1.8
$V_{th\text{-}CV}$ (V)	-2.8	-1.9
$I_{g\,leak}$ (mA/mm) @ V_g = - 40 V	1.8x10^{-4}	4.2x10^{-6}
BV (Volt)	124	230
$V_{ON\,forward}$ (Volt)	1.0	1.5

The dc I_{DS}-V_{DS}, current collapse measurements using Agilent 4156c semiconductor parameter analyzer, and breakdown (*BV*) characteristics using Sony-Tektronix 370A were studied. Capacitance-Voltage (*C-V*) measurements were carried out at 1MHz using HP4845 LCR meter. The measured device parameters from these experiments are listed in Table III for HEMTs and MIS-HEMTs.

The AFM micrograph for AlN/AlGaN/GaN heterostructure on silicon (figure not shown) has increased surface roughness probably due to any mismatch arising out of the growth of AlN on silicon. Periodic trenches with pitch in the range of 100-200 nm were observed with increased R_{MS} (1.03 nm) and *P-V* (9.52 nm). However the R_{MS} roughness of the present AlN on silicon is less than one reported for AlN on sapphire (R_{MS} = 1.4 nm) [39] which implies that the morphology of AlN is improved in the present growth. The inclusion of 2 nm *i*-AlN cap layer increases the sheet carrier

density as high as 1.37 x 10^{13} cm^{-2}, with a mobility reduction to 1032 cm^2/Vs. It is the characteristic of semiconductor heterostructures that increase in the sheet carrier concentration is accompanied by a decrease in mobility due to increased interface-roughness scattering.

The two dimensional electron gas (2DEG) carrier concentration ($N_{D\text{-}2DEG}$) *vs* depth profile (see Fig. 2.13) measured using *C-V* also confirms that polarized 2DEG carrier density is increased for AlN/AlGaN/GaN MIS-HEMTs. For an AlGaN/GaN HEMT in the absence of a gate insulator, large amount of surface states are present to trap electrons near the surface which tend to partially deplete the channel and reduce the 2DEG density. But in the case of MIS-HEMT, the number of surface states is greatly reduced leading to high channel carrier density. This is due to an increased polarization effect because of the presence of a highly insulating AlN between the Schottky and AlGaN/GaN 2DEG channel. Though there is an additional 2 nm AlN layer, the 2DEG channel is formed at low depth (20 nm) for the MIS-HEMT than the HEMT (22 nm). This shows that the channel is shifted close to the interface of AlGaN/GaN heterostructure due to increased 2DEG density ($N_{D\text{-}2DEG}$ =1.6 x 10^{20} cm^{-3}). Antoszewksi et al.,[40] have reported that for AlGaN/GaN heterostructures with high n_s, the mobility decreases with increasing n_s due to increased interface roughness scattering as a result of 2DEG shifting towards the AlGaN/GaN interface. Thus we interpret that the increased carrier concentration as the factor which shifts the 2DEG position close towards the AlGaN/GaN interface. The inset of Fig. 2.13 shows schematically

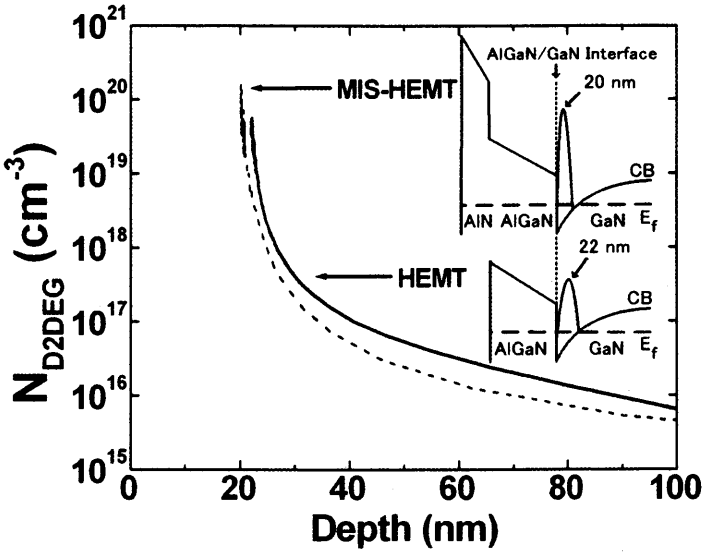


Fig. 2.13. 2DEG carrier concentration vs depth profile from *C-V*. Inset shows the position of 2DEG channel shifted towards the AlGaN/GaN interface for AlN MIS-HEMTs.

the shift of 2DEG position towards the interface. This would also mean that the Schottky-channel separation is shortened.

In general the increase in the sheet carrier concentration (n_s) and the polarized 2DEG carrier density ($N_{D\text{-}2DEG}$) for the AlN/AlGaN/GaN MIS-HEMTs is attributed to (i) reduction of the interface states that usually trap the electrons and (ii) the presence of high band gap AlN cap layer enhancing the potential barrier between the gate and the active layers.

From figure 2.14(a) it is clear there is a decrease in the maximum drain current density ($I_{DS\,max}$) observed for AlN based MIS-HEMTs, irrespective of the increase in the 2DEG density. The reduction in the $I_{DS\,max}$ is believed to be due the poor surface morphology of the 2 nm AlN film grown on silicon. Further the shortening of the gate-channel separation brings the 2DEG channel close to the interface where the interface scattering is dominant resulting in mobility reduction. Therefore we observed a reduced $I_{DS\,max}$ for AlN MIS-HEMTs, but the $I_{DS\,max}$ reported for our device (361 mA/mm) is the highest observed for any AlN cap layered AlGaN/GaN MIS-HEMT on silicon.

The maximum transconductance ($g_{m\,max}$) of the MIS-HEMTs are higher (152 mS/mm) than AlGaN/GaN HEMTs (134 mS/mm) as shown in Fig. 2.14(b). The intrinsic transconductance calculated theoretically using the source resistance (R_S) were 439 mS/mm and 390 mS/mm for MIS-HEMTs and HEMTs respectively. The AlN based MIS-HEMTs also show increased gate voltage swing (-2V to 5V) which is characteristic of a MISFET. Due to the presence of an additional 2 nm AlN layer, there should be an increase in the gate-2DEG channel separation which usually degrades the transconductance as we have reported.[8] However in this case, the maximum transconductance of AlN/AlGaN/GaN MIS-HEMT rather increased despite an increase in total spacer layer thickness. This is because of the shift in the 2DEG position towards the AlGaN/GaN interface for increased carrier concentration profiles [40]. Therefore this shift in the 2DEG position

towards the interface brings the 2DEG electrons close to the Schottky under increased influence of the gate bias ultimately resulting in increased transconductance for AlN based MIS-HEMTs. Though the AlGaN/GaN HEMTs show a maximum drain current density ($I_{DS\,max}$) of 541 mA/mm, the $I_{DS\,max}$ decreases under pulsed bias conditions leading to current collapse. A pulsed bias of 1 μs duration with 50% duty cycle is applied while measuring *I-V* measurements [31]. The AlGaN/GaN HEMTs show severe current collapse when compared to AlN/AlGaN/GaN MIS-HEMTs as it can be seen from Fig. 2.14(c). This is the behavior observed by many [41,42] that significant current collapse exists for AlGaN/GaN HEMTs in the absence of an insulating passivation layer at the Schottky. This indicates that for AlN based MIS-HEMTs, a thin insulating passivation layer of AlN between the source, drain and gate contacts suppresses the effect of surface traps thereby eliminating one of the cause for current collapse.

The two terminal gate leakage measurements in Fig. 2.15(a) show that a thin 2 nm AlN passivation decreases the gate leakage by two orders of magnitude. This indicates that the AlN gate insulator is effective in suppressing not only the gate leakage current but also in enhancing the forward turn-on voltage as shown in Fig. 2.15 (b). Therefore growing a high quality AlN as the ate insulator will suppress the gate leakage to a large extent and possibly shift the device

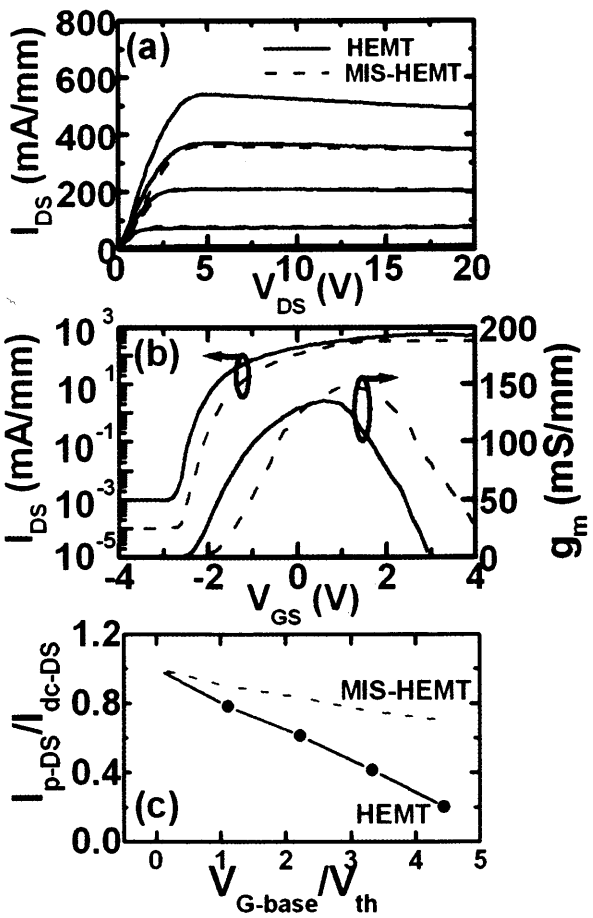


Fig. 2.14. (a) dc I_{DS}-V_{DS} measurements with V_g = +1.5V and ΔV_g = -1V; (b) I_{DS} and g_m characteristics; (c) pulse current normalized to the dc ($I_{dc\text{-}DS}$) at zero gate bias vs gate gate voltage ($V_{G\text{-}base}$) normalized to threshold voltage.

threshold voltage to 0 V and achieve a normally off type operation. The gate leakage reduction due to the presence of thin AlN insulator is accompanied by a high breakdown voltage (*BV*). The *BV* measurements done on 200 μm HEMTs with identical gate-drain spacing (L_{gd}) are shown in the inset of Fig. 2.15 (a). The AlN based MIS-HEMTs show breakdown over 230 V which is larger than the breakdown of AlGaN/GaN HEMTs. Thus in general any suppression of the gate leakage by inserting an insulator at the Schottky of the AlGaN/GaN HEMTs will improve the device breakdown as reported in literature [8].

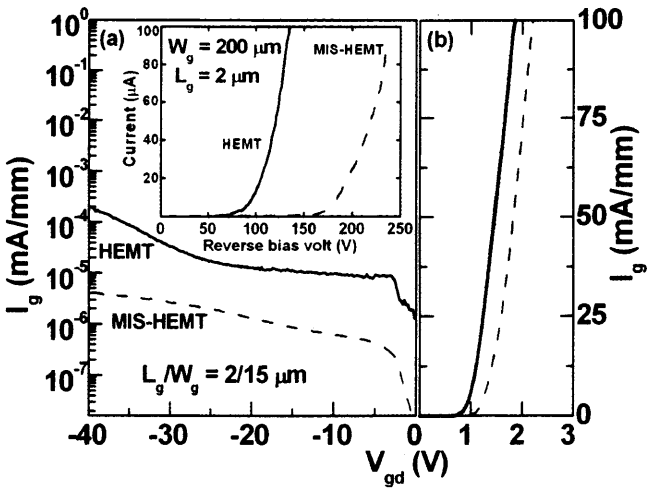


Fig. 2.15. (a) Two terminal gate leakage *I-V* measurements; Inset: Reverse breakdown measurements; (b) Forward I_g-V_{gd} characteristics.

References:

[1]. T. Kikkawa, Jpn. J. Appl. Phys. **44** (2005) 4896.

[2]. S. Arulkumaran, M. Miyoshi, T. Egawa, H. Ishikawa and T. Jimbo, IEEE Electron Device Lett. **24** (2003) 497.

[3]. B. Zhang, T. Egawa, H. Ishikawa, Y. Liu and Takashi Jimbo, Appl. Phys. Lett. **86** (2005) 071113.

[4]. T. Nanjo, T. Oishi, M. Suita, Y. Abe and Y. Tokuda, Appl. Phys. Lett. **88** (2006) 043503.

[5]. P. Samanta and M. Chan, J. Appl. Phys. **96** (2004) 1547.

[6]. T. Hashizume, S. Anantathanasarn, N. Negoro, E. Sano, H. Hasegawa, K. Kumakura and T. Makimoto, Jpn. J. Appl. Phys. **43** (2004) L777.

[7]. S. Arulkumaran T. Egawa, S. Matsui and H. Ishikawa, Appl. Phys. Lett. **86** (2005) 123503.

[8]. S. Arulkumaran, T. Egawa and H. Ishikawa, Solid State Electron., 49 (2005) 1632.

[9]. S. Arulkumaran, T. Egawa, L. Selvaraj and H. Ishikawa, Jpn. J. Appl. Phys. **45** (2006) L220.

[10]. M. Higashiwaki and T. Matsui, Jpn. J. Appl. Phys. **43** (2004) L1147.

[11]. P. Kordos, G. Heidelberger, J. Bernat, A. Fox, M. Marso and H. Luth, Appl. Phys. Lett. **87** (2005) 143501.

[12]. T. Ide, M. Shimizu, A. Suzuki, X. Shen, H. Okumura and T. Nemoto, Jpn. J. Appl. Phys. **40** (2001) 4785.

[13]. Y. Liu, H. Jiang, S. Arulkumaran, T. Egawa, B. Zhang and H. Ishikawa, Appl. Phys. Lett. **86** (2005) 223510.

[14]. S. Arulkumaran, T. Egawa and H. Ishikawa, Jpn. J. Appl. Phys. **25** (2005) L812.

[15]. P.D.Ye, B.Yang, K.K.Ng and J.Bude, Appl. Phys. Lett. **86** (2005) 063501.

[16]. H.W.Jang, J.M.Baik, M. Lee, H.Shin and J.Lee, J. Electrochem. Soc. **151** (2004) G536.

[17]. H.N. Alshareef, H.F. Luan, K. Choi, H.R. Harris, H.C. Wen, M.A. Quevedo-Lopez, P. Mahji and B.H. Lee, Appl. Phys. Lett. **88** (2006) 112114.

[18]. T. Hashizume, J.Kotani, A.Basile and M.Kaneko, Jpn. J. Appl. Phys. **45** (2006) L111.

[19]. S. L. Selvaraj, T. Ito, Y. Terada and T. Egawa, *Appl. Phys. Lett.*, **90**, (2007) 173506.

[20]. T. Hashizume, S. Anantathanasarn, N. Negoro, E. Sano, H. Hasegawa, K. Kumakura and T. Makimoto, *Jpn. J. Appl. Phys.*, **43** (2004) L777.

[21]. W. D. Hu, X. S. Chen, Z. J. Quan, C. S. Xia, W. Lu and P. D. Ye, *J. Appl. Phys.* **100** (2006) 074501.

[22]. C. Wang, N. Maeda, M. Kiroki, H. Yokoyama, N. Watanabe, T. Makimoto, T. Enoki and T. Kobayashi, *Jpn. J. Appl. Phys.*, **45** (2006) 40.

[23]. S. Guha, E. Cartier, N. A. Bojarczuk, J. Bruley, L. Gignac and J. Karasinski, *J. Appl. Phys.*, **90** (2001) 512.

[24]. D. H. Kim, V. Kumar, G. Chen, A. M. Dabiran, A. M. Wowchak, A. Osinsky and I. Adesida, *Electron. Lett.*, **43** (2007) 127.

[25]. P. D.Ye, G. D. Wilk, B. Yang, J. Kwo, H. J. L. Gossmann, M. Hong, K. K. Ng and J. Bude, *Appl. Phys. Lett.*, **84** (2004) 434.

[26]. S. Steinberg, W. Ducer, G. Vigil, C. Hyukjin, C. Frank, M. Z. Tseng, D. R. Clarke, J. N. Israelachvili, *Science* **260** (1993) 656.

[27]. Y. Ishihara, N. Itou, T. Kimijima and T. Hirano, *J. Vac. Sci. Technol.*, **A 17** (1999) 3139.

[28]. A. E. T. Kuiper. M. F. Gillies, V. Kottler and G. W. Hooft, *J. Appl. Phys.*, **89** (2001) 1965.

[29]. P. Kordos, D. Gregusova, R. Stoklas, S. Gazi and J. Novak, *Sol. St. Electron.*, 52 (2008) 973.

[30]. P. Kordos, D. Gregusova, R. Stoklas, K. Cico and J. Novak, *Appl. Phys. Lett.*, 90 (2007) 12352.

[31]. S. L. Selvaraj and T. Egawa: *Appl. Phys. Lett.*, **89** (2006) 193508.

[32]. T. Hashizume, J. Kotani, A. Basile and M. Kaneko, *Jpn. J. Appl. Phys.*, Part 2 **45** (2006) L111.

[33]. D. K. Schroder, *Semiconductor materials and device characterization,* 2nd edition, IEEE Press, Wiley-Interscience: (2006) p. 72.

[34]. J. R. Kotani, T. Hashizume and H. Hasegawa, *J. Vac. Sci. Technol.*, B **22** (2004) 2179.

[35]. S. Strite and H. Morkoc, Critical Review, J. Vac. Sci. Technol. **B 14** (1992) 1237.

[36]. E. Alekseev, A. Eisenbach and D. Pavlidis, Electron. Letts. **35** (1999) 2145.

[37]. M. Higashiwaki, T. Mimura and T. Matsui, IEEE. Electron. Dev. Letts. **27** (2006) 719.
[38]. T. Hashizume, E. Alekseev, D. Pavlidis, K. S. Boutros and J. Redwing, J. Appl. Phys. **88** (2000) 1983.
[39]. K. Kawaguchi and A. Kuramata, Jpn. J. Appl. Phys. **44** (2005) L 1400.
[40]. J. Antoszewski, M. Gracey, J. M. Dell, L. Faraone, T. A. Fisher, G. Parish, Y. F. Wu and U. K. Mishra, J. Appl. Phys. **87** (2000) 3900.
[41]. S. Arulkumaran, T. Hibino, T. Egawa and H. Ishikawa, Appl. Phys. Lett. **85** (2004) 5745.
[42]. H. Hasegawa, T. Inagaki, S. Ootomo and T. Hashizume, J. Vac. Sci. Technol. **B 21** (2003) 1844.

Chapter 3

Breakdown Studies on AlGaN/GaN HEMTs on Si

High breakdown field of GaN ($E_c \approx 3$ MV/cm) which is approximately 3 times greater than Si or GaAs makes it attractive for high power device applications. AlGaN/GaN high electron mobility transistors (HEMT) have a high *figure of merit* (FOM) BV^2/ R_{on}, [1] owing to much lower on-state resistance (R_{on}) and higher breakdown volt (BV) because of higher sheet carrier density, n_s in the two dimensional electron gas. The substrates widely used for AlGaN/GaN HEMTs are SiC, sapphire and silicon. Among these, Si is emerging as the most suitable choice for commercialization due its low cost and large size availability. Though higher lattice and thermal mismatches of Si generates a large number of dislocation and cracks, AlGaN/GaN HEMT devices on Si have shown attractive device performance for high-power applications.

Several device improvements have been developed to achieve a high BV AlGaN/GaN HEMTs. These include a field plate inclusion at gate and increase in gate-drain length (L_{gd}). Experimental results for standard HEMT structures show a large electric field peak at the drain side edge of the gate electrode. This peak field leads to premature breakdown of the device and can be reduced by using a field plate technology. A high breakdown of 1900 V was achieved using a slant field plate [2]. In the case of increased L_{gd} the increase in BV was accompanied by drain current (I_{Dmax}) degradation. A record high breakdown of 1580 V was obtained for devices with large L_{gd} of 16 μm, however with a decreased I_{Dmax} [3]. In all these approaches though a high BV was achieved; they are accompanied by their own demerits.

Therefore, it is our objective to attempt for BV enhancement without using a field plate or large L_{gd} distance. This was investigated by improving the quality of GaN growth and strengthening the buffer. The breakdown mechanism is also affected by excess leakage through i-GaN due to

imperfections and dislocation density (D_D) in growth. As these D_D are high for GaN on Si due to large lattice mismatch, it is necessary to decrease the D_D by improving the buffer between GaN and Si. Further the buffer layer and the Si junction should be strong enough to enhance the breakdown [4].

3.1. MOCVD growth of thick AlGaN/GaN HEMTs

In this section, the growth of crack free thick AlGaN/GaN HEMT epi-layer up to a total thickness (T_{Tot}) of 9 μm using 2 μm i-GaN and 7 μm super lattice structured (SLS) buffer on silicon and its breakdown property will be discussed . Our SLS buffer scheme consists multi pairs of GaN / AlN (20 / 5 nm). *BV* measurements carried on HEMTs fabricated from these epi-layer showed an enhancement in *BV* as the total thickness of the epi-layer is increased. The dependence of *BV* with regard to GaN thickness (T_{GaN}) and buffer layer thickness (T_{Buf}) are studied and their limitations are presented.

Figure 3.1 shows the photograph of crack free 9 μm T_{Tot} grown epi-layer on 4 inch silicon wafer. All the HEMT structures reported here were grown on 4 inch p-silicon substrate (resistivity of 1-3 Ω cm) by metal-organic chemical vapor deposition (MOCVD). The epi-layer includes nucleation layers of 100 nm i-AlN / 40 nm i-$Al_{0.3}Ga_{0.7}N$ common for all the hetero-structures. Then in order to understand the role and influence of buffer on device breakdown, multi pairs of GaN/AlN (20/5 nm) buffers varying from thickness 0.5 to 8.0 μm were grown. Here it should be noted that increasing the T_{Buf} facilitated the growth of thick GaN (beyond 1 μm) on Si. For buffers exceeding T_{Buf} of 5 μm, growth of thick GaN upto 2 μm thickness was possible. Thus we could achieve a crack free

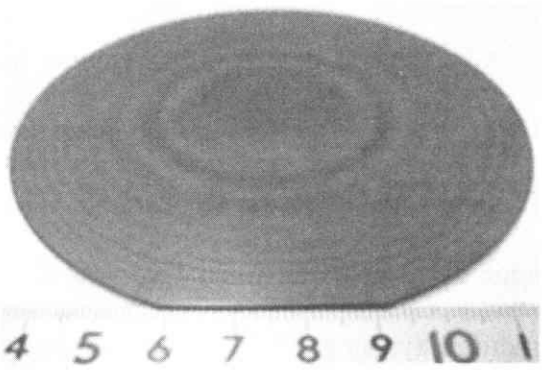


Fig. 3.1. Photograph of the 4 inch wafer with 9 μm total thick epi-layer including a 7 μm buffer and 2 μm i-GaN on silicon.

epi-layers up to a total thickness of 9 μm. The bowing of the grown wafers increased with T_{Tot} and was 80 μm for 9 μm T_{Tot}. For wafers with a T_{Tot} of 10 μm (2 μm GaN / 8 μm buffer), cracks were found up to 15-20 mm from the edge of the wafer.

The quality of the MOCVD grown GaN was studied by calculating the screw component ($D_{D\text{-}Screw}$) and edge component ($D_{D\text{-}Edge}$) dislocation density from full width at half maximum (FWHM) peaks of x-ray diffraction [5,6] measured using Philips X'Pert in the directions (0004) and (10-10) respectively. Fig. 3.2(a) showed a decrease in the $D_{D\text{-}Screw}$ as the total thickness increased. Further from Fig. 3.2(b) it is understood that for same growth conditions, GaN grown by us throughout maintained a decrease in the $D_{D\text{-}Screw}$ with increased T_{GaN}. Appropriate thick buffers up to 320 pairs of SLS were used in order to keep the $D_{D\text{-}Screw}$ below 2.0 x 10^9 cm^{-2}. For GaN grown on buffers exceeding 200 pairs, the $D_{D\text{-}Screw}$ is well below 1x10^9 cm^{-2}. This illustrates that the quality of GaN grown is gradually improved upon growing over thick buffer. Hence we understand that thick buffer layers tend to minimize the lattice mismatch between GaN and Si so as to grow a GaN of increased thickness and with less D_D. Also the $D_{D\text{-}Edge}$ measured from FWHM (10-10) peaks for GaN up to 1.5 μm shows a decrease in $D_{D\text{-}Edge}$ with an increase in T_{Tot} and T_{GaN} as shown in figures 3.2(c) and 3.2(d) respectively.

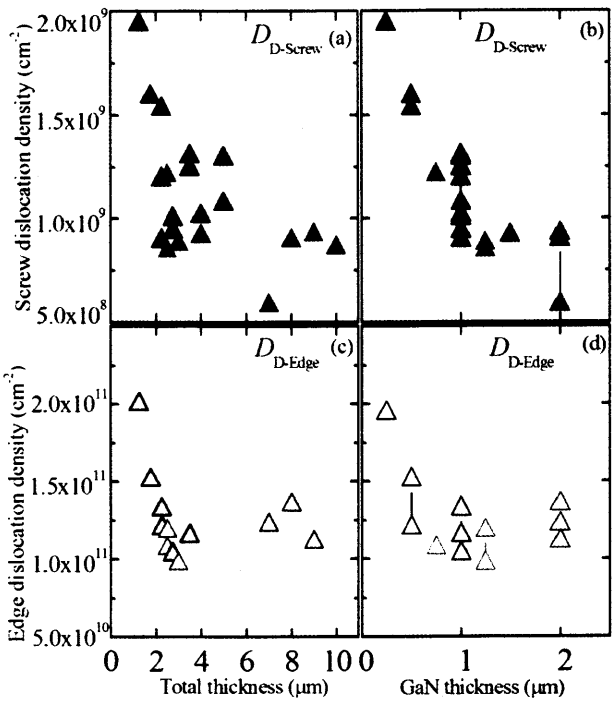


Fig. 3.2. Screw dislocation measured as a function of (a) total thickness and (b) GaN thickness; Edge dislocation measured as a function of (c) total thickness and (d) GaN thickness

Van der-Pauw Hall measurements on all these samples showed a sheet carrier concentration of 1.1x10^{13} cm^{-2} and Hall mobility above 1100 cm^2/Vs. The grown samples were cut

15 x 15 mm for HEMT device fabrication as per the process details in our previous report [7]. All the devices were passivated with 100 nm electron beam evaporated SiO_2 and the dimensions of the devices are W_g / L_g = 15 μm / 1.5 μm. Excellent *DC* characteristics, including a complete pinch-off (at -2.2 V) were observed for our HEMTs with I_{Dmax} of 625 mA/mm and transconductance (g_{mmax}) of 190 mS/mm.

Three terminal off-*BV* measurements were carried out using Sony Tektronix 370A curve tracer. The samples were immersed in an inert liquid Fluorinert (FC-40) to avoid any atmosphere influence at the gate-drain area while *BV* measurement. The gate bias was maintained at a sub-threshold voltage of -5.0 V with Si substrate grounded. Our *BV* is defined as the drain-source voltage at which a drain current of 1 mA/mm was observed. L_{gd} which is very important for the breakdown phenomenon was 3 μm for all devices tested for *BV* as our primary aim is to enhance the *BV* without increasing the L_{gd}. Figure 3.3(a) shows the breakdown of HEMTs for T_{GaN} of 1 μm increasing with an increase in T_{Tot} from 1.5 – 3.5 μm (i.e., T_{Buf} from 0.5-2.5 μm). Thus a HEMT with a *BV* of 110 V for 1 μm thick GaN can increase to a *BV* of 210 V if the buffer is strengthened by increasing its thickness. This increased T_{Buf} offers a GaN with less D_D, low leakage through GaN thereby improving the *BV*. This is found true for other devices with GaN thickness of 1.5 μm and 2.0 μm yielding the highest *BV* of 403 V for a heterostrucure of 9 μm total thickness without

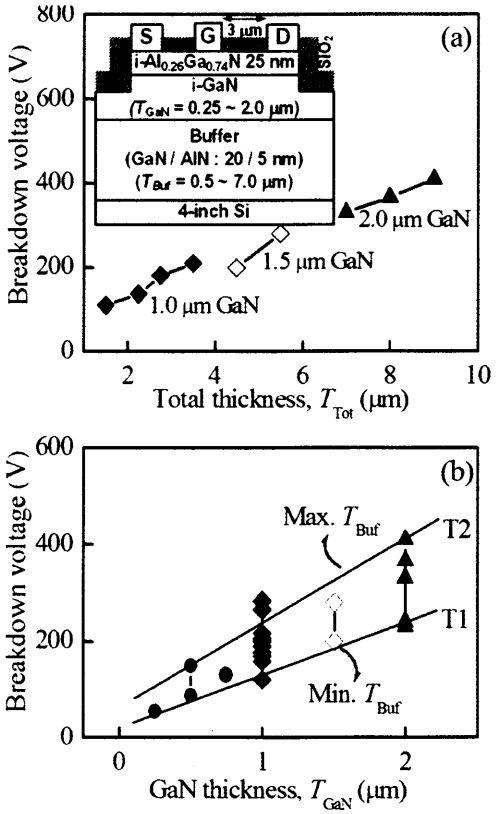


Fig. 3.3. (a) *BV* obtained for HEMTs as a function of buffer thickness; Inset shows the device used for measuring 3 terminal off-breakdown ($L_g/W_g/L_{gd}$ = 1.5/15/3 μm) with 2DEG channel at the AlGaN/GaN interface (b) *BV* of HEMTs as a function of GaN thickness

using field plate. In Fig. 3.3(b), the *BV* of the devices were summarized with increase in T_{GaN}. More than one *BV* plots for a particular T_{GaN} (0.5, 1.0, 1.5 and 2.0 μm) are the breakdown values for devices in which GaN is grown on increased T_{Buf}. Though the *BV* of GaN HEMTs increase with increase in GaN thickness, however to push the breakdown of GaN beyond the limits achieved so far, it is necessary to strengthen the buffer by increasing the T_{Buf}, which would increase the resistance of the i-GaN epi-layer [8]. In Fig. 3b, the trend line T1 represents the lowest breakdown achieved in this study for every thickness of GaN. This T1 refers to breakdown of the GaN HEMTs with a dependence on T_{GaN} which is a well known fact until now. However, by increasing the T_{Buf} for GaN of same thickness, the breakdown is improved upon to the trend line T2. Thus T2 line refers to the T_{Buf} dependence on breakdown of GaN HEMTs. This illustrates that, increasing the total thickness of the epi-layers is important for improving the breakdown of AlGaN/GaN HEMTs.

For devices exceeding a *BV* of 300 V they undergo premature breakdown which is due to high field developed in the short L_{gd} of 3 μm. Burn marks were found on these devices at the gate-drain region. Thus for a low L_{gd} (≤ 3μm), there is an upper limit in achieving a high breakdown by increasing the T_{Buf}. Our breakdown volt of 403 V achieved for 2 μm GaN/7 μm buffer is the highest for any AlGaN/GaN HEMT on silicon substrate reported for a short L_{gd} spacing of 3 μm without using a field plate structure or gate insulator.

In order to study the *BV* across i-GaN, we measured the *BV* between two isolation pattern (10 μm gap) available in the same HEMT mask as shown in Fig. 3.4. When the

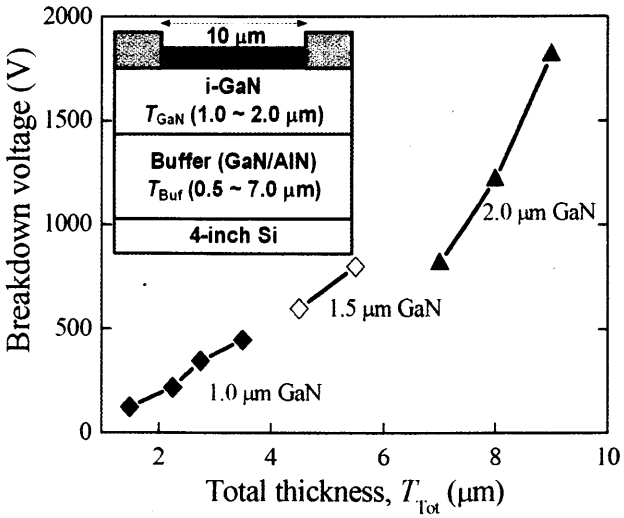


Fig. 3.4. *BV* of i-GaN across 10 μm gap ohmic contacts after etch removing the AlGaN; Inset: Pattern used for measuring the *BV* of i-GaN.

voltage approaches breakdown, the leakage current increases rapidly and is therefore destructive for the device. Thus in this measurement across i-GaN, *BV* refers to voltage at which the device fails catastrophically. A steady increase in the *BV* with T_{Buf} with a high *BV* of 1813 V was achieved using 9 μm thick epi-layer. Our results (1813 *BV* at 10 μm gap) are better compared to Ikeda et al [9] reporting a *BV* of 1.8 kV for i-GaN measured at an isolation of large 30 μm gap. Hence our effort to grow a GaN on thick buffer improved the GaN quality in addition to strengthening the buffer for *BV* enhancement.

3.2. Study of Various Leakage Currents

The successfully grown crack free 9 μm T_{tot} epi-layer is shown in Fig.3.5(a). Excellent device properties including an I_{Dmax} of 625 mA/mm and g_{mmax} of 190 mS/mm were observed (Fig. 3.5 (b)) along with a *3TBV* of 403 V measured using Sony Tektronix curve tracer 370A (Fig. 3.5(c)). Here it is noted that *3TBV* of HEMTs improved with an increase of T_{buf}.

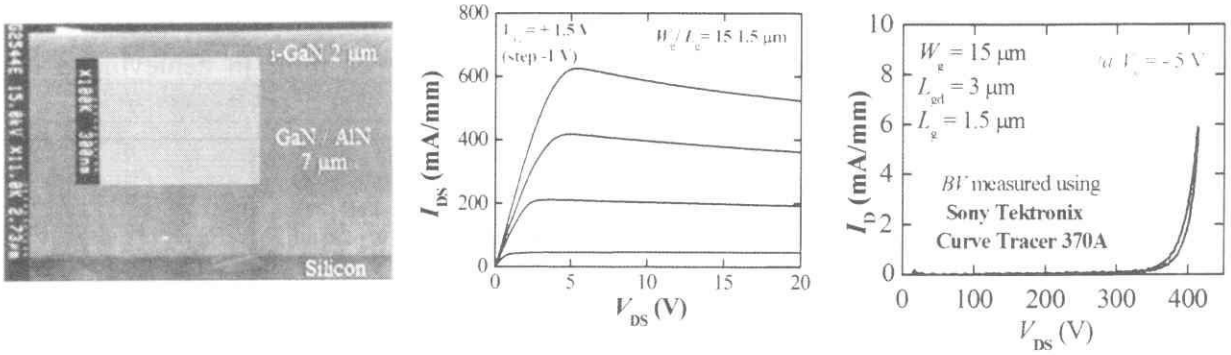


Fig. 3.5 (a) SEM image of the successfully grown 9 μm thick AlGaN/GaN HEMT; Inset shows the GaN/AlN SLS multilayers; 3.5(b) Good pinch-off characteristics of the HEMT and 3.5(c) Breakdown measurements using Sony-Tektronix curve tracer.

Due to curve tracer limitations, it is difficult to understand the path of leakage influencing the breakdown. Hence for selected devices, we carried out the breakdown measurements using Keithley pico-ammeters interfaced with a probe station as in Fig. 3.6. At a negative gate bias since the channel is closed, buffer and substrate are the paths available for leakage current. Keeping V_g @ -5 V, when V_{DS} is increased, the leakage currents I_{buf} and I_{sub} were low compared to the gate leakage

(I_{gate}). For an AlGaN/GaN on T_{buf} = 1.25 μm, when V_{DS} exceeds 100V, I_{buf} and I_{sub} began to increase, finally undergoing a destructive breakdown at 130 V. Thus we find that for T_{buf} of 1.25μm, suppressing the I_{sub} leak could not be extended to higher V_{DS} beyond 100 V. For the same 1.0 μm i-GaN thickness on a T_{buf} of 4.0 μm, the suppression of I_{sub} and I_{buf} could be extended, however the device undergoes a premature breakdown because of the gate-drain region failing at 282 V (Fig. 3.7(b)). At 282 V_{DS}, we call this as a premature breakdown because of high field developed at the gate drain region giving rise to an extremely high I_{gate}. The less defective GaN and the increased resistance between the surface electrode and the silicon substrate reduced the leakage to enhance the breakdown [2] in-spite of small L_{gd}.

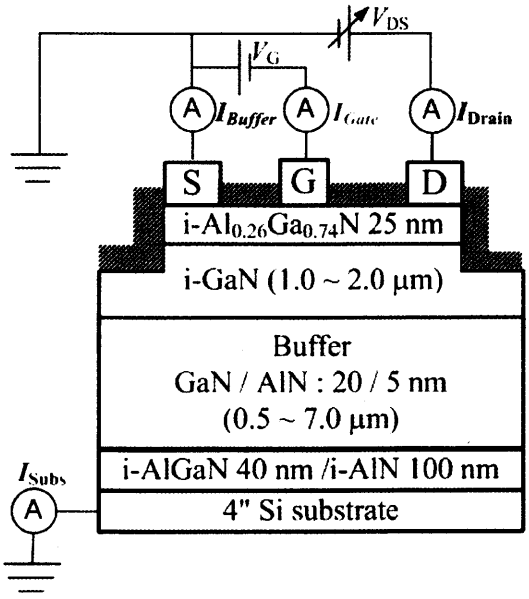


Fig. 3.6. HEMT structures grown and the experimental setup used to study various leakage mechanism.

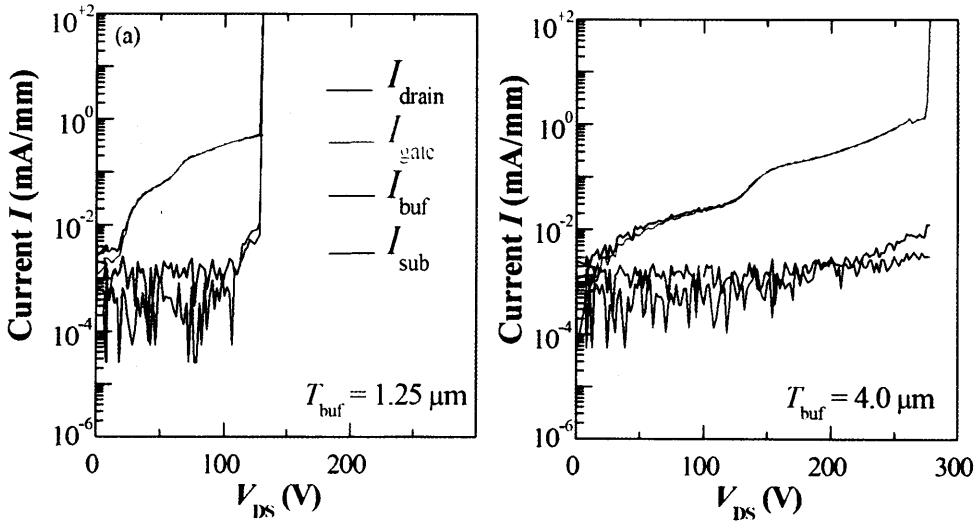


Fig. 3.7 (a&b). Three terminal breakdown shows that by increasing the buffer thickness I_{sub} and I_{buf} currents are reduced very much.

To investigate the insulating nature of our i-GaN grown on various thick buffers, the top 100 nm including the AlGaN was etch removed thereby eliminating the 2DEG channel. Fig. 8

summarizes the breakdown of i-GaN across 10 μm ohmic electrode increasing with the T_{buf}. The i-GaN grown on 1.25 μm buffer thickness reaches the breakdown limit at 144 V (Fig. 3.8(a)) due to high I_{sub} and I_{buf}. When the thickness of buffer is increased to 4.0 μm, the breakdown increases to 722 V (Fig. 3.8(b)) because of the improved i-GaN growth resulting in high resistivity. Our highest breakdown of 1813 V was observed for 2 μm i-GaN on 7μm T_{buf}. This is higher than previously reported breakdown across a large Ohmic gap of 30 μm [3].

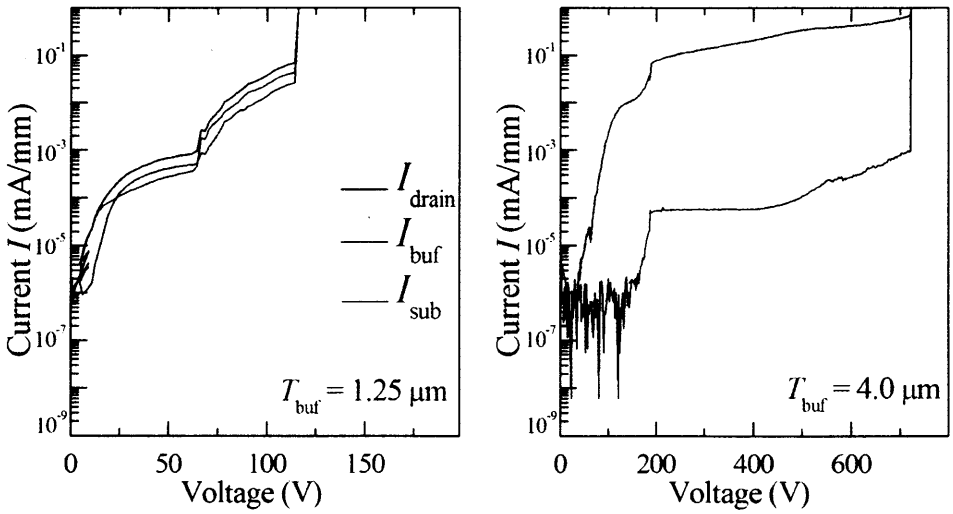


Fig. 3.8 (a&b). Breakdown measurements across 10 μm *Ohmic* contact on i-GaN grown on two different buffer thickness namely 1.25 μm and 4.0 μm.

For i-GaN on 1.25 μm buffer the breakdown across i-GaN (144 V) and *3TBV* (130 V) are similar as in both cases the possible limit to suppress the leakage is reached. But on the other hand for i-GaN on 4.0 μm buffer, there is a large difference as *3TBV* (282 V) obtained is very low compared to *BV* across i-GaN (722). This illustrates that by making a considerable increase in L_{gd}, a 1 μm GaN on 4 μm buffer could very well offer the *BV* beyond 700 V. It is therefore concluded that growing GaN HEMTs on thick buffer improves the quality of epi-layers and offers a high resistance between surface and substrate yielding a high breakdown.

3.3. In-situ MOCVD grown 2 nm i-GaN cap

For HEMTs grown on thin buffer, as V_{DS} increased there is a sudden increase in the leakage current observed as shown in Fig. 3.9(a). This we call a "*two step breakdown*" is due to large dislocations driven low resistive i-GaN buffer. To achieve a truly insulating i-GaN, different approaches were demonstrated like carbon doping [10] and Fe doping [11]. This doping compensation creates deep-level acceptors in the buffer which causes device instability especially at high drain voltages [12]. Therefore our approach is based on growing high resistive i-GaN with less dislocations made possible by using a thick buffer. The BV_{OFF} measured for the HEMT grown on thick buffer is shown in Fig. 3.9(b) in which the two-step breakdown was not observed. Thus same hetero-structure when grown on thick buffer offers a good improvement in the breakdown.

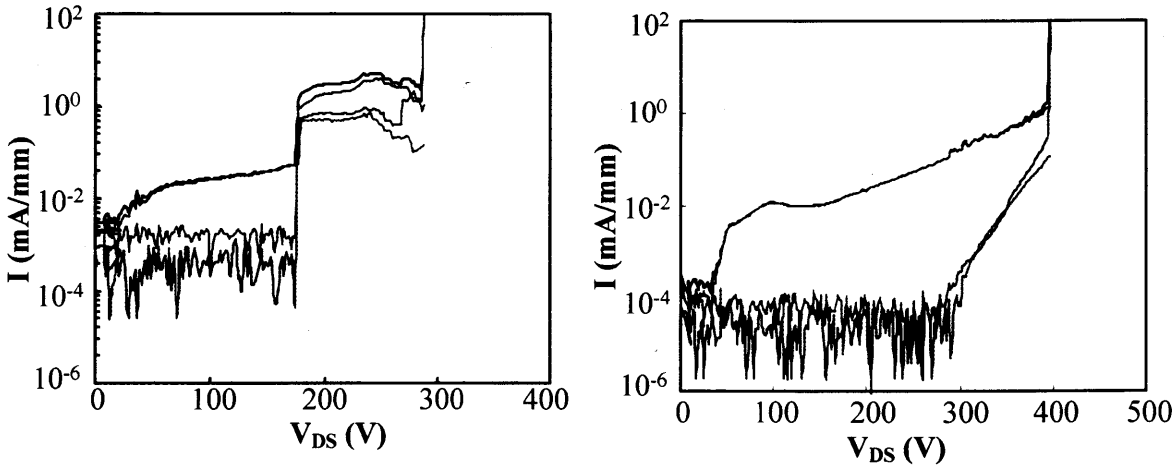


Fig. 3.9 (a) Two step breakdown observed for a HEMT grown on Si using thin buffer; (b) HEMT grown using thick buffer offers a high resistive GaN which eliminates the two-step breakdown.

As our devices have the Schottky contact at the gate terminal, the I_g is high and dominant when compared to I_{sub} and I_{buf}. An insulating layer at the gate is the solution for reducing the I_g which in turn improves the breakdown [13]. As the Nitride semiconductors lack a native oxide, the use of ex-situ grown insulators like SiO_2, Al_2O_3 etc., leads to large interface density of affecting

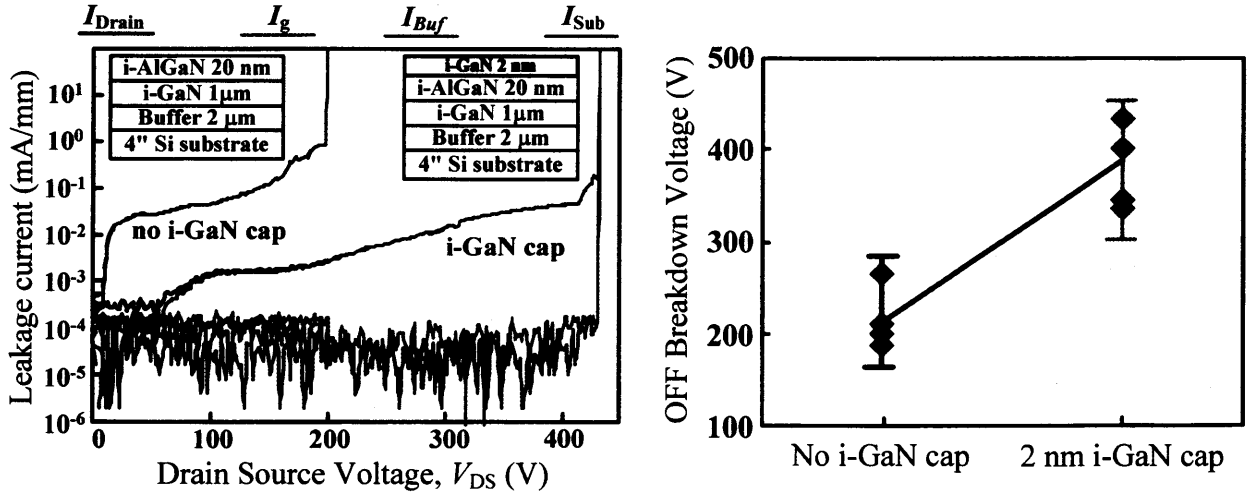


Fig. 3.10.(a) *BV* of i-GaN across 10 μm gap ohmic contacts after etch removing the AlGaN; Inset: Pattern used for measuring the *BV* of i-GaN; (b) Average breakdown observed for HEMTs with and without 2 nm i-GaN caplayer.

the device performance. Therefore, to grow a in-situ i-GaN of 2 nm thin layer on top of the AlGaN which certainly lowers the I_g. The breakdown for devices with 2 nm i-GaN has considerably low I_g which extends the drain bias application to higher voltage as shown in Fig. 3.10. A high breakdown of 432 V was achieved for i-GaN capped AlGaN/GaN HEMTs. AlGaN/GaN HEMTs with a combination of thick buffer and i-GaN cap layer enhances the BV_{OFF} as they contribute to lowering the leakage currents through buffer, substrate and gate respectively. Further, the in-situ grown i-GaN cap layer does not create any interface defect states as observed by other ex-situ grown insulators.

In Fig.3.11, a comparison between the BV_{OFF} and breakdown i-GaN measured across 10 μm ohmic contact were presented. Thus the BV_{OFF} of 2 μm thick HEMT with and without 2 nm i-GaN caplayer fits very well with the measured experimental breakdown values. For i-GaN on 1.25 μm buffer the breakdown across i-GaN (144 V) and *3TBV* (130 V) are nearly similar as in both cases the possible limit to suppress the buffer and substrate leakage is reached. But on the other hand for i-GaN on 4.0 μm buffer, there is a large difference as *3TBV* (282 V) obtained is very low compared to *BV* across i-GaN (722). This shows that there is still a possibility to increase the

BV_{OFF} by controlling the dominant gate leakage currents or by making a small increase in L_{gd}. It is therefore concluded that growing GaN HEMTs on thick buffer improves the quality of epi-layers and offers a high resistance between surface and substrate yielding a high breakdown.

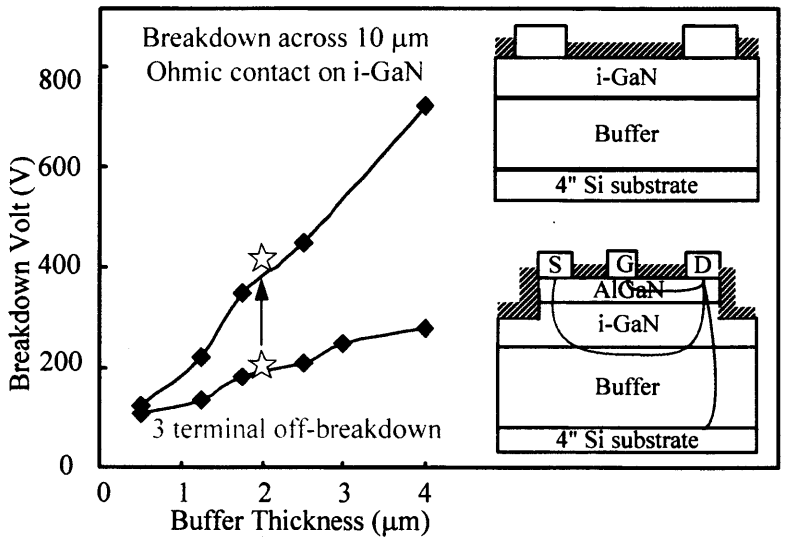


Fig. 3.11. Comparison of 3-terminal off-breakdown observed and the corresponding breakdown across 10 μm Ohmic contact on i-GaN.

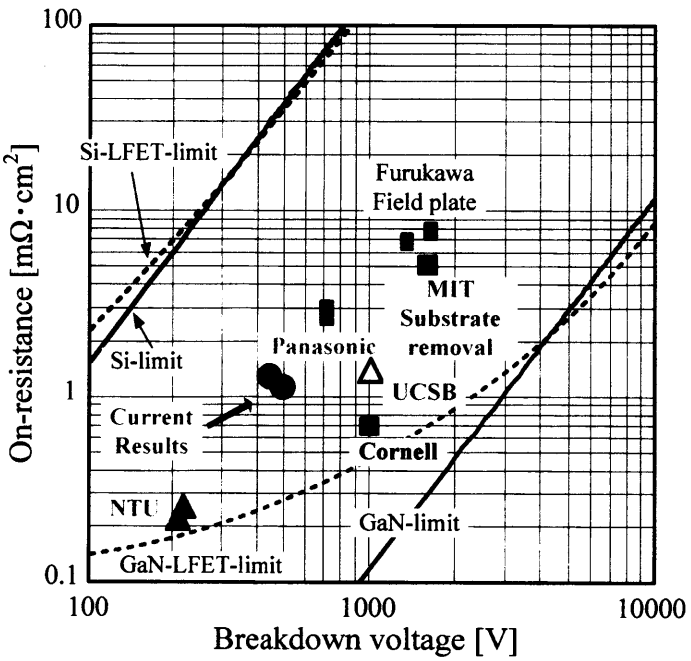


Fig. 3.12. *Specific-ON resistance vs* breakdown of our devices compared with other literature reports on AlGaN/GaN HEMTs.

The R_{ON} of our devices vs breakdown voltage is shown in Fig. 3.12 and it is compared with

other leading groups working on the breakdown of AlGaN/GaN HEMTs. Thus for our MOCVD grown AlGaN/GaN HEMTs on thick buffer, we observed a high figure-of-merit (BV^2/R_{ON}) of 5.4 x 10^8 $V^2\Omega^{-1}cm^{-2}$.

References

[1]. N. Tipirneni, A. Koudymov, V. Adivarahan, J. Yang, G. Simin, and M. A. Khan, *IEEE Electron Device Lett.*, **27** (2006) 716.

[2]. Y. Dora, A. Chakraborty, l. McCarthy, S. Keller, S. P. DenBaars, and U. K. Mishra, *IEEE Electron Device Lett.*, **27** (2006) 713.

[3]. J. Shi, Y. C. Choi, M. Pophristic, M. G. Spencer, and L. F. Eastman, *Phys. Stat. Solidi (c,)* **5** (2008) 2013.

[4]. S. Arulkumaran, T. Egawa, S. Matsui, and H. Ishikawa, *Appl. Phys. Letts.*, **86** (2005) 123503.

[5]. R. Chierchia, T. Bottcher, H. Heinke, S. Einfeldt, S. Figge and D. Hommel, *J. App. Phys.*, vol. **93** (2003) 8918.

[6]. T. Metzger, R. Hopler, E. Born, O. Ambacher, M. Stutzmann, R. Stommer, M. Schuster, H. Gobel, S. Christiansen, M. Albrecht and H. P. Strunk, *Philosophical Magazine* A, 77 (1998) 1013.

[7]. S. L. Selvaraj, and T. Egawa, *Appl. Phys. Lett.* vol **89** (2006) 193508.

[8]. S. Iwakami, O. Machida, M. Yanagihara, T. Ehara, N. Kaneko, H. Goto and A. Iwabuchi, *Jpn J. Appl. Phys.* vol. **24**, no. 24, pp. L587-589, 2007.

[9]. N. Ikeda, S. Kaya, J. Li, Y. Sato, S. Kato, and S. Yoshida, *Proc. of 20th Int. Symp. on power Semiconductor Devices and IC's,* (2008) 287.

[10]. J. B. Webb, H. Tang, S. Rolfe, and J. A. Bardwell, *Appl. Phys. Lett.,* **75** (1999) 953.

[11]. Y. C. Choi, M. Pophristic, H. Y. Cha, B. Peres, M. G. Spencer, and L. F. Eastman, *IEEE Trans.Electron Devices,* **53** (2006) 2926.

[12]. M. Wang, and K. J. Chen, *IEEE Trans. Electron Devices,* **58** (2011) 460.

[13]. S. L. Selvaraj and T. Egawa, Appl. Phys. Lett. **90** (2007) 173506.

Chapter 4

Challenges before GaN on Si

The growth of AlGaN/GaN high-electron-mobility transistors (HEMTs) on silicon substrate is attractive because of its low cost and large size availability. However the growth on silicon is hampered by large lattice mismatch and a difference in thermal expansion coefficients between GaN and silicon. In order to obtain high-crystalline quality of GaN on silicon, buffer layers are essential to reduce the dislocation density and improve the GaN crystal quality. Buffer layers with various thicknesses were grown which improved the breakdown of the AlGaN/GaN HEMTs [1]. Increasing the buffer thickness greatly improved the quality of i-GaN with reduced dislocation density [2]. Both screw and edge dislocation components of i-GaN decrease as they were grown on increased buffer thickness.

An important issue before the growth of AlGaN/GaN hetero-structures is appearance of pits on surface of the growth completed wafer. The nature of these deep pits and their impact on the device properties needs further investigation as they are detrimental to device performance. Earlier, the formation of deep pits and their relation to edge dislocation density were reported,[3] but no report is available regarding the deep pits and their influence on the device properties. It is the objective of this letter to highlight how the AlGaN/GaN hetero-structures with deep pits will affect the device breakdown. We have made an analysis on the three terminal off-breakdown of HEMTs by measuring the leakage currents through gate, buffer and substrate. This report helps to understand not only the defects of HEMT epi-layers with deep pits, but also highlights the need to grow a completely pit free epi-layers for high power device applications.

Figure 4.1 shows the hetero-structure of AlGaN/GaN HEMTs on silicon grown by Taiyo-Nippon Sanso (SR4000) horizontal metalorganic chemical vapour deposition (MOCVD)

system. The HEMTs were grown on super-lattice structured buffer of a thickness of 1.25 μm. Even with same buffer scheme and total epi-layer thickness, pits with various densities were observed for different wafers grown in our center. The observed pits are of two kinds by size namely shallow and deep. Shallow pits are quite normal and cannot be observed by an ordinary microscope. These shallow pits can be viewed only through atomic force microscopy (AFM) as shown in Fig. 4.2(a). On the other hand, deep pits of hexagonal pyramid shape are bigger in size and are easily visible even through a regular microscope as it can be seen from the Nomarski microscopic image in Fig. 4.2(b). The hexagonal pyramid shaped pits which reflect crystal symmetry of GaN were observed after growth without any etching treatment. Therefore these pits observed are different from etch pits in which the semiconductor surface is intentionally treated with an etchant to view the pits underneath the top layer.

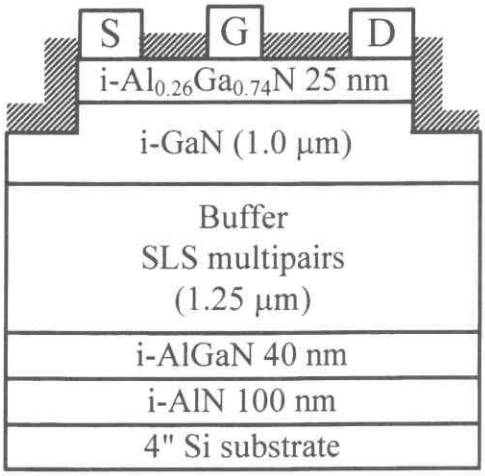


Fig.4.1. AlGaN/GaN HEMT structures grown by MOCVD

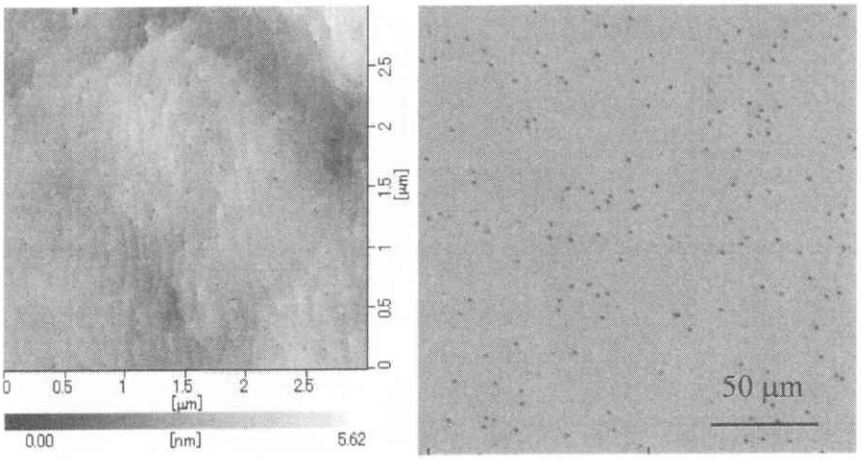


Fig. 4.2. (a) AFM image of shallow pits (b) Normal microscopic image of deep pits.

The deep pits of hexagonal/polygonal pyramid shape (Fig. 4.3), bigger in size and are easily visible even through a regular microscope. The hexagonal pyramid shaped pits which reflect crystal symmetry of GaN were observed after growth without any etching treatment.

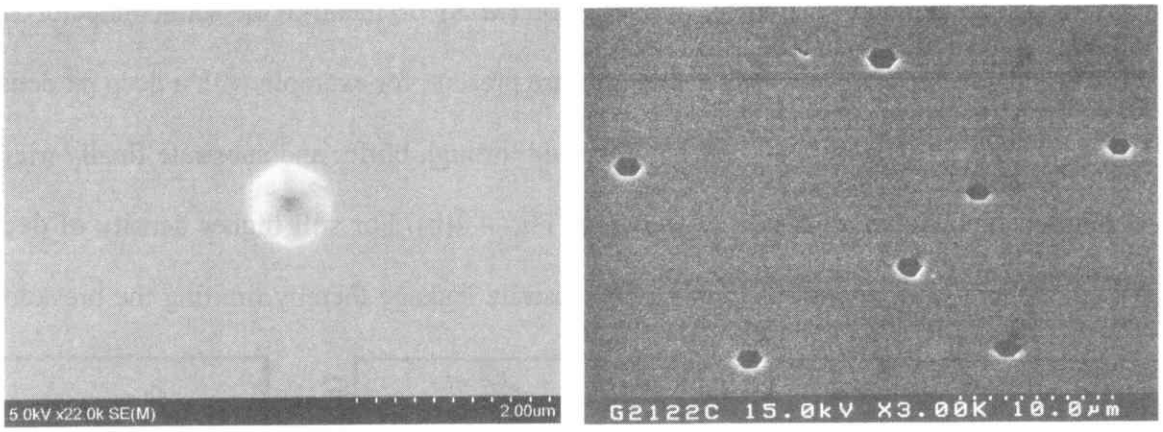


Fig. 4.3. SEM view of hexagonal shaped deep pits on the surface of AlGaN/GaN HEMT on Si grown by MOCVD.

4.1. Influence of Pits on the device breakdown

In order to study the implications of these pits, 100 nm SiO_2 passivated HEMTs were processed. The HEMT process details can be found in our previous report [4]. The dimensions of the processed HEMTs were $W_g/L_g/L_{gd}$ = 15 µm / 1.5 µm / 3.0 µm. All devices had a good I_{DS}-V_{DS} characteristics with a complete pinch-off at -2.5 V. Finally, the devices were tested for 3 terminal-off breakdown (*3TBV*) using Keithley pico-ammeters interfaced with a probe station [5] as described in chapter-3 in Fig. 3.6. The gate terminal is kept at a constant bias of -5.0 V well below the device threshold voltage. The breakdown voltage was applied at the drain terminal and various leakage currents were measured. At a gate bias of -5.0 V, since the channel is closed, buffer and substrate are the paths available for the leakage currents flow in addition to the gate leakage. Therefore drain leakage current (I_{Drain}) comprises leakage currents through gate (I_{Gate}), buffer (I_{Buf}) and substrate (I_{Sub}).

Figure 4.4(a) shows that a HEMT with only shallow pits and almost no deep pit has a

breakdown around 325 V accompanied by a burn mark on the device surface. A low leakage through buffer (I_{Buf}) and substrate (I_{Sub}) was observed until breakdown at 325 V. However, the high gate leakage is understood as our devices have a Schottky contact and this gate leakage can be lowered by using a metal-insulator-semiconductor (MIS) or metal-oxide-semiconductor (MOS) structure at the gate terminal. But when deep pits are present, for example with a deep pit density of $2.5x10^3$ cm^{-2} there is an additional leakage observed through buffer and substrate finally triggering a pre-matured breakdown at 246 V as shown in Fig. 4.4(b). For still higher density of deep pits ($3x10^4$ cm^{-2}) there is an enormous increase in substrate leakage thereby limiting the breakdown to

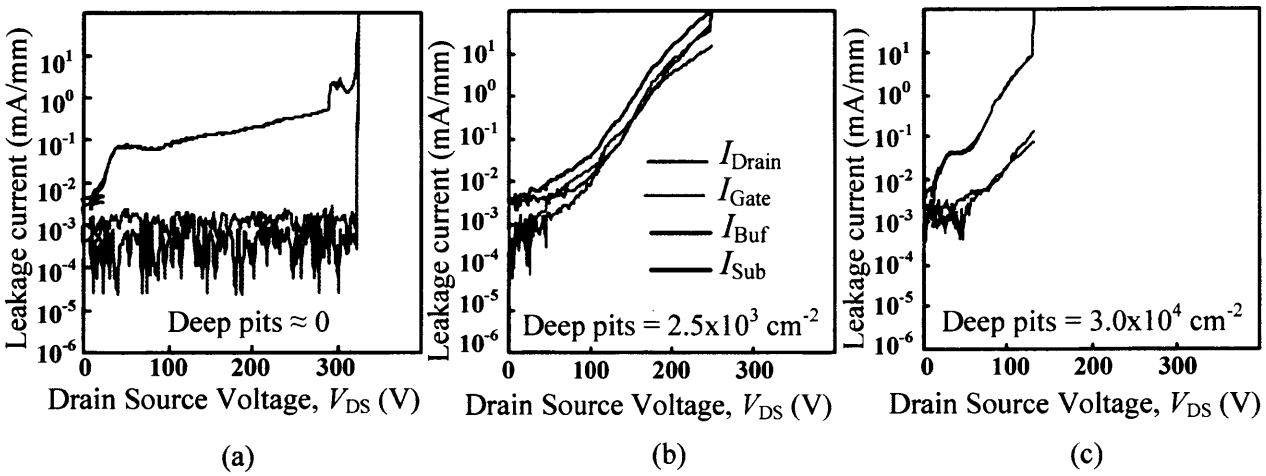


Fig. 4.4. (a) Three terminal-off breakdown of the HEMT which has only shallow pits (b) low density of deep pits and (c) high density of deep pits.

130 V [Fig. 4.4(c)]. All the devices present in a single wafer with deep pits showed a very low breakdown irrespective of the presence of deep pits at the gate-drain area. Thus we find that presence of only shallow pits does not affect the device breakdown whereas the presence of few or more deep pits degrade the breakdown property due to high leakage through buffer and substrate. The intention of growing a thick epi-layer HEMT is to increase the breakdown so as to find its application as a high power device. But on the contrary here we find that occurrence of deep pits very much affect the device breakdown as can be seen from the summary illustrated in Fig. 4.5. As the density of deep pits increase, the breakdown steadily decrease and reaching a lowest breakdown

of 48 V for devices with maximum density of deep pits. Further, no burn mark was found on these devices as they undergo a breakdown in the buffer/Si junction.

In order to find the reason for high substrate leakage on devices with deep pits, cross sectional images using transmission electron microscopy (TEM) were performed. The TEM image was recorded for our sample having the maximum deep pit density (7.5×10^5 cm^{-2}) in which the AlGaN/GaN hetero-structure was grown over a 4-μm-thick buffer. For TEM measurement, 4 μm thick buffer was used for the reasons namely; to find the nature and depth of these deep pits, and also to check whether thick buffer has any control over the deep pits. The TEM image as in Fig. 4.6(a) showed a hexagonal V-shaped pit originating down from the substrate and running throughout the epi-layer. In Fig. 4.6(b), the SEM view of corresponding AlN/Si junction shows an etch pit observed on the Si substrate.

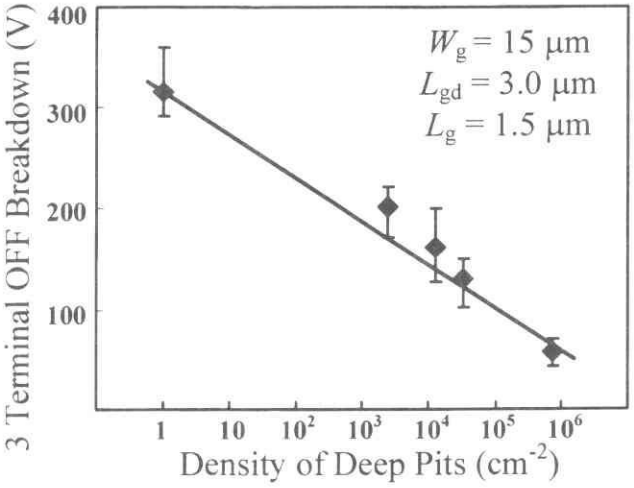
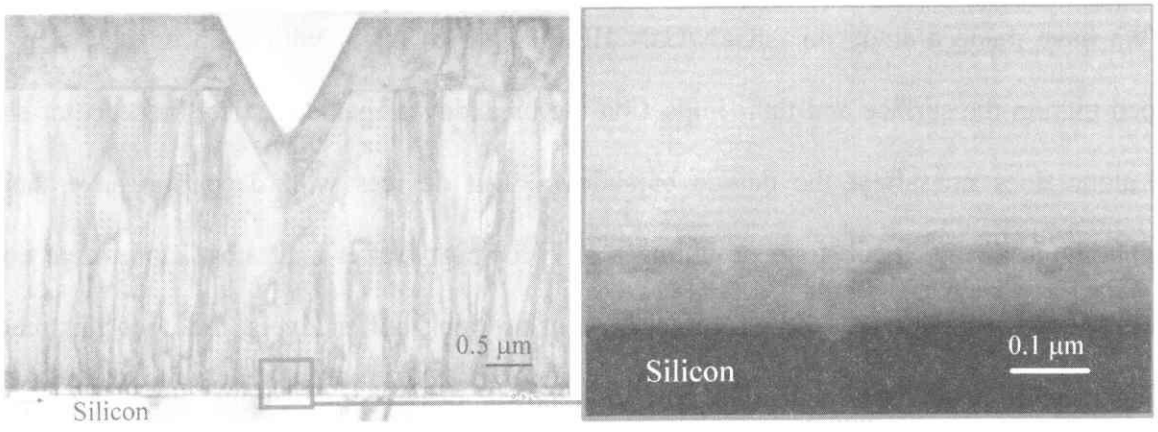


Fig.4.5. Summary of three terminal-off breakdown of the HEMTs with various densities of deep pits.



(a) (b)

Fig. 4.6. (a) TEM view of deep pits originating from Si substrate and terminate at the surface as deep pits, (b) SEM view of etch pit observed at the AlN/Si junction.

In-spite of using 100 nm AlN to prevent Ga (in 40 nm AlGaN) etching the Si substrate at a high growth temperature, the Si substrate undergo this unexpected etching. These etch pits originating at the silicon substrate run throughout the epi-layers up to the surface causing deep surface pits. And even using a thick buffer layer cannot stop the deep pits reaching the AlGaN surface layer. The prevention and control of deep pits largely depend on the condition of the MOCVD growth chamber. Thus we conclude that deep pits found on surface originate from the substrate and behave like micro-pipes for high I_{Sub} leakage flow. During breakdown measurements, due to high V_{DS} these micro-pipes tend to act as a trapping path for the flow of high leakage current through buffer and substrate. Though we could understand the influence of pits on excess leakage through buffer and substrate, we also find a considerable increase in gate leakage current. According to Bang *et al.*[6] AlGaN/GaN HEMTs on SiC having similar deep pits yielded high gate leakage (I_{Gate}). This is because of high density of the tunneling path due to defect levels caused by poor crystalline quality around the pits or lowering of Schottky barrier due to high density of free carriers. Thus we find for devices with deep pits, there is an overall degradation of the breakdown property caused by excess leakage currents namely I_{Gate}, I_{Buf}, and I_{Sub}. This limits the breakdown of AlGaN/GaN HEMTs in-spite of strengthening the buffer/Si junction with increased buffer thickness.

We have made a study on AlGaN/GaN HEMTs grown on Si with deep hexagonal pyramid shaped pits on the surface and their impact on the breakdown characteristics. Presence of shallow pits alone does not affect the device breakdown. But devices with deep pits have their pits originating from the Si substrate providing a path for high buffer and substrate leakage currents which limits the device breakdown. In-spite, of using thick buffer layers, the deep pits reach the AlGaN surface layer from substrate. For high power device applications, thick epi-layers are preferred which are completely free from deep pits in order to find its application for high power device applications.

4.2. Influence of Pits on the device characteristics

AlGaN/GaN HEMTs are attractive for high-power switching device applications. Among the available substrates (SiC, Sapphire and Si) Si is the most suitable choice for epitaxial growth due to its large size availability and low cost. The advantage with Si is that it offers growth on large diameter substrate up to a size of 200 mm, which is not possible using either SiC or sapphire. However, the limiting factor for the growth of GaN on Si is the large lattice and thermal mismatches which lead to large density of dislocations resulting in wafer bowing and cracking.

Apart from these common issues before GaN growth on Si, another important issue which needs investigation is the presence of hexagonal shaped deep-pits on the surface of the growth completed wafer. In the previous section we reported the nature of these pits and their impact on the three terminal-OFF breakdown (BV_{OFF}) [7]. These pits originate from the Si substrate and are present until the top AlGaN surface layer irrespective of using buffers of various thickness. It is difficult to grow pit-free structures on Si as the best grown wafers still have few deep-pits. Some of the grown wafers have very low density of deep pits and if HEMTs are fabricated on such wafers, the pits are found either within or outside the device active region (between source and drain) as illustrated in Fig. 4.7. It is therefore necessary to study the detrimental effect of these pits on the device characteristics with relevant to their distance from the active region. In other way, we have to investigate the influential area of these pits that interferes with normal device operation of a HEMT. Identifying this influential region is important for avoiding the same during device fabrication to demonstrate ideal power and reliability characteristics. Therefore, in the current study, we selected samples which have low pit density (830 cm^{-2}) and investigated the influence of these pits on the HEMT characteristics like I_{DSmax}, V_{th} and BV_{OFF} with respect to

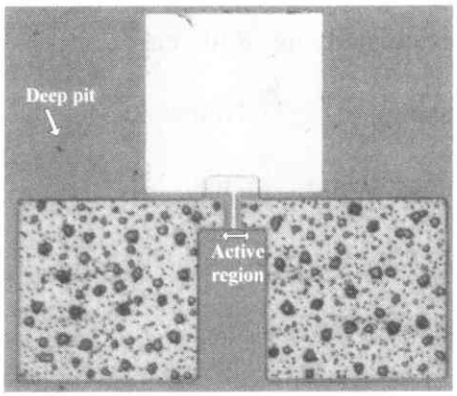


Fig. 4.7. A HEMT device and the nearby deep-pit.

distance from the active region of a HEMT. Further, these electrical characteristics were compared with optical measurements namely cathodoluminescene (*CL*) and Raman spectra measured at various distance from a deep-pit. Analyzing electrical and optical characteristics of deep-pits revealed more about its nature and the significant region around a pit affected by high dislocations and increased strain.

AlGaN/GaN HEMT heterostructures were grown using Taiyo-Nippon Sanso SR4000 horizontal MOCVD reactor. The current HEMT epi-layers were grown on 4-inch Si starting with 100 nm AlN followed by 40 nm AlGaN, 4.0 μm thick super-lattice structure (*SLS*) buffer, 1 μm i-GaN and final 25 nm top $Al_{0.26}Ga_{0.74}N$ layer. The density of deep-pits on these structures were calculated as 830 cm^{-2} using Nomarski microscope image. In figure 4.8, the cross-sectional transmission electron microscope image shows pit size of 1.5 μm diameter originating from the Si substrate. The v-shaped defect present throughout the grown epi-layer starting from Si until the surface layer as it can be seen from figure 4.8(a). A more clear view of *SLS* buffer at v-shaped defect is shown in Fig. 4.8(b). These pits originate from the Si substrate as shown in Fig. 4.8(c).

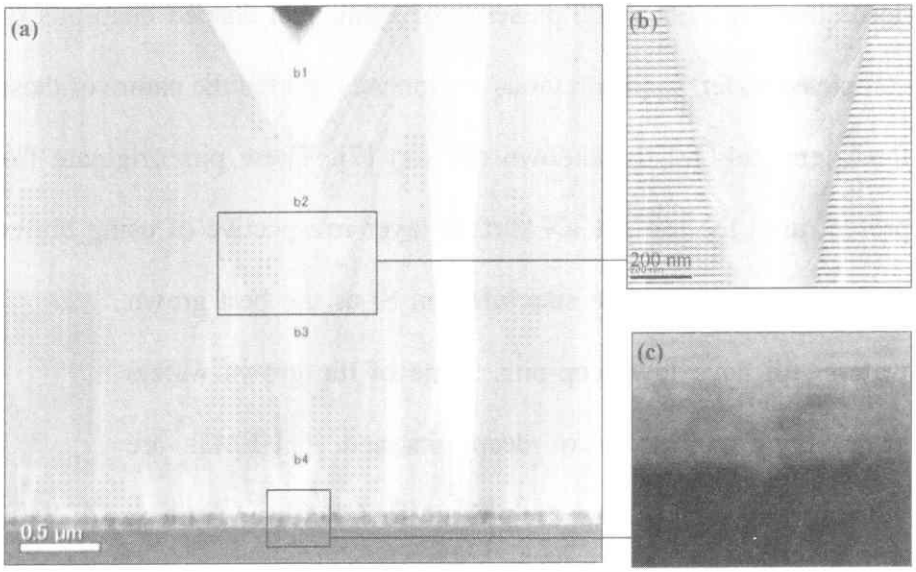


Fig. 4.8. (a) Cross sectional Transmission Electron Microscope image of AlGaN/GaN grown on Si substrate; (b) magnified view of the *SLS* buffer at v-shaped defect; (c) origin of the pit from Si substrate.

HEMT devices passivated with 100 nm SiO_2 were fabricated with dimensions of gate width (W_g) = 15 μm, gate length (L_g) = 1.5 μm and gate-drain length (L_{gd}) = 4 μm. The process

details of the HEMT fabrication are similar to our earlier report [8]. The *dc* current-voltage (I_{DS}-V_{DS}) characteristics of the HEMTs were measured using Agilent 4156 semiconductor parameter analyzer. Since the pit density is low (< 830 cm^{-2}) only one or two pits were present in the vicinity of the device region. A number of devices were carefully chosen in two categories namely (i) devices which had pit within the source-drain active region and (ii) devices which had pits outside active region. In both cases, nearest distance (d) of the gate finger was calculated from a pit. All these HEMTs showed good pinch-off characteristics irrespective of the position of pit. However, there was a difference in the I_{DSmax} observed with regard to the position of these pits from active region. Figure 4.9 summarizes the I_{DSmax} observed for HEMTs with respect to pit at a distance. The HEMTs showed better I_{DSmax} when pits are beyond 50 μm away from the device active region. However, 19 % reduction in I_{DSmax} was observed when a pit is found within the active region as shown in figure 2. Further, this reduction in the I_{DSmax} were accompanied by a shift in the threshold voltage. HEMTs which had pit far away (d > 50 μm) underwent complete pinch-off at -2.2 V, where as HEMTs which had pit near active region (d < 10 μm) showed a positive shift in V_{th} causing an early pinch-off at -1.8 *V*. This positive shift in V_{th} for HEMTs having pit within or near the active region signifies that dislocation densities are high around the region of a pit. Because it is known that dislocations in III-V nitride heterostructures can produce acceptor-like trap states [9,10] which

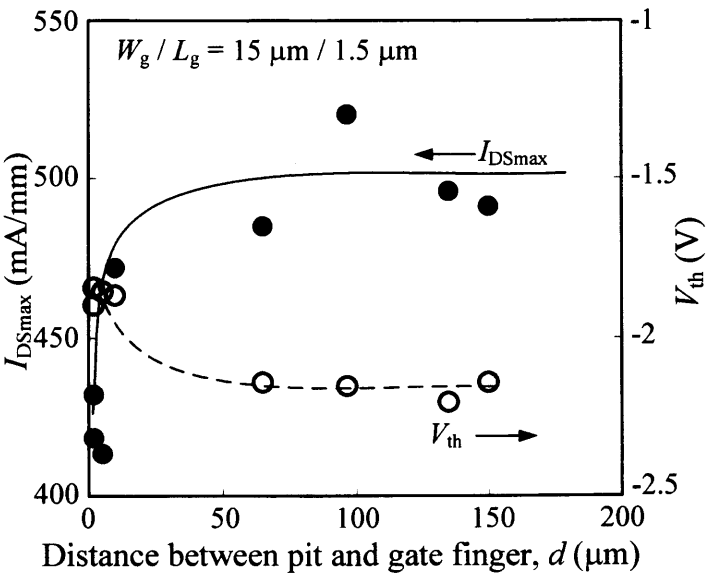


Fig. 4.9. I_{DSmax} (solid circle) and V_{th} (open circle) measured for HEMTs having pits at various distance (d) from the gate terminal.

become negatively charged [11]. Therefore, for HEMTs located near the pit, high dislocations around the pit act as trapping centers for electrons in the 2-dimensional electron gas (*2DEG*) channel. This results in partial depletion of *2DEG* at the AlGaN/GaN interface causing a low I_{DSmax} and a positive V_{th} shift.

The three terminal-OFF breakdown measured on these devices remain unaffected when these pits are 50 μm away from the active region. A drastic 50% reduction in the breakdown with high buffer and substrate leakage was observed when pits are found within the active region as summarized in figure 4.10. We reported that growing a thick buffer for the growth of GaN on Si restricts the buffer and substrate leakage causing a high breakdown.[6] However, in these samples with deep-pits, in-spite of using a 4 μm thick buffer, the presence of deep-pits causes high buffer and substrate leakage thus deteriorating the breakdown to a large extent. Therefore, the position of these deep-pits found to affect the device performances especially when they are within a short range (d < 50 μm) from the active region. Hence, it is necessary to further study the quality of the GaN around 50 μm radius of a deep-pit for further understanding.

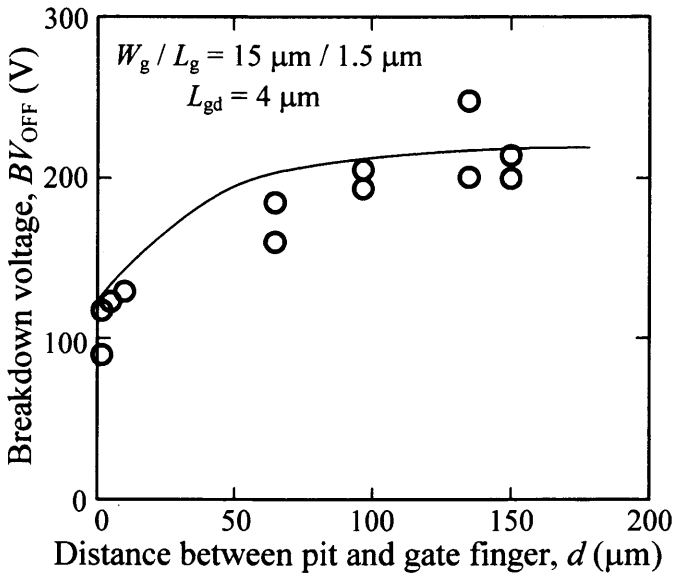


Fig. 4.10. Three-terminal OFF-breakdown (BV_{OFF}) measured for HEMTs having pits at various distance (d) from the gate terminal; BV_{OFF} defined as V_{DS} at which a leakage of 1 mA/mm was observed.

In order to investigate the region around pits, *CL* was measured in a Hitachi SU-70 scanning electron microscope (SEM) using an Oxford instruments MonoCL4 system. After confirming the position of a pit with the help of *SEM*, *CL* was measured at various distance from

the pit. The normalized *CL* spectra as in figure 4 shows the band edge emission (I_{Edge}) at 364 nm corresponding to GaN band gap (3.4 eV). At wavelengths around 550 nm, yellow luminescence (I_{Yel}) with varying peak intensity was observed for intensity measured at various distance from the pit. The intensity of yellow band emission depends on the growth conditions [12] and reflects the quality, un-intentional doping of the GaN grown. A highest I_{Yel} was observed for *CL* measured at the pit and it gradually became weak as the beam spot moved away from the pit. The relative intensity ratio (I_{Yel}/I_{Edge}) as in the inset of figure 4.11 shows a decrease in intensity ratio with increase in the distance from the pit. For *CL* measured at distances beyond 50 μm from the pit, there is not much change in the intensity ratio. This illustrates that yellow luminescence is high for regions within 50 μm of the deep-pits signifying a larger dislocation density for regions around deep-pits. The inset of Fig. 4.11 shows a *CL* image captured around a deep-pit.

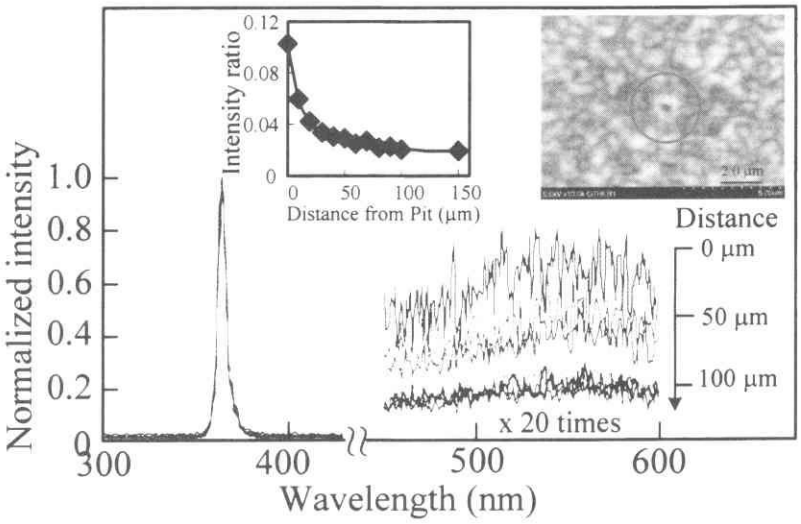


Fig. 4.11. Cathodoluminescence measured for an AlGaN/GaN epi-layer having pit. The *CL* was recorded by focusing the beam spot at various distances from a pit. Inset: Intensity ratio (I_{Yel}/I_{Edge}) decreased as *CL* was measured at a farther distance from a deep-pit, and a *CL* image captured around a deep-pit marked by a circle.

In order to study the stress created by deep-pits, we performed micro-Raman measurements in E_2 Raman mode which is known to be shifted by stress alone [13]. To start with, E_2 Raman spectra was measured on GaN substrate (shift at 567.6 cm^{-1}), which is considered as the reference (dashed line in Fig. 4.12) for unstressed GaN films. Then for samples with deep-pits, micro-Raman

measurements were measured starting at the pit and at various distance from the pit. Before measurement it was confirmed that no other pits were present in the neighboring vicinity of 300 μm radius of the pit chosen for investigation. The Raman shift peak position measured at various distance from the pit are shown in Fig. 4.12. Comparing with the peak position for unstressed GaN films, the E_2 mode observed for our GaN on Si substrate confirms the presence of tensile stress [14]. It is well known that the type of stress observed for GaN grown on Si and sapphire is tensile and compressive respectively. From figure 4.12, it is concluded that there is an additional tensile stress for regions within the 40 μm range of a deep-pit. However, as we move away from the pit (beyond 40 μm), the Raman shift peak position remained constant without any additional change in tensile stress. This further confirms that regions beyond 50 μm from a deep-pit do not pose any detrimental effects on the device performance.

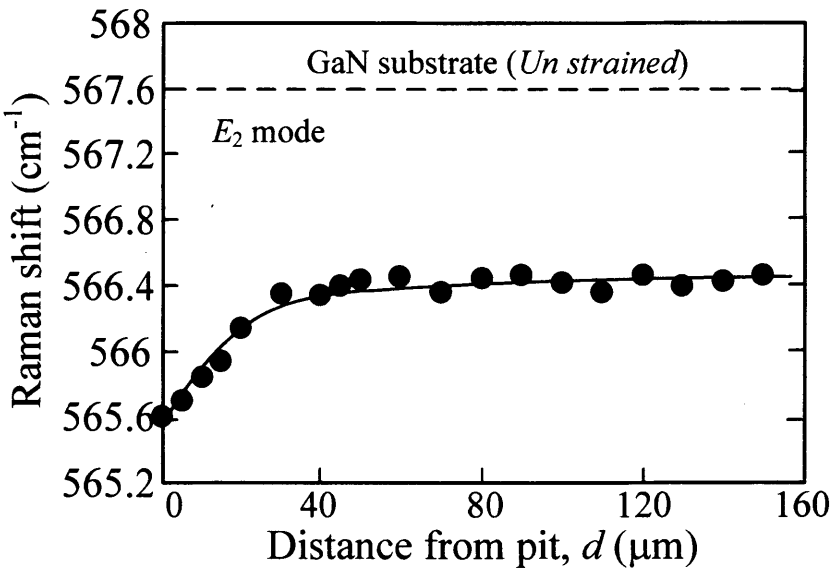


Fig. 4.12. E_2 Raman shift measured at various distance from a pit. The E_2 Raman shift peak position for a GaN substrate is identified with a dashed line.

As a summary, we have made an in-depth study on the regions around deep-pits and their limitations on the performance of MOCVD grown AlGaN/GaN HEMTs on Si substrate. It is concluded that for regions within 50 μm distance of deep-pits, there is a degradation observed in device performance. If the active region of the HEMTs are within the 50 μm distance from a deep-pit, then it leads to 19% decrease in the I_{DSmax} and positive shift in the V_{th} signifying an early

pinch-off. The early pinch-off for devices within the 50 μm distance of deep-pit confirms the presence of high dislocations causing dislocation scattering. These high dislocations cause 50% decrease in BV_{OFF} due to large buffer and substrate leakage current. Further, the 50 μm radius defective region around the pits were confirmed by *CL* and Raman shift measurements. Therefore, for AlGaN/GaN epi-layers grown on Si having a low density of deep-pits on the surface, the pits does not impede the normal performance of the HEMTs if the source/drain active region is located far away at a distance of 50 μm from the deep-pits.

References

[1]. S. L. Selvaraj, T. Suzue, and T. Egawa: IEEE Electron Device Lett. **30** (2009) 587.

[2]. S. L. Selvaraj, T. Suzue, and T. Egawa: 67th DRC Dig. 2009, p. 283.

[3]. H. Sasaki, S. Kato, T. Matsuda, Y. Sato, M. Iwami, and S. Yoshida: Jap. J. Appl. Phys. **45** (2006) 2531.

[4]. S. L. Selvaraj, T. Ito, Y. Terada, and T. Egawa: Appl. Phys. Lett. **90** (2007) 173506-1.

[5]. Y. C. Choi, M. Pophristic, H. Y. Cha, B. Peres, M. G. Spencer, and L. F. Eastman: IEEE Trans. Electron Devices **53** (2006) 2926.

[6]. H. Bang, T. Mitani, S. Nakashima, H. Sazawa, H. Hirata, M. Kosaki, and H. Okumura: J. Appl. Phys. **100** (2006) 114502-1.

[7]. S. L. Selvaraj, T. Suzue and T. Egawa, Appl. Phys. Express **2**, 111005 (2009).

[8]. S. L. Selvaraj and T. Egawa, Appl. Phys. Lett. **89**, 193508 (2006).

[9]. F. A. Ponce, D. P. Bour, W. Götz, and P. J. Wright, Appl. Phys. Lett. **68**, 57 (1996).

[10]. D. M. Schaadt, E. J. Miller, E. T. Yu and J. M. Redwing, Appl. Phys. Lett. **78**, 88 (2001).

[11]. P. J. Hansen, Y. E. Strausser, A. N. Erickson, E. J. Tarsa, P. Kozodoy, E. G. Brazel, J. P. Ibbetson, U. Mishra, V. Narayanamurti, S. P. DenBaars and J. S. Speck, Appl. Phys. Lett. **72**, 2247 (1998).

[12]. S. L. Selvaraj, T. Suzue and T. Egawa, Electron. Dev. Lett., **30**, 587 (2009).

[13]. T. Ogino and M. Aoki, Jap. J. Appl. Phys. **19**, 2395 (1980).

[14]. C. Kisielowski, J. Krüger, S. Ruvimov, T. Suski, J. W. Ager III, E. Jones, Z. L. Weber, M. Rubin, E. R. Weber , M. D. Bremser and R. F. Davis, Phys. Rev. B **54**,17745 (1996).

Chapter 5

Summary of Results

MOCVD grown AlGaN/GaN HEMTs on 4-inch Si substrate were studied for enhancing the drain current density and breakdown. Al_2O_3 based thin gate dielectrics were used to control the gate leakage and increase the positive gate biasing. Thick AlGaN/GaN HEMT epi-layers were grown to control buffer and substrate leakage currents and offer high breakdown. The challenges before the GaN on Si were studied in detail. The following are the summary of the results discussed in this report:

[1]. The effect of thin 3 nm Al layer deposition prior to the gate metal (Pd/Ti/Au) was studied and found that the Al layer oxidized into an oxide layer of 3.75 nm thickness. Due to the oxide formation, there is an increase in (i) drain current density and (ii) density of electrons at the 2DEG channel. The oxide formation was confirmed by AES and identified as Al_2O_3 by XPS spectra. A systematic study of oxidizing Al into high quality Al_2O_3 should be further explored for providing an ideal gate insulator and passivation for high power device requirements.

[2]. The device characteristics of AlGaN/GaN HEMTs, MOS-HEMTs grown on Silicon were studied using plasma oxidized Aluminum at the Schottky contact. The Al based MOS-HEMTs are reported to enhance the drain current density (1086 mA/mm) with a possible application of gate bias as high as +3.5 V. On the other hand plasma treated MOS-HEMTs have reduced drain current density due to plasma damage during O_2 plasma oxidation leading to a high interface state density in the Al_2O_3/AlGaN interface. The inclusion of a thin oxide layer, or plasma oxidized Al reduces the gate leakage current by an order. This is due to the removal or absorption of oxide interface states present at the AlGaN

cap layer by thin Al metal which forms aluminum based oxide (Al_2O_3). The use of thin Al_2O_3 as the gate dielectric is recommended for AlGaN/GaN based MOS-HEMTs with a possible high gate voltage operation.

[3]. AlN cap layered MIS-HEMTs on 4 in. silicon with good device properties were studied. The MOCVD grown AlN morphology was improved with R_{MS} roughness of 1.03 nm. However this is the best morphology reported so far for any thin AlN grown as cap layer over AlGaN/GaN HEMT on silicon. For AlN MIS-HEMT the increase in the sheet carrier density was observed to shift the 2DEG channel towards the AlGaN/GaN interface thereby increasing the transconductance. The decrease in $I_{DS\,max}$ for MIS-HEMTs is due to surface roughness arising out of lattice mismatch at the top AlN insulating layer. The fabricated AlN/AlGaN/GaN MIS-HEMTs show reduced current collapse with two orders of magnitude less gate leakage and high breakdown.

[4]. Without using a field plate, a high breakdown was demonstrated successfully for AlGaN/GaN HEMTs. A high breakdown of 403 V for AlGaN/GaN HEMTs with a L_{gd} of 3 μm and a breakdown of 1813 V for i-GaN were achieved. These results indicate a method to enhance the breakdown of AlGaN/GaN HEMTs without using field plate structure.

[5]. Based on the experimental results, the following points are noteworthy to enhance the breakdown of AlGaN/GaN HEMTs on Si substrate: (a) Growing thick wide band gap material increases the resistance between the surface electrode and the silicon wafer to improve the breakdown, (b) Increasing the T_{Buf} will improve the quality of GaN growth on Si thereby reducing the D_D which in turn increases the breakdown, (c) However for devices with very small L_{gd} (= 3 μm) there is an upper limit to this type of breakdown enhancement by increased T_{Buf} as they undergo premature breakdown due to high field developed at the gate-drain region. This breakdown could be improved further by increasing the L_{gd} without

compromising on the device properties like I_{Dmax} and g_{mmax}. Further detailed study is needed to understand the relation between the dislocation density and breakdown enhancement.

[6]. AlGaN/GaN HEMTs grown on Si with deep hexagonal pyramid shaped pits on the surface pose a challenge for these devices. The deep-pits and their impact on the breakdown characteristics were studied. Presence of shallow pits alone does not affect the device breakdown. But devices with deep pits have their pits originating from the Si substrate providing a path for high buffer and substrate leakage currents which limits the device breakdown. In-spite, of using thick buffer layers, the deep pits reach the AlGaN surface layer from substrate. For high power device applications, thick epi-layers are preferred which are completely free from deep pits in order to find its application for high power device applications.

[7]. An in-depth study on the regions around deep-pits and their limitations on the device characteristics of MOCVD grown AlGaN/GaN HEMTs on Si substrate were studied. It is concluded that for regions within 50 μm distance of deep-pits, there is a degradation observed in device performance. If the active region of the HEMTs are within the 50 μm distance from a deep-pit, then it leads to 19% decrease in the I_{DSmax} and positive shift in the V_{th} signifying an early pinch-off. The early pinch-off for devices within the 50 μm distance of deep-pit confirms the presence of high dislocations causing dislocation scattering. These high dislocations cause 50% decrease in BV_{OFF} due to large buffer and substrate leakage current. Further, the 50 μm radius defective region around the pits were confirmed by *CL* and Raman shift measurements. Therefore, for AlGaN/GaN epi-layers grown on Si having a low density of deep-pits on the surface, the pits does not impede the normal performance of the HEMTs if the source/drain active region is located far away at a distance of 50 μm from the deep-pits.