1. AlGaN/GaN high-electron-mobility transistors on sapphire, silicon carbide and silicon substrates

AlGaN/GaN High-Electron-Mobility Transistors on Sapphire, Silicon Carbide and Silicon substrates

Abstract

Investigations of AlGaN/GaN high-electron-mobility transistors (HEMTs) have been performed on different substrates such as 2-inch diameter sapphire, 2-inch diameter semi-insulating (SI) SiC, 4-inch diameter sapphire and 4-inch diameter Si substrates. Before going studying AlGaN/GaN HEMTs, different metal (Ag, Ti, Au, Pd and Ni) based Schottky barrier diodes (SBDs) were fabricated and characterized on GaN and AlGaN layers [1,2]. The annealing effects were performed in Ti/AlGaN, Ni/AlGaN and Pd/AlGaN Schottky contacts to observe the high temperature stability [3]. Rectifying behavior has been observed up to the annealing temperature 450 °C/1 hr for Ni/*n*-$Al_{0.11}Ga_{0.89}N$ and 500 °C/1 hr for both Ti and Pd/n-$Al_{0.11}Ga_{0.89}N$ Schottky diodes. The Al-content (20, 27, 34 and 52%) effects in AlGaN barrier layer of AlGaN/GaN HEMTs was performed on 2-inch sapphire substrate [4,5]. Comparison studies were performed between 2-inch diameter sapphire and SI-SiC based AlGaN/GaN HEMTs [6]. Similarly the HEMTs on 4-inch sapphire and Silicon based HEMTs were also fabricated and compared [7]. For the mass production point of view, uniformity of material and device characteristics of AlGaN/GaN HEMTs was performed on one fourth of 4-inch diameter sapphire grown AlGaN/GaN HEMTs [8]. The observed average maximum drain current density, extrinsic transconductance and threshold voltage values for HEMTs on 4-inch sapphire were 515 mA/mm, 197 mS/mm and -2.30 V with standard deviations 9.34%, 4.82% and 6.52%, respectively. Enhancement of OFF-state breakdown voltage in AlGaN/GaN HEMTs with the increase of buffer AlN thickness was observed on 4-inch Si substrates [9]. Small drain current collapse devices were fabricated on SiC substrates when compared to the devices on sapphire substrates. The OFF-state breakdown voltage mechanism of AlGaN/GaN on 2-inch sapphire substrate was obtained using temperature dependent leakage current measurements [10]. Suppression of drain current collapse studies were observed on passivated AlGaN/GaN HEMTs using different dielectric layers such as plasma enhanced chemical vapor deposition (PECVD) SiO_2, Si_3N_4 and silicon oxy nitride (SiON) [11]. Drain current collapse free *i*-GaN/AlGaN/GaN HEMTs with and without surface layer passivation were demonstrated on sapphire substrates [12]. The effect of different cap layers (*i*-GaN, *n*-GaN, *p*-GaN and InGaN) in current collapse and dc characteristics were investigated [13]. The effect of recess gate process on the current collapse was also investigated in different cap layers grown AlGaN/GaN HEMTs [14].

1. Device design and fabrication

1.1. Schottky Diodes on GaN and AlGaN

The GaN and $Al_{0.11}Ga_{0.89}N$ epilayers were grown on sapphire (0001) substrate using the horizontal atmospheric pressure Metal Organic Chemical Vapor Deposition (MOCVD) method.[1)] Trimethylgallium (TMG), Trimethylaluminium (TMA) and NH_3 were used as source materials, and H_2 (10 ppm) diluted SiH_4 was used as n-type dopant. GaN (30 nm) buffer layer was deposited at 530 °C after sapphire substrate was heated at 1100 °C for 10 minutes in a steam of hydrogen. Then silicon doped GaN layer (3.0 μm) was grown at 1080 °C on buffer layer. This GaN has been used for the fabrication of Schottky contacts. For $Al_{0.11}Ga_{0.89}N$ growth, 2.5 μm thick silicon doped n^+-GaN layer was grown on GaN buffer layer. Un-doped GaN layer (1 μm) was grown on 2.5 μm silicon doped n^+-GaN. Finally $Al_{0.11}Ga_{0.89}N$ layer (0.3 μm) was grown with the silane flow rate 0.3 sccm. Aluminum concentration was determined using X-ray method. The fabricated device structure consisted of an array of 150 μm diameter Schottky dots separated 175 μm radially from the bi-layer Ti/Al (25nm/150 nm) Ohmic contacts (Guard-ring) [1]. Schottky dots were patterned using the metal lift-off technique. Prior to transferring the samples into the evaporation chamber, the samples were dipped in concentrated HCl solution for 60 seconds and rinsed in DI-water. Electron beam evaporation was used to deposit all the metals except silver (Ag) to a thickness of 100 nm. Ag was evaporated using resistive heating method. Fig. 1 shows the schematic diagram of fabricated n-GaN and n-AlGaN Schottky diodes. The fabricated Ti, Pd and Ni/n-$Al_{0.11}Ga_{0.89}N$ Schottky diodes were annealed at various temperatures from 100 to 550 °C for different annealing time in a nitrogen atmosphere.

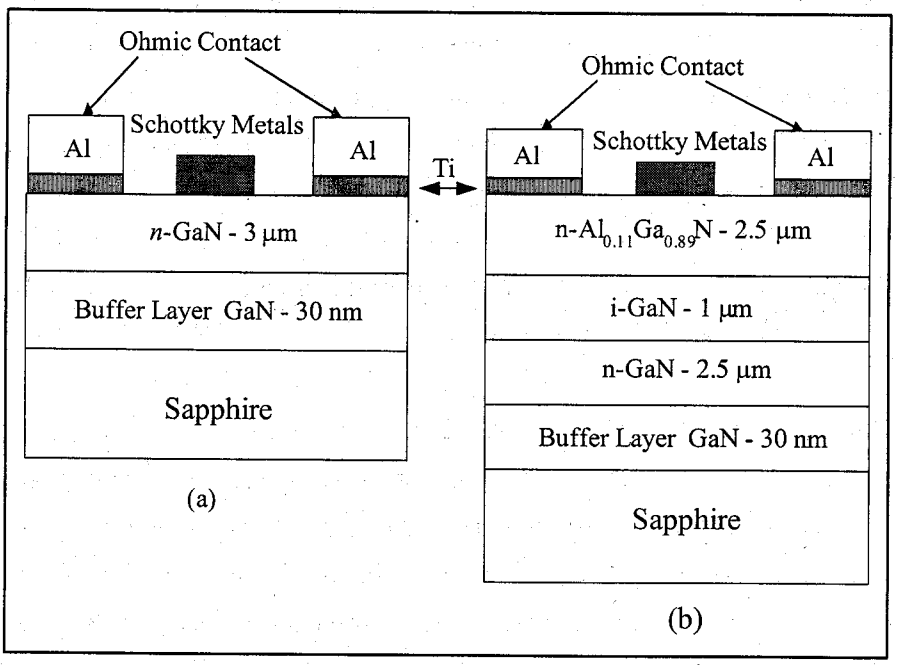

Fig. 1. Schematic diagram of (a) n-GaN (b) n-$Al_{0.11}Ga_{0.89}N$ Schottky diodes

1.2. Different Al-content AlGaN/GaN HEMTs on 2-inch Sapphire

The $Al_xGa_{1-x}N$/GaN ($0.20 \leq x \leq 0.52$) HSs were grown on (0001)-oriented sapphire substrates using horizontal atmospheric pressure MOCVD (Nippon Sanso, SR-2000). Trimethylgallium (TMG), trimethylaluminum (TMAl) and ammonia (NH_3) were used as source materials. Monosilane (10 ppm, diluted in hydrogen) was used as n-type dopant. The sapphire substrate was heated at 1100 °C for 10 min in a hydrogen atmosphere to clean the surface. The device consists of 3 nm undoped AlGaN barrier layer, 15 nm silicon doped AlGaN supply layer ($4x10^{18}$ cm^{-3}), 7 nm intentionally un-doped AlGaN spacer layer, 3000 nm insulating GaN (*i*-GaN) layer and a 30 nm low temperature (550 °C) grown un-doped GaN buffer layer on top of the sapphire substrate. Both $Al_xGa_{1-x}N$ and GaN layers were grown at 1080 °C.

The mesa isolation was accomplished by mesa dry etching down to the *i*-GaN of HEMT structure by BCl_3 plasma reactive ion etching (RIE). The Ohmic contact was made by the deposition of a Ti/Al/Ti/Au (25/100/45/55 nm), which was subsequently alloyed at 760 °C for 60 s in nitrogen atmosphere. The gate metals of Pd/Ti/Au (40/40/80 nm) with 2.0-, 2.2-, 2.5-, 3.0- and 5.0-μm-long-gates (L_g) were optically defined using lithography through conventional lift-off method. High temperature stable Pd/AlGaN Schottky diodes were obtained and reported elsewhere [1,2]. Before loading the sample for evaporation of gate and ohmic metals, the samples were dipped in conc. HCl solution for 60 sec to remove the native oxide. The schematic diagram of the fabricated device structure is shown in Fig. 2.

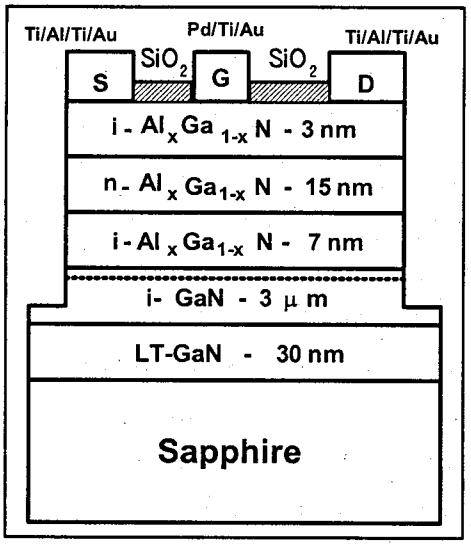

Fig.2. Schematic diagram of fabricated $Al_xGa_{1-x}N$/GaN HEMTs (x=0.20, 0.27, 0.34 and 0.52) on 2-inch sapphire

1.3. AlGaN/GaN HEMTs on 2-inch SI-SiC substrate

The $Al_{0.26}Ga_{0.74}$/GaN layers were grown by atmospheric-pressure MOCVD on (0001)-oriented semi-insulating 4H-SiC substrates using the following growth conditions. The device structure consists of a 3 nm undoped AlGaN barrier layer, a 15 nm silicon-doped AlGaN supply layer (n=$4x10^{18}$ cm^{-3}), a 7 nm undoped AlGaN spacer layer, a 3000 nm insulating GaN (i-GaN) layer and a 200 nm AlN buffer on top of the SI-SiC substrate. Growth temperatures of 1130°C and 1150°C were maintained for AlGaN and AlN layers, respectively. Aluminium content of all AlGaN layers was maintained at 26%.

The device isolation was accomplished by mesa dry etching down to i-GaN by BCl_3 plasma reactive ion etching [4,5]. SiO_2 was used as the etch mask. The ohmic contact was performed by the deposition of Ti/Al/Ti/Au (25/100/45/55 nm), which was subsequently alloyed at 760°C for 1 min in N_2 atmosphere. The gate metals Pd/Ti/Au (40/40/80 nm) were optically defined, into 2.2-, 3.0- and 5-μm-long-gates with 15- and 200-μm gate widths using optical lithography through a conventional lift-off method. Both ohmic and gate metals were evaporated using an electron beam evaporation system. The cross-sectional view of the fabricated device structure is shown in Fig. 3.

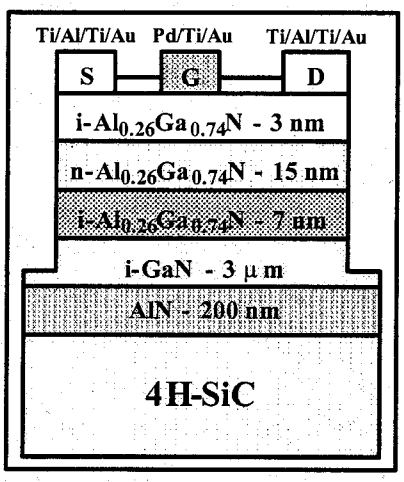

Fig.3. Schematic diagram of fabricated $Al_xGa_{1-x}N$/GaN HEMTs on SI-SiC

1.4. AlGaN/GaN HEMTs on 4-inch sapphire and Si substrates

The AlGaN/GaN device structures were grown on 4-inch diameter (111) oriented *p*-Si (530 μm) and c-face sapphire (630 μm) substrate using metal organic chemical vapor deposition (MOCVD) (Taiyo Nippon Sanso, SR-4000). Trimethylgallium (TMG), trimethylaluminum (TMA) and ammonia (NH_3) were used as Ga, Al and N sources, respectively, and monosilane (SiH_4) was used as the n-type dopant. The schematic diagrams of the device structures on Si and sapphire are shown in Fig. 4. The device structure on Si substrate consists of, from top to bottom, a 25-nm-thick undoped *i*-AlGaN, 1-μm-thick undoped *i*-GaN, 20 pairs of GaN/AlN (20/5 nm) multi layers, 40 nm-thick undoped *i*-AlGaN on a 8-nm-thick AlN buffer layer. All the layers were grown at 1130 °C. The 20 pairs of GaN/AlN (20/5 nm) multi layers are useful to get high quality GaN layers. The structure on sapphire consists of, from top to bottom, a 3-nm-thick undoped AlGaN layer, a 20-nm-thick Si-doped AlGaN layer with the doping density of $5 \times 10^{18}/cm^3$, a 7-nm-thick undoped AlGaN layer and a 3-μm-thick undoped GaN layer on a 25-nm-thick GaN low- temperature buffer layer (LT-BL) [7]. The aluminum composition x in $Al_xGa_{1-x}N$ layers were designed to be 0.26 for both the substrates.

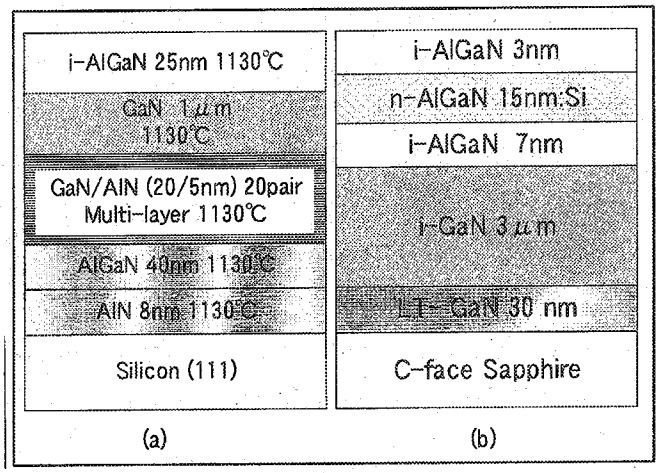

Fig. 4. Schematic diagram of AlGaN/GaN HEMTs on 4-inch (a) Silicon and (b) Sapphire Substrates

After the growth of AlGaN/GaN heterostructures, the HEMTs fabrication was performed as follows. Device isolation was accomplished by mesa dry etching down to GaN layers by 10 W

BCl_3 plasma reactive ion etching. After mesa isolation, ~100 nm thick SiO_2 was deposited at 150 °C by electron-beam (EB) evaporation. The source and drain ohmic contacts were formed by the deposition of Ti/Al/Ni/Au (18/72/12/40 nm), which were subsequently annealed at (750°C for Si) [45] 775°C (sapphire) [7] for 30 s in a N_2 atmosphere. Gate contacts were formed by the deposition of Pd/Ti/Au (40/20/80 nm). Three different (15, 200 and 400 μm) gate width (W_g) devices with 2-um gate-length (L_g) HEMTs were used for this study. The device dimensions are as follows: $W_g/L_{sd}/L_{sg}/L_g$=15/9/3.5/2.0 μm; $W_g/L_{sd}/L_{sg}/L_g$=200/11/4.5/2.0 μm; $W_g/L_{sd}/L_{sg}/L_g$=400/9/4.5/2.0 μm.

1.5. AlGaN/GaN HEMTs with different AlN buffer layer on 4-inch Si substrate

The growth of AlGaN/GaN HEMTs on 4-inch p-Si (111) substrate (resistivity=0.01Ω-cm) was done by metalorganic chemical vapour deposition (MOCVD) system (Nippon Sanso SR-4000). All the layers were grown at 1130°C. The device structure consist of AlN buffer layers with different thicknesses (8, 200, 300 and 500 nm), 40 nm thick $Al_{0.26}Ga_{0.74}N$, 20 pairs of GaN/AlN (20/5 nm) intermediate transition layer, 1-μm-thick *i*-GaN layer, 1-nm-thick AlN spacer layer [15], and *i*-$Al_{0.26}Ga_{0.74}N$ (25nm) top layer. Crack free AlGaN/GaN heterostructures (HSs) were obtained except the HSs with 500 nm buffer layer. The BCl_3 plasma etching was performed for mesa isolation [7]. The source & drain ohmic contacts were formed using Ti/Al/Ni/Au (20/72/12/40 nm) metals followed by lamp annealing at 750 °C for 30 sec. The contact resistance (R_c) values of 2.33, 1.92, 1.80 and 1.23 Ω-mm were obtained for the AlN buffer thicknesses of 8, 200, 300 and 500 nm, respectively. The gate metal Pd/Ti/Au (40/20/60nm) was formed using conventional photolithography. The schematic diagram of AlGaN/GaN HEMTs on 4-inch Si is shown in Fig 5.

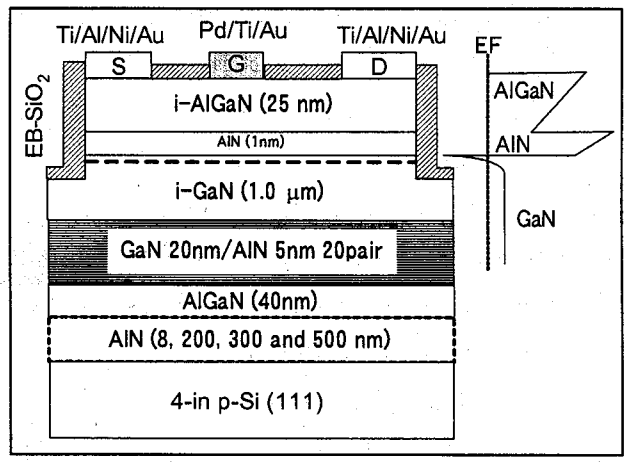

Fig. 5. Schematic diagram of AlGaN/GaN HEMTs with diffferent thickness AlN buffer layer on 4-inch Si substrate

1.6. Surface passivation of AlGaN/GaN HEMTs on 2-inch Sapphire

The AlGaN/GaN heterostructure was grown on 2-inch diameter sapphire substrate using metalorganic chemical vapor deposition (Nippon Sanso SR2000). The device structure is similar to the device structure of section 1.3. After the device isolation with BCl_3 plasma reactive ion etching, SiO_2, Si_3N_4 and SiON dielectrics with a thickness of ~100 nm were deposited at 300 °C

by plasma enhanced chemical vapor deposition (PECVD). Refractive indices of the deposited SiO_2, Si_3N_4 and SiON were 1.47, 1.88 and 1.58, respectively. The XPS spectra revealed the deposited SiO_2 and Si_3N_4 dielectrics [16] were slightly silicon rich and SiON was slightly nitrogen rich. The source drain ohmic contacts were formed after etching the dielectrics with optimized buffered HF solution using Ti/Al/Ni/Au (20/72/12/40 nm) metals followed by lamp annealing at 775 °C for 30 sec. The samples contact resistances were in the range between 1.25 to 1.77 Ω-mm. The gate metal Pd/Ti/Au (40/20/60 nm) was formed by conventional lithography [7]. Fig. 6 shows the schematic diagram of the surface passivated HEMTs. The dielectric layers: i) source-gate gap, ii) gate-drain gap and iii) isolated region were covered. To observe the effect of surface passivation, un-passivated AlGaN/GaN HEMTs were also fabricated on the same wafer.

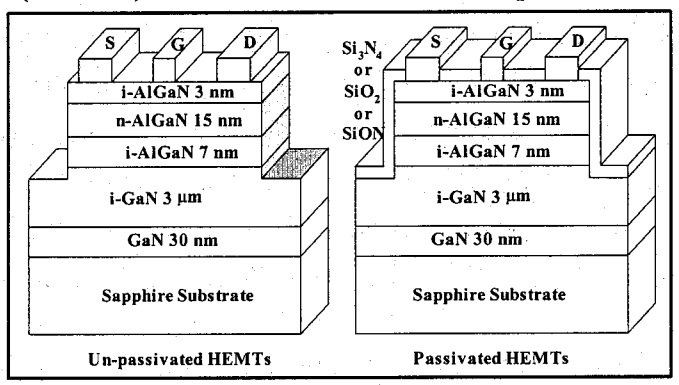

Fig.6. Schematic diagram of un-passivated and Si_3N_4 and SiON passivated AlGaN/GaN HEMTs on 2-inch sapphire substrate

1.7. AlGaN/GaN HEMTs with different Cap Layers (i-GaN, n-GaN, p-GaN and InGaN)

The device structures were grown by metal organic chemical vapor deposition (MOCVD) (Taiyo Nippon Sanso, SR-2000) on a (0001) sapphire substrate. Trimethylgallium, Trimethylaluminum, Trimethylindium and Ammonia were used as source materials. Monosilane (10 ppm, diluted in hydrogen) and Cp_2Mg were used as *n*- and p-type dopant. Two types of device structures, i) typical AlGaN/GaN HEMTs structure [10,11] and ii) AlGaN/GaN HEMTs structure, were grown with different cap layers *i*-GaN [12], *n*-GaN, *p*-GaN and InGaN of thickness 3 nm. The schematic and band diagrams of the grown structures are shown in Fig 7. The dotted line in the band diagram denotes the InGaN cap layer. The growth details of typical AlGaN/GaN HEMTs structures have already been

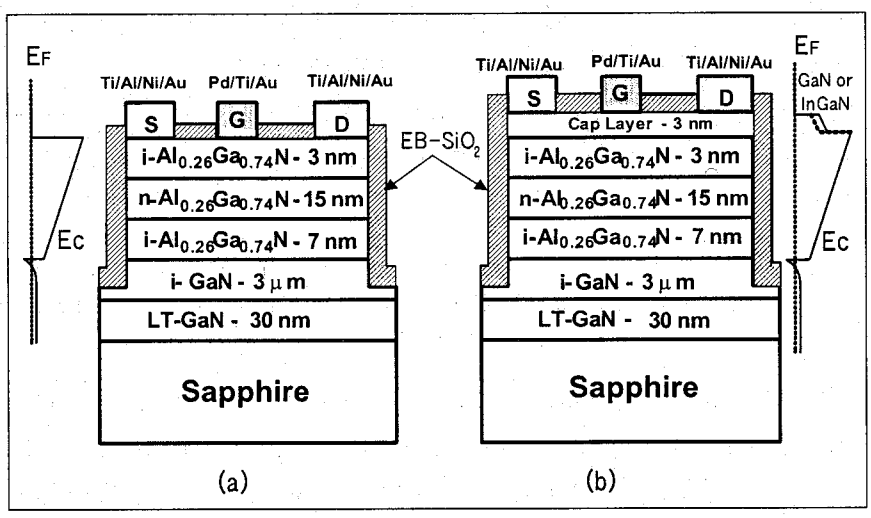

Fig 7. Schematic diagram of AlGaN/GaN HEMTs (a) without cap layers and (b) with cap layers

published elsewhere [10,11]. From the X-ray rocking curve measurements, Al-content (26%) of AlGaN/GaN HEMT structures was confirmed. Three cap layers such as *i*-GaN, *n*-GaN and *p*-GaN layers were grown at 1180 °C and the InGaN was grown at 860 °C. The indium content of the grown InGaN is ≅ 5%. The *n*-GaN and *p*-GaN cap layers were doped with Si and Mg at a level of 4 x 10^{18} and 1 x 10^{18} cm^{-3}, respectively. No explicit Mg activation was needed since the sample was cooled down in nitrogen after the growth.

The device mesa isolation was accomplished by dry etching down to the *i*-GaN of HEMT structure by BCl_3 plasma reactive ion etching [12]. A 100 nm-thick SiO_2 dielectric film was used as a mask, which was deposited on the dry etched samples using EB evaporation. The openings of ohmic and gate metals were formed by etching the SiO_2 using buffered HF solution with photolithography. The ohmic contact was made by the deposition of Ti/Al/Ni/Au (15/72/12/40 nm), which was subsequently alloyed at 775 °C for 30 s in N_2 atmosphere by lamp annealing system [10,11].

2. Electrical, Structural, Optical, Surface, and Device Characterization

The grown device structures electrical properties were measured using Hall Effect measurements with van der Pauw configuration at 300 K and 77 K. Hall measurements were also performed at different temperatures (8 to 300 K) on SiC-based AlGaN/GaN structures. Photoluminescence (PL) measurements were carried out at 77 K using a 10 mW, 325.5 nm CW He-Cd laser as an excitation source [3]. To check the crystalline quality and Al-content of the grown $Al_xGa_{1-x}N$/GaN HSs, (0004) and $(20\bar{2}4)$ crystallographic reflections HRXRD rocking curve measurements were performed by Philips X'pert X-ray diffractometer [3]. The surface properties of respective device structures were measured using Atomic Force Microscopy (AFM) with the scan area of 1x1 μm^2, 3x3 μm^2 and 5x5 μm^2. To measure the thickness of recess etching, AFM measurements [14] were made with the scanning area of 1 μm^2.

To find out the Schottky parameters of as-deposited and further annealed samples, Current-voltage (*I-V*) and capacitance-voltage (*C-V*) measurements were carried out using HP4145B semiconductor parameter analyzer and HP4845A inductance, capacitor and resistance (LCR) meter respectively. The *dc* current-voltage (I_{DS}-V_{DS}) characteristics were measured under dark using HP4145B and Agilent 4156c semiconductor parameter analyser. To measure the 2DEG charge carrier density as a function of channel depth, C-V measurements were carried out at 1 MHz on Schottky diodes using HP4845A LCR meter. The device ON-state and OFF-state breakdown voltage (*BV*) characteristics of the devices were carried out under dark using Sony-Tektronix 370A curve tracer and Agilent 4156c semiconductor parameter analyzer. To check

the high temperature suitability of HEMTs on sapphire and SiC substrates, dc I_{DS}-V_{DS} characteristics were performed at temperatures between 25 to 500°C with an increment of 50°C in N_2 ambient using HP4145B and Agilent 4156c semiconductor parameter analyser.

The *dc* and small frequency 120 Hz sinusoidal wave superimposed *dc* I_{DS}-V_{DS} characteristics (hereafter, called as ac measurements) of the fabricated devices were performed using Sony Tektronix 370A high-resolution programmable curve tracer. To observe the drain current (I_D) collapse of the devices, the ac characteristic of AlGaN/GaN HEMTs on 2-inch sapphire and SIC substrates were carried out at different drain sweep-voltages (V_{DS}) of 0-4 V, 0-8 V, 0-12 V, 0-15 V and 0-20 V. To obtain thermally-activated deep traps, dc I_{DS}-V_{DS} characteristics were measured at different temperatures (25 to 500 °C in a step of 50 °C) [5]. The ac I_{DS}-V_{DS} characteristics were carried out at different drain sweep voltages (V_{DS}=0-8, 0-12, 0-15, 0-20, 0-25 and 0-30 V) for un-passivated and surface passivated AlGaN/GaN HEMTs using Tektronix 370A curve tracer [9]. For the confirmation of trapping-effects, I_{DS}-V_{DS} characteristics were carried out under white light illumination using Agilent 4156c semiconductor parameter analyzer. For the cap layered AlGaN/GaN HEMTs, ac characteristics were carried out with different drain sweep voltages (V_{DS}=0-4, 0-8, 0-12, 0-15, 0-20, 0-25, 0-30, 0-35 and 0-40 V). Drain current transient characteristics were also carried out using Agilent 4156c parameter analyzer for a fixed V_{DS}=10V and V_g=0V [11].

3. Result and Discussions

3.1. GaN and AlGaN Schottky Diodes

Fig. 8 shows the typical forward-bias log(I)-V characteristics of Ag, Ti, Au, Pd and Ni Schottky contacts on $Al_{0.11}Ga_{0.89}N$. The barrier height ($q\phi_b$) and ideality factor (n), were determined using the equation

$$I = AA^{*}T^{2}\exp\left(\frac{-q\phi_b}{k_BT}\right)\exp\left[\left(\frac{qV}{nk_BT}\right)-1\right] \qquad (1)$$

Where A is the diode area, and A^* is the Richardson constant (26.4, 29.34 $Acm^{-2}K^{-2}$ were used for GaN and $Al_{0.11}Ga_{0.89}N$ [1,17] respectively). The C-V barrier height and donar density can be determined using the equation,

$$\left(\frac{A}{C}\right)^2 = \frac{2\left(V_{bi} - V - \frac{k_BT}{q}\right)}{q(\varepsilon_o K_s N_d)} \qquad (2)$$

Where N_d is the donar density. The barrier height is defined by $q\phi_b=q(V_{bi}+V_o)$, where $V_o = k_BT/q \ln(N_c/N_d)$, and $V_{bi}=V_i+k_BT/q$. V_i is the intercept voltage that can be extracted from $(A/C)^2$ versus V plot. N_c ($2.55\text{x}10^{18}$ cm^{-3} for GaN and $3.03\text{x}\ 10^{18}$ cm^{-3} for $Al_{0.11}Ga_{0.89}N$ [1,17]) is the effective density of states in conduction band. The donar density $N_d=2/(q\varepsilon_o K_s$ slope) can be calculated from the slope of $(A/C)^2$ versus V plot. The effective dielectric constant (K_s) of $Al_{0.11}Ga_{0.89}N$ (11.64) was calculated based on the values of GaN (9.1) and AlN [17]. C-V based N_d values are $2.45\text{x}\ 10^{16}$ cm^{-3} for GaN and $2.10\text{x}10^{16}$ cm^{-3} for $Al_{0.11}Ga_{0.89}N$.

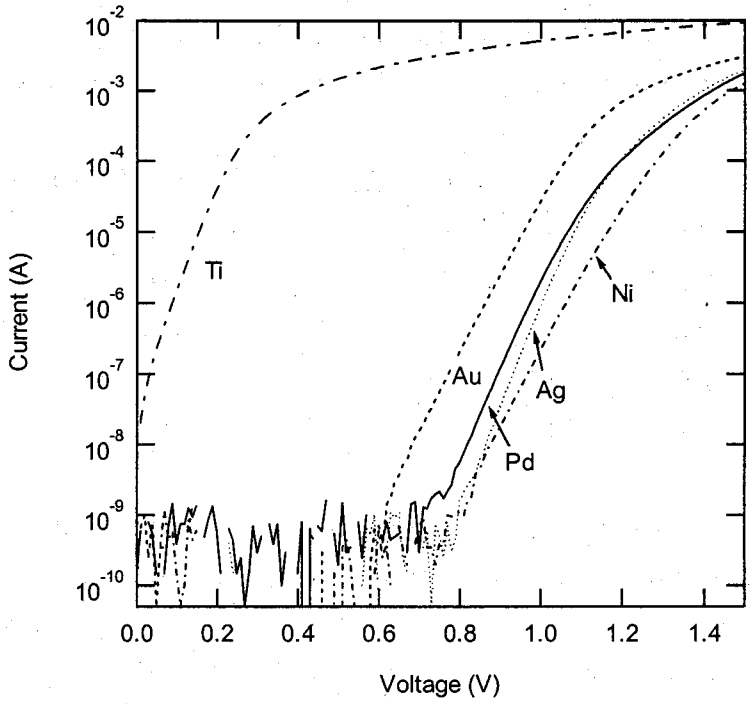

Fig. 8. Forward-bias log (I)-V *characteristics of Ag, Ti, Au, Pd and Ni Schottky contacts on* $Al_{0.11}Ga_{0.89}N$

Table I summarizes the Ag, Ti, Au, Pd, and Ni Schottky parameters observed from both I-V and C-V measurements. Each data given in table I was an average of individual 4-5 Schottky contacts. The standard deviation was about 0.03-0.04. The ideality factor (Table I) indicates that thermionic emission is the primary transport mechanism in these diodes. So the barrier height deduction from ln(I) vs. V plot is reasonably well. The series resistances of all the metal contacts were found to be about 35 - 200 Ω. The Schottky barrier height of GaN and $Al_{0.11}Ga_{0.89}N$ obtained from both I-V and C-V were increasing with metal work function (Φ_M) except Ag Schottky contacts. With respect to Schottky theory, Ag has to give low barrier height values. However, silver Schottky contacts on both GaN and $Al_{0.11}Ga_{0.89}N$ exhibit high barrier height values (Table I). Kampen and Monch [18] using Metal-Induced-Gap-State (MIGS) and electro negativity model explained the higher value of barrier height for Ag. Ti Schottky contacts of both GaN and $Al_{0.11}Ga_{0.89}N$ were showing small barrier height values compared with other Schottky contacts. Some authors have not found Ti Schottky contact on GaN [19]. C-V barrier height values were higher than the I-V barrier height values for both GaN [19] and $Al_{0.11}Ga_{0.89}N$ [20] Schottky contacts. The difference between I-V and C-V barrier height was about 0.07 - 0.25 eV for all the metal contacts except for Ag Schottky contacts (0.02 – 0.72 eV). The large difference in I-V and C-V barrier height values may be due to the presence of oxide interfacial layer at the Metal/GaN interface [20]. All the metal Schottky contacts of n-GaN were showing higher barrier height

compared with other reported values [19]. This variation may be depends on processing condition. The Ni/$Al_{0.11}Ga_{0.89}N$ Schottky barrier height values are in agreement with the reported values [21].

Table I. Metal work function (Φ_M), Ideality factor (n) and Barrier height (ϕ_b) values of Ag, Ti, Au, Pd and Ni Schottky contacts on GaN and $Al_{0.11}Ga_{0.89}N$. *All data in the table are average values of 4-5 diodes. The standard deviation was about 0.03-0.04.

Metal*	Φ_M (eV)	n		$q\phi_b$(I-V) (eV)		$q\phi_b$(C-V) (eV)	
		GaN	$Al_{0.11}Ga_{0.89}N$	GaN	$Al_{0.11}Ga_{0.89}N$	GaN	$Al_{0.11}Ga_{0.89}N$
Ag	4.26	1.34	1.19	0.89	1.12	1.61	1.14
Ti	4.33	1.29	1.10	0.63	0.60	0.8	0.67
Au	5.1	1.46	1.26	0.91	0.93	1.05	1.13
Pd	5.12	1.35	1.27	0.93	0.95	1.14	1.15
Ni	5.15	1.25	1.38	0.96	0.97	1.18	1.22

The S($=d\phi_b/d\Phi_M$)-parameter values were calculated from the I-V and C-V barrier heights and its individual metal work functions (Table I). The S-parameter variation between I-V and C-V is bit high for $Al_{0.11}Ga_{0.89}N$ Schottky contacts compared with GaN Schottky contacts. The S-parameter values 0.38 and 0.44 from I-V and 0.41 and 0.63 from C-V were extracted for GaN and $Al_{0.11}Ga_{0.89}N$ respectively. S-parameter from I-V barrier height is in agreement with the reported value [19]. S-parameter values of $Al_{0.11}Ga_{0.89}N$ are the first reported value in the literature. The variation of S-parameter values are mainly depends on the process of Schottky contact fabrication. The Cowley-Sze model gives an uniform density of surface states $D_s=(1-S)\varepsilon_i/Sq^2t_i$, suggesting that deviation of S from the ideal Mott-Schottky value of unity is an indicator of the density of gap states on the initial surface. Where t_i is the interfacial layer thickness and ε_i is the permittivity of the interfacial layer. With the assumptions of Cowley and Sze, the D_s value calculations were completed. The calculated density of surface state values of GaN and $Al_{0.11}Ga_{0.89}N$ were 1.63×10^{13} states/cm^2/eV (I-V), 1.44×10^{13} states/cm^2/eV (C-V) and 1.27×10^{13} states/cm^2/eV (I-V), 5.87×10^{12} states/cm^2/eV (C-V) respectively. The value of D_s for GaN (I-V) is in good agreement with the reported value 1.77×10^{13} states/cm^2/eV [19]. The calculated D_s value of AlGaN (5.87×10^{12} states/cm^2/eV) is much less than that of n-GaN (1.44×10^{13} states/cm^2/eV; 1.77×10^{13} states/cm^2/eV)[2)], Si, GaP (both 2.7×10^{13} states/cm^2/eV)[2)] and GaAs (1.25×10^{14} states/cm^2/eV). From the above results, it is clear that the degree of surface pinning of the Schottky barrier on n-GaN and n-$Al_{0.11}Ga_{0.89}N$ were expected to be much less than that of GaAs, GaP and Si, but n-GaN and n-$Al_{0.11}Ga_{0.89}N$ may be similar to CdS.

3.2. Annealing effects in AlGaN Schottky Diodes

I-V characteristics of Ti, Pd and Ni Schottky diodes as a function of annealing temperatures (100, 200, 300, 400, 450 and 500 °C for different annealing time) are shown in Fig. 9 a), b) and c). For thermionic emission ($V>3\ k_bT/q$), the general diode equations are

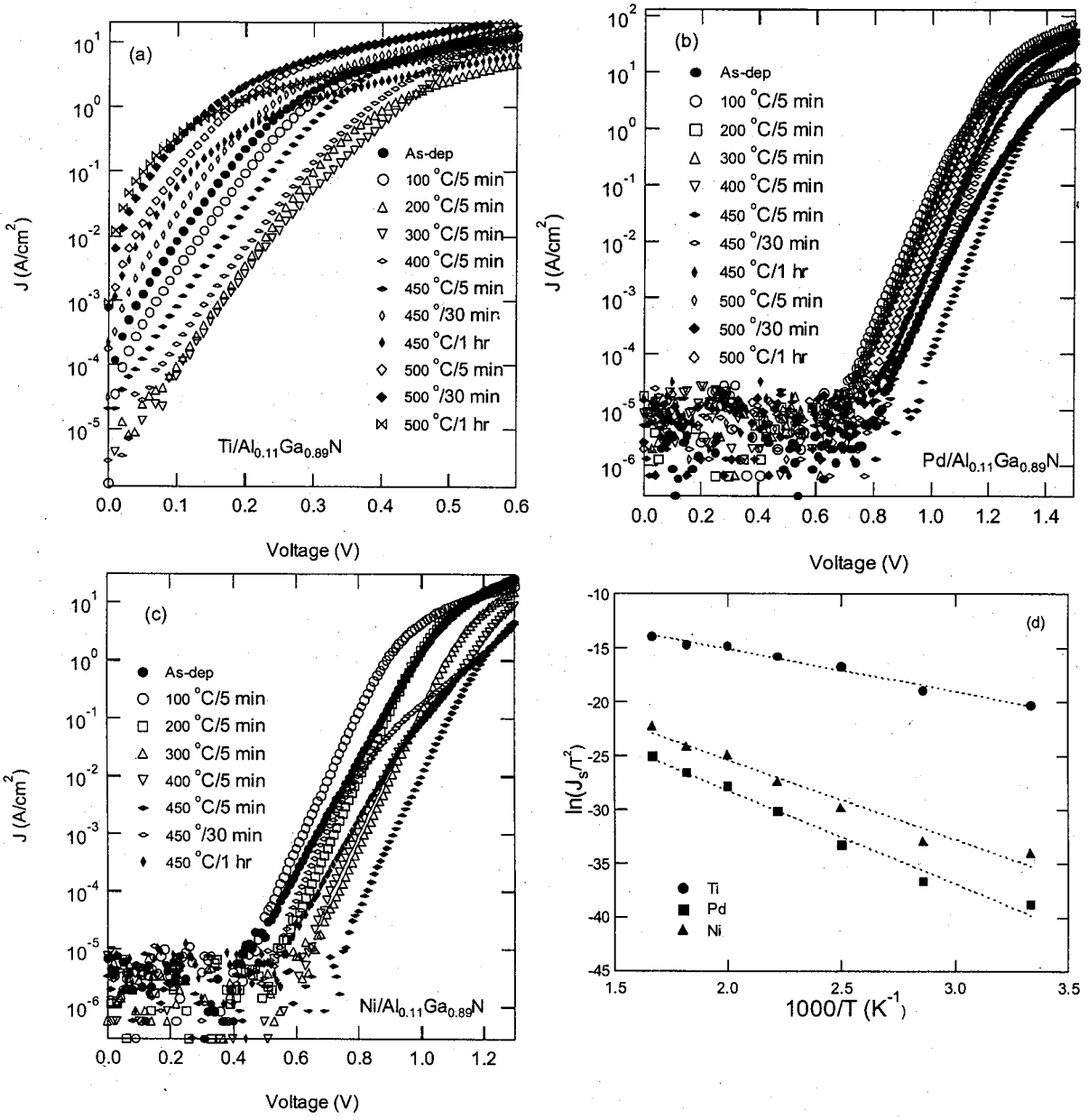

Fig. 9. Forward J-V characteristics of (a) Ti/n-$Al_{0.11}Ga_{0.89}N$, (b) Pd/n-$Al_{0.11}Ga_{0.89}N$ and (c) Ni/$Al_{0.11}Ga_{0.89}N$ Schottky diodes as a function of annealing temperatures. (d) A plot of $\ln(J_s/T^2)$ as a function of $1000/T$ derived from the forward-biased *I-V* characteristics.

$$I = I_s \exp\left(\frac{qV}{nk_BT}\right) \qquad (3)$$

$$I_s = AA^*T^2 \exp\left(\frac{-q\phi_b}{k_B T}\right) \qquad (3a)$$

Where I_s the saturation current density, n the ideality factor, k_B Boltzmann constant, T the absolute temperature, A is the contact area, A^* is the effective Richardson constant, and ϕ_b is the barrier height. The current axis intercept for the straight-line portion of the semi-log plot at V=0 is given by I_s. The barrier height ϕ_b is calculated from I_s in equation (4)

$$\phi_b = \frac{k_B T}{q} \ln\left(\frac{AA^*T^2}{I_s}\right) \qquad (4)$$

The A^* value 29.34 $Acm^{-2}K^{-2}$ were used for $Al_{0.11}Ga_{0.89}N$ [22]. The ideality factor n has been calculated from the slope of the semi-log plot [ln(I) vs V plot]. The effective barrier height and Richardson constant of fabricated Schottky diodes can be calculated using the equation (3a). Richardson plot [ln(J_s/T^2) vs 1000/T] of Ti, Pd and Ni Schottky contacts are shown in Fig 9 (d). The low barrier height and small Richardson constant (A^*) found by the I-V-T method are the possibility of non-uniform current distribution in the diodes [23]. The non-ideal behavior is probably due to surface defect, which leads to in-homogeneities in the transport current. After thermal treatment at 300 °C, I-V measurements were also carried out at room temperature. Improved barrier height (parentheses values) has been observed on the 300 °C treated Schottky diodes (Table II). This may be due to the interfacial reaction between metal and semiconductor contacts [24].

C-V measurements of the Ti, Pd and Ni Schottky contacts were also conducted as a function of annealing temperature. The C-V barrier height and donar carrier density can be determined

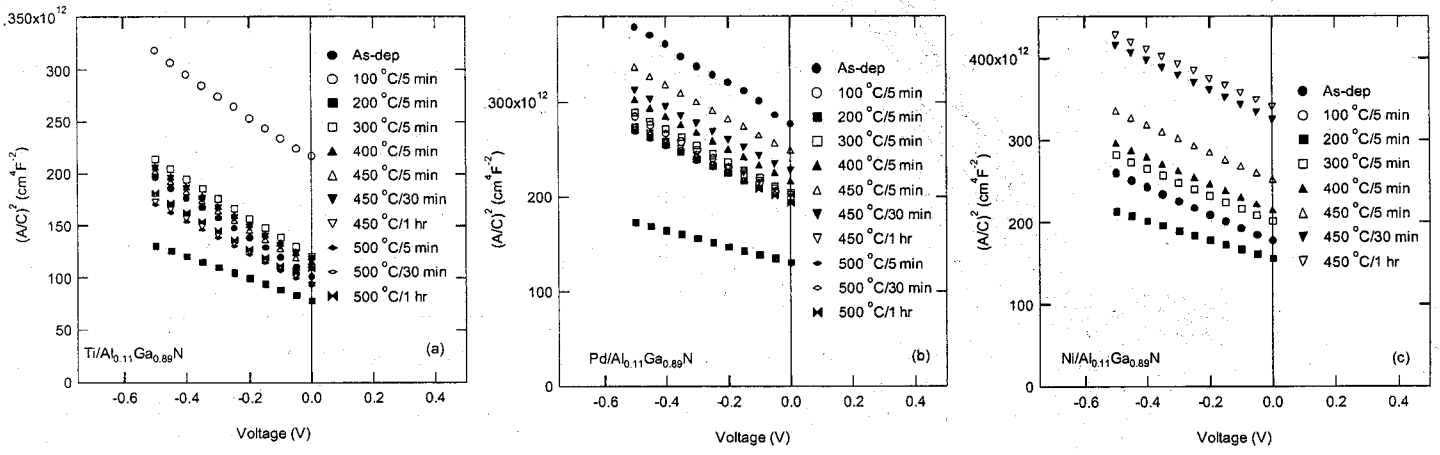

Fig. 10. (A/C)² Vs V plot for (a)Ti/n-$Al_{0.11}GaN_{0.89}N$ (b) Pd/n-$Al_{0.11}GaN_{0.89}N$ and (c) Ni/n-$Al_{0.11}GaN_{0.89}N$ Shottky diodes as a function of annealing temperatures

using the equation (2). Fig. 10 a), b) and c) show the $(A/C)^2$ vs. V plot for the as-deposited and annealed Ti, Pd and Ni Schottky diodes respectively. C-V measured doping carrier density value of $Al_{0.11}Ga_{0.89}N$ is in the range of $2.1x10^{16} - 3.3 \times 10^{16}$ cm^{-3} [1].

Schottky parameters from I-V and C-V measurements of as-deposited and annealed Ti, Pd and Ni/n-$Al_{0.11}Ga_{0.89}N$ Schottky diodes are shown in Fig. 11 and Table II and III. The data in the

tables are the average value from 4-5 diodes. As generally known, chemical reactions between metal and semiconductor can substantially influence the electrical properties of metal-semiconductor contact. C-V barrier height values are higher than the I-V barrier heights of as-deposited and annealed Schottky diodes. The reason might be partly due to the image-force barrier lowering effect. Many authors have observed the same behavior [1, 25-28].

In the case of Ti Schottky diodes, the Schottky barrier height (I-V) increases with the annealing temperature up to 350 °C/5 min and further the barrier height decreases with the increase of annealing temperatures 400 °C/5 min – 500 °C/1 hr (Fig 11). The value of ideality factor is also nearly equal to 1.0 for 100 – 200 °C/5 min annealed Ti diodes. The increase of barrier height and decrease of ideality factor with annealing temperature are due to the intimate Ti contact with AlGaN layer (Fig. 11). This behavior has also been reported for Ti contacts on *n*-GaN [24]. No considerable macroscopic interfacial changes were observed up to 450 C/1 hr (Fig. 12). Hirch et al [24] observed no considerable macroscopic interfacial changes on Ti/GaN interface using Rutherford Backscattering Spectroscopy (RBS) up to the annealing temperature 230 °C. The increase of C-V barrier height has also been observed up to the annealing temperature 150 °C/5 min, after that the barrier height gradually decreased with the annealing temperature. The Schottky parameters of annealed diodes at different temperatures with different times are shown in Table III. From the table III, I-V barrier height of Ti Schottky diode decreases with the increase of annealing time at both 450 °C and 500 °C. However, not much change has been observed in ideality factor. C-V barrier height of the Ti diode increases for 450 °C/30 min annealing, and then decreases for 450 °C/1 hr annealing time.

Table II. Calculated Schottky parameters of Ti, Pd and Ni/n-$Al_{0.11}Ga_{0.89}N$ Schottky diodes from I-V, I-V-T and C-V measurements. Values within the parenthesis: 300 °C thermal treated Schottky diode parameters measured at room temperature.

Metal	Φ_M (eV)	n	ϕ_b(I-V) (eV)	ϕ_b(C-V) (eV)	ϕ_b(I-V-T) (eV)	A^* (A/cm^2F^2)
Ti	4.33	1.10 (1.24)	0.60 (0.70)	0.67	0.62	0.02[
Pd	5.12	1.27 (1.30)	0.95 (1.23)	0.98	0.93	0.0007
Ni	5.15	1.38 (1.34)	0.97 (1.09)	1.22	0.91	0.0006

Table III. Schottky barrier height (I-V & C-V), Ideality factor and reverse bias voltage at fixed reverse leakage currents (10 mA for Ti diode; 4 nA for Pd diode; 0.1 nA for Ni diode) of Ti, Pd and Ni/n- $Al_{0.11}Ga_{0.89}N$ Schottky diodes as a function of annealing temperatures (450 °C/ 30 min, 450 °C/1 hr, 500 °C/30 min and 500 °C/1 hr)

T (°C)	ϕ_b (*I-V*) (eV)			ϕ_b (*C-V*) (eV)			n			Reverse voltage (volts)		
	Ti	Pd	Ni	Ti	Pd	Ni	Ti	Pd	Ni	Ti	Pd	Ni
As-deposited	-See table II-									12.4	7.2	10.3
450/5 min	0.66	1.34	1.17	0.79	1.55	1.66	1.1	1.39	1.49	13.2	30	27.5
450 /30 min	0.57	1.28	1.06	0.96	1.47	1.95	1.13	1.38	1.40	12.9	24.9	28.4
450 /1 hr	0.55	1.24	1.01	0.74	1.58	2.10	1.11	1.41	1.76	12.2	22.2	30.0
500/5 min	0.53	1.21	**	0.74	1.46	**	1.17	1.34	**	11.5	16	**
500 /30 min	0.50	1.27	**	0.71	1.38	**	1.14	1.34	**	8.9	21	**
500 /1 hr	0.49	1.23	**	0.79	1.39	**	1.15	1.35	**	6.5	21	**

For Pd and Ni Schottky diodes, increase of I-V and C-V barrier heights with annealing temperatures were observed (Fig. 10). There was a sudden increase of C-V barrier height of Pd and Ni diodes for the annealing temperatures 200 °C/5 min and 250 °C/5 min. The same behavior was observed at 100 °C/5 min and 150 °C annealed Ti diodes [24]. Increase of C-V barrier height may be due to the change of effective dielectric constant due to annealing. Not much I-V barrier height changes with annealing temperature have been observed for Ni Schottky diodes (Fig. 11). C-V barrier height of Ni diodes increased (1.47 – 2.1 eV) for 400 °C/5 min – 450 °C/1 hr annealing temperatures. This increase of barrier height might be due to the intimate contact between metal and semiconductor [24]. AES spectrum (Fig. 12) reveals that no macroscopic interfacial reaction has been observed from

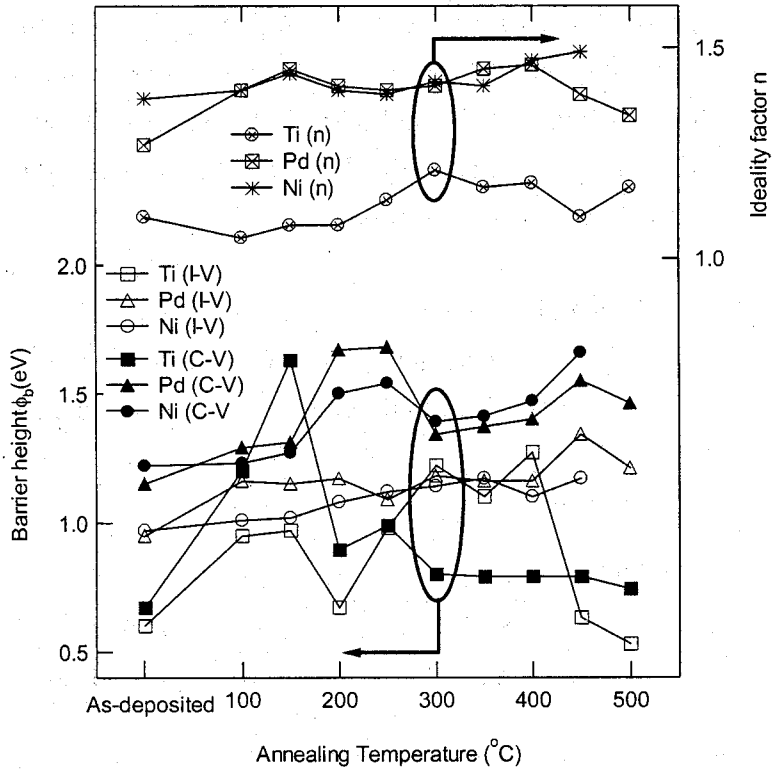

Fig. 11. A plot I-V and C-V barrier height and Ideality factor of Ti, Pd and Ni/n- $Al_{0.11}Ga_{0.89}N$ as a function of annealing temperature (°C). Annealing time is 5 min for each temperature.

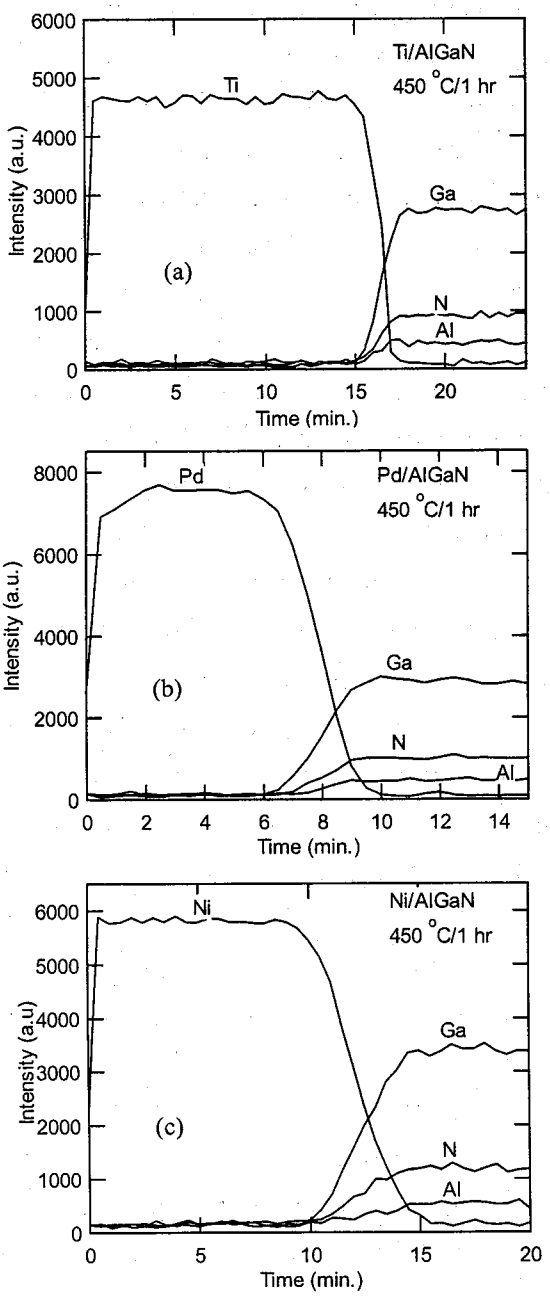

Fig. 12. Auger electron spectroscopy of 450 °C/1 hr annealed (a) Ti, (b) Pd and (c) Ni/$Al_{0.11}GaN_{0.89}N$ contacts

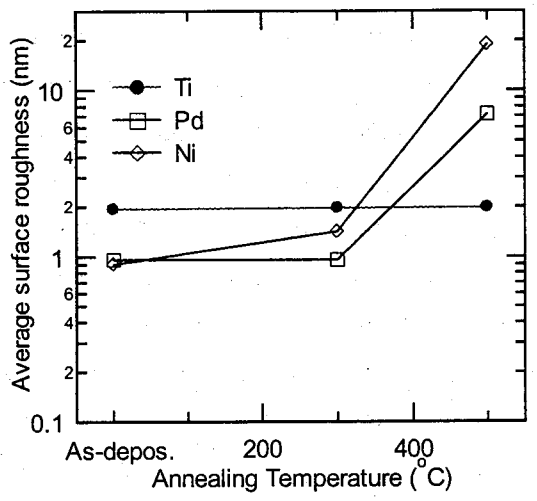

Fig.13. Average surface roughness with different annealing temperaturure of Ti, Pd and Ni/n-$Al_{0.11}GaN_{0.89}N$ Schottky diodes

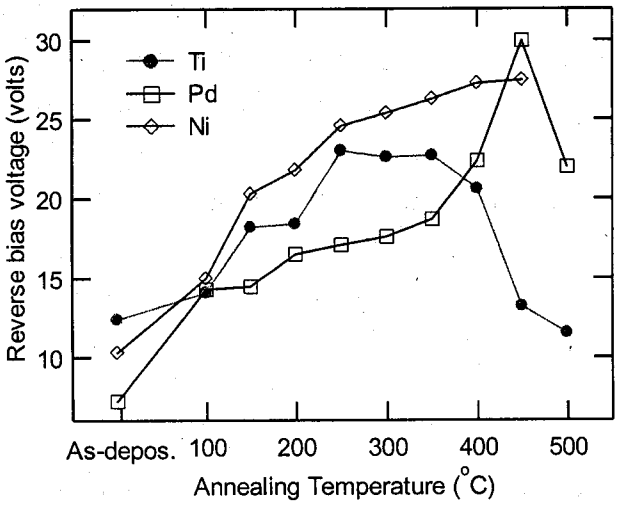

Fig. 14. Reverse bias at particular reverse leakage current (10 mA for Ti diodes; 4 nA for Pd diodes; 0.1 nA for Ni diodes) of Ti, Pd and Ni/n-$Al_{0.11}Ga_{0.89}N$ Schottky diodes as a function of annealing temperature (C). Annealing time is 5 min for each temperature.

metal-semiconductor interfaces. This leads to the ceramic behavior of AlGaN surface [29]. Annealed Pd Schottky diodes are showing higher I-V and C-V barrier height values. The change in ideality factor for Ti and Ni Schottky diode are comparably small with Pd diodes. This means, the thermionic emission is dominant for Ti and Ni Schottky diodes. Rectifying behavior of Ti and Pd Schottky diodes were observed up to the temperature 500 °C for 1 hr annealing time [Fig. 9 (a) and (b)]. I-V barrier height of Pd Schottky diode decreases with annealing time (5 min – 1 hr) for 450 °C. However, not much change was observed on ideality factor in 500 °C annealed samples.

C-V barrier height of Ni Schottky contact increases with annealing time for 450 °C. However, no rectifying characteristics have been observed for 500 °C annealed Ni Schottky diodes (Table II). This increase of barrier height with annealing time leads the dielectric constant of the material. The rectifying behavior of Ni Schottky diodes was observed only up to the temperature 450 °C for 1 hr annealing time (Table III). The failure of rectifying behavior at high temperature annealing may be due to the interfacial reaction between Ni and AlGaN layers. Liu etal [29] has observed that the Ni/n-GaN Schottky diodes were rectifying up to the annealing temperature 600 °C for 1 hr.

Increase of surface roughness was observed for both Pd and Ni Schottky diodes with annealing temperature. The average roughness value of 500 °C annealed Ni (18.89 nm) diodes was one order high as compared with Pd (7.22 nm) and Ti (1.98 nm) diodes (Fig. 13). The increase of surface roughness may be because of island formation [28,30] due to thermal annealing. Not much average roughness changes have been observed for Ti Schottky diodes with annealing temperature when compared with Pd and Ni Schottky diodes. From this we understand that not much island formation on the surface of Ti Schottky diodes due to annealing. The formation of island might be high for Ni diode when compared with Pd and Ti diodes. No macroscopic interfacial reaction has been observed on the annealed diodes (Fig. 12). From this, we understand that AlGaN surface has ceramic like behavior with both Pd [28] and Ni than semiconductor. Duxtard etal [30] reported that Pd surface morphology become rougher and de-laminated from GaN after annealing at 725 °C for 1 hr. However, no de-lamination has been observed on Pd/$Al_{0.11}Ga_{0.89}N$ interface even after 900 °C/5 min annealing [28].

Reverse bias voltage (RV) of Schottky diodes were noted for a fixed reverse leakage current 10 mA for Ti diodes, 4 nA for Pd diodes and 0.1 nA for Ni diodes. RV of Ti Schottky diode increases up to the annealing temperature 250 °C/5 min, and then it decreases gradually with the increase of annealing temperature (Fig. 14 & Table III). RV for Pd diode gradually increases with annealing temperatures up to 450 °C/5 min and it gradually decreases with higher annealing temperatures. But RV for Ni diode gradually increases with annealing temperatures up to 450 °C/1 hr. After that, the characteristics went bad due to thermal annealing. Highest reverse voltage (30 V) has been observed for both Pd (450 °C/5 min) and Ni (450 °C/1 hr) diodes. The increase of reverse voltage with annealing temperature may be attributed to the intimate contact between metal and semiconductor. The same behavior was observed on indium tin oxide/n-GaN Schottky diodes [31]. The RV of Ti and Pd Schottky diodes decreases at a particular leakage current with annealing time for both 450 and 500 °C. However, Ni Schottky diode RV increases with annealing time (5 min-1 hr) for 450 °C. From these experimental results, we found that the Pd and Ni are suitable Schottky metal for high temperature operating AlGaN/GaN HEMTs.

3.3. AlGaN/GaN HEMTs on 2-inch SI-SiC Substrate

Hall measurements show mobilities of 1281 and 5474 cm^2/Vs and sheet carrier densities of $1.2x10^{13}$ and $1.1x\ 10^{13}\ cm^{-2}$ at room temperature and 77 K, respectively. Due to such a high value of $n_s\mu_H$=$1.54x10^{16}$/Vs, the grown AlGaN/GaN heterostructures will be able to give high-current-density devices. 2-DEG channel carrier density of $4\ x\ 10^{19}\ cm^{-3}$ was measured at a depth of 17.75 nm using C-V measurements (Fig. 15).

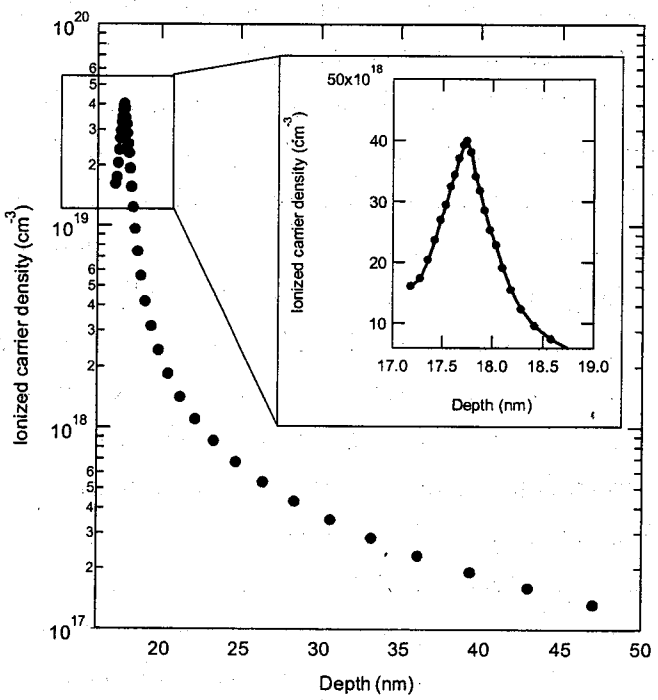

Fig. 15. Ionized carrier density profile of 150-um-diameter Schottky diodes, which are fabricated on a AlGaN/GaN HEMT structure on SI-SiC

Good current-voltage (I_{DS}-V_{DS}) characteristics of a 2.2-μm-gate-length and 15- μm-gate-width HEMTs are shown in Fig. 16, and exhibit a maximum current density of 867 mA/mm and a peak extrinsic transconductance of 287 mS/mm. The device dimensions are as follows: L_{sd}=8.5 μm; W_g=15 μm; L_g=2.2 μm and L_{sg}=2.2 μm. The gate source voltage ranges from –3.0 to 1.5 V in steps of 0.5 V. The I_{DS}-V_{DS} characteristics are noteworthy for their minimal current decrease at large dissipation levels due to self-heating. Due to the excellent thermal conductivity of the SiC substrate, the

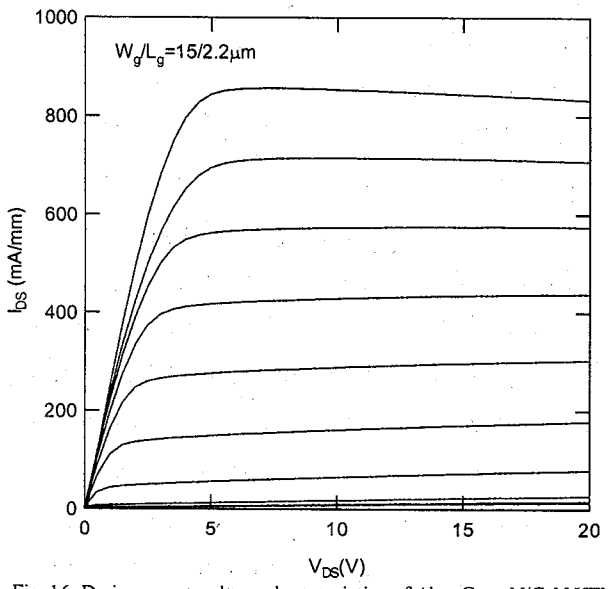

Fig. 16. Drain current-voltage characteristics of $Al_{0.26}Ga_{0.74}N$/GaN HEMT's on SI-SiC substrate. Top trace was at V_g=+1.5 V and step was -0.5 V.

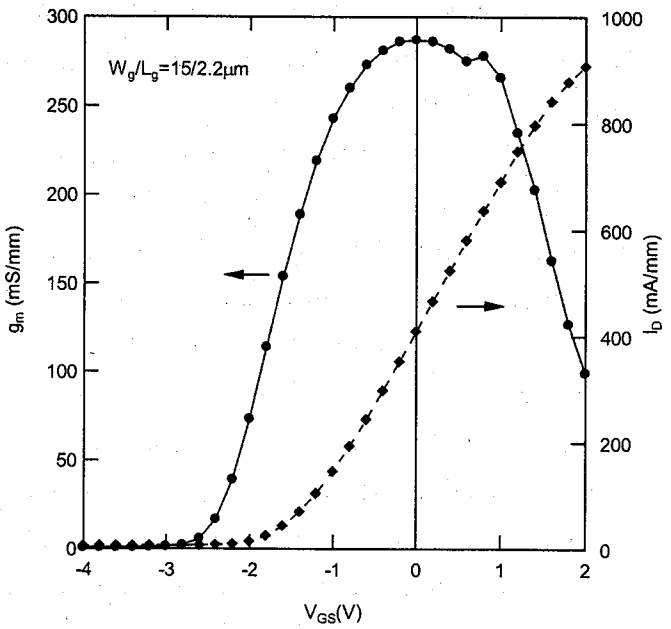

Fig. 17. Transfer characteristics of AlGaN/GaN HEMTs on SI-SiC

current density of both 15- and 200-μm-wide devices decreases during the sweep by only 3% when the drain bias is increased to 20 V. A one order higher percentage (13%) of drain-source current reduction has been observed in 200-μm-wide HEMTs on sapphire substrates. Thus, we understand that the device self-heating effect is small for devices on SiC substrates compared with devices on sapphire substrates, because SiC substrates have a high value of thermal conductivity (4.9 W/cm-K). The device threshold voltage values are reported between –2.4 to –2.7 V. Khan et al. [32] have achieved the highest reported threshold voltage (-9.0 V) from SiC-grown AlGaN/GaN HFETs. Large-gate-width (200 μm) HEMTs gave a maximum extrinsic transconductance of 216 mS/mm with drain-source current density of 635 mA/mm. The ohmic contact for this wafer resistance, measured on a transmission line model (TLM), ranged from 1.8 to 2.6 Ω-mm depending on the wafer location. This value is higher than desired and degrades the performance of the devices. The presented I_{DS}-V_{DS} characteristics are better than those reported by Vescan et al.[33] Moreover, the peak transconductance was observed at a gate voltage of approximately -4.5 V. In the case of higher gate voltages region, the transconductance values are small [33] however, our devices show high transconductance values for a range of gate voltages.

Fig. 17 shows the transfer characteristics of 15-μm-wide and 2.2-μm-gate-length HEMTs. The peak transconductance at a gate voltage of 0 V is 287 mS/mm with a drain-source current density of 467 mA/mm for the applied drain-source voltage of +6.0 V. To our knowledge, this is the highest transconductance value recorded for 2.2-μm-gate-length $Al_{0.26}Ga_{0.76}N$/GaN HEMTs grown on a SI-SiC substrate. The extrinsic transconductance values reported here are high compared to previously reported values [33-37]. We have observed high transconductance values even for 2.2-μm-gate-length devices. However, the drain-source current density values for 15-μm-gate-width devices are lower than previously reported values [3,34,37,38]. This is due to the high value of contact resistance (2.3 Ω-mm), which was measured using a transfer length method (TLM). We have also measured the source resistance (R_s) of the device to be 1.59 Ω-mm.

The device extrinsic transconductance values depend on the quality of the AlGaN/GaN heterostructure, intrinsic transconductance values and source resistance values. The intrinsic transconductance (g_{m0}) of the devices were calculated from the expression $g_{m0}=g_m/(1-R_s g_m)$. The calculated intrinsic transconductance of 15-μm-gate-width HEMTs is 528 mS/mm. Our g_{m0} values are twice the values of the reported g_{m0} values of 258 mS/mm [38]. The crystalline quality of our samples is similar to that reported previously however, the g_{m0} values are higher than the reported values [38]. This may be the reason for such high extrinsic transconductance values. These high dc transconductance value devices will exhibit good small-signal characteristics [39]. Still, more research is required to understand the exact mechanism of obtaining high extrinsic transconductance values. Further improvements are necessary with regard to contact resistance of the devices in order to realize high-power and high-frequency device applications. Studies on

the temperature dependent dc characteristics of the devices are underway. Using sapphire-grown AlGaN/GaN HEMTs lower transconductance values (166 mS/mm) were achieved compared to the SiC-based AlGaN/GaN HEMTs [32,36]. Thus, we realized that the AlGaN/GaN epilayers grown on SI-SiC substrates are of better quality than the epilayers grown on sapphire substrates. The HEMTs on SI-SiC substrates exhibit superior characteristics to HEMTs on sapphire substrates [32,36].

3.4. $Al_xGa_{1-x}N$/GaN HEMTs on 2-inch sapphire

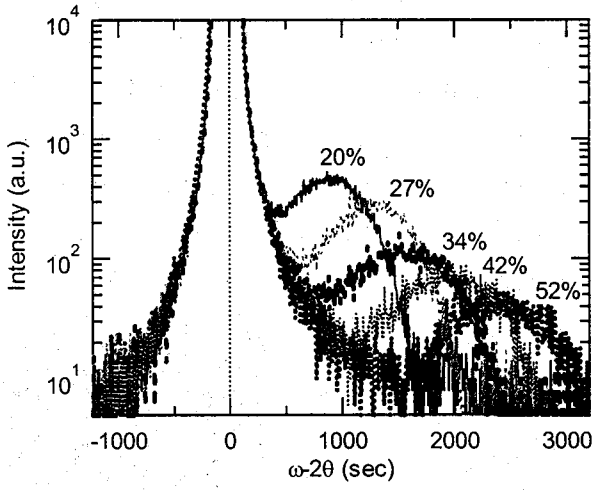

Fig. 18. (0004) reflection X-ray rocking curve of various Al-content AlGaN/GaN HSs.

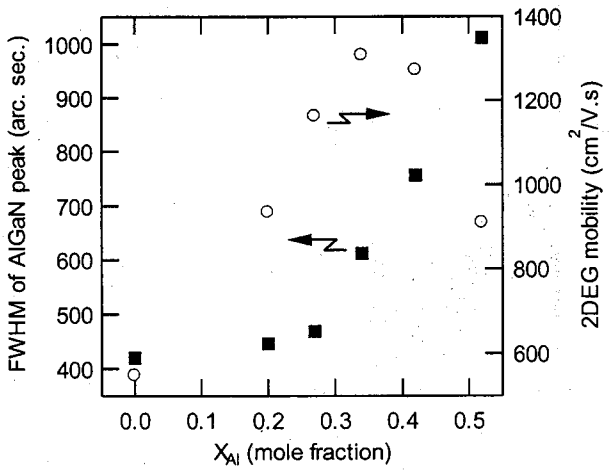

Fig. 19. FWHM of AlGaN (20-24) x-ray reflection peak as a function of Al-content.

The Al-content of the grown $Al_xGa_{1-x}N$/GaN ($0.20 \leq x \leq 0.52$) HSs on sapphire substrate were obtained from (0004) X-ray rocking curve measurements (Fig. 18) using Vegards law [2]. The measured Al-content values are in good agreement with the growth parameters. Figure 19 shows the full width at half maximum (FWHM) of $(20\bar{2}4)$ x-ray reflection peak of AlGaN and a 2DEG mobility of AlGaN/GaN as a function of Al-content. The increase of FWHM values with the increase of Al-content is due to the large lattice mismatch between GaN and $Al_xGa_{1-x}N$. This has been correlated with the dislocation density [16], 2DEG mobility [40-42] and average surface roughness [41]. Fig. 20 shows the 77 K PL spectrum of different-Al-content AlGaN/GaN HSs, which reveals the free exciton (3.491 eV) , free exciton LO (3.408 eV) and donor acceptor pair (3.316 eV) peaks. The e^1_{2DEG}-h peak (3.433 eV) was observed in 52% Al-content HSs. A small hump peak of e^1_{2DEG}-h has also been observed in both 34 and 42% Al-content HSs. The absences of e^1_{2DEG}-h peak in the low-Al-content HSs is possibly due to the low value of conduction band off-set (ΔE_c). Fig. 21 shows the ΔE_c and energy band-gap as a function of Al-content. The

presence of e^1_{2DEG}-h peak in 34, 42 and 52% Al-content is due to the creation of more number of energy levels (because of large conduction band off-set) in the triangular quantum well.

Figure 22 a) shows the AFM pictures of four different-Al-content $Al_xGa_{1-x}N/GaN$ (x=0.20, 0.27, 0.34 and 0.52) HSs. The increase of Al-content leads to the formation of defect and transition into an island growth mode. Keller *etal.*[41] pointed out that, the defects did not form at the AlGaN/GaN interface but developed in a later stage of growth. The defect formation is not very clear at this stage. The increase of island growth with the increase of Al-content has been confirmed. Figure 22 b) shows the root mean square surface roughness (R_{MS}) and peak to valley (P-V) distance of AlGaN/GaN HSs as a function of Al-content. The R_{MS} and P-V distance values of $Al_xGa_{1-x}N$ ($0.20 \le x \le 0.52$) were obtained from 25 and 1 μm^2 scan area AFM pictures, respectively. The increase of R_{MS} value with the increase of Al-content is due to the increase of lattice stress between GaN and AlGaN layers. Also increase of granular size and P-V distance with the increase of Al-content has been observed. Low P-V distances were observed with the increase of AlGaN thickness [43].

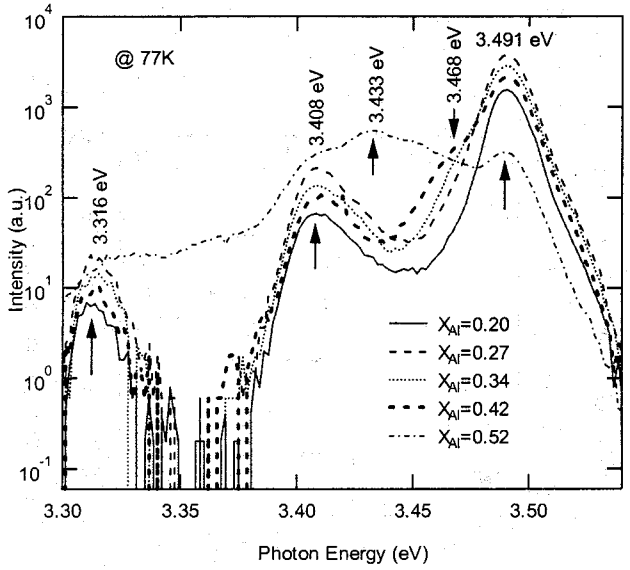

Fig. 20. PL spectrum of $Al_xGa_{1-x}N/GaN$ HSs measured at 77K.

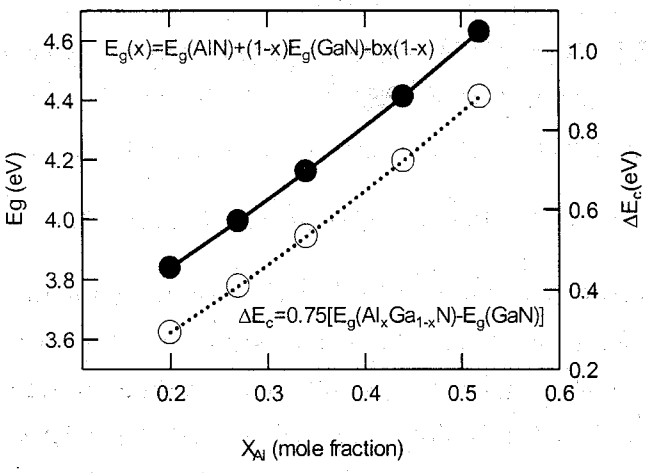

Fig. 21. Energy band gap and conduction band off-set of $Al_xGa_{1-x}N/GaN$ HSs as a function of Al-content.

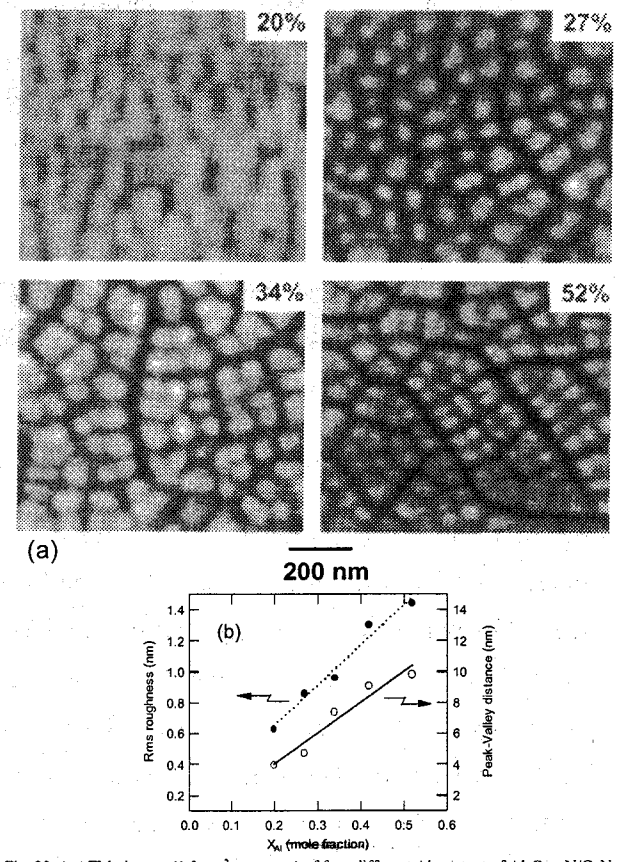

Fig. 22 a). AFM pictures (1.0 μm^2 scan area) of four different Al-content of $Al_xGa_{1-x}N/GaN$ (x=0.20, 0.27, 0.34 and 0.52) HSs. b) Values of surface *RMS* roughness (obtained from 25 μm^2 scan area) and Peak-Valley (P-V) distance (obtained from 1 μm^2 scan area) of AlGaN/GaN HSs as a function of Al-content.

Figure 23 shows the sheet carrier density (n_s), 2DEG mobility measured at 300 and 77 K as a function of Al-contents. The 2DEG mobilities of grown $Al_xGa_{1-x}N$/GaN HSs were 936, 1163, 1310, 1274 and 911 cm^2/Vs for the x values of 0.20, 0.27, 0.34, 0.42 and 0.52, respectively. From the Fig. 23, we understand that the 2DEG mobility increases up to the Al-content of 34% and it slowly decreases for high Al-content HSs. The enhancement of 2DEG mobility is mainly due to the enhanced polarization-induced (spontaneous and piezoelectric polarization) electron confinement in the hetero-interface [44]. Keller *et al.*[41] have observed the highest 2DEG mobility from 30% Al-content HSs. Ambacher *et al.*[42] has also observed the increase of 2DEG mobility with Al-content x of the AlGaN barrier from x=0.24 to x=0.31. At room temperature, the maximum electron mobility is limited by polar phonon scattering. At low sheet carrier densities, impurity and piezo-acoustic scattering diminish the mobility. For higher densities (n_s>1x10^{13} cm^{-2}), these scattering processes are screened, which explains the increase in 2DEG mobility [45]. The decrease of 2DEG at high sheet charges can be explained by the electron "spill over" from quantum well at the HSs in to the localized state in the doped channel [45]. The value of n_s rises approximately linear with x_{Al}, following dn_s/dx_{Al} = 2.01x10^{13} cm^{-2} (Fig. 21). Our results are in close agreement with the earlier reports [45,46]. From this we understand that, donor-like charge densities of the order of 2.01x10^{13} $cm^{-2}.x_{Al}$ are produced at pseudomorphic AlGaN/GaN interfaces, through piezo-electric induction. The low 2DEG mobility value for 44 and 52% Al-content heterostructure are due to the lattice stress, interface roughness [41,42,45,47,48] and alloy scattering [42]. High surface roughness and FWHM of AlGaN $(20\bar{2}4)$ x-ray reflection peak confirms the increase of interface roughness and lattice stress which was observed from AFM measurements (see Fig. 22 a) and b)) and XRD measurements (see Fig. 19), respectively.

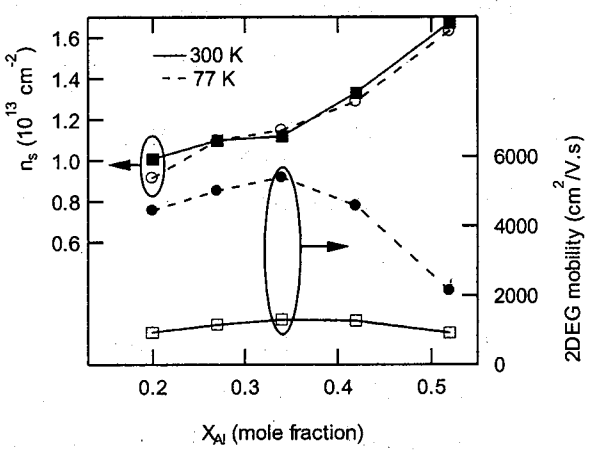

Fig. 23. Sheet carrier density and 2DEG mobility of AlGaN/GaN HSs measured at 300 and 77 K as a function of Al-content.

The high value of n_s comes from both the piezo-induced charge (due to stress in the cap layer) and from the induced polarization field for the Ga terminated surface. The increase of n_s with the increase of Al-content has been confirmed theoretically [49] as

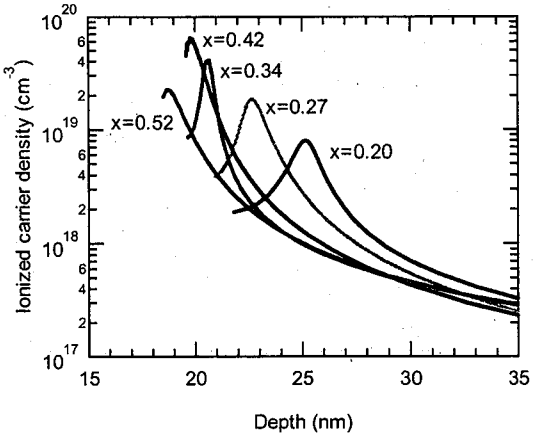

Fig. 24. Ionized carrier density of different Al-content $Al_xGaB_{1-x}N$/GaN HSs measured from C-V measurements.

well as experimentally [41,45,46] by other authors. On the contrary, Ambacher *etal* [42] observed the decreasing trend of n_s for high Al-content HSs. At 77 K, low 2DEG mobility was observed for 42 and 52% Al-content AlGaN/GaN HSs. This is possibly originating from poor interface quality HSs. Highest 300 and 77 K 2DEG mobility was observed on 34% Al-content AlGaN/GaN HSs. This is consistent with other reports [41,42].

The C-V profiling technique allows one to measure the carrier concentration.

$$n_{s(C-V)} = \frac{2}{qK_s\varepsilon_o A^2\left[d\left(1/C^2\right)/dV\right]} \qquad (1)$$

as a function of depth

$$Z_{(C-V)} = \frac{K_s\varepsilon_o A}{C} \qquad (2)$$

Where K_s is a relative dielectric constant of semiconductor, which was calculated based on the values of GaN (=9.5) and AlN(=9.0), ε_o is the dielectric constant of free space, A is the area of the Schottky contact, C is the measured capacitance of the Schottky device and $Z_{(C-V)}$ is the depth measured from C-V. The doping concentration is obtained from a C-V curve by ploting $1/C^2$ versus V and taking the slope $d(1/C^2)/dV$. The doping concentration profile as a function of channel depth at can be determined using the equation (2). Fig. 24 shows the carrier density profile for different-Al-content HSs. 2DEG behaviour has been observed in all Al-content HSs. The carriers are primarily located at AlGaN/GaN interface. As the Al-content decreases, carrier distribution becomes steeper and spreads in to *i*-GaN layer. This can be explained using conduction band-offset (Fig. 21).

Table IV. Maximum drain current density (I_{Dmax}) of 15-μm-wide-gate device, contact resistance (R_c) and sheet resistivity (ρ_{sh}) values of $Al_xGa_{1-x}N$/GaN HEMTs for different Al-content.

x_{Al}	I_{Dmax}		R_c	ρ_{sh}
(mole fraction)	L_g= 2.0 μm	L_g=2.2 μm	(Ω-mm)	(Ω)
0.20	385	350	1.68	620
0.27	440	420	2.06	513
0.34	525	501	2.46	420
0.42	512	489	2.69	400
0.52	500	467	2.89	450

High Al-content AlGaN layer on GaN gives larger conduction band discontinuity (ΔE_c) and enhanced piezo-electric effect with spontaneous polarisation, which improves the carrier confinement, allowing a high 2DEG mobility to coexist with a large carrier density [42,46]. The increase of carrier distribution with the increase of Al-content is due to the increase of surface roughness scattering as a result of 2DEG towards the interface [50]. The reduction of n_s for 52% Al-content HS is possibly due to the reduction of charge screening effect.

The minimum sheet resistivity (ρ_{sh}) for intentionally undoped AlGaN/GaN HSs containing barriers with alloy composition between x=0.20 and 0.34 is determined to be 621 and 420 Ω (see Table IV). The high saturation velocity, high thermal stability, high n_s and low ρ_{sh} values of AlGaN/GaN HSs, make suitable for high-power and high-frequency HEMTs.

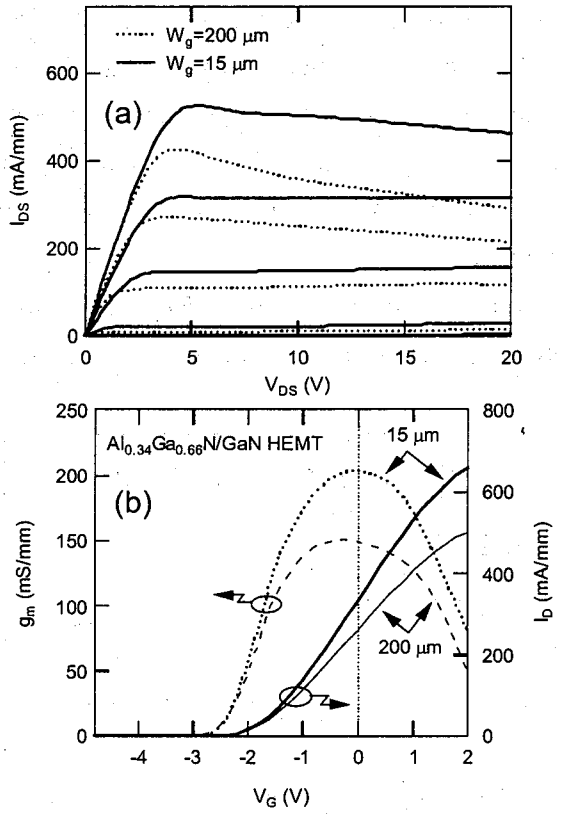

Fig. 25. (a) I_{DS}-V_{DS} characteristics of $Al_{0.34}Ga_{0.66}N$/GaN HEMT structure: Vgs =-3.5 to 1.5 V in steps of 1 V. (b) transfer characteristics of $Al_{0.34}Ga_{0.66}N$/GaN HEMT structure: V_{DS}=6V. Solid lines: Wg=15 mm, Lg=2.0 μm, LSD=10 μm, Lsg= 4 μm; dotted lines: Wg= 200 μm, Lg=2.0 μm, Lsd=5 μm, Lsg= 1.5 μm.

Figure 25 a) and b) shows the 34% Al-content HEMTs I_{DS}-V_{DS} characteristics and transfer characteristics of 15 and 200 μm wide gate devices with 10 and 5 μm source-drain spacing, respectively. The gate to source voltage ranges from -3.5 to 1.5 V in the steps of 1 V. The maximum drain current density (I_{DS}) of 525 mA/mm (V_{DS}=5.4 V) with maximum g_m of 202 mS/mm (V_{GS}=0 V) were observed for 2.0-μm-gate-length and 15-μm-wide gate $Al_{0.34}Ga_{0.66}N$/GaN devices (Fig. 25 b)). This is the highest value reported in the literature for 2.0-μm-gate-length MOCVD grown HEMTs on sapphire substrate. Mishra *etal* [47] demonstrated maximum g_m of 240 mS/mm with maximum I_{DS} of 1130 mA/mm for 0.25-μm-gate-length $Al_{0.5}Ga_{0.5}N$/GaN HEMTs. Table I shows the I_{DS} values of two different gate-length (2.0 and 2.2-μm) AlGaN/GaN HEMTs for different-Al-contents. The I_{DS} also increases up to the Al-content of 34% and then it slowly decreases for high Al-content HSs. One can get more I_{DS} values with the help of sub-micron devices (channel velocity reaches closer to saturation) [47].

The decrease of I_{DS} with the increase of drain-source voltage (V_{DS}=20 V) for positive gate voltage has been observed for all Al-content HEMTs. 9.0 to 12 % of current reduction from

maximum I_{DS} (V_{gs}=+1.5 V) has been observed for 15 μm-wide-gate devices. The current reduction percentage of I_{DS} has been observed to be 25 to 32% for 200-μm-wide-gate devices (see Fig. 25a)). The I_{DS} reduction when applying high V_{DS} is due to the effect of heat generation (self-heating) in the device structures [51]. The drain current collapse has been recovered to some extent with the help of SiC substrate [4,5,52] (instead of sapphire substrate) or complicated flip-chip technology [53]. The 34% Al-content HEMTs provide high values of both g_m=202 mS/mm and high I_{DS} =525 mA/mm).

The maximum g_m of HEMTs as a function of Al-content is shown in Fig. 26. Many devices were characterised with identical dimensions. The increase of g_m has been observed up to the Al-content of 34% and then it slowly decreases

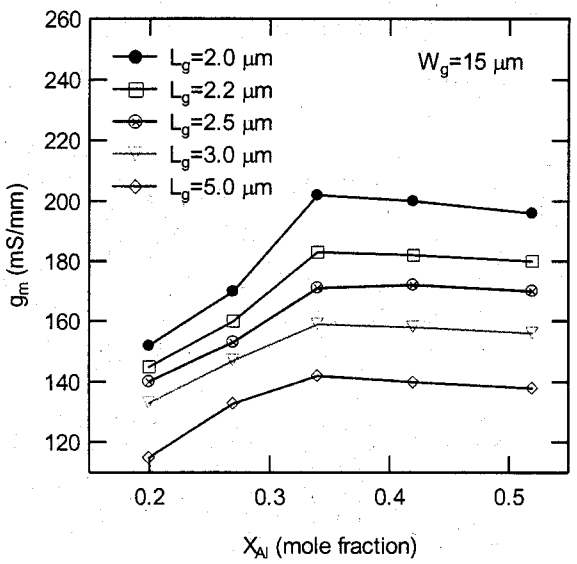

Fig. 26. g_m of different L_g HEMTs as a function of Al-content.

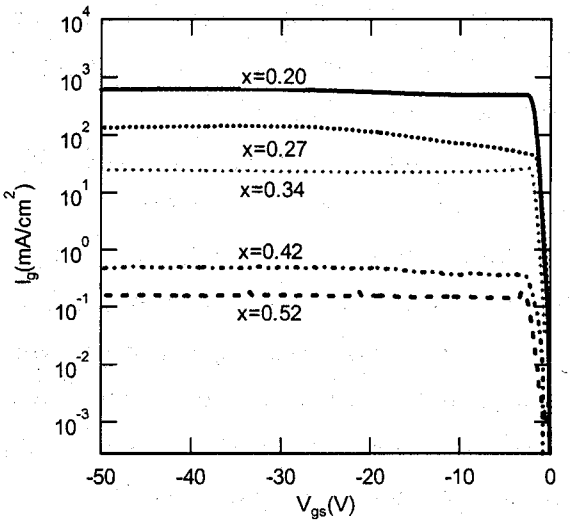

Fig. 27. Two terminal gate-leakage current characteristics of $Al_xGa_{1-x}N$/GaN Schottky diode for different-Al-content.

for the Al-contents of 42 and 52%. The g_m versus x_{Al} is in good agreement with the 2DEG mobility of HSs versus x_{Al} (see Fig. 23). The heterostructure contact resistances (R_c) were measured using transfer length model (*TLM*). Average R_c values as a function of Al-content is shown in Table IV. The R_c values increase linearly with the increase of Al-content of AlGaN/GaN HSs. The increase of R_c is due to the increase of AlGaN band gap with the increase of Al-content (see Fig. 21). These values are one order high compared with the reported values [54,55]. The changes in source-drain current densities of different-Al-content AlGaN/GaN HEMTs depend upon the values of contact resistance, source resistance and the interface quality of GaN and AlGaN. High value of *P-V* distance and surface roughness for 52% Al-content HSs has been confirmed using AFM measurements. Further reductions in R_c are needed to get more I_{DS} values.

Fig. 27 shows the two terminal gate-leakages current for different-Al-content 150-μm Schottky diodes. From this, we understand that the decrease of gate-leakage current with the increase of Al-content is due to the increase of band gap with Al-content (Fig. 21). About 3 to 4

orders of magnitude low gate leakage current has been observed for 42 and 52% Al-content AlGaN/GaN HEMTs when compared with the low Al-content (20%) AlGaN/GaN HEMTs. The reduction of gate leakage current is not very high for 52% device when compared with 42% device. This is possibly due to the high values of *P-V* distance obtained from AFM measurements (see Fig. 22 b)). Though the high Al-content (50%) of AlGaN/GaN HSs exhibited low 2DEG mobility, an increase of RF output power density with the increase of Al-content was reported by Mishra *etal* [47]. From our experimental results, we understand that high Al-content $Al_xGa_{1-x}N/GaN$ (x_{Al}=0.34 to 0.42) HSs provides good device dc characteristics with low gate-leakage current.

3.5. AlGaN/GaN HEMTs on Sapphire and SI-SiC at High temperature operation

The room temperature Hall measurement shows mobility's of 1163 and 1281 cm^2/Vs and sheet carrier densities of $1.0x10^{13}$ and $1.2x10^{13}$ cm^{-2} for AlGaN/GaN heterostructures on sapphire and SI-SiC substrates, respectively. The device dimensions for this studies are as follows: source-drain distance (L_{sd})=8.5 μm; gate width (W_g)=15 μm; gate length (L_g)=3 μm and source-gate distance (L_{sg})=2.0 μm. Table V shows the extrinsic transconductance (g_m), the maximum drain current (I_{dmax}), source resistance (R_s) and drain resistance (R_d) values of HEMTs on Sapphire and SI-SiC substrates, respectively. The g_m and I_d decreasing trend with the increase of temperature (Fig. 28) is due to the decrease of both 2DEG mobility and electron velocity [56]. The decrease in 2DEG mobility of HEMTs on SiC substrate with the increase of temperature has been confirmed with the Hall measurements (inset of Fig. 28). The 2DEG mobility above room temperature is limited by LO-phonon scattering [57]. Little low g_m decreasing trend with the increase of temperature (25 to 500°C) have been observed for HEMTs on sapphire (78%) compared with the HEMTs on SiC (84%) substrates.

Table V. Device dc parameters of AlGaN/GaN HEMTs on sapphire and SI-SiC substrates. *Parameters of high-temperature stressed (500°C) device measured at 25°C

T (°C)	g_{mmax} (mS/mm)		I_{dmax} (A/mm)		R_s (Ω-mm)		R_d (Ω-mm)	
	Sapphire	SI-SiC	Sapphire	SI-SiC	Sapphire	SI-SiC	Sapphire	SI-SiC
25	158	210	0.37	0.51	4.1	2.6	8.7	8.4
250	73	79	0.22	0.17	5.9	6.8	29.4	19.5
500	38	33	0.10	0.11	16.3	12.8	42.8	35.0
25*	140	201	0.36	0.55	4.7	3.5	9.5	6.5

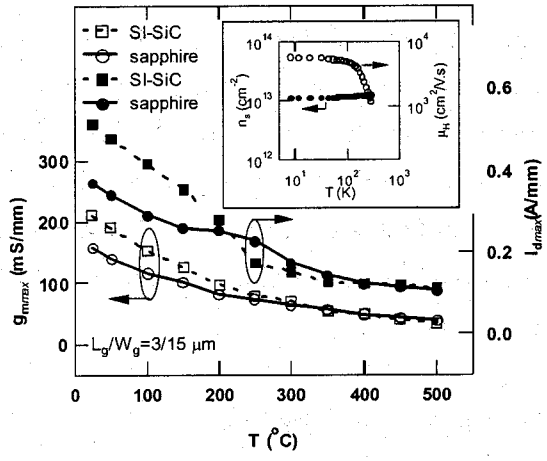

Fig. 28. Maximum transconductance (g_{mmax}) and drain current (I_{Dmax}) of AlGaN/GaN HEMTs on sapphire and SI-SiC substrates as a function of temperatures. The g_m was determined at V_{ds}=6 V and V_{gs}=0.8 V. The inset shows the 2DEG mobility (μ_H) and sheet carrier density (n_s) of AlGaN/GaN structure on SI-SiC substrate as a function of measurement temperature (8 to 300 K).

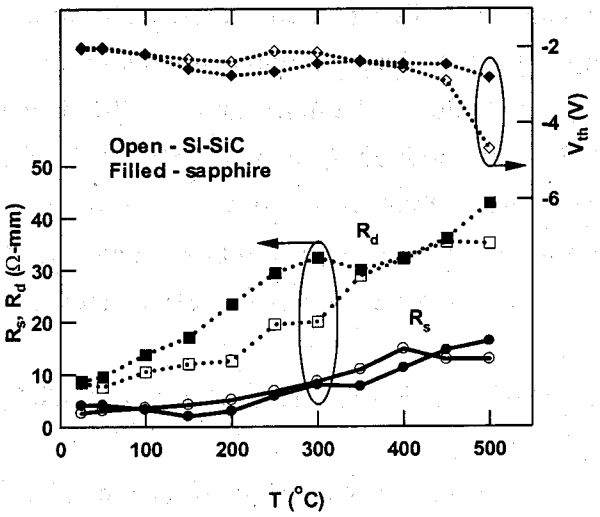

Fig. 29. Source-resistance (Rs), drain-resistance (Rd) and threshold voltage (Vth) of HEMTs as a function of temperature

The device g_m values depend on the quality of AlGaN/GaN heterostructure, device intrinsic transconductance (g_{m0}) and source resistance (R_s). With the help of g_m and R_s, g_{m0} have been estimated using the expression: $g_{m0} = g_m/(1 - R_s g_m)$. The decrease in g_{m0} with the increase of temperature (25 to 500°C) was also observed for both sapphire- (449 to 100 mS/mm) and SiC- (463 to 57 mS/mm) based AlGaN/GaN HEMTs. From this, we confirmed that, the channel mobility decreases with the increase of temperature. The decrease-ratio of g_m and I_d is low at and above 300°C (see Fig. 28) [58]. Similar behaviour was observed for 2DEG mobility decrease-ratio by Maeda et al [59]. The low degradation rates in gm at high-temperatures are a favourable characteristic for high-temperature operating devices.

At and above 300°C, g_m and I_d of both device structures showed similar values (Fig. 28). Gaska et al [60] claimed, due to the high thermal conductivity, the SiC-based HFETs exhibited better device characteristics at elevated temperatures (300°C) compared with sapphire-based devices. Our results are in good agreement with Gaska *et al* [60] up to 300°C. Above 300°C, both devices have exhibited similar characteristics (Fig. 28). At and above 300°C, it is difficult to explain the SiC-based device characteristics with the help of substrate thermal conductivity. Drastically enhanced leakage-current activation energy (1.0 eV) above 400°C on sapphire substrate supports the above argument [60]. Further, research is needed to understand the exact mechanism of SiC-based device high-temperature characteristics at and above 300°C.

The R_s and R_d values were extracted from current-voltage (I_{DS}-V_{DS}) characteristics. The increase R_s and R_d with the increase of temperatures was observed on both the HEMTs (see Table V and Fig. 29). The increase-ratio is similar for both the substrate HEMTs. Threshold voltages (V_{th}) of the devices were extracted from $I_D^{1/2}$ vs. V_G plot. Sapphire-based devices exhibited small variations in V_{th} values (-2.8 to -2.0 V) with the measurement temperature (see Fig. 29). Except the measurement temperature of 500°C, V_{th} is ranging from -2.9 to -2.0 V. Due to the increase of drain leakage-current, SiC-based HEMTs exhibited a low V_{th} value of -4.5 V at 500°C. From this, we understand that the HEMTs on sapphire show better high-temperature dc characteristics with small V_{th} shift [57]. Maeda et al [58] observed superior pinch-off characteristics with the threshold voltage of -7.0 V at 400°C. We have also observed good pinch-off characteristics up to the temperature 400°C in both the substrate HEMTs. Above the temperature 450°C, the increase of leakage-current has been observed from SiC-based AlGaN/GaN HEMTs [61]. The SiC-based device leakage-current is also high at 500°C compared with the sapphire-based devices. Both the substrate devices were operational even at 500°C. Daumiller *et al* [61] reported that, the AlGaN/GaN HEMTs on sapphire substrate are operational even up to 750°C with Pt/Au gate metal.

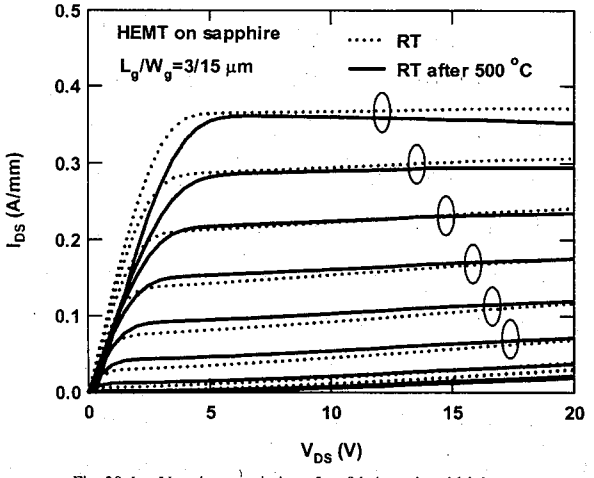

Fig. 30. I_{DS}-V_{DS} characteristics of as-fabricated and high-temperature stressed (up to 500°C) AlGaN/GaN HEMTs on sapphire substrate measured at room temperature.
Top trace was at V_g=+1.5 V and step was -0.5 V.

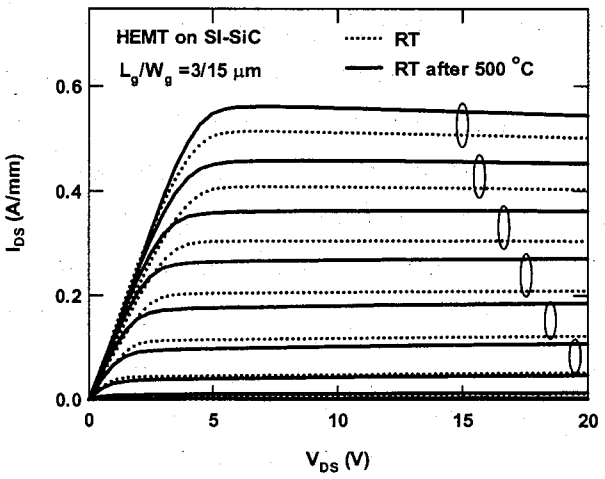

Fig. 31. I_{DS}-V_{DS} characteristics of as-fabricated and high-temperature stressed (up to 500°C) AlGaN/GaN HEMTs on SI-SiC substrate measured at room temperature.
Top trace was at V_g=+1.5 V and step was -0.5 V.

Fig. 30 and 31 shows the I_{DS}-V_{DS} characteristics of as-fabricated and high-temperature (up to 500°C) stressed AlGaN/GaN HEMTs on sapphire and SiC measured at room temperature, respectively. The V_{gs} ranges from –3.0 to 1.5 V with ΔV_{gs}=0.5 V. The dotted and solid lines represent as-fabricated and high-temperature (500°C) stressed devices, respectively. A small increase in R_d (9.5 Ω-mm) was observed on sapphire-based HEMTs due to high-temperature stress. This degradation may be enhanced by the bias induced stress [61]. About 7% high value of drain current has been observed on high-temperature stressed SiC-based HEMTs compared with the

as-deposited HEMTs (Table V). An increase of drain current in the high-temperature stressed HEMTs is due to (i) the increase of 2DEG carrier density and (ii) the reduction of drain resistance. An increase of 2DEG carrier density ($5.2x10^{13}$ cm^{-2}) and decrease of drain resistance (Table V) has been confirmed using C-V and I_{DS}-V_{DS} measurements, respectively. The contact resistance (R_c) of the ohmic contact were measured on as-fabricated and high-temperature stressed samples using transmission line model (TLM). The R_c values of AlGaN/GaN on sapphire- and SiC samples are 4.0 and 2.9 Ω-mm, respectively. Low values of R_c (3.4 Ω-mm for Sapphire & 2.0 Ω-mm for SiC) were observed on the high-temperature stressed HEMTs. The decrease of R_c supports the enhanced dc characteristics of high-temperature stressed SiC-based HEMTs. Very little (2%) I_d reduction has been observed on high-temperature stressed sapphire-based HEMTs. Only 12 and 4% reduced g_m values were observed from the high-temperature stressed (500°C) sapphire- and SiC-based HEMTs compared with the as-deposited HEMTs, respectively (Table V). The large g_m reduction percentage on sapphire based HEMTs may be due to the slow cooling rate compared with the SiC-based HEMTs (high thermal conductivity).

The device degradation is highly possible through Schottky/gate-metal contacts at high-temperature. The rms roughness values of as-deposited and thermally-stressed HEMTs on sapphire and SiC substrates are 4.1 & 2.1 nm and 7.0 & 13.3 nm, respectively. An increase of rms surface roughness has been observed on the thermally stressed HEMTs. Similar behaviour has been observed on the annealed Pd/AlGaN Schottky diodes [1,2]. The increase of surface roughness is also low in the case of high-temperature stressed sapphire-based Pd/AlGaN interfaces. The Pd/AlGaN interface studies are reported elsewhere [1,2]. Rectifying behaviour of Pd/AlGaN Schottky diodes with the *I-V* barrier height of ϕ_b=1.23 eV and ideality factor of n=1.35 was observed up to the annealing temperature 500°C/1 h. No de-lamination of Pd metal from AlGaN surface was observed even after 900°C annealing [2]. Moreover, no interfacial reactions were observed even at 750°C annealed Pd/AlGaN interfaces, which were confirmed using Auger Electron Spectroscopy (AES). From this we conclude that Pd/AlGaN interface is stable up to 500°C.

3.6. AlGaN/GaN HEMTs on 4-inch sapphire substrate

The isolation current was measured at 40 different locations on a quarter of 4-inch wafer. Except the periphery of the wafer, the isolation current of *i*-GaN varies between 0.17 nA to 0.5 μA [7]. The dc characteristics of the fabricated HEMTs were measured using Agilent 4156c semiconductor parameter analyser. Identical device dimensions (W_g=15 μm, L_g=2.0 μm, L_{sg}=2.0 μm, L_{sd}=9.0 μm) were chosen for the uniformity studies across the wafer. Fig. 32 shows the typical I_{DS}-V_{DS} characteristics of HEMTs with good pinch-off on 4-inch substrates. Maximum drain current density (I_{Dmax}) of 644 mA/mm and extrinsic transconductance (g_{mmax}) of 212 mS/mm has been observed among the HEMTs from a quarter of 4-inch wafer.

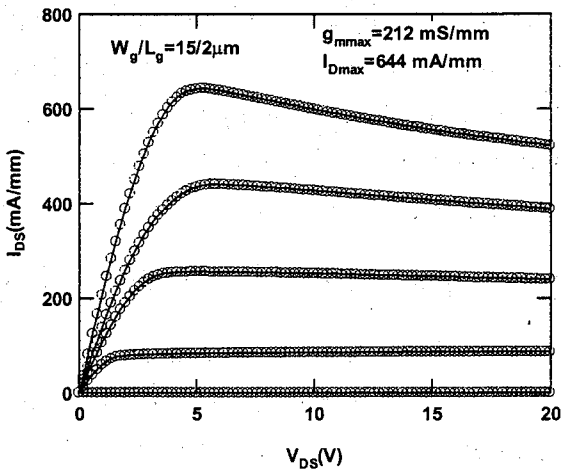

Fig. 32. I_{DS}-V_{DS} characteristics of AlGaN/GaN HEMTs on 4-inch sapphire. Gate voltage (V_g) range is +1.5 to -3.5 V with the step of -1.0 V. Device dimensions: W_g=15 um, L_g=2.0 um, L_{sg}=2.0 um, L_{sd}=9.0 um.

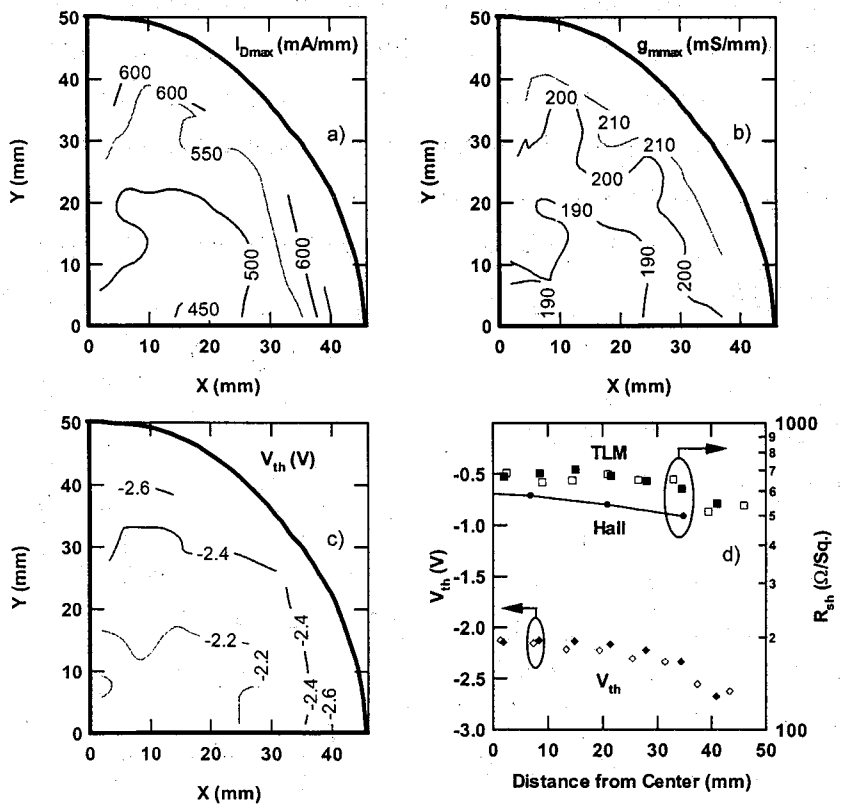

Fig. 33. Contour mapping of a) I_{Dmax}, b) g_{mmax} and c) V_{th} of AlGaN/GaN HEMTs on a quarter of 4-inch diameter wafer. d) Line scan distribution of Vth from $(I_D)^{0.5}$-Vplot and sheet resistance measured from Hall and TLM method. Open and filled symbols denote the X- and Y-axis distribution of a quarter of 4-inch wafer.

Figure 33 a), b) and c) show the contour mapping of I_{Dmax} and g_{mmax} and threshold voltage (V_{th}) of AlGaN/GaN HEMTs on a quarter of 4-inch sapphire substrate. The average g_{mmax} and I_{Dmax} values of 197 mS/mm and 515 mA/mm with standard deviations of 4.82% and 9.34% respectively were observed on a quarter of 4-inch wafer. The uniformity of the devices are in agreement with the uniformity of Hall mobility (μ_H) and sheet carrier density (n_{sHall}) of 1322 cm^2/Vs and

8.36×10^{12} cm^{-2} with standard deviations of 4.27% and 6.75%, respectively. Normally, the 2DEG carrier density depends on both the AlGaN doping concentration and AlGaN thickness. In this case, we believe that the AlGaN thickness is a more dominant cause for the variation of 2DEG carrier density when compared with the AlGaN doping concentration. The average values of source (R_s) and drain (R_d) resistance are 2.64 ±0.20 Ω-mm and 5.80 ±0.37 Ω-mm, respectively. It is clear that both the R_s and R_d distributions are less than 7.5%. The average V_{th} values of the devices are –2.30 V with a standard deviation of 6.52% [Fig. 33c)]. The C-V measured average V_{th} values (-2.33 V with a standard deviation of 6.65%) are in good agreement with the values obtained from $\sqrt{I_D} - V_G$ plot of HEMTs. From this, it is clear that, the AlGaN/GaN HEMTs on 4-inch sapphire substrates were in good homogeneity across the wafer.

The sheet resistance measurements of AlGaN/GaN HSs were carried out at room temperature using Transfer Length Method (TLM) and Hall Effect measurements. The average contact resistance (R_c) values were 2.07 ±0.26 Ω-mm. Both Hall and TLM measured sheet resistance values decrease from the centre to periphery of the wafer [see Fig. 33 d)]. The average sheet resistance values measured from TLM and Hall were 621 and 575 Ω/Sq. with a total variation of 16.98 and 13.16%, respectively. These sheet resistance values are in agreement with the values of non-contact measured sheet resistance of 558 Ω/Sq. with a total variation of 14.5% [62,63]. Uren et al [3] have reported the average sheet resistance of 695 Ω/□ with a total variation of 12.3% for AlGaN/GaN HSs grown on 2-inch sapphire. From this, we understand that the grown AlGaN/GaN HSs were in good uniformity across the 4-inch diameter wafer.

To measure the 2DEG carrier density, capacitance-voltage (C-V) measurements were carried out at 1 MHz on 40 identical diameter Schottky diodes at different locations of a quarter of 4-inch wafer using HP4845A LCR meter. The average 2DEG carrier density measured from C-V measurements are 3.69×10^{19} cm^{-3} at a depth of 22.51 ±1.78 nm. The carrier density at a depth above 2 μm was as lows as 5×10^{12} cm^{-3}. The combination of low leakage current of *i*-GaN and the observation of minimum carrier density at a depth of 2 μm indicate that the grown AlGaN/GaN HSs were of good quality with highly insulating GaN layer across 4-inch sapphire. Fig. 34 shows

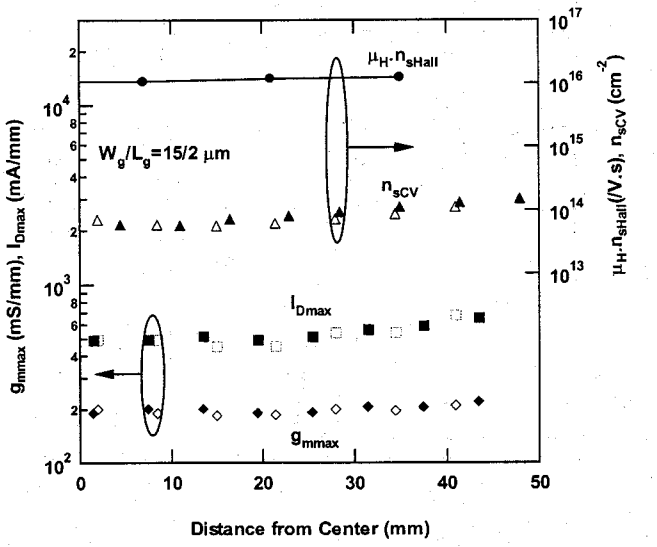

Fig. 34. Line scan distribution of I_{Dmax}, g_{mmax}, product $\mu_H.n_{sHall}$ and C-V measured sheet carrier concentration (n_{sCV}), form a center of the 4-inch wafer. Open and filled symbols denote the X- and Y-axis line scan distribution of a quarter of 4-inch wafer.

the line scan distribution of g_{mmax}, I_{Dmax}, product $\mu_H.n_{sHall}$ and 2DEG sheet carrier density (n_{sCV}) measured from C-V measurements as a function of distance from the centre of wafer. The g_{mmax} and I_{Dmax} values increase towards the periphery of the wafer, which is consistent with the product values of $\mu_H.n_{sHall}$ (see Fig. 34). It is also clear that, both n_{sCV} and n_{sHall} values increase towards the periphery of the wafer. From these, we understand that the uniformity of HEMTs dc properties were in agreement with the uniformity of Hall mobility and sheet carrier density across the 4-inch wafer.

3.7. AlGaN/GaN HEMTs on 4-inch sapphire and Si substrate: Comparison

3.7.1. Electrical, Structural and Surface properties

Hall Effect measurements were carried out on both the substrate based AlGaN/GaN heterostructures using van der Pauw configuration. An average of seven samples electrical property values are listed in Table VI. The room temperature 2DEG mobility of 950 and 1321 $cm^2/V.s$ were observed on Si and sapphire based AlGaN/GaN heterostructures, respectively. More than 70 % increase in low temperature (77 K) 2DEG mobility of 3505 and 5340 $cm^2/V.s$ were obtained on Si and sapphire based AlGaN/GaN heterostructures, respectively. Small values of sheet carrier density (n_s) values were obtained for AlGaN/GaN HSs on sapphire substrate. The sheet resistance (R_{sh}) values measured by Hall Effect are almost similar to each other. The full width at half maximum (FWHM) of (0004) reflection X-ray rocking curve revealed high values for AlGaN/GaN HSs (783 arcsec) on Si substrate when compared to AlGaN/GaN HSs (215 arcsec.) on sapphire substrates (See Table VI). The increase of FWHM values for X-ray rocking curve is due to the large lattice mismatch between GaN and Si substrate. This leads to

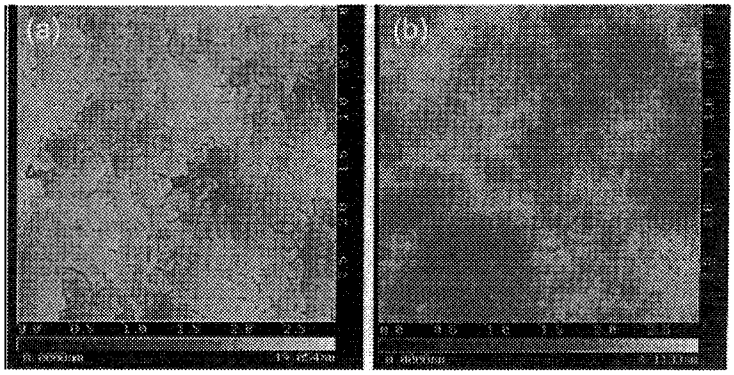

Fig. 35. AFM micrograph from the surface of AlGaN/GaN HEMTs on (a) Si and (b) sapphire substrates. Scan area: 3 μm x 3 μm

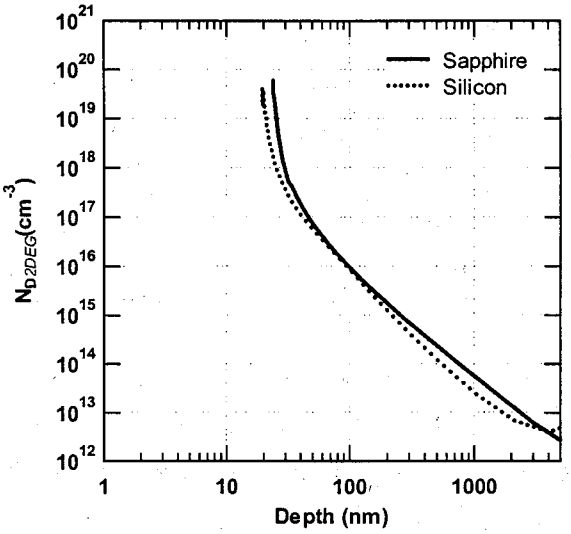

Fig. 36. Capacitance-Voltage profiling of AlGaN/GaN HEMTs on Si and sapphire substrates

the reduction of 2DEG mobility in AlGaN/GaN HEMTs on Si substrate.

Table VI. Device parameters of AlGaN/GaN HEMTs on 4-inch Si and 4-inch Sapphire

Parameters	**Si**	**Sapphire**
2DEG Mobility ($cm^2/V.s$) @ 300K	950	1321
2DEG Mobility ($cm^2/V.s$) @ 77K	3505	5340
n_s ($x10^{13}$ cm^{-2})	1.28	0.84
R_{sh} (Ω/sq.) Hall Effect	552	569
FWHM of (0004) XRD (arcsec)	783	285
R_{MS} roughness (nm) 3x3 μm^2	1.28	0.29
P-V (nm)	10.9	4.11
Depth (nm)	19.49	23.93
$n_{D\,2DEG}$ (x 10^{19} cm^{-3})	4.05	6.05
ϕ_B (eV)	0.92	1.01
n	2.22	1.25
R_c(Ω-mm) TLM method	2.67	2.07
R_{sh} (Ω/sq.) TLM method	1123	621
ρ_c (x 10^{-5} Ω-cm^2) TLM method	6.88	5.32
I_{Dmax} (mA/mm)	378	511
g_{mmax} (mS/mm)	148	198
V_{th}(V)	-1.76	-2.21
P_{out} (W/mm)	1.51	2.0
I_{gLeak}(mA/cm^2) @ V_g=-40V	171	4.23
ON-state BV_{gd} (V)	90	84
OFF-state BV_{gd} (V)	106	150
T_{Dmax} (°C) W_g=400 μm	41	74
$I_{Dreduc.}$(%) W_g=15 μm	3.92	15.85
$\Delta I_{Dreduc.}/\Delta W_g$	0.038	0.098
$\Delta T_D/\Delta W_g$	0.032	0.104
R_{th} (K/W)	44	139

Fig. 35 shows the 3 μm x 3 μm AFM micrograph of a) Si based and b) sapphire based AlGaN/GaN HSs surface. Typical step flow patterns were observed on sapphire based AlGaN/GaN HSs. About one order of high values of RMS surface roughness (R_{MS}) and peak-valley (P-V) distance were observed on Si based AlGaN/GaN HEMTs. Fig. 36 shows the ionized donor carrier density (n_{D2DEG}) depth profile of both Si and sapphire based AlGaN/GaN HEMTs which was measured by C-V measurements. From this, we understand that 2DEG profile

peak was formed at a depth of 19.5 nm for Si based and at a depth of 23.4 nm for Sapphire based AlGaN/GaN HEMTs (see Table VI). Due to the modulation doping, large n_{D2DEG} was observed on sapphire based AlGaN/GaN HEMTs. The values of Schottky barrier height (ϕ_B) and ideality factor (n) of AlGaN/GaN HEMTs are shown in Table VI. High values of ϕ_B with near ideal I-V characteristics were observed on sapphire based AlGaN/GaN HEMTs when compared to the HEMTs on Si substrates. The observations of high ϕ_B with good diode characteristics are due to the occurrence of smooth AlGaN surface [64] (see Fig. 35 and Table VI).

3.7.2. dc characteristics of AlGaN/GaN on 4-inch Si and Sapphire

The source and drain ohmic contact properties were measured using transfer length model (TLM) method. The measured contact resistance (R_c), specific contact resistivity (ρ_c) and sheet resistance (R_{sh}) values are listed in table I. Due to the poor surface quality of Si based AlGaN/GaN, high values of R_{sh} were observed. The poor surface morphology with high R_{MS} and P-V values were confirmed by AFM measurements. Due to the undoped AlGaN barrier layer, high R_c values were observed on Si based AlGaN/GaN HEMTs. Fig. 37 shows typical I_{DS}-V_{DS} characteristics of 4-inch diameter Si and sapphire based (W_g/L_g=15/2 μm) AlGaN/GaN HEMTs. The device *dc* parameter values of Si and sapphire based HEMTs are tabulated in Table VI. The maximum extrinsic transconductance (g_{mmax}) of 148, 198 mS/mm with maximum drain current density (I_{Dmax}) of 378, 511 mA/mm has been observed for 2.0 μm-gate-length HEMTs on Si and sapphire substrates, respectively. The observation of large g_{mmax} and I_{Dmax} values for AlGaN/GaN on sapphire substrates is consistent with the values of 2DEG mobility when compared to AlGaN/GaN HEMTs on Si substrate. Due to the undoped AlGaN barrier layer in the HEMTs on Si, the threshold voltage (V_{th}) shifted towards positive direction. An influence of thick AlN buffer layer, improved I_{DS}-V_{DS} characteristics of AlGaN/GaN HEMTs on 4-inch Si substrate with high I_{Dmax} and g_{mmax} values have been reported elsewhere [45]. The total output power of AlGaN/GaN HEMTs was calculated with: $P_{out} = (I_{Dmax}/2)(V_{DS}-V_{knee})/2$ by fixing the V_{DS} of 20 V. High P_{out} was observed on sapphire based AlGaN/GaN HEMTs (2.0

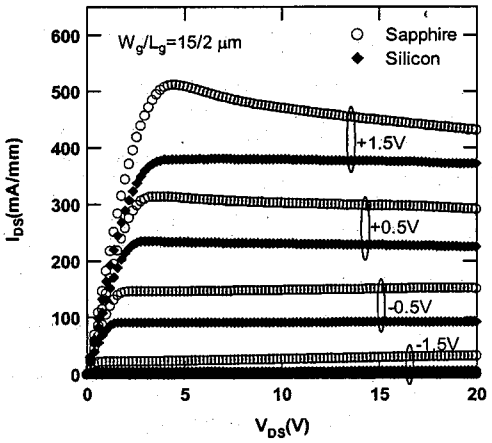

Fig. 37. Good pinch-off dc I_{DS}-V_{DS} characteristics of AlGaN/GaN HEMTs on Si and Sapphire substrates

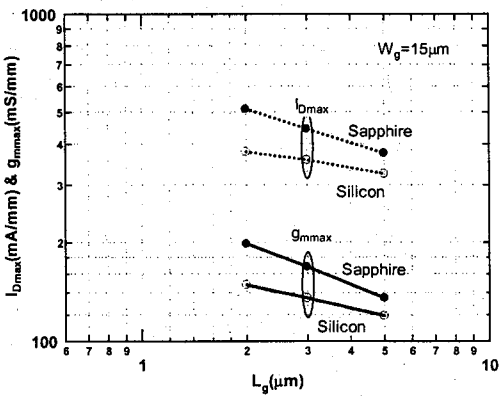

Fig. 38. Good pinch-off dc I_{DS}-V_{DS} characteristics of AlGaN/GaN HEMTs on Si and Sapphire substrates.

W/mm) when compared to Si based HEMTs (1.51 W/mm). Fig. 38 shows the I_{Dmax} and g_{mmax} values as a function of L_g. It is clear that the increase of I_{Dmax} and g_{mmax} with L_g was observed on both the substrate based AlGaN/GaN HEMTs. It is be possible to get more I_{Dmax} and g_{mmax} with sub-micron devices.

3.7.3. Gate leakage current and Breakdown voltage characteristics

Two terminal gate leakage current (I_{gLeak}) characteristics of AlGaN/GaN HEMTs on Si and sapphire substrates are shown in Fig. 39. About two orders of magnitude low I_{gLeak} measured at V_g=-40 V was observed on sapphire based AlGaN/GaN HEMTs (See table VI) when compared to Si based AlGaN/GaN HEMTs. The observation of large I_{gLeak} is possibly due to the existence of poor surface morphology with high value of R_{MS} and P-V value [64]. Fig. 40 shows the ON-state and OFF-state breakdown voltage (BV_{gd}) characteristics of 200 μm-wide gate AlGaN/GaN HEMTs on Si and sapphire substrates. ON-state BV_{gd} and OFF-state BV_{gd} was measured by destroying the devices at V_g=+1.5 V and V_g=-4.5 V, respectively. Low value of OFF-state BV_{gd} was observed on Si based HEMTs when compared to sapphire based AlGaN/GaN HEMTs. Fig. 41 shows the OFF-state BV_{gd} of 200-μm-wide and 2.0-μm-length gate HEMTs for different I_{gLeak}. An increase of OFF-state BV_{gd} with the decrease of I_{gLeak} has been observed in both the substrate based AlGaN/GaN HEMTs. From this we understand that the observation of low OFF-state BV_{gd} is due to the existence of large I_{gLeak} (see Fig. 39). The observation of high ON-state breakdown voltage for the HEMTs on Si substrate is due to the large amount of heat dissipation from the device. This is confirmed by measuring the device surface temperature by IR microscope camera. High ON-state BV_{gd} devices are suitable for high power switching devices.

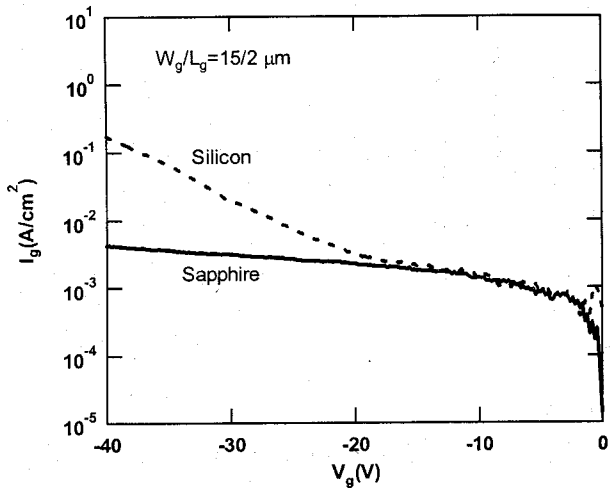

Fig. 39. Two terminal gate leakage current I-V characteristics of AlGaN/GaN HEMTs on Si and Sapphire

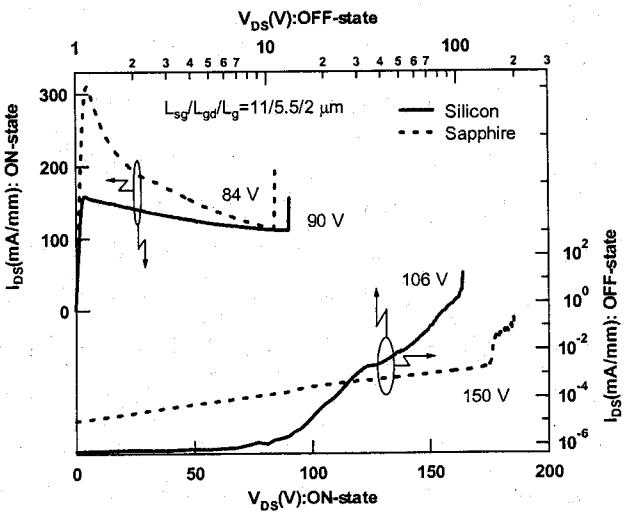

Fig. 40. Three terminal ON-state and OFF-state breakdown voltage (BV_{gd}) characteristics for AlGaN/GaN HEMTs on Si and Sapphire

3.7.4. Device self-heating and temperature measurements

The device surface temperature (T_D) in an active AlGaN/GaN HEMTs have been measured using IR microscope camera by applying V_{DS}=0-20 V with Vg=+1.5 and +0.5 V. Fig. 42 shows the T_D with relative time of V_{DS} scan with tow different gate supply voltages (V_g) of +1.5 V and +0.5 V for single finger 400 μm-wide-gate Si and sapphire based AlGaN/GaN HEMTs. Highest T_D of 74 °C was observed on sapphire based AlGaN/GaN HEMTs. However, small T_D of 41 °C was observed on Si based AlGaN/GaN HEMTs. Brown etal. [65] have observed high (320 °C) and low (95 °C) value of T_D for 10 finger-gate AlGaN/GaN HEMTs (6 W/mm) on sapphire and Si, respectively. The difference of T_D between Si and sapphire based HEMTs must be high for multi finger devices [66]. When applying drain bias 0-20 V for a fixed V_g of +1.5V, the T_D fluctuations were observed on sapphire based HEMTs. These T_D fluctuations are due to the slow thermal dissipation from the device structures. Due to the slow thermal dissipation, low ON-state BV_{gd} was observed (see Fig.40). The rate of increase in temperature (7.86 for V_g=+1.5 V and 6.11 for V_g=+0.5V) is high for sapphire based AlGaN/GaN HEMTs. However, Si based AlGaN/GaN HEMTs showed small rate of increase in temperature (1.81 for V_g=+1.5 V and 1.02 for V_g=+0.5 V). The rate of increase in temperature difference for two different V_g is small for sapphire based AlGaN/GaN HEMTs. From this, we found that the amount of heat dissipation is high for Si based AlGaN/GaN HEMTs when compared to sapphire based HEMTs. Large amount of heat dissipation from the devices are due to the inherent Si property of high thermal conductivity (1.5 W/cm-K) when compared to sapphire substrate. Fig. 43 shows the *IR* camera recorded thermal image of (a) Si based and (b) sapphire based single finger

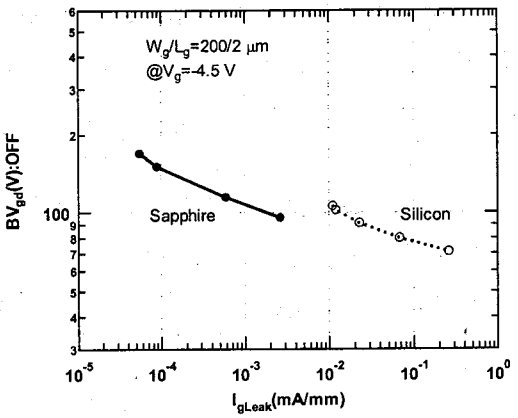

Fig. 41. OFF-state BV_{gd} as a function of I_{gLeak} for AlGaN/GaN HEMTs on Si and Sapphire

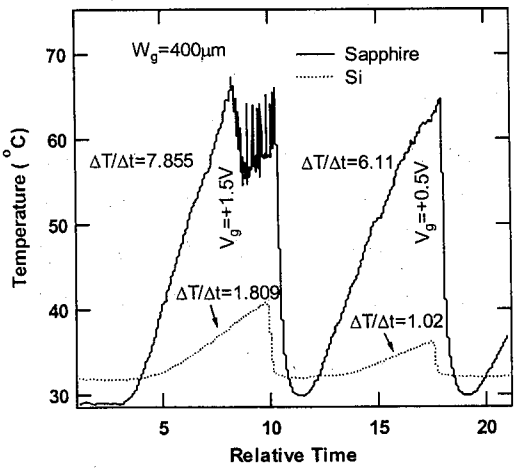

Fig. 42. Measured T_D as a function of time while applying drain-source bias 0-20 V with a gate voltage of +1.5 V and +0.5 V for AlGaN/GaN HEMTs on Si and Sapphire

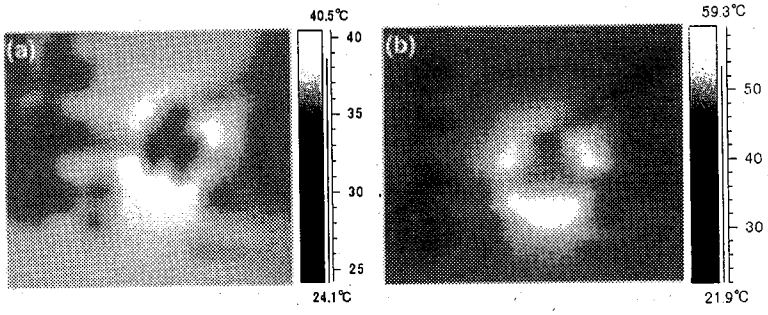

Fig. 43. Thermal mapping of 400-μm-gate-width HEMTs on (a) Si and (b) sapphire at V_{DS} =20 V and V_g = +1.5 V.

400-μm-gate-width and 2.0-μm-gate-length AlGaN/GaN HEMTs. This image was taken from an active device at a fixed V_g=+1.5 V and V_D=20 V. From this we conclude that the self-heating effects are high in sapphire based AlGaN/GaN HEMTs.

Fig. 44 shows the drain current reduction (I_{Dreduc} =(I_{Dmax}-I_{Dmin})/I_{Dmax}) measured at V_g=+1.5 V and T_D as a function of different W_g HEMTs on a) Si and b) sapphire substrates. The ratio of $\Delta I_D/\Delta W_g$ and $\Delta T_D/\Delta W_g$ for the respective substrates are equivalent. From this, we confirmed that there is a direct correlation between I_{Dreduc} and self-heating. The device thermal impedance (R_{th}) of Si and sapphire based AlGaN/GaN HEMTs were estimated by calculating the power of different W_g HEMTs and T_D measured by IR camera. Fig. 45 shows the measured T_D as a function of device power. Low and high R_{th} value of 44 °C/W and 139 °C/W were observed on Si and sapphire based

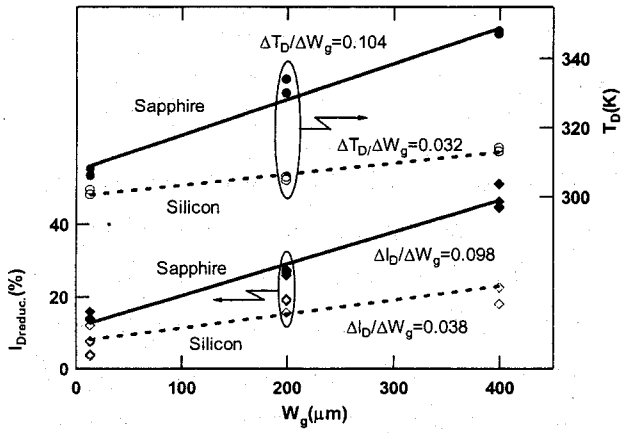

Fig. 44. A comparison between I_{Dreduc} and measured T_D with different W_g of AlGaN/GaN HEMTs on Si and Sapphire

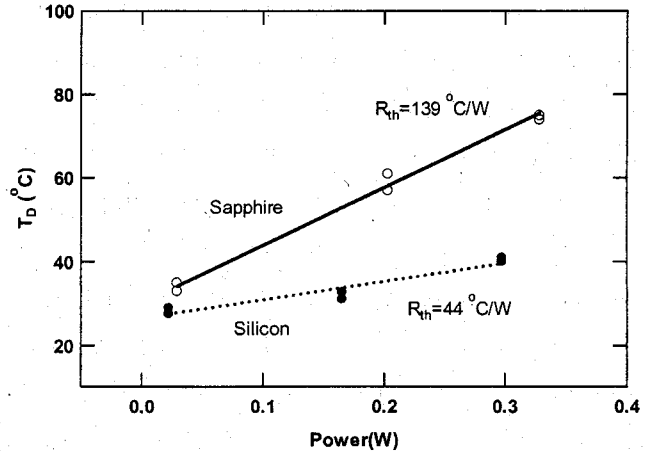

Fig. 45. Measured T_D as a function of device output power (P_{out})

AlGaN/GaN HEMTs, respectively. Park etal [67] observed peak T_D of 67 °C which was measured for 0.29 W AlGaN/GaN HEMTs on sapphire by direct pneumatic liquid crystal. The R_{th} values are 231°C/W. The observations of high R_{th} values are due to the effect of two finger AlGaN/GaN HEMTs. The increase of device surface temperature for multi finger HEMTs was observed by other authors [66,68]. The R_{th} of 293 °C/W was observed by Kim etal. [69] on GaN Misfits using CL method. The ratio of R_{thSi}/R_{thSapp}=0.30 was obtained from our investigations are consistent with the previously reported values of 0.297 [70].