3.8. AlGaN/GaN HEMTs on 4-inch Si: influence of AlN Buffer layer

Fig. 46 a) shows the good pinch-off I_{DS}-V_{DS} characteristics of 15-μm-wide AlGaN/GaN HEMTs grown on 300 nm thick AlN buffer layer. The maximum extrinsic transconductance (g_{mmax}) and maximum drain current density (I_{Dmax}) values increases up to the buffer layer thickness of 300nm. The I_{Dmax} of 632 mA/mm with g_{mmax} of 186 mS/mm were observed for HEMTs with 300 nm AlN buffer layer. However, HEMTs with 500-nm-thick buffer layer showed rather reduced I_{Dmax}. This is possibly due to the occurrence of cracks. The enhancement of device performance with AlN buffer layer thickness (200 and 300 nm) may be due to the suppression of electrically active defects from Si substrate. Similar behaviour was observed on the devices fabricated in GaAs on Si substrate [71]. The increase of structural properties with the increase of AlN buffer thickness were confirmed on AlGaN/GaN HSs using X-ray rocking curve (XRC) measurements. The full width at half maximum (FWHM) values of XRC's symmetric (0004) and asymmetric $(20\bar{2}4)$ reflections for different AlN buffer layer thicknesses on Si are shown in table I. From this data, it is confirmed that the increase of AlN buffer layer thickness reduces the dislocation density. We have also realized low dislocation density [72] with improved dc characteristics of AlGaN/GaN HEMTs on 1-μm-thick AlN/sapphire templates [73]. In addition, the decrease of R_c with the AlN buffer layer thickness is

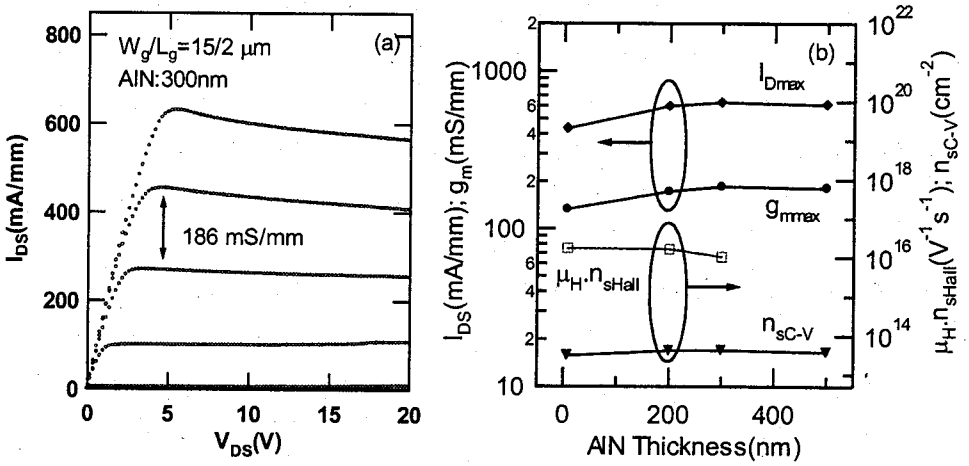

Fig. 46. a) I_{DS}-V_{DS} characteristics of AlGaN/GaN HEMTs (W_g/L_g=15/2 um) with 300 nm AlN buffer layer. Top V_g=+1.5V, V_g=-1.0 V; b) I_{Dmax}, g_{mmax}, $\mu_H.n_{sHall}$ and n_{sC-V} values of HEMTs as a function of AlN thicknesses.

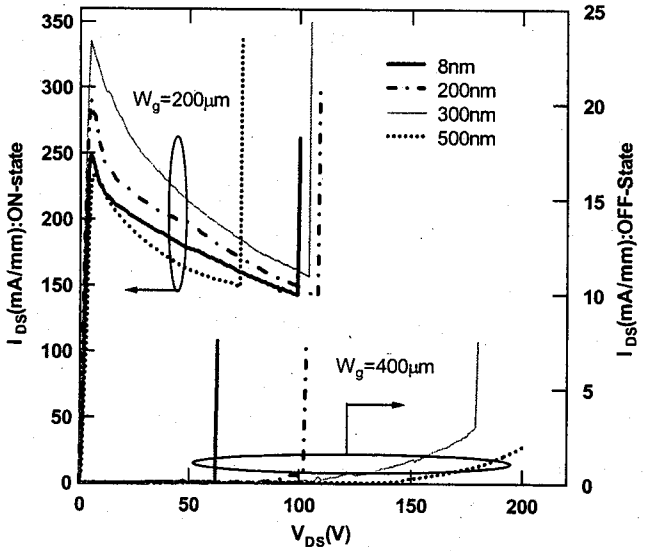

Fig. 47. BV:ON and BV:OFF characteristics of AlGaN/GaN HEMTs for different thicknesses of AlN buffer layers.

also an indication of the suppression of electrically active defects. Fig. 46 b) shows the AlN buffer layer thickness dependence of I_{Dmax}, g_{mmax}, sheet carrier density ($n_{sC\text{-}V}$) from capacitance-voltage measurements and the product of 2DEG mobility (μ_H) and sheet carrier density (n_{sHall}) of grown AlGaN/GaN HEMT structure. The HEMTs with 300-nm-thick buffer showed rather small product values, however the measured $n_{sC\text{-}V}$ values with AlN buffer thicknesses were in the similar dependences of I_{Dmax} and g_{mmax} values. Due to the occurrence of crack, Hall parameters were not successfully obtained for HEMTs with 500-nm-thick buffer layer.

Table VII. Parameter values *BV*:OFF, *BV*:ON, *BV* for two adjacent device ohmic contacts and R_{on} for AlGaN/GaN HEMTs with different AlN buffer layer thicknesses.

AlN thickness (nm)	FWHM (arc. sec.)		*BV*:OFF (V)		*BV*:ON (V)	R_{on} (mΩ-cm^2)		*BV* (V) [3]
	(0004)	(2024)	W_g= 200 μm[1]	W_g = 400 μm[2]	W_g= 200 μm	W_g = 200 μm	W_g = 400 μm	W_g= 200 μm
8	740	1620	115	62	99	0.46	0.58	113
200	688	1555	196	102	108	0.27	0.35	196
300	670	1535	215	158	104	0.28	0.33	218
500	654	1500	243	192	73	0.47	0.53	244

[1] @ I_D= 5.0 mA/mm,

[2] @ I_D= 1.5 mA/mm,

[3] two adjacent device (buffer layer breakdown)

Many devices with an identical dimension ($L_{sd}/L_g/L_{gd}/W_g$=11/2/5.5/200μm and $L_{sd}/L_g/L_{gd}/W_g$= 9.5/2/4/400μm) were destroyed to obtain *BV* characteristics. Fig. 47 shows the OFF-state-*BV* (*BV*:OFF) and ON-state-*BV* (*BV*:ON) characteristics of 400 and 200-μm-wide gate AlGaN/GaN HEMTs for different thicknesses of AlN buffer layers, respectively. The device *BV*:ON and *BV*:OFF were measured at the gate voltage of +1.5V and -4.5V, respectively. Not much change was observed in *BV*:ON values except the HEMTs with 500 nm-thick buffer layer (see table VII). This may be due to the enhancement of leakage current through the cracked surface region. The *BV*:OFF values of HEMTs at a

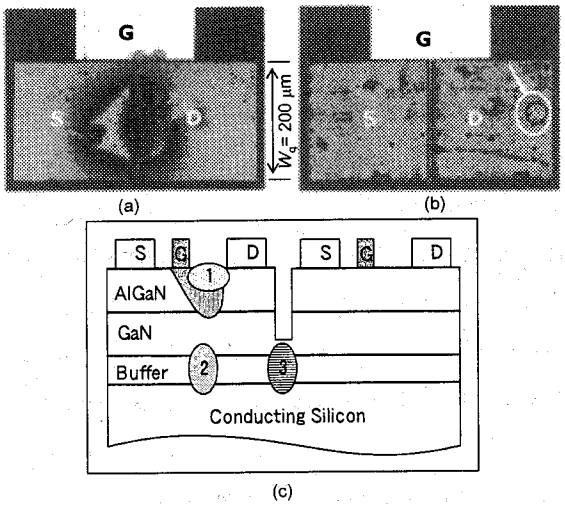

Fig. 48. 200-μm-wide HEMTs top-view photograph a) after *BV*:ON; b) after *BV*:OFF; c) Cross-sectional schematic diagram of two adjacent devices with breakdown junction/region.

fixed drain current density (of 1.5 mA/mm for W_g=400 μm and 5 mA/mm for W_g=200 μm) are shown in Table VII. From the Fig. 47 and Table VII, it is clear that the *BV*:OFF increases with the increase of AlN buffer layer thickness. Due to the dislocation reduction (see table VII) in the HEMTs with 200, 300 and 500 nm-thick-AlN buffer layer, the carrier multiplication process in the bulk may be small [74]. This is an additional possible reason for the increase of *BV*:OFF. About 46% of enhancement in *BV*:OFF was observed on 200-μm-wide HEMTs with 300-nm-thick AlN buffer layer when compared to the HEMTs with 8-nm-thick AlN buffer layer. The maximum *BV*:OFF and *BV*:ON values of 215 and 104 V were observed on HEMTs with 300 nm AlN buffer layer, respectively (see Table VII).

Fig. 48 a) and b) shows the device micrographs after *BV*:ON and *BV*:OFF measurements. No burn marks were observed after *BV*:OFF measurements except a burn dot on the drain contact (see Fig. 48 b)). There is no burn-mark in the drain-source gap. Two junctions were involved for the possibility of device breakdown such as, AlGaN/GaN junction and GaN/AlN/Si junction. To identify the location of junction breakdown, *BV* characteristics were carried out in between the ohmic metals (for e.g. drain contact of one device and the source contact of an adjacent device) of two adjacent 200-μm-wide devices with the isolation gap of 50 μm (see Fig. 48 c). The *BV* values are tabulated in table I. The measured *BV* of two adjacent device ohmic contacts is similar to the *BV*:OFF of a single device (region 2 and 3 of Fig. 48 c)). From this, it is confirmed that the breakdown did not occur at AlGaN/GaN junction (region 1 of Fig.4 c)). The actual breakdown occurred at GaN/AlN/Si junction (region 2 of Fig. 48 c)). From this experimental evidence it is concluded that the GaN/AlN/Si junction is weaker than AlGaN/GaN junction. To see the direct evidence of junction breakdown, transmission electron microscopy measurements of these devices are under progress. It may be possible to increase the *BV*:OFF values using high-resistive-Si substrate.

The measured specific on-resistance (R_{on}) values for 200 and 400 μm-wide HEMTs with different buffer layers are tabulated in Table VII. Here the channel resistance dominates the R_{on} for the HEMTs, because the *BV* is less than 1kV [75]. Our devices have exhibited low values of *BV*:OFF values when compared with the reported values (370 to 1300 V) [75,76,77,78] however, about an order of low R_{on} was observed for a similar *BV* [79]. This is possibly due to the suppression of electrically active defects from Si substrate while using 200 and 300 nm-thick buffer layer [71]. Due to the cracks, high R_{on} values were observed in 500 nm-thick buffer layer device. From these experimental results, it is clear that the AlGaN/GaN HEMTs on 4-inch Si is a promising candidate for high power switching applications.

3.9. Drain current collapse in AlGaN/GaN HEMTs on sapphire and SiC

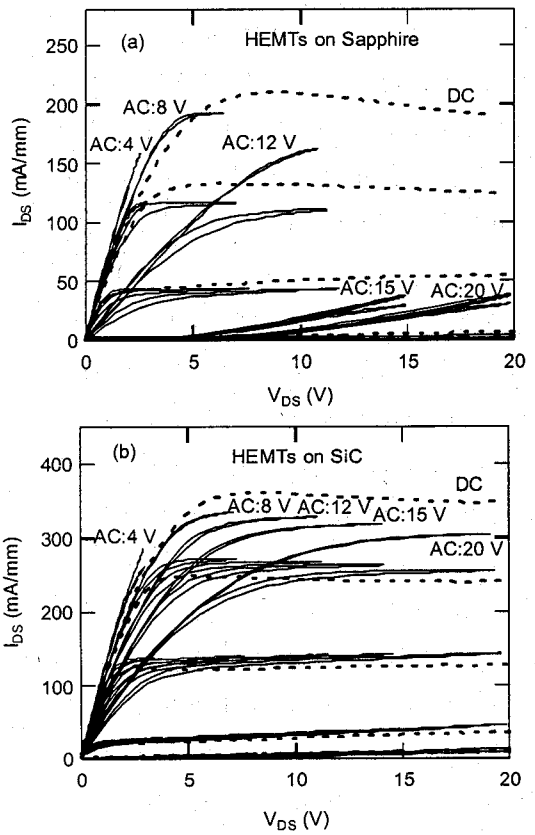

Fig. 49. Measured dc and ac I_{DS}-V_{DS} characteristics (for different drain sweep voltages V_{DS}= 4, 8, 12, 15 and 20 V) of AlGaN/GaN HEMTs on (a) sapphire and (b) SI-SiC substrates. Top trace was at V_g=+1.5 V step voltage was -1.0 V

For this study, device dimensions are as follows: source-drain distance (L_{sd}) 10 μm; gate-width (W_g) 200 μm; gate-length (L_g) 2 μm, and source-gate distance (L_{sg}) 3.5 μm. Several devices with an identical dimension were used for this study. Fig. 49(a) and (b) shows the *dc* and ac I_{DS}-V_{DS} characteristics of AlGaN/GaN HEMTs on sapphire and SiC substrates, respectively. Though the drain-current collapse has been observed on a reproducible basis in both the HEMTs fabricated on sapphire and SiC substrates, the drain current collapse in HEMTs on SiC was very small compared with the HEMTs on sapphire substrates. The current collapse reaches high for the sweep voltage of 15 V, low thermal conductivity of sapphire substrate may partly involve in the current collapse mechanism. About 3.5% and 9.3% of dc drain current reduction due to the device temperature effect has been observed at V_g= +1.5 V on the SiC-based HEMTs and sapphire-based HEMTs, respectively [52].

Figure 50 shows the maximum drain current density (I_{Dmax}) as a function of drain sweep-voltage for different gate voltages of HEMTs on sapphire and SiC substrates. It is clear that, the drain-current collapse is severe for sapphire grown AlGaN/GaN HEMTs when compared with the HEMTs on SiC substrates. The current collapse behavior of both sapphire and SiC grown HEMTs is due to the existence of deep traps associated with the material defects/dislocations. To observe the trapping-effects, the drain-leakage-current (I_{DLeak}) of HEMTs was measured at different temperatures [5]. An activation energy plot of I_{DLeak} measured at the gate voltage of -5V with the drain voltage of 10V is shown in Fig. 51. Two deep trap activation energies

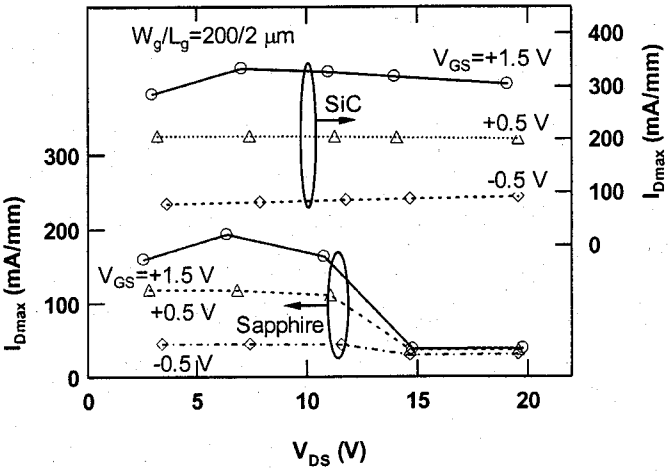

Fig. 50. Maximum drain-current (I_{Dmax}) of AlGaN/GaN HEMTs on sapphire and SI-SiC substrates as a function of ac drain sweep-voltages for V_g = +1.5 V, +0.5 V and -0.5 V.

of ΔE=1.05 and 0.040 eV were observed on the SiC-based HEMTs [81]. However, three deep trap activation energies of ΔE=1.23, 0.61 and 0.046 eV were observed on the sapphire-based HEMTs.

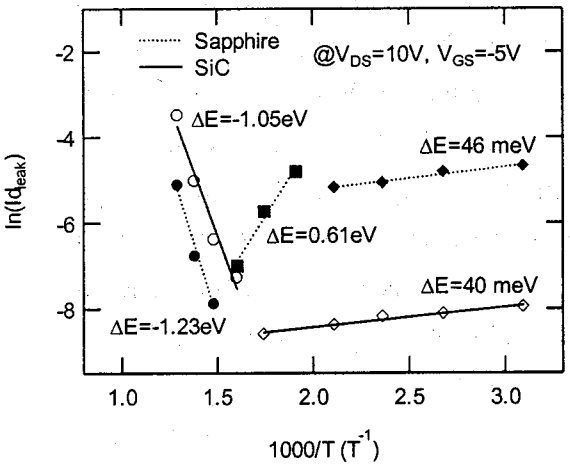

Fig. 51. Activation energy plot of I_{DLeak} measured at the gate voltage of V_g=-5 V and drain voltage of V_{DS}=10V

These deep trap activation energies are related with the material defects/dislocations. Low defect density has been realized on GaN epilayers grown on SiC substrates ($2x10^8$ cm^{-2}) when compared with the GaN epilayers on sapphire substrates ($6x10^8$ cm^{-2}). The low dislocation density of GaN on SiC is related to its small lattice mismatch and thermal expansion coefficient with GaN. Moreover, low radiative recombination centers have also been observed on the SiC grown GaN using electron beam induced current (EBIC) measurements [82]. The product of Hall mobility and sheet carrier density ($\mu_H \cdot n_s$) values were also high for AlGaN/GaN heterostructures on SiC substrate [4,5].

Fig. 52 shows the dc I_{DS}-V_{DS} characteristics of HEMTs measured at V_g=0V under dark and white-light illumination. The increase in percentage of drain current under white light illumination was high for sapphire-based HEMTs (33%) when compared with the SiC-based HEMTs (5%). The white-light illuminated I_{DS}-V_{DS} characteristics support the existence of more number of traps in the sapphire-based HEMTs. The ac I_{DS}-V_{DS} curve of sapphire grown HEMTs shows (see Fig 49(a)) large hysteresis width (≤910 mV) when compared with the HEMTs on SiC substrates (≤310 mV). Large values of hysteresis width confirm the presence of more deep traps located adjacent to the channel, which increases the device capacitance. Both the low thermal conductivity of sapphire and an additional activation energy deep trap (ΔE=+0.61 eV) level located nearer to the valence band severely degraded the drain current of sapphire-based HEMTs (see Fig 49 (a) and Fig. 51). These results are in good agreement with the low dislocation density, high value of $\mu_H \cdot n_s$ and small number of radiative recombination centers of GaN on SiC substrates, which was measured by Atomic Force Microscopy, Hall effect and EBIC and published elsewhere [4,5,82].

More number of deep traps captured almost all of the channel carriers when high drain voltages (≥15V) were applied. This trapped charge depletes the 2-DEG from beneath the

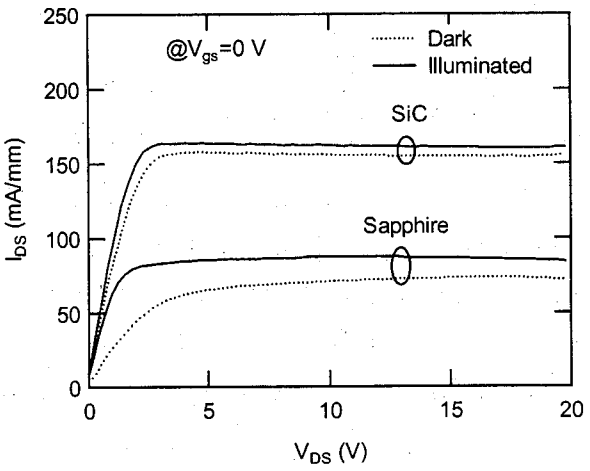

Fig. 52. *dc I_{DS}-V_{DS} characteristics of AlGaN/GaN HEMTs on sapphire and SiC substrates measured under dark and white-light illumination.*

active channel and results in the reduction of drain current and hence the output power [83,84]. For example, the dc characteristics of AlGaN/GaN HEMTs on SI-SiC [4] with a maximum saturation current about I_{DS}=850 mA/mm and the knee voltage of V_{KN}= 4.5 V at a moderate V_{DS}=30 V, would deliver an output power of $P_{OUT} \approx (I_{DS}/2)\times(V_{DS}-V_{KN})/2 \approx 5.4 \;\; W/mm$. Small knee voltage ($V_{KN}$) shift (2.31 V for drain sweep-voltage of 12 V) with small current reduction has been observed for SiC-based HEMTs. However, drastic V_{KN} shift with severe current collapse was observed for sapphire-based HEMTs (see Fig. 49 (a) and Fig. 50). The current collapse may be suppressed by low dislocation density GaN epilayer growth and passivation processes [83,85,86,87,88]. Further studies are required to understand the properties of existing deep traps in the device structure. From these results, it is clear that the HEMTs on SiC substrates show better dc and ac characteristics when compared with the HEMTs on sapphire substrates.

3.10. Surface Passivation Effects in AlGaN/GaN HEMTs on sapphire substrate

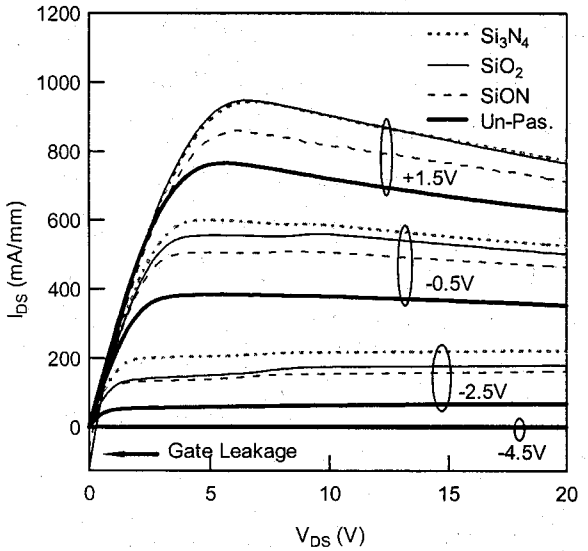

Fig. 53. dc I_{DS}-V_{DS} characteristics of Si_3N_4, SiO_2, SiON passivated and un-passivated AlGaN/GaN HEMTs on sapphire substrate. Top V_g=+1.5V; Step=-2.0V

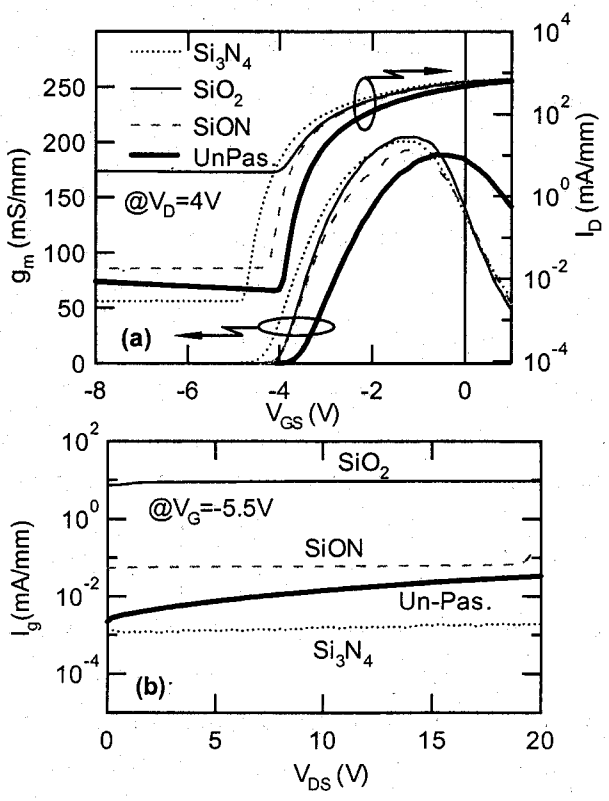

Fig. 54. a) Transfer characteristics of Si_3N_4, SiO_2 and SiON passivated and un-passivated AlGaN/GaN HEMTs measured at V_D=4V. b) I_g-V_{DS} characteristics of passivated and un-passivated HEMTs measured at sub-threshold regime (V_g=-5.5V)

Fig.53 shows the good pinch-off I_{DS}-V_{DS} characteristics of un-passivated and passivated 15-μm AlGaN/GaN HEMTs. Table VIII shows the dc parameters of un-passivated and passivated HEMTs. The device dimensions are: W_g=15 μm, L_{sd}=11 μm, L_{sg}=5 μm, L_g=1.5 μm. An increase in the maximum drain current (I_{Dmax}) and extrinsic transconductance (g_{mmax}) of approximately 19 and 8% for SiO_2, 19 and 6% for

Si_3N_4 and 11 and 2% for SiON passivated HEMTs, respectively were observed when compared with the un-passivated HEMTs. Fig 54a) shows the transfer characteristics of passivated and un-passivated HEMTs. Though, the I_{Dmax} and g_{mmax} increased due to the surface controlled effect [85,86,89], the rise in gate-leakage current (I_{gLeak}) was observed [89,90] except Si_3N_4 passivated HEMTs [91]. Fig. 54 b) shows the I_{gLeak} of un-passivated and passivated HEMTs measured at sub-threshold regime (V_G=-5.5V). Two terminals I_{gLeak} were also measured on Schottky diode and the results were similar to the results of three terminals I_{gLeak}. About an order of magnitude low I_{gLeak} and three orders of magnitude high I_{gLeak} was observed on Si_3N_4 and SiO_2 passivated HEMTs, respectively when compared with the unpassivated HEMTs. Similar behavior was observed for drain leakage current (see Fig. 54 a)). The rise in I_{gLeak} for the SiO_2 and SiON passivated devices results in a significant output conductance, which was observed by other authors [89,90] and would have implications for increased RF noise. The surface related traps with activation energy of 0.2 eV accounted for the I_{gLeak} mechanism [10].

The I_D collapse behavior was realized using AC I_{DS}-V_{DS} characteristics [9]. Inset of Fig. 55 shows the output resistance [ratio of knee voltage (V_{knee}) and I_{Dmax}] of passivated and un-passivated HEMTs for different V_{DS}. The I_D reduction with the increase of V_{DS} up to 30 V was high for SiO_2 passivated HEMTs when compared with the other dielectric passivated and un-passivated HEMTs (See Table VIII). The observation of high I_D collapse in SiO_2 passivated HEMTs are due to the effect of surface related traps, which was confirmed by the occurrence of hysteresis in AC I_{DS}-V_{DS} measurements. The V_{knee} variation at a particular I_D is high for SiO_2 passivated HEMTs, Very little variation has been observed in un-passivated HEMTs. The device output power (P_{out}) was calculated with: $P_{out}=(V_{DS}-V_{knee})(I_D/2)$ by fixing the V_{DS}=30 V [9]. Highest P_{out} was observed on Si_3N_4 passivated HEMTs. SiO_2 passivated HEMTs exhibited lowest P_{out}. Bernat et al. [92] were also observed similar behavior with SiO_2 passivation. The hysteresis (looping) effects were observed on both the passivated and un-passivated HEMTs.

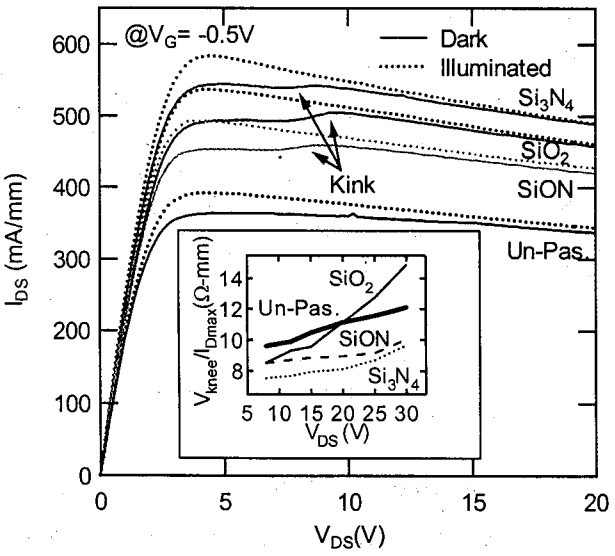

Fig. 55. dc I_{DS}-V_{DS} characteristics of Si_3N4, SiO_2, SiON passivated and un-passivated AlGaN/GaN HEMTs measured at V_g=-0.5V under dark and white-light illumination. Inset is V_{knee}/I_{Dmax} vs. drain sweep voltages (V_{DS}=0-8, 0-12, 0-15, 0-20, 0-25 and 0-30 V) measured from AC I_{DS}-V_{DS} characteristics.

Table VIII. Device dc parameters of SiO_2, Si_3N_4 and SiON passivated and un-passivated AlGaN/GaN HEMTs on sapphire substrate.

Para-meters	I_{Dmax} (mA/mm)	g_{mmax} (mS/mm)	$(I_{dI}-I_{dd})/I_{dI}$ (%) @V_D=4.45V & V_G=-1.5V	V_{th} (V)	V_{th} Vari. (%)	V_{hys} (V) @30V	I_{dAC} Reduc. (%) @V_G=+1.5V & V_D=30V	V_{knee} Vari. (%)	BV_{gd} (V)	P_{out} (W/mm)
Un-Pas.	766	189	7.00	-3.67	1.89	0.68	0.89	6.80	112	4.39
SiO_2	949	205	8.33	-4.19	5.80	2.27	6.83	40.2	132	3.60
Si_3N_4	943	201	6.91	-4.41	1.59	0.70	2.39	19.2	56	4.72
SiON	860	193	8.18	-4.07	3.00	0.08	1.51	20.4	108	4.36

Relatively high P_{out} with low I_D collapse and hysteresis width (V_{hys}) was observed on SiON passivated HEMTs when compared with un-passivated HEMTs. Maximum V_{hys} (2.27V) was observed at V_G=+1.5V for SiO_2 passivated HEMTs (see Table VIII) which indicates the existence of traps. The carrier trapping effects were confirmed using dark and white-light illuminated dc characteristics [9]. Fig. 55 shows the dc I_{DS}-V_{DS} characteristics of un-passivated and passivated HEMTs measured under dark and white-light illumination. The percentage of increase in I_D under illumination was high for SiO_2 and SiON passivated HEMTs when compared with the Si_3N_4 and un-passivated HEMTs (see Table VIII). The kink or current slump was high on passivated HEMTs. Similar behavior was observed on Si_3N_4 passivated AlGaN/GaN HEMTs by Ando et al [93]. There is no kink was observed on un-passivated HEMTs. Due to the occurrence of deep traps, large V_{th} variation with respect to applied V_{DS} was observed for SiO_2 (5.8%) and for SiON (3%) passivated HEMTs. Small I_{gLeak}, small V_{hys}, small V_{th} variation, small kink, small I_D collapse with high P_{out} was observed on Si_3N_4 and un-passivated HEMTs.

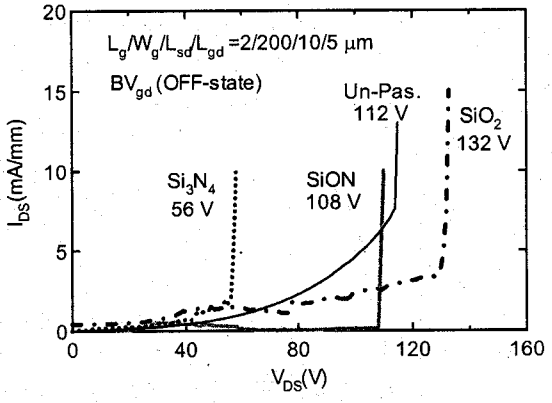

Fig. 56. OFF-state (V_g=-5.5V) breakdown voltage (BVgd) characteristics of Si_3N_4, SiO_2, SiON passivated and un-passivated AlGaN/GaN HEMTs.

Fig. 56 shows breakdown voltage (BV_{gd}) characteristics, was measured on un-passivated and passivated HEMTs at sub-threshold regime (V_G=-5.5V) with L_{gd}=5.0 μm and W_g=200 μm. The SiO_2 passivated HEMTs exhibited high BV_{gd} (See Table VIII) when compared with the passivated (Si_3N_4 & SiON) and un-passivated HEMTs. The observation of low BV_{gd} values on Si_3N_4 passivated HEMTs are due to the occurrence of lateral depletion by shallow traps between gate-drain regions. The observation of high BV_{gd} from SiO_2 passivated HEMTs are due to the formation of deep traps in the SiO_2/AlGaN interface [94]. The enhancement of BV_{gd} (~48%) with

low V_{hys} for SiON (80 mV) passivated HEMTs are probably due to the occurrence of both shallow and deep traps when compared with Si_3N_4 passivated HEMTs. The occurrence of very small V_{hys} on SiON passivated HEMTs are an indication to get high switching speed (see Table VIII). Reasonably good ac and dc characteristics with enhanced BV_{gd} was observed on SiON passivated HEMTs.

3.11. Breakdown Voltage Mechanism of AlGaN/GaN HEMTs on sapphire

The device dimensions used for this study are as follows: source-drain distance (L_{sd})=8.0 μm; gate width (W_g)=15 μm; gate-length (L_g)=2 μm and source-gate distance (L_{sg})=3.0 μm. Fig. 57 shows high voltage drain biased I_G-V_{DS} characteristics of AlGaN/GaN HEMTs measured at sub-threshold regime (at V_{GS}=-6.5 V) for different temperatures 20, 40, 50, and 70 °C. The observation of negative temperature dependence of I_{GLeak} in AlGaN/GaN HEMTs is due to the occurrence of impact ionization phenomena [95-97]. Fig. 58 shows high voltage drain biased I_G-V_{DS} characteristics of HEMTs measured at sub-threshold regime (at V_{GS}=-6.5 V) for different temperatures 120, 150, 200, 300, and 400 °C. Above 80 °C, the I_{GLeak} current started increasing with the increase in temperatures. The positive temperature dependence of leakage currents are due to the temperature assisted tunneling phenomena [89,98,99,100]. Similar temperature dependence of I_D-V_{DS} characteristics (similarly with Fig.57 and Fig.58) has also been observed (not shown here). The negative and positive temperature dependence of drain- and gate-leakage current measured at V_{DS}=50 V and at sub-threshold regime is shown in Figure 59. An activation energy

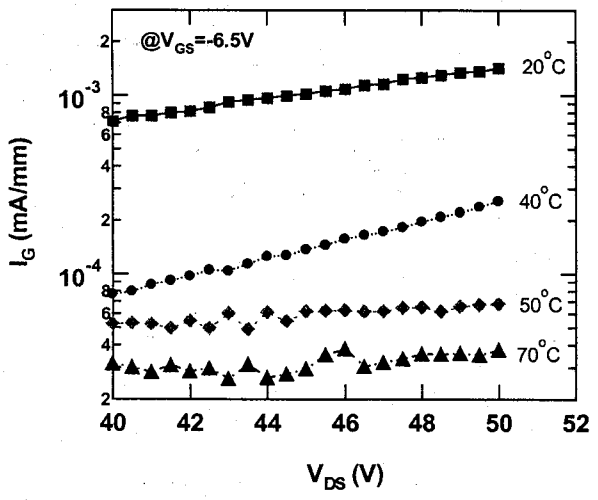

Fig. 57. I_G-V_{DS} characteristics of AlGaN/GaN HEMTs for the gate voltage V_{GS}=-6.5V at different temperatures (20, 40, 50, and 70 °C). I_G values are negative

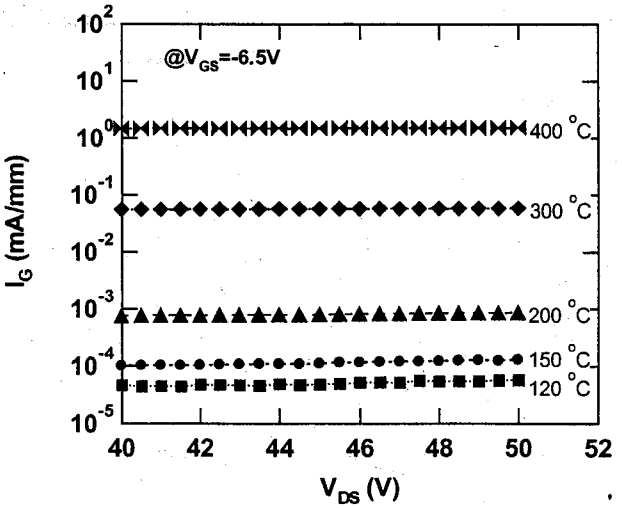

Fig. 58. I_G-V_{DS} characteristics of AlGaN/GaN HEMTs for the gate voltage V_{GS}=-6.5V at different temperatures (120, 150, 200, 300, and 400 °C). I_G values are negative

plot of the I_{GLeak} measured at sub-threshold regime (V_{GS}=-6.5V), is shown in inset of Fig 59. Up to

the temperature of 80 °C, the leakage-current decreases with the activation energy of +0.61 eV. This is due to the occurrence of deep acceptor initiated impact ionization [102]. Trivedi et al. [102] theoretically predicted the avalanche breakdown mechanism on wide band-gap semiconductors namely SiC and GaN. The I_{GLeak} increase-rate is considerably small with the activation energy -0.20 eV, at the temperature between 90-150 °C (See Fig.59).

Table IX. The temperature coefficient of breakdown values for different devices from previous reports. The values with an asterisk denote values obtained in this work.

Device	Temperature coefficient (V/K)	
	Positive	Negative
GaN and AlGaN Diodes	~0.02 [95], ~0.20 [103], 0.0045 [104]	0.34 [99], 6.0 [98]
AlGaN/GaN HEMTs	~0.33 [105], ~0.05 [97], 0.28 *	0.11 [89], ~0.16 [100], 0.53*
AlGaAs/InGaAs HEMTs	-	~0.033 [106]
InGaAsP APDs	~0.042 [107]	~0.02 [107]
InP APDs	~0.029 [107]	-

Similar activation energy (see Table IX) was observed for the temperature range of 20 to 200 °C by Tan et al [89]. The small increase of I_{GLeak} is responsible for surface related hopping conduction [89]. Above 150 °C, the leakage current increases exponentially with an activation energy of -0.99 eV. It is clear that the increase of I_{GLeak} is associated with the temperature assisted tunneling mechanism.[9]

In order to estimate the temperature dependence of the V_B, we used the drain voltage (V_D) at

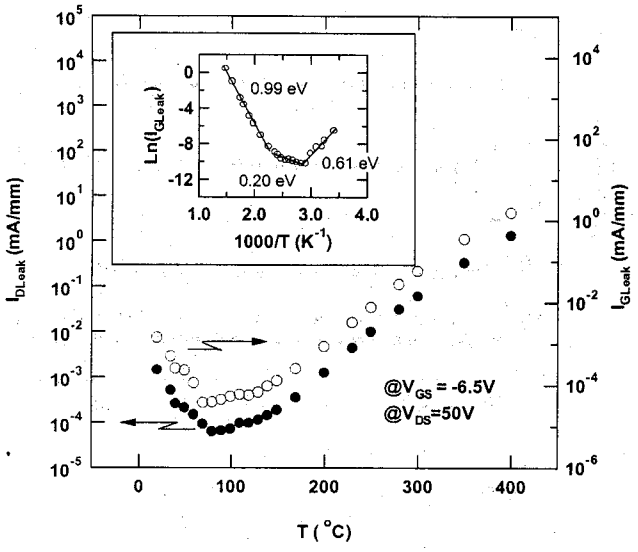

Fig. 59. Drain- and gate-leakage current of AlGaN/GaN HEMTs for V_{DS}=50 V and VGS=-6.5 V (sub-threshold regime).
Inset figure activation energy plot of I_{GLeak} measured at V_{GS}=-6.5 V.

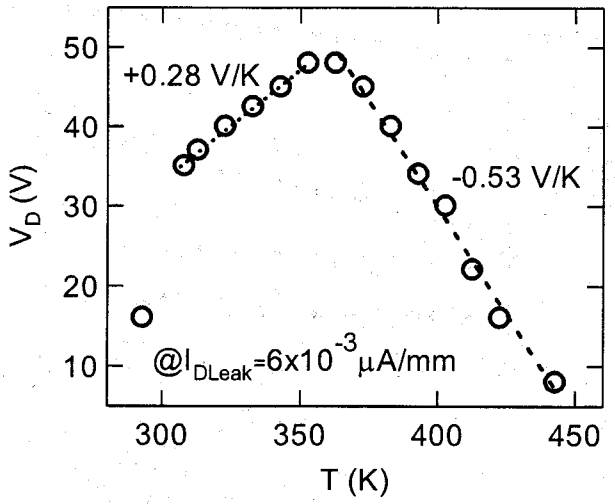

Fig. 60. Drain voltage (V_D) of AlGaN/GaN HEMTs at sub-threshold regime (V_{GS}=-6.5V) for a fixed I_{DLeak} of 6x10^{-3} µA/mm

a fixed I_{DLeak} [105]. The temperature

dependence of the V_D for a fixed I_{DLeak} of 6 x 10^{-3} μA/mm is shown in Fig. 60. Temperature coefficients were calculated and tabulated in Table IX. Up to the temperature of 80 °C, positive temperature coefficient +0.28 V/K of V_D was obtained. Small values of temperature coefficient, as obtained by other researchers [97,104,105] (see Table IX) may be related to the presence of defects related microplasmas [104]. However, Aggarwal et al [103] predicated that the increase of V_B with temperature is ~ 0.20 V/K for the temperature ≥ 200 K. The positive sign of V_D temperature coefficient agrees with the results obtained for a AlGaN/GaN HEMTs [97,105], GaN p-n diode [95], GaN p-n-n^+ diode [103], GaN photodiode [104], InP avalanche photo diodes (APDs) [107] and InPGaAs APDs [107]. This also agrees with the theoretical predictions for the impact ionization process in Si and Ge [108]. For temperatures greater than 80 °C, the devices exhibited negative temperature coefficient of -0.53 V/K. The negative temperature coefficient of V_D agreed with the results obtained for AlGaN/GaN HEMTs [89,100], AlGaAs/InGaAs HEMTs [106], GaN Schottky and GaN p-i-n diodes [99]. This suggests that impact ionization in the channel, rather than gate-tunneling, is the dominant breakdown mechanism up to the temperature of 80 °C. Above 80 °C, gate-tunneling is the dominant breakdown mechanism in the channel. Similar avalanche and tunneling breakdown mechanisms were observed on InGaAsP APDs by Takanashi and Horikoshi [107] for the temperature range of -190 to 23 °C.

3.12. i-GaN/AlGaN/GaN HEMTs with and without surface passivation

The device dimensions used for these studies are as follows: $L_{sd}/L_{sg}/W_g/L_g$=9/3/15/2 μm; $L_{sd}/L_{gd}/W_g/L_g$=10/5/200/2 μm. Good pinch-off high V_{DS} (=40V) *dc* I_{DS}-V_{DS} characteristics of *i*-GaN/AlGaN/GaN HEMTs (W_g/L_g=15/2 μm) with and without SiO_2 passivation are shown in Fig. 61a). The maximum extrinsic transconductance (g_{mmax}) and I_{Dmax} of un-passivated and SiO_2 passivated *i*-GaN/AlGaN/GaN HEMTs are 153 & 137 mS/mm and 623 & 585 mA/mm, respectively (see Table X). The exhibited values of g_{mmax} and I_{Dmax} are consistent with the product of $\mu_H \cdot n_s$=1.5x10^{16} $V^{-1}.s^{-1}$.

For clear visibility, selected pulse I_{DS}-V_{DS} characteristics (V_{DS}=0-12, 0-20, 0-30 and 0-40V) of HEMTs with and without passivation for the gate voltages of V_g=+1.5 and +0.5 V are shown in the Fig.61 b). To quantify the I_D collapse, the knee drain current (I_{Knee}) of HEMTs was determined from pulsed I_{DS}-V_{DS} characteristics (see Fig. 61c)) for different V_{DS}. Table I shows I_{Knee} values measured from static ($I_{Kstatic}$) and pulse (I_{Kpulse}) modes. The filled symbols in Fig. 61c) denote the I_{knee} measured at static mode. Though the percentage of decrease in I_{Kpulse} with respect to $I_{Kstatic}$ is small (~0.13%) for un-passivated AlGaN/GaN HEMTs, the percentage of decrease in I_{Kpulse} is high (~10.75%) for passivated AlGaN/GaN HEMTs. From the estimation of $I_{Kstatic}$ and I_{Kpulse} values, it is clear that the I_D collapse is high for surface passivated AlGaN/GaN HEMTs when compared to

i-GaN/AlGaN/GaN HEMTs with and without surface passivation. Also, no dispersion was observed in *i*-GaN/AlGaN/GaN HEMTs up to the pulse width of 80 μs. From this, we found that

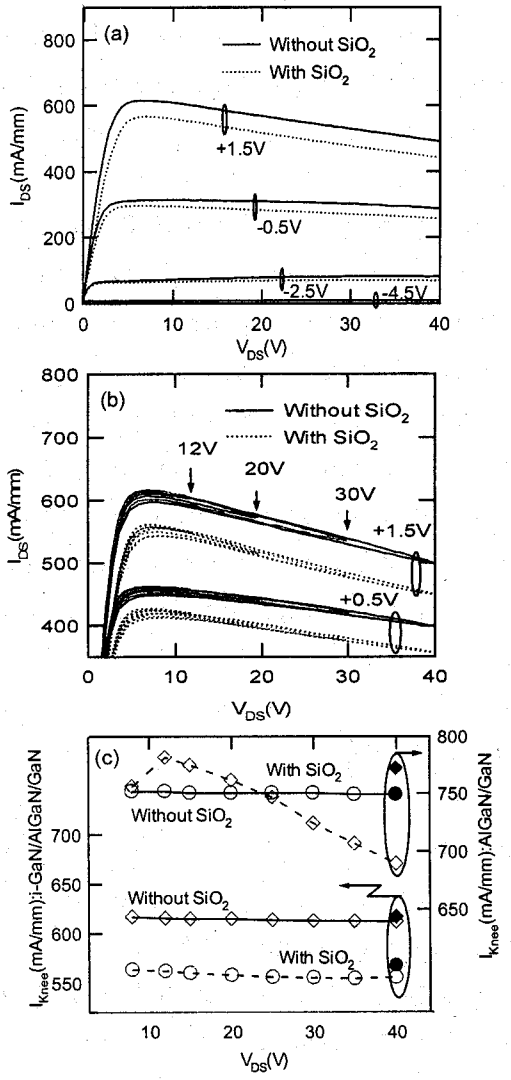

Fig. 61. (a) Good pinch-off static I_{DS}-V_{DS} characteristics of i-GaN/AlGaN/GaN HEMTs with and without SiO_2 surface passivation. (b) Selected VDS (0-12, 0-20, 0-30, 0-40 V) pulsed (120 Hz) I_{DS}-V_{DS} characteristics of i-GaN/AlGaN/GaN HEMTs with and without SiO_2 surface passivation measured at Vg=+1.5 and +0.5V. (c) Knee drain current (I_{knee}) of HEMTs with and without SiO_2 passivation measured from pulsed I_{DS}-V_{DS} characteristics as a function of different drain sweep voltages. Filled symbols are denoting the values from static I_{DS}-V_{DS} characteristics.

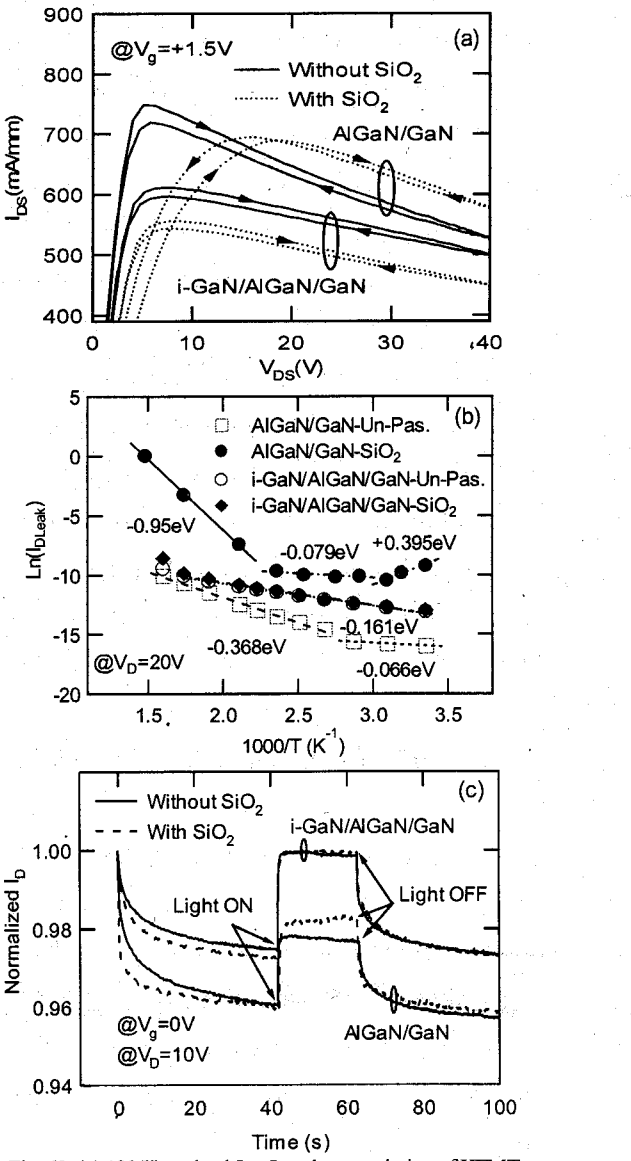

Fig. 62. (a) 120 Hz pulsed I_{DS}-I_{DS} characteristics of HEMTs for Vg=+1.5V. (b) Activation energy plot of both passivated and un-passivated HEMTs for IDleak at Vg= -5.5 V and VDS=20V. (c) Effects of ID transients for white light illumination (ON and OFF).

the traps/charge responsible for the current collapse came from surface/gate electrode. This is confirmed by hysteresis-directions of pulsed characteristics. We have recently demonstrated small I_D collapse in Si_3N_4, Silicon Oxynitride passivated and un-passivated AlGaN/GaN HEMTs [11].

Fig. 62 a) shows the pulsed (120 Hz) I_{DS}-V_{DS} characteristics measured at V_g=+1.5V and V_{DS}=0-40V for *i*-GaN/AlGaN/GaN and AlGaN/GaN HEMTs with and without surface passivation. The clockwise (CW) hysteresis loop was observed on *i*-GaN/AlGaN/GaN HEMTs. A mixture of

counter-clockwise (CCW) and CW hysteresis loop was observed on AlGaN/GaN HEMTs with surface passivation. Moreover, hysteresis width (ΔV_{hys}) is small for both un-passivated and passivated *i*-GaN/AlGaN/GaN HEMTs when compared with the AlGaN/GaN HEMTs (see Table X). The occurrence of very small ΔV_{hys} in *i*-GaN/AlGaN/GaN HEMTs is an indication of high switching speed [11]. From this, it is possible to conclude that the surface states/traps responsible for the current collapse are dominant in SiO_2/AlGaN interface when compared to SiO_2/GaN interface. Thermally activated trap levels were determined from drain leakage current (I_{DLeak}) Richardson's plot (see Fig. 62b). Three and two trap levels were identified in passivated (+0.395, -0.079 and -0.949 eV) and un-passivated (-0.066 and -0.368 eV) AlGaN/GaN HEMTs, respectively. However, *i*-GaN/AlGaN/GaN HEMTs with and without surface passivation exhibited only one trap level at -0.161 eV. The existence of traps with the activation energies of +0.395 and –0.949 eV in the passivated AlGaN/GaN HEMTs are due to the deep acceptor initiated impact ionization and temperature assisted tunneling, respectively [10].

Table X. List of selected parameters for HEMTs with and without SiO_2 passivation.

Passivation Layer	HEMT Structure	I_{Dmax} (mA/mm)	g_{mmax} (mS/mm)	ΔV_{hys} (V) @ V_{DS}=40V	V_{DS} (V) @ I_D=2 mA/mm	BV_{gd} (V)	I_{gLeak} (mA/mm)	I_{Kpulse} (mA/mm) @ V_{DS}=40V	$(I_{Kstatic}-I_{Kpulse})/I_{Kstatic}$ (%)
Without SiO_2	*i*-GaN/AlGaN/GaN	617	153	0.65	62	88	0.94	613	0.65
	AlGaN/GaN	749	189	0.85	77	112	0.032	748	0.13
With SiO_2	*i*-GaN/AlGaN/GaN	565	137	0.66	145	183	0.017	556	2.11
	AlGaN/GaN	772	187	3.48	89	128	10.7	689	10.75

From this, it is clear that, the deep acceptor trap level is responsible for the severe I_D collapse in SiO_2 passivated AlGaN/GaN HEMTs. This is in good agreement with our previously reported results [9]. The increase of I_{DLeak} with activation energies of –0.079 and –0.066 eV are due to the surface based hopping conduction [10]. The I_D transients were performed for a fixed V_{DS}=10V and V_g=0V with white-light switched ON and OFF conditions. Fig 62c) shows the normalized I_D transients of passivated and un-passivated *i*-GaN/AlGaN/GaN and AlGaN/GaN HEMTs. Large transients (~4.0% at 40s) were observed on both un-passivated and passivated AlGaN/GaN HEMTs. However, *i*-GaN cap layer HEMTs with and without surface passivation showed small transients (~2.5-2.7% at 40s). The observation of small transients prevents the formation of depletion region on the surface of the device in the gate-drain region [109]. The percentage of increase in I_D under illumination was high (0.69%) for passivated AlGaN/GaN HEMTs when compared to un-passivated HEMTs. However, the percentage of increase in I_D under illumination

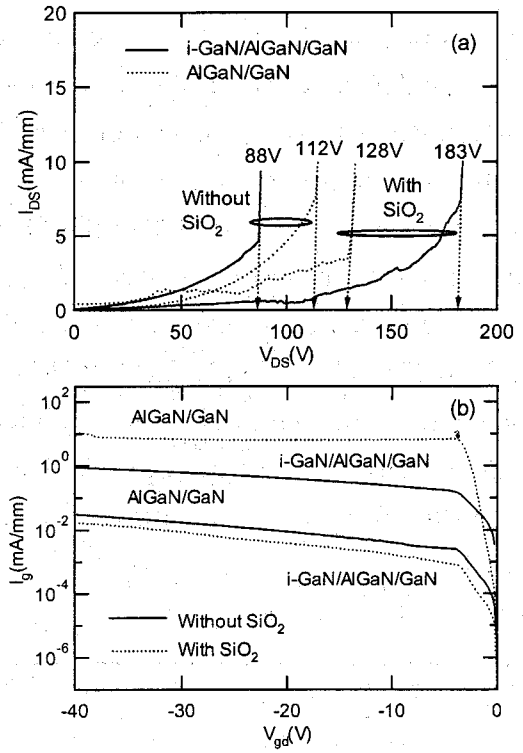

Fig. 63. (a) BV_{gd} characteristics of HEMTs with and without SiO_2 surface passivation measured at Vg=-5.5V. (b) Two terminal gate leakage current (I_{gLeak}) characteristics of HEMTs with and without SiO_2 passivation.

was negligibly small (0.09%) for *i*-GaN/AlGaN/GaN HEMTs. Small transients with small illumination effects lead the suppression of collapse related traps.

Fig. 63a) shows the OFF-state breakdown voltage (BV_{gd}) characteristics of HEMTs with and without SiO_2 passivation measured at sub-threshold regime (V_g=-5.5V) by destroying the devices with identical dimensions: $W_g/L_{sd}/L_{gd}/L_g$=200/10/5/2 μm. More than 50 % improvement in BV_{gd} was observed on the passivated *i*-GaN/AlGaN/GaN HEMTs. Similar improvement was observed in V_{DS} at 2 mA/mm (see table X). The observation of high BV_{gd} for SiO_2 passivated *i*-GaN/AlGaN/GaN HEMTs is due to the occurrence of low gate leakage current. About two orders of low gate leakage current (I_{gLeak}) was observed in *i*-GaN/AlGaN/GaN HEMTs (see table X and Fig. 63b)). A small improvement in BV_{gd} with high I_{gLeak} in passivated AlGaN/GaN HEMTs may be due to the influence of deep traps in SiO_2/AlGaN interface, which depletes the channel vertically [11].

3.13. AlGaN/GaN HEMTs with different Cap layers (i-GaN, n-GaN, p-GaN and InGaN)

3.13.1. Hall Effect, Surface and Schottky contact properties

Table XI shows the values of two dimensional electron gas (2DEG) mobility (μ_H) and 2DEG sheet carrier density (n_s) for AlGaN/GaN HEMT structures with different cap layers (*i*-GaN, *n*-GaN *p*-GaN and InGaN) and the HEMTs without cap layers measured at 300 and 77 K. It is clear to emphasize the electrical properties of HEMT structure using product values of n_s and μ_H, which is an important characteristic of the current carrying capability of the HEMTs. About 16%, 13%, 27% and 15% decrease in $n_s \cdot \mu_H$ values were observed on HEMTs with *i*-GaN, *n*-GaN, *p*-GaN and InGaN cap layer when compared to the HEMTs without cap layers, respectively. The decrease of $n_s \cdot \mu_H$ by the addition of thin cap layer on AlGaN/GaN structure is possibly due to the ionization of few surface states [110,111]. It leads to the reduction of 2DEG mobility of AlGaN/GaN interface. Fig. 64 a), b), c), d) and e) show the AFM micrographs of AlGaN/GaN heterostructures with cap layers of *i*-GaN, *n*-GaN, *p*-GaN, InGaN and without cap layers, respectively. The root mean square surface roughness (R_{MS}) values of AlGaN/GaN heterostructures are tabulated in Table XI. The step flow growth patterns were observed in all sample surfaces except the HEMTs with InGaN cap layer. The InGaN cap layer surface looks like a combination of 2 dimensional island growth and step flow growth patterns. The surface morphology change for the HEMTs with InGaN cap layer is attributed to the growth temperature of InGaN. Similar observations were made on the homoepitaxial growth of GaAs [112]. Low R_{MS} values were observed in AlGaN/GaN with cap layers when compared to the AlGaN/GaN without cap layers. The surface of heterostructure smoothens by the addition of thin cap layer.

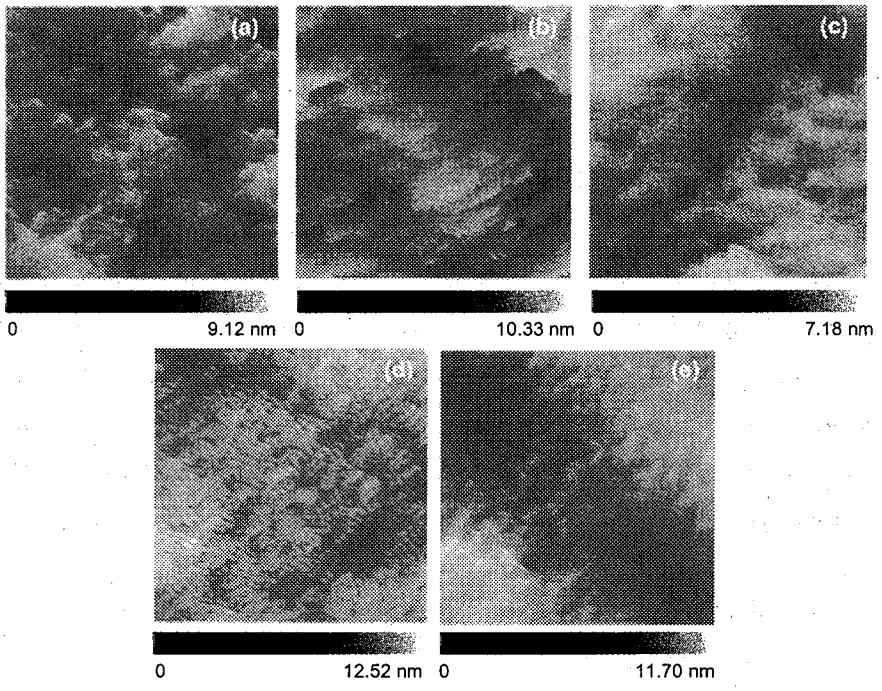

Fig.64. AFM micrograph (scan area= 5 μm X 5 μm) of HEMT surface with cap layers a) *i*-GaN, b) *n*-GaN, c) *p*-GaN, d) InGaN and e) without cap layers.

Table XI. Electrical properties of AlGaN/GaN HEMTs with different cap layers of *i*-GaN, *n*-GaN, *p*-GaN and InGaN and the HEMTs without cap layers.

Cap Layers	μ_H (cm^2/V.s)		n_s ($x10^{13}$ cm^{-2})		$n_s.\mu_H$ @ 300 K ($x\ 10^{16}\ V^{-1}s^{-1}$)	R_{MS} (nm)	P-V distance (nm)	ϕ_B (eV)	R_c (Ω-mm)
	300K	*77K*	*300K*	*77K*					
i-GaN	811	3692	1.75	1.34	1.42	1.16	9.12	0.76	1.82
n-GaN	889	3857	1.65	1.27	1.46	1.38	10.33	0.72	1.47
p-GaN	770	3250	1.69	1.37	1.30	0.99	7.18	0.51	1.30
InGaN	673	2652	2.14	2.02	1.44	0.96	12.52	0.47	1.44
No Cap	1036	4316	1.55	1.35	1.61	1.84	11.70	0.70	1.61

The Schottky barrier height (ϕ_B) was estimated [1,2] and tabulated in Table XI. Improved ϕ_B values were observed in Au/Ti/Pd/*i*-GaN (0.76 eV) and Au/Ti/Pd/*n*-GaN (0.72 eV) Schottky contacts when compared to Au/Ti/Pd/*i*-AlGaN (0.70 eV) Schottky contacts. The increase of ϕ_B can be correlated with the observation of low R_{MS} surface roughness and peak-valley values (see Table XI) of their individual surfaces [64]. Reduced values were observed in Au/Ti/Pd/*p*-GaN (0.51 eV) and Au/Ti/Pd/InGaN (0.47 eV) Schottky contacts. Due to the Schottky-Mott relation, high metal work function (ϕ_M=5.12 eV) metal exhibits low ϕ_B values on *p*-GaN [113.114]. The observation of low ϕ_B in Au/Ti/Pd/InGaN is attributed to the poor quality of InGaN layer. Similarly, low ϕ_B values were observed on Au/InGaN Schottky contacts [115].

Table XII. Selected device parameter (I_{Dmax}, g_m, R_s, I_{gLeak} and BV_{gd}) values of AlGaN/GaN HEMTs with and without cap layers.

Cap Layers	I_{Dmax} (mA/mm)	g_m (mS/mm)	V_{th} (V)	R_s (Ω-mm)	I_{gLeak} (mA/mm) @V_g=-40V	BV_{gd} (V)
i-GaN	568	204	-3.74	2.65	0.017	183
n-GaN	648	249	-3.54	1.88	0.052	114
p-GaN	634	222	-3.81	2.02	0.320	184
InGaN	598	255	-3.10	2.34	0.564	161
No Cap	693	264	-3.78	2.26	10.674	132

3.13.2. dc I_{DS}-V_{DS} characteristics

The device dimensions used for these studies are as follows: $L_{sd}/L_{sg}/W_g/L_g$=9/3/15/2 μm; $L_{sd}/L_{gd}/W_g/L_g$=10/5/200/2 μm. The direct-current (*dc*) and alternative-current (*ac*) I_{DS}-V_{DS} characteristics were carried out on the HEMTs using Agilent 4156c semiconductor parameter analyzer and Sony Tektronix 370A curve tracer, respectively. To study the I_D collapse behavior, the *ac* I_{DS}-V_{DS} measurements [9,11] were carried out on the devices with different drain sweep voltages (V_{DS}=0-4, 0-8, 0-12, 0-15, 0-20, 0-25, 0-30, 0-35 and 0-40 V). For the confirmation of trapping-effects, I_{DS}-V_{DS} characteristics were carried out under white light illumination. The fabricated devices were also characterized at different measurement temperatures.

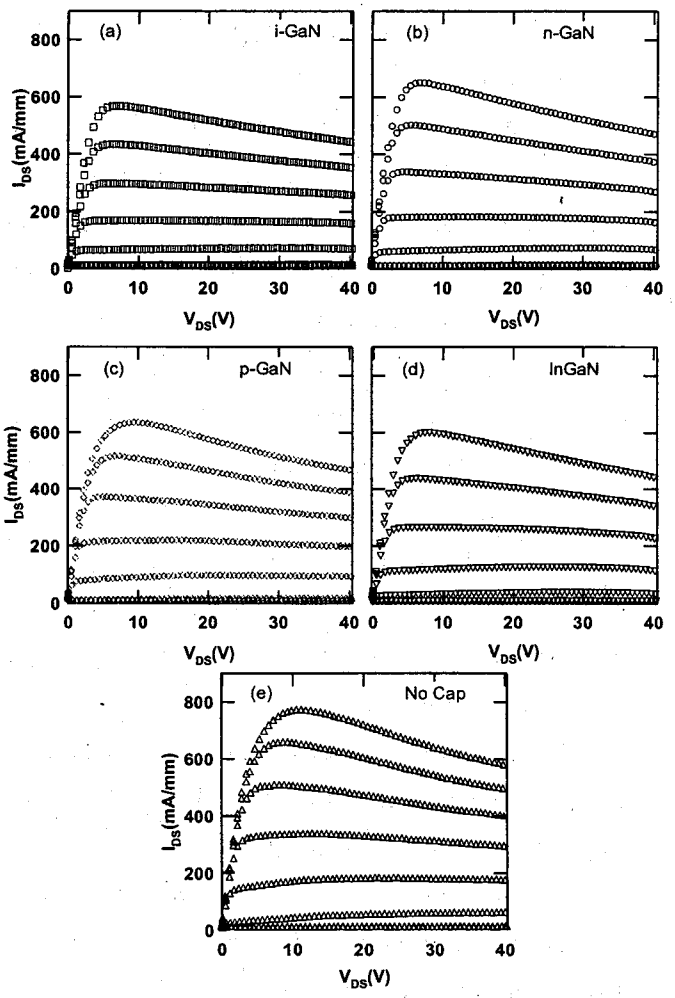

Fig. 65.High drain voltage (40 V) dc I_{DS}-V_{DS} characteristics of HEMTs with cap layers (a) i-GaN, (b) n-GaN, (c) p-GaN, (d) InGaN and (e) without cap layers: Vg=+1.5V, Vg=-1.0V

Fig. 65 shows the high drain-source voltage (V_{DS}=40 V) *dc* I_{DS}-V_{DS} characteristics of 2-μm-gate-length and 15-μm-gate-width AlGaN/GaN HEMTs with a) *i*-GaN, b) *n*-GaN, c) *p*-GaN, d) InGaN cap layers and e) without cap layers. All the devices exhibited good pinch-off characteristics. Table XII shows the device parameters of HEMTs with and without cap layers. More than 10 identical devices each were probed and the average values tabulated. The HEMTs without cap layer exhibited highest maximum drain current density (I_{Dmax}) with maximum extrinsic transconductance (g_m) among the other HEMTs. The decrease of g_m and I_{Dmax} has been observed on the AlGaN/GaN HEMTs with cap layers when compared with the HEMTs without cap layers. The decrease of g_m and I_{Dmax} values agrees with the product values of μ_H and n_s of AlGaN/GaN HEMT structures (see Table XI and XII). The HEMTs with InGaN cap layer shows low I_{Dmax} with high g_m value. This behavior is not clear now. Nearly equal values of I_{Dmax} have been observed on the HEMTs with *n*-GaN and *p*-GaN cap layers. Due to the existence of silicon doping (~4×10^{18} cm^{-3}), low contact (R_c) and source (R_s) resistance values were observed on the HEMTs with *n*-GaN cap layers.

3.13.3. Gate leakage current and Breakdown voltage characteristics

Fig 66 shows the two terminal gate-leakage current (I_{gLeak}) characteristics of 2-μm-gate length and 15-μm-gate width AlGaN/GaN HEMTs with and without cap layers. The I_{gleak} values at -40 V are listed in table XII. Approximately more than one and two orders of low I_{gLeak} was observed on HEMTs with InGaN & *p*-GaN cap layers and *i*-GaN & *n*-GaN cap layers, respectively when compared to the HEMTs without cap layer. This is due to the effect of piezoelectric and spontaneous polarization at cap layer/AlGaN interface [113]. The increase of I_{gLeak} in the HEMTs with doped cap layer is due to the formation of conducting path near the surface of the structure. The high value of I_{gLeak} on the HEMTs with InGaN cap layer may be correlated with the poor quality of InGaN cap layer. The channel can be associated with the lowering of conduction band level relative to the Fermi level in the doped GaN cap layer.[7] Minimum I_{gLeak} of 0.017 mA/mm was observed at V_g=-40V on the HEMTs with *i*-GaN cap layers.

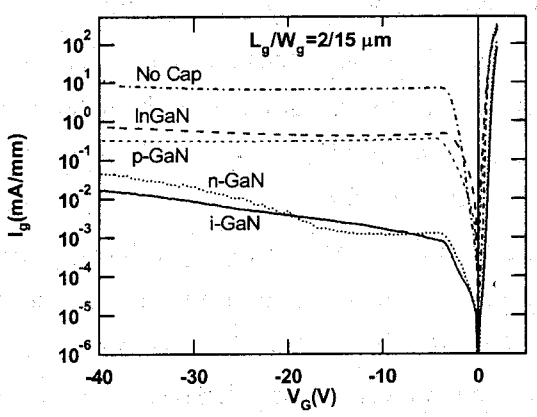

Fig. 66. Two terminal I_{gLeak} characteristics of 15μm-wide-gate AlGaN/GaN HEMTs with and without cap layers.

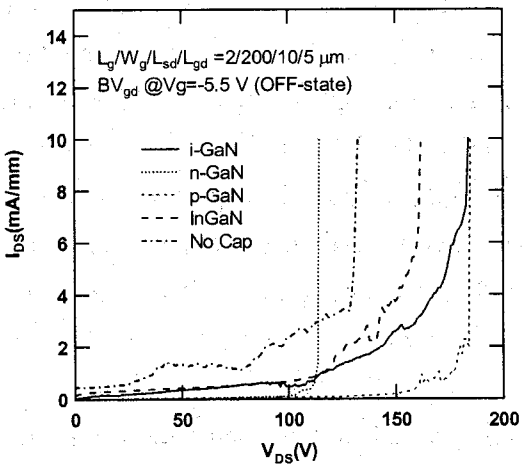

Fig. 67. BV_{gd} characteristics of 200 μm-wide-gate AlGaN/GaN HEMTs with and without cap layers.

Fig 67 shows the breakdown voltage (BV_{gd}) characteristics of HEMTs with and without cap layers measured at sub-threshold regime (V_g=-5.5V) with L_{gd}=5.0 μm and W_g=200 μm. The measured values are tabulated in Table XII. The enhancement of BV_{gd} for HEMTs without cap layers can be explained by vertical depletion by deep traps (from EB-SiO_2 passivation) instead of lateral depletion. However, the effects of passivation layer on the BVgd of HEMTs with cap layers are relatively small, because, all the devices were passivated with EB-SiO_2. The possible reason for the change of BV_{gd} is due to the effect of different cap layers. With respect to the HEMTs without cap layers, an enhancement of BV_{gd} for the HEMTs with *i*-GaN (21%), *p*-GaN (28%), and InGaN (18%) cap layers were observed. The increase of BV_{gd} in the HEMTs with *i*-GaN cap layer is attributed to the reduction of gate leakage current. The observation of surface related deep traps (see the section 3.13.1) in the HEMTs with *p*-GaN and InGaN cap layer depletes the channel vertically instead of lateral depletion [11]. It leads to the enhancement of BV_{gd}. The observation of low BV_{gd} values from the HEMTs with *n*-GaN cap layer (114 V) may be due to

the increase of doping concentration in the drift region by silicon doped ($4x10^{18}$ cm^{-3}) cap layer. The increase of doping level has been confirmed from the observation of low contact resistance (R_c) values (see Table XI) by transfer length method. Impact ionization is the dominant breakdown mechanism for HEMTs without cap layers up to the temperature of 80 °C has been observed and reported [10]. Similar behavior was observed on the HEMTs with *p*-GaN cap layers. Due to the deep acceptor initiated impact ionization, decrease of leakage current with the increase of temperature has been observed on the HEMTs without cap layers and the HEMTs with *p*-GaN cap layers. This has been confirmed with the high temperature I_{DS}-V_{DS} measurements (see also the section 3.13.5) [12]. Further studies are under progress to understand the exact mechanism of BV_{gd} for the HEMTs with different cap layers. The HEMTs with *i*-GaN cap layer exhibited low I_{gLeak} with high BV_{gd} among the other HEMTs. These parameters are a good sign for high-power and high frequency device applications.

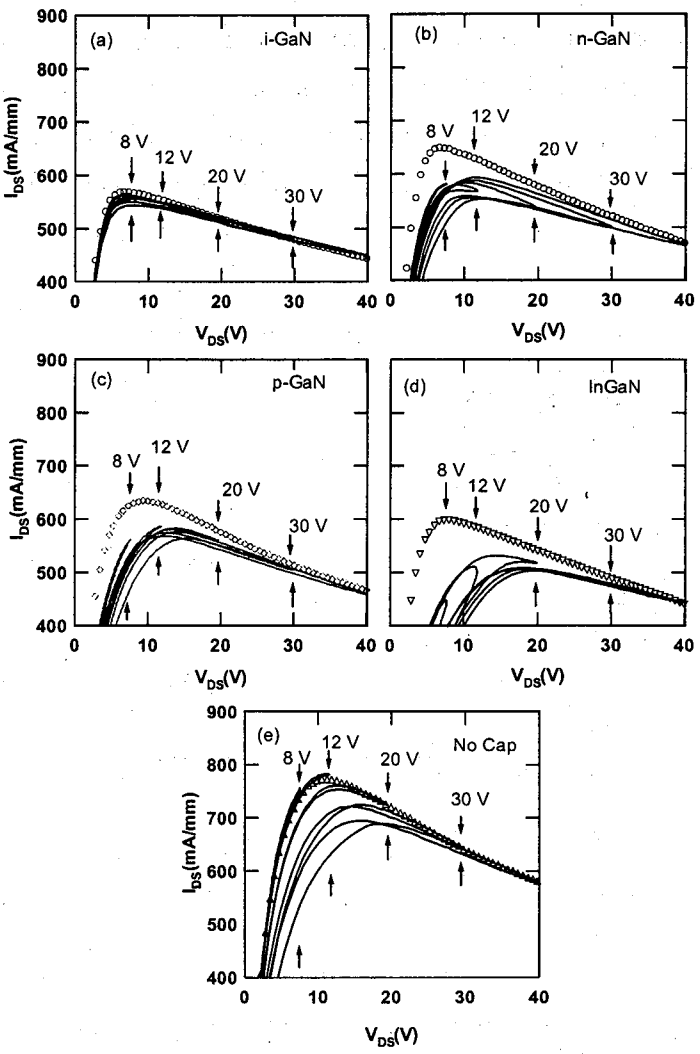

Fig. 68. ac and dc (0-40 V) I_{DS}-V_{DS} characteristics of HEMTs with cap layers (a) i-GaN, (b) n-GaN, (c) p-GaN, (d) InGaN and (e) without cap layers, which was measured at Vg=+1.5V for different drain sweep voltages of 0-8, 0-12, 0-20, 0-30, and 0-40 V.

3.13.4. Drain Current Collapse

High-drain voltage (40 V) applied *ac* I_{DS}-V_{DS} characteristics with good pinch-off were observed on AlGaN/GaN HEMTs with and without cap layers for different V_{DS} of 0-4, 0-8, 0-12, 0-15, 0-20, 0-25, 0-30, 0-35, 0-40 V. For a clear understanding, only few V_{DS} (0-8, 0-12, 0-20, 0-30 and 0-40 V) of *ac* and *dc* (0-40 V) I_{DS}-V_{DS} characteristics of HEMTs with and without cap layers for the gate voltage of V_g=+1.5V are shown in Fig. 68 a), b), c), d) and e). From this graph, we understand that the I_D collapse-free characteristics were observed on AlGaN/GaN HEMTs with *i*-GaN cap layer. We have also reported I_D collapse-free *i*-GaN/AlGaN/GaN HEMTs with and without surface passivation [12]. The knee resistance (R_{knee}=V_{knee}/I_{knee}) of HEMTs with and without cap layers for different V_{DS} are shown in Fig. 69. The increase of R_{knee} measured from *ac*

characteristics (open symbols) are relatively very small (14%) with respect to the R_{knee} measured from *dc* characteristics (filled symbols) for the HEMTs with *i*-GaN cap layers when compared to HEMTs without

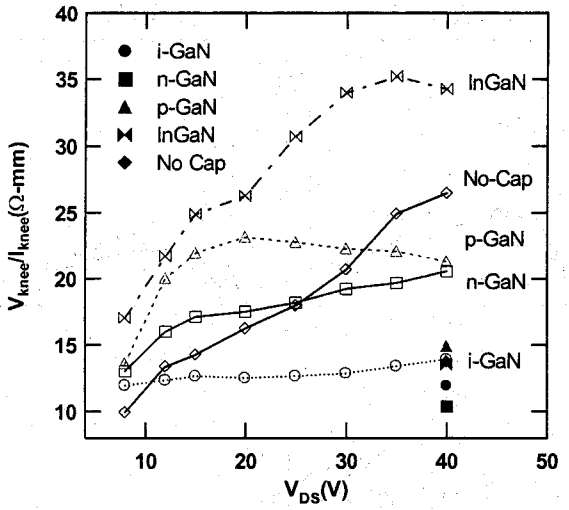

Fig. 69. Knee resistance ($R_{knee}=V_{kee}/I_{knee}$) of HEMTs with and without cap layers as a function of drain sweep voltages. Filled symbols are indicating the values measured from dc I_{DS}-V_{DS} characteristics.

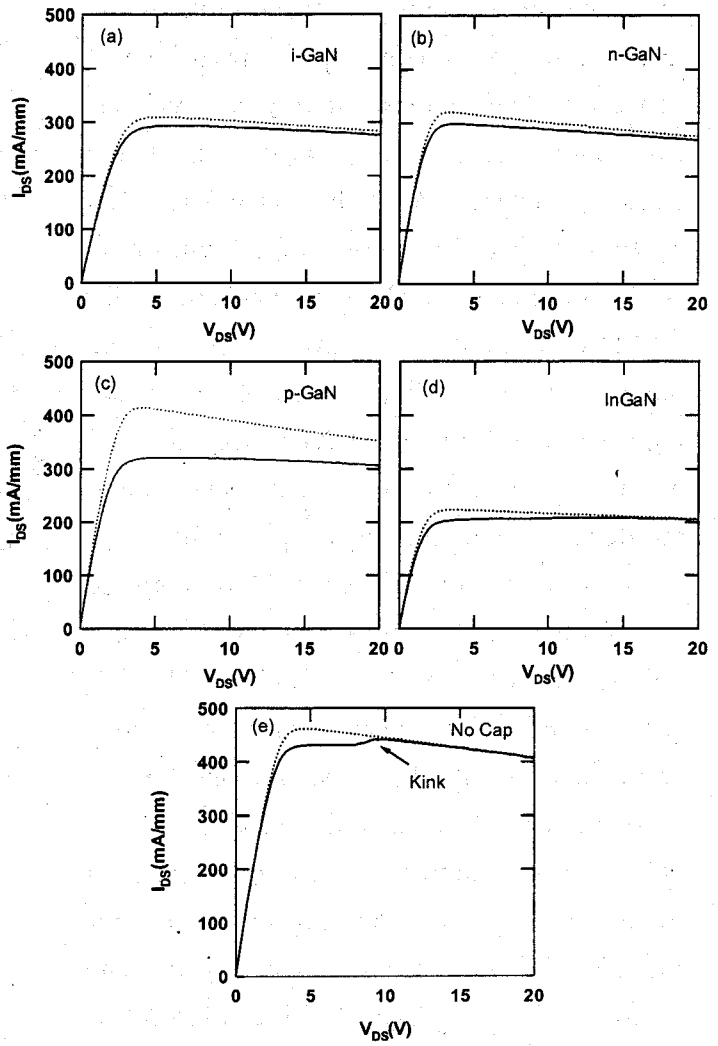

Fig. 70. dc I_{DS}-V_{DS} characteristics measured at V_g=-0.5 V under dark (solid lines) and white light illumination (dotted lines) of HEMTs with cap layers (a) i-GaN, (b) n-GaN, (c) p-GaN, (d) InGaN and (e) without cap layers. It measured at V_g=-0.5V

and with other cap layers. The R_{knee} variation percentages of the devices with respect to the individual *dc* characteristics (filled symbols of Fig. 69) are tabulated in Table XIII. Large increase of R_{knee} was observed on the HEMTs with InGaN cap layers. From this it is found that the HEMTs with *i*-GaN cap layers exhibited free of I_D collapse among the other HEMTs with and without cap layers. Hence, the HEMTs with *i*-GaN cap layers show collapse-free characteristics.

3.13.5. Trapping mechanism

The variation of V_{th} with respect to applied V_{DS} has been observed on these HEMTs (see the table II). Small and large V_{th} variations of 0.23% and 3.46% were observed on *i*-GaN cap layer and without cap layer HEMTs, respectively. The change in V_{th} with V_{DS} is due to the existence of deep traps [11]. From this, it is clear that the HEMTs without cap layer exhibit more collapse-related traps when compared to the HEMTs with cap layer [11]. The trapping effects were confirmed by illuminated I_{DS}-V_{DS} characteristics. Fig. 70 a), b), c), d) and e) shows the *dc* I_{DS}-V_{DS} characteristics of AlGaN/GaN HEMTs with and without cap layers measured under dark and white light

illuminated conditions for the gate voltage of -0.5 V. The percentage of change in drain current under illumination (I_{dI}) with respect to the drain current under dark (I_{dd}) were estimated using the formula $(I_{dI}-I_{dd})/I_{dI}$ (see Table XIII). A 5.83% small increase in I_D under illumination was observed on HEMTs with *i*-GaN cap layer when compared to HEMTs without and with other cap layers. There was no kink or current slump observed on the HEMTs with different cap layers measured under dark conditions. The observation of kink is related to the existence of hot electron injection and trapping in the buffer layer [88]. On the contrary, no kink was observed on un-passivated AlGaN/GaN HEMTs, but the kink was observed on AlGaN/GaN HEMTs passivated with SiO_2, Si_3N_4 and silicon oxynitride [11]. From our experimental results, we found that the kink originated from the occurrence of surface related traps and not from the hot-electron injection from the buffer layer [88]. An addition of thin cap/screen layer is an effective way to suppress the kink effect. The HEMTs with doped cap layers showed high illumination effects when compared to the HEMTs with un-doped cap layer. This may be due to the incorporation of dopant related surface states in the 2DEG channel. The percentage of increase in I_D under illumination was as high as 23% for the HEMTs with *p*-GaN cap layers. This may be the influence of doped acceptors (Mg) in the cap layer. Fig. 71 shows the I_D hysteresis width (ΔV_{hys}) for different HEMTs measured at a fixed I_D (533 mA/mm for *i*-GaN, *n*-GaN and *p*-GaN cap layers; 433 mA/mm for InGaN cap layers; 667 mA/mm for without cap layers) as a function of V_{DS}. The observation of high values of ΔV_{hys} (see Table XIII) from HEMTs without and with InGaN cap layers are due to the existence of deep traps [9,11,116]. An increase of ΔV_{hys} was observed approximately at a V_{DS} of 15 V on the HEMTs without and with the cap layers of *p*-GaN and InGaN. This may be possibly due to the existence of surface related traps.

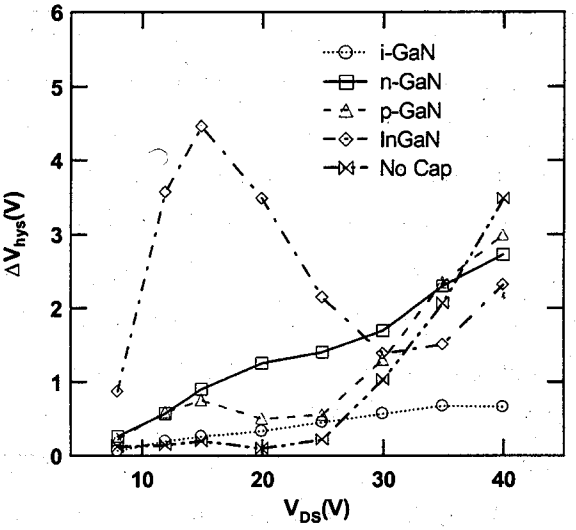

Fig. 71. I_D hysteresis width (ΔV_{hys}) of the HEMTs with and without cap layers as a function of drain sweep voltages

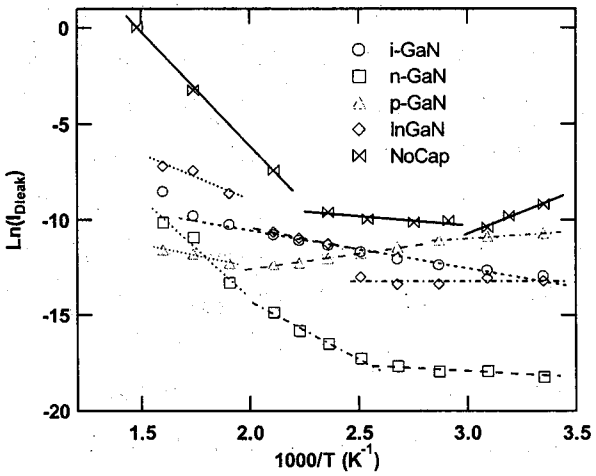

Fig. 72. The drain leakage current activation energy plot (Richardson's plot) for AlGaN/GaN HEMTs with and without cap layers (See Table XIII)

To find out thermally activated energy levels, I_{DS}-V_{DS} characteristics were carried out on HEMTs at different measurement temperatures (room temperature to 350 °C) in N_2 ambient [10,12]. All the devices with and without cap layers except the HEMTs with InGaN cap layers were operational up to the device measurement temperature of 350 °C. No change in the I_{DS}-V_{DS} characteristics measured at room temperature, after thermal treatment of up to 350 °C, were observed on the HEMTs with the cap layers of *i*-GaN, *n*-GaN, *p*-GaN and without cap layers. Increase in leakage current was observed on the HEMTs with InGaN cap layers while measuring at 350 °C and at room temperature after cooling from 350 °C. The device degradation at high temperature measurement is due to the degradation of Schottky contacts with InGaN layer. Fig. 72 shows the Richardson plot for drain leakage current (I_{DLeak}) measured at sub-threshold regime (V_g=-5.5 V) for AlGaN/GaN HEMTs with and without cap layers. The determined energy level values are tabulated in Table XIII. Only one trap level at -0.161 eV was observed on AlGaN/GaN HEMTs with *i*-GaN cap layer [12]. However, more than one thermally activated trap level was observed in HEMTs with other cap layers and without cap layers.

Table XIII. Current collapse related parameters (R_{knee} variation, $(I_{dI}-I_{dd})/I_{dI}$, V_{th} vari., and Thermal Activation Energy) of AlGaN/GaN HEMTs with and without cap layers

The observation of activation energy levels at -0.90 and -0.949 eV from the HEMTs are due to the temperature assisted tunneling [5,10,12]. The activation energy level at -0.51 eV is possibly due to the ionized donor (Si) like defects [10]. The increase of I_{DLeak} with activation energy levels of –0.079, –0.066 and -0.003 eV is due to the surface-based hopping conduction [10]. The deep acceptor related trap level at +0.395 eV was observed in the HEMTs without cap layers [5,10,12]. However, no positive activation energy levels were observed in the HEMTs with cap layers of *i*-GaN, *n*-GaN and InGaN. The HEMTs with *p*-GaN and InGaN cap layers shows the activation energy level at -0.20 eV. The positive temperature dependence of I_{DLeak} with the activation energy -0.20 eV is due to the surface related traps [10,117]. The negative temperature dependence of I_{DLeak} with two activation energy levels at +0.143 and +0.064 eV in the HEMTs with p-GaN cap layers are due to the effect of doped Mg atoms [118]. The HEMTs without cap layers and with n-GaN,

Cap Layers	R_{knee} Var. (%)	$(I_{dI}-I_{dd})/I_{dI}$ (%) @V_g=-0.5V	V_{th} vari. [%]	Max. $\Delta V_{hys}(V)$	Thermal Activation Energy (eV)
i-GaN	14.11	5.83	0.23	0.659	-0.161
n-GaN	49.40	7.17	0.26	2.722	-0.900, -0.511, -0.064
p-GaN	29.95	23.06	0.84	2.987	-0.202, +0.143, +0.064
InGaN	60.45	8.93	1.11	4.463	-0.408, -0.207, -0.003
No Cap	48.14	6.80	3.46	3.481	-0.949, -0.079, +0.395

p-GaN and InGaN cap layers are affected by additional thermally activated trap levels (see the table XIII). These additional traps may be responsible for the observation of current collapse in the HEMTs without cap layers and with other cap layers of n-GaN, p-GaN and InGaN. From the above experimental results, it is concluded that the thin *i*-GaN cap layer screens the 2DEG effectively from collapse-related traps when compared to the HEMTs without and with other cap layers. The *i*-GaN cap layer is suitable for I_D collapse-free AlGaN/GaN HEMTs.

3.14. Recess Etching effects on different cap layer AlGaN/GaN HEMTs

Recess etching was carried out on AlGaN/GaN HEMTs with i-GaN, n-GaN and p-GaN cap layers for 1 min using 5 W BCl_3 plasma. The photo-resist was used as an etch mask for both gate recess and mesa etching. No post etching treatments were done for the removal of discharge-gas-related residues, because no Boron and Cl_2 based residues were observed on low power (5 W) etched samples, which has been confirmed by X-ray Photoelectron Spectroscopy. An average etching rate is 5.04nm/min, which was determined from BCl_3 plasma etched samples with different etching time by measuring thicknesses of etched patterns at 4-5 locations using atomic force microscopy (AFM). To confirm the gate recess depth, 1 MHz capacitance-voltage (C-V) measurements were also carried out on the fabricated Schottky diodes. The measured etching depths from AFM are in agreement with the two dimensional electron gas (2DEG) carrier profile depth, which was measured by C-V measurements (see Table XIV). The gate metals of Pd/Ti/Au (40/20/60 nm) were optically defined using lithography through conventional lift-off method. High temperature (up to 500 °C) stable Pd/AlGaN and Au/Ti/Pd/AlGaN/GaN [11] Schottky diodes were obtained and reported elsewhere. Before loading for the evaporation of gate and ohmic metals, the samples were dipped in conc. HCl solution for 60 s to remove the native oxide. The device dimensions used for these studies are as follows: $L_{sd}/L_{sg}/W_g/L_g$=9/3/15/2 μm; $L_{sd}/L_{gd}/W_g/L_g$=10/5/200/2 μm.

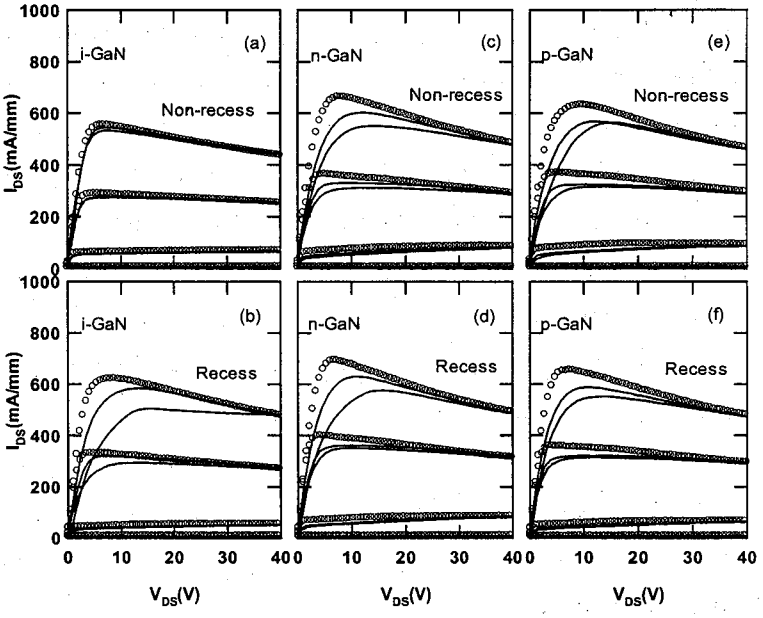

Fig.. 73. Good pinch-off dc (open circles) and pulsed (solid line) I_{DS}-V_{DS} characteristics of (a) i-GaN cap layer (non recess), (b) i-GaN cap layer (recess) c) n-GaN cap layer (non-recess), (d) n-GaN cap lyare (recess), (e) p-GaN cap layer (non-recess) and (f) p-GaN cap layer (recess) on AlGaN/GaN HEMTs. Top Vgs=+1.5 V and the step =-2 V.

Fig.73 a), b), c), d), e) and f) shows the respective good pinch-off high V_{DS} *dc* (open circles) and pulsed (solid lines) I_{DS}-V_{DS} characteristics of *i*-GaN, *n*-GaN and *p*-GaN cap layer HEMTs (W_g/L_g=15/2 μm) with and without gate recess etching. The device parameter values of different cap layers HEMTs with and without gate recess process are tabulated in Table XIV. The threshold voltage (V_{th}) was positively shifted on the recessed gate HEMTs. Due to the reduction of parasitic/source resistance (R_s) by gate recess etching, increase of g_{mmax} and I_{Dmax} were obtained in all gate recessed HEMTs [57,119]. The knee resistance ($R_{knee}=V_k/I_k$) of pulsed I_{DS}-V_{DS} characteristics of individual drain-source sweep voltage (V_{DS}=0-8, 0-12, 0-15, 0-20, 0-25, 0-30, 0-35 and 0-40 V) were measured on recess and non-recess gate devices. Fig. 74 shows the R_{knee} as a function of V_{DS} for a) *i*-GaN, b) *n*-GaN and c) *p*-GaN cap layer grown AlGaN/GaN HEMTs with and without gate recess etching. After gate recessing, the decrease of I_D collapse was observed on n-GaN and p-GaN cap layers HEMTs when compared to the non-recessed gate HEMTs. However, increase of I_D collapse was observed in *i*-GaN cap layer HEMTs after gate recess process. The increase of I_D collapse is due to the increase of collapse related traps by gate recess etching. The decrease of I_D collapse may be due to the reduction of collapse related traps through compensation by gate recess etching. Okamoto *etal* [120]. has observed a decrease in I_D collapse on both recessed gate and non-recessed gate AlGaN/GaN HEMTs.

The trapping effects in recess and non-recess gate devices were confirmed qualitatively by white light illuminated I_{DS}-V_{DS} characteristics. Fig. 75 shows the *dc* I_{DS}-V_{DS} characteristics of a) *i*-GaN, b) *n*-GaN, c) p-GaN cap layer HEMTs with gate recess etching measured under dark and white light illuminated conditions for the gate voltage of -0.5 V. The percentage of change in drain current under illumination (I_{dI}) with respect to the drain current under dark (I_{dd}) were estimated using the formula $(I_{dI}-I_{dd})/I_{dI}$ (see Table XIV). High percentage (15.30%) of I_D under illumination was observed on gate recessed *i*-GaN cap layer AlGaN/GaN HEMTs.

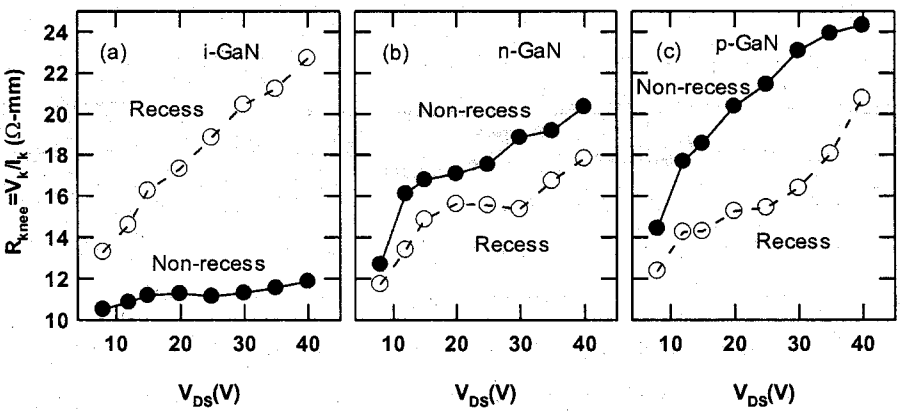

Fig. 74. Knee resistance (R_{knee}) as a function of V_{DS} for recess and non-recess gate (a) i-GaN cap layer (b) n-GaN cap layer and (c) p-GaN cap layers grown AlGaN/GaN HEMTs

Table XIV. Device dc parameters of *i*-GaN, *n*-GaN and *p*-GaN cap layer grown AlGaN/GaN HEMTs with and without gate recess process.

Cap Layers	BCl_3 Plasma	I_{Dmax} (mA/mm)	g_m (mS/mm)	V_{th} (V)	R_s (Ω-mm)	I_{gLeak} (mA/mm) @V_g=-40V	$(I_{dI}-I_{dd})/I_{dI}$ (%)
i-GaN	Non-recess	568	204	-3.74	2.65	0.017	5.83
	Recess	624	240	-3.35	2.36	5.76	15.30
n-GaN	Non-recess	648	249	-3.54	1.88	0.052	7.17
	Recess	695	266	-3.34	1.73	4.49	4.28
p-GaN	Non-recess	634	222	-3.81	2.02	0.320	23.06
	Recess	657	254	-3.32	1.93	5.77	7.33

However, non-recessed gate HEMTs shows small percentage (5.83%) of I_D under illumination (see Table XIV). The observation of decrease in I_D under illumination after gate recess etching on doped (*n*-GaN and *p*-GaN) cap layer HEMTs are due to the compensation of dopant or collapse related traps. From this, we understand that the doped cap layers are suitable for gate recess AlGaN/GaN HEMTs process. Due to the observation of I_D collapse-free AlGaN/GaN HEMTs, thin *i*-GaN cap layer is suitable for non-recess gate process. An increase of gate leakage current (I_{gLeak}) was observed in all gate recessed HEMTs (see Table XIV). However, Okamoto etal. [120] observed the reduction of I_{gLeak} after gate recess etching. The increase of I_{gLeak} is due to the BCl_3 plasma induced damage. Similar results have been observed on Pd/*n*-GaN Schottky diodes [121].

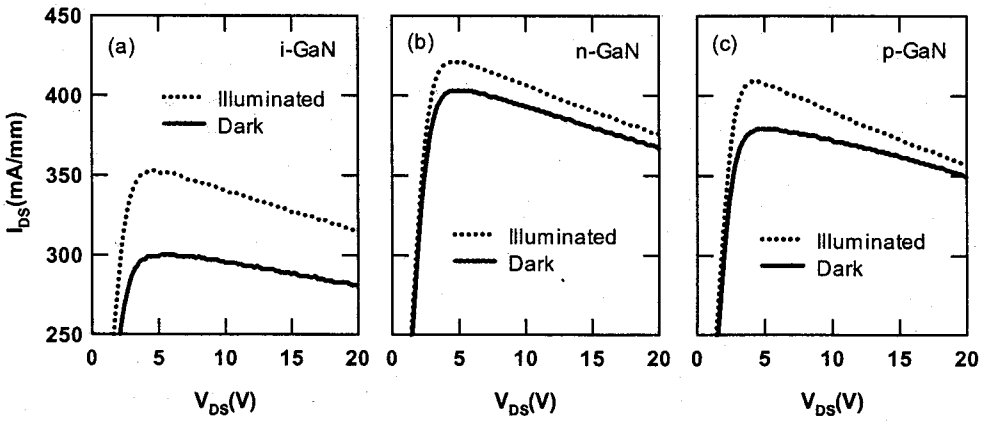

Fig. 75. Dark and white-light illuminated I_{DS}-V_{DS} characteristics of (a) i-GaN cap layer, (b) n-GaN cap layer and (c) p-GaN cap layer grown AlGaN/GaN HEMTs with and without gate recess measured at -0.5V gate voltage.

4. Summary

Investigations of AlGaN/GaN high-electron-mobility transistors (HEMTs) have been performed on different substrates such as 2-inch diameter sapphire, 2-inch diameter semi-insulating (SI) SiC, 4-inch diameter sapphire and 4-inch diameter Si substrates. We have presented the good rectifying Schottky contacts of *n*-GaN and *n*-$Al_{0.11}Ga_{0.89}N$ using different metals such as Ag, Ti, Au, Pd and Ni. $Al_{0.11}Ga_{0.89}N$ Schottky barrier height values are bit higher than the values of GaN contacts except Ti contacts. Schottky characteristics of *n*-$Al_{0.11}Ga_{0.89}N$ using different metals are the first reports in the literature. From the value of S-parameter and density of surface states, Fermi-level pinning has been observed for both GaN and $Al_{0.11}Ga_{0.89}N$ Schottky contacts. The surface pinning of n-GaN and n-$Al_{0.11}Ga_{0.89}N$ would expected to be much less than GaAs, Si and GaP, but similar to CdS. Rectifying behavior has been observed up to the annealing temperature 450 °C/1 hr for Ni/*n*-$Al_{0.11}Ga_{0.89}N$ and 500 °C/1 hr for both Ti and Pd/n-$Al_{0.11}Ga_{0.89}N$ Schottky diodes. From the experimental results, we understand that Ni and Pd metal will be a good Schottky metal for high temperature (up to 450 °C) $Al_xGa_{1-x}N$/GaN based device structures. From the experimental results, we understand that $Al_{0.11}Ga_{0.89}N$ surface is behaving more like ceramic than semiconductor.

The higher Al-content (34%) in AlGaN barrier layer is suitable to get high current/power AlGaN/GaN HEMTs. Better AlGaN/GaN HEMTs was obtained from SI-SiC based AlGaN/GaN HEMTs when compared to the HEMTs on sapphire and Si. The HEMTs on SI-SiC exhibited a high transconductance and drain current density of 287 mS/mm and 857 mA/mm, respectively. From the mass production point of view, uniformity of material and device characteristics of AlGaN/GaN HEMTs was performed on one fourth of 4-inch diameter sapphire grown AlGaN/GaN HEMTs. The observed average maximum drain current density, extrinsic transconductance and threshold voltage values for HEMTs on 4-inch sapphire were 515 mA/mm, 197 mS/mm and -2.30 V with standard deviations 9.34%, 4.82% and 6.52%, respectively. Enhancement of OFF-state breakdown voltage in AlGaN/GaN HEMTs with the increase of buffer AlN thickness was observed on 4-inch Si substrates. The AlGaN/GaN HEMTs on 4-inch Si substrates with thicker AlN buffer layer (crack free) is promising for high power switching device applications. Highest device surface temperature (T_D) of 74 °C at V_{DS}=20 and V_{GS}=+1.5 V was observed on sapphire based 400-μm-wide AlGaN/GaN HEMTs. However, small T_D of 41 °C was observed on Si based 400-μm-wide HEMTs. Though the Si based HEMTs characteristics are not up the extent of sapphire based HEMTs, the amount of heat dissipation from the device is good. The 4-inch diameter Si is an alternative substrate for the fabrication of low cost AlGaN/GaN HEMTs based high power and high frequency applications. Although the HEMTs on SiC exhibited better dc characteristics up to the temperature of 300°C compared with sapphire-based HEMTs, similar dc characteristics were observed on both the HEMTs at and above 300°C. For

high-temperature applications (≥300°C), additional cooling arrangements are essential for both devices. The g_{mmax} and I_{Dmax} values increase towards the periphery of the wafer, which is consistent with the product values of $\mu_H.n_{sHall}$. The Hall and TLM measured sheet resistance of the AlGaN/GaN HSs were in good uniformity with the standard deviations of 9.01 and 9.43%, respectively. The uniformity of HEMTs dc properties were in good correlation with the electrical characteristics of AlGaN/GaN heterostructures, which was obtained from the Hall Effect and Capacitance-Voltage measurements. In conclusion, the fabricated AlGaN/GaN HSs on 4-inch sapphire by MOCVD are suitable for the mass production of high power microwave device applications.

Small drain current collapse device were fabricated on SiC substrates when compared to the devices on sapphire substrates. The positive (+0.28 V/K) and negative (-0.53 V/K) temperature coefficients of drain voltage have been realized at a fixed drain-leakage current (6 x 10^{-3} μA/mm) of AlGaN/GaN HEMTs on 2-inch sapphire substrates. This leads to the occurrence of both avalanche and tunneling breakdown mechanism in the HEMTs on sapphire substrates. Currently, the epitaxial growth and the device process have been optimized to get drain current collapse free AlGaN/GaN HEMTs on sapphire substrates. The suppression of drain current collapse studies were observed on passivated AlGaN/GaN HEMTs using different dielectric layers such as plasma enhanced chemical vapor deposition (PECVD) SiO_2, Si_3N_4 and silicon oxy nitride (SiON). The SiON is a very promising candidate as a surface passivant for AlGaN/GaN HEMTs because it shows better breakdown with small current collapse than Si_3N_4 passivated HEMTs. Drain current collapse free *i*-GaN/AlGaN/GaN HEMTs with and without surface layer passivation was demonstrated on sapphire substrates. The observation of low I_{gLeak}, high BV_{gd} and free of drain current collapse AlGaN/GaN HEMTs with *i*-GaN cap layers will be a suitable candidate for high-power, high-temperature and high-frequency device applications. For drain current collapse-free devices, non-recessed gate process is suitable for AlGaN/GaN HEMTs with *i*-GaN cap layer. To get enhanced power with low drain current collapse, the gate recess etching process is suitable for doped cap layers based AlGaN/GaN HEMTs.

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