Chapter 5

GaN MOS Structures

5.1 Introduction

GaN has attracted much interest for high-temperature and high-power electronic applications because of its outstanding properties, such as a wide band gap of 3.39 eV, a high breakdown field of $5x10^6$ V/cm, and a high saturation drift velocity of $2.7x10^7$ cm/s [1,2]. Recently, a number of GaN field-effect transistors (FETs) such as hetero bipolar transistors, metal-oxide-semiconductor heterostructure FETs, and metal-oxide-semiconductor (MOS) FETs have been reported [3-6]. In particular, the GaN MOS structure equipped with a surface inversion mode as a minority-carrier channel is very important for high-power switching applications in EV electronics since it would provide for lower leakage currents and reduce power consumption, enabling normally-off operation with high blocking voltage even at high temperatures. However, the potential of advanced GaN MOS devices has been yet hard to garner because of inferior insulators and insulator/GaN interfaces. The first GaN MOS structure using a gate insulator consisting of deposited Ga_2O_3 (Gd_2O_3) has been reported by Ren *et al.* [5]. Since then, several approaches have been employed to develop an insulator/GaN MOS structure using either a GaN native oxide (β-Ga_2O_3) or a deposited insulator using Ga_2O_3 (Gd_2O_3), AlN, SiO_2, Si_3N_4, Pb(Zr,Ti)O_3, PBT (p-phenylenebenzobisthiazole), MgO, and Sc_2O_3 in view of gate insulator materials [6-18]. However, none exhibits optimal characteristics. The bottlenecks have been surface Fermi-level pinning at the insulator/GaN interface, which is a well-known problem with most GaN, and poor insulator quality. Thus, both issues need to be overcome for the fabrication of advanced GaN MOS devices. In particular, conventional GaN MOS structures have been found to have a large interface state density on the order of 10^{12} $eV^{-1}cm^{-2}$, resulting in the Fermi-level pinning

at the GaN surface. In addition, in-depth data on the electrical properties of the GaN MOS structures have not yet been reported. In this chapter, we have focused on the electrical characterization of some kinds of GaN MOS structures. First, in section 5.2, we investigate the interface properties of conventional SiO_2/n-GaN MOS structures by using capacitance-voltage (*C-V*) and capacitance transient techniques [19].

Among a number of GaN MOS structures that have been previously reported, a thermal dry-oxidation technique used for β-Ga_2O_3 formation has only limited success on GaN and has been proven to reduce the interface trap by more than one order of magnitude compared to the other deposition methods in addition to its simple and easy way [8]. β-Ga_2O_3 is generally known to have a wide band gap of 4.7 eV at room temperature [20]. Depending on growth conditions, β-Ga_2O_3 can be an insulator or a semiconductor; growing under oxidizing conditions results in insulating β-Ga_2O_3, while that grown under reducing conditions is semiconductive. Thus, the β-Ga_2O_3 layer grown by thermal dry oxidation might be expected to exhibit intrinsic properties with applications in dielectrics especially important for the MOS characteristics. However, in-depth data on the electrical properties of the thermally oxidized GaN MOS structures have not yet been reported. In section 5.3, the interface properties of the thermally oxidized n-GaN MOS structures have been investigated electrically, and the results are compared to those of sputtered SiO_2/n-GaN MOS structures [18].

Regarding interface states at the GaN MOS interfaces, thermal dry and photoelectrochemical (PEC) oxidation of GaN is known to be effective in reducing the interface state density at the β-Ga_2O_3/GaN interface [7,8,15,21-24]. In section 5.3, the thermally grown β-Ga_2O_3/n-GaN MOS structures have been proven to display a low interface state density on the order of 10^{10} $eV^{-1}cm^{-2}$, resulting in an unpinning of the surface Fermi-level at the β-Ga_2O_3/n-GaN interface [18]. In a narrow sense, the interfacial Ga-oxynitride layer is considered to play a significant role in improving the electrical interface properties. However, β-Ga_2O_3/n-GaN MOS structures also showed relatively large gate leakage current compared to that of the SiO_2/n-GaN MOS structures, which may be caused by a poor quality of β-Ga_2O_3 layer and a small conduction-band offset of ~0.9 eV between GaN and β-Ga_2O_3, bearing in mind that β-Ga_2O_3 has a band gap

of 4.7 eV at room temperature [20]. Therefore, a stacked gate insulator consisting of β-Ga_2O_3 and well-known dielectric SiO_2 might be expected to improve the gate dielectric characteristics [25,26]. That is, in the SiO_2/β-Ga_2O_3/n-GaN MOS structures, the β-Ga_2O_3 interlayer can provide good electrical interface properties and the SiO_2 layer should reduce gate leakage currents and enhance oxide breakdown voltages, resulting in overcoming the troublesome issues of GaN-based MOS structures, as stated earlier. However, an in-depth study on the electrical properties of the SiO_2/β-Ga_2O_3/n-GaN MOS structures have not yet been reported. In section 5.4, we have fabricated the stacked SiO_2/β-Ga_2O_3/n-GaN MOS structures by using thermal dry oxidation and SiO_2 deposition techniques, and have investigated the characteristics of SiO_2/n-GaN interfaces with β-Ga_2O_3 interlayers, in comparison with those of conventional SiO_2/n-GaN interfaces [27].

The p-GaN MOS structure, important for power switching devices, is generally known to show no surface inversion due to the extremely slow thermal generation of minority carriers caused by the wide band gap of 3.39 eV [10]. Recently, Kim *et al.* have reported that MgO/p-GaN and Sc_2O_3/p-GaN gate-controlled MOS diodes with n^+ source regions show inversion behavior at room temperature [16,17]. In their reports, the selective-area Si-implanted regions play an effective role to provide an external source of minority carriers. However, the bottlenecks in these diodes may be a large interface state density on the order of 10^{12} $eV^{-1}cm^{-2}$ and poor electrical activation of the Si-implanted regions, resulting in the large onset voltages of surface inversion. Regarding interface states, thermal dry oxidation of GaN is known to be effective in reducing the interface trap at the β-Ga_2O_3/GaN MOS interface, as stated above [8,21]. In section 5.3, the thermally grown β-Ga_2O_3/n-GaN MOS structures have been proven to display a low interface state density on the order of 10^{10} $eV^{-1}cm^{-2}$ [18]. In addition, an improvement of n-type implantation-doping characteristics for the n^+ source is needed to form a satisfactory n^+p junction under the gate insulator. From this point of view, we have also reported that co-implantation of Si+N and subsequent annealing at high temperatures enhance electrical n-type activation and structural properties of the implanted regions, based on a site-competition effect, as stated in section 2.3. [28-30]. Thus, the thermally oxidized p-GaN MOS structures with n^+ source

regions fabricated by using thermal dry oxidation and Si+N co-implantation techniques might be expected to garner their outstanding potential. β-Ga_2O_3 has a wide band gap of 4.7 eV at room temperature and a dielectric constant of 10.2 - 14.2 [20]. Therefore, a thermally grown β-Ga_2O_3 layer is expected to exhibit intrinsic properties with applications in dielectrics especially important for GaN MOS devices. The issue as to whether or not the β-Ga_2O_3/GaN MOS structures easily have a surface inversion mode should depend on their interface properties. However, in-depth data on the electrical properties of the thermally oxidized p-GaN MOS structures have not yet been reported. In section 5.5, we have fabricated thermally oxidized p-GaN MOS diodes with n^+ source regions by combining Si+N co-implantation and thermal dry oxidation techniques, and have investigated their interface properties electrically [22].

5.2 SiO_2/n-GaN MOS Structures

5.2.1 Experimental

The epitaxial GaN films were grown by atmospheric pressure metal-organic chemical-vapor deposition (MOCVD) on a-plane sapphire substrates. First a 20 nm AlN buffer layer was deposited at 400 °C, and then Si-doped 3-μm-thick GaN layer was grown at 1050 °C as an active layer. The GaN active layer had free electron concentrations of ~7.6×10^{17} cm^{-3}, mobilities of ~440 cm^2/Vs and threading dislocation densities of 2-5×10^9 cm^{-2} as determined by room-temperature Hall-effect measurements and transmission electron microscopic observations. The Si concentration was also confirmed to be ~6.8×10^{17} cm^{-3} by secondary ion mass spectrometry measurements. After growth, lateral dot-and-ring GaN MOS diodes were fabricated as shown in Fig. 5.1. First a 100-nm-thick SiO_2 layer was deposited on the top surface of the GaN samples as a gate insulator by radio-frequency sputtering using an SiO_2 target. The sputtering conditions are shown in Table 5.1. The SiO_2 layer was selectively removed by wet-etching using a photolithographic technique for ohmic contact directly on the GaN active layer, and then Al metal was evaporated through a shadow mask to provide gate and ohmic electrodes. The dot gate electrode was 500 μm in diameter, and was surrounded by the ring ohmic electrode. After metallization, the MOS samples were annealed at 450 °C for 30 min in a

nitrogen atmosphere.

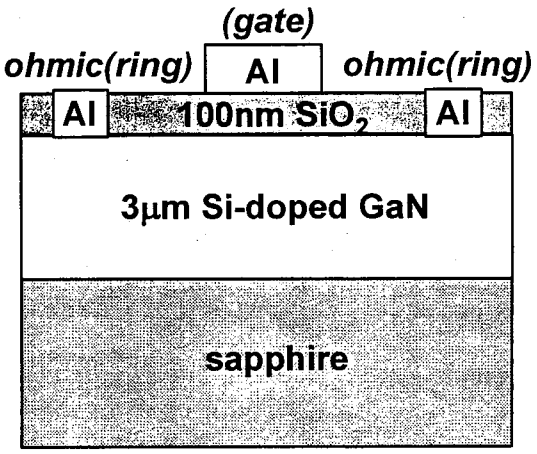

FIG. 5.1. Schematic cross-section of an SiO_2/n-GaN MIS diode fabricated.

TABLE 5.1. Sputtering conditions for deposition of an SiO_2 gate layer

Parameter	Set value
Target-Substrate Distance (mm)	40
Base Pressure (Torr)	$< 2x10^{-6}$
Substrate Temperature (K)	300
Sputtering Gas	Ar-30%O_2
Processing Pressure (Torr)	$7x10^{-3}$
Input RF-Power (W)	200

The fabricated SiO_2/GaN MOS diodes were characterized by means of current-voltage (*I-V*), *C-V*, capacitance-time (*C-t*) and deep-level transient spectroscopy (DLTS) techniques. The *I-V* measurements

were carried out in the dark at a voltage step of 0.1 V under a conventional dc mode. On the *C-V* measurements, conventional *C-V* (normal *C-V*) and pulsed *C-V* [31] methods have been employed. Both the measurements were performed in the dark at a frequency of 1 MHz and a voltage step of 0.1 V with various delay time t_d. On the pulsed C-V measurements, one unit of the pulse pattern consists of two stages, as shown in Fig. 5.2. At first stage, a pulsed voltage of +20 V is applied to approach an accumulation region temporarily. The holding time t_h is fixed at 1 ms. Sequentially, bias voltage is applied and the capacitance is measured after t_d. The bias voltage and t_d are independently varied. Photo *C-V* measurements were also conducted under white light illumination by using a mercury lamp. In addition, to evaluate time dependence of charging and discharging in deep depletion at the SiO_2/GaN interface, conventional *C-t* measurements were performed in the dark by using the pulsed *C-V* technique, as stated above. Furthermore, DLTS measurements were carried out at temperatures between 85 and 475 K under the same condition as the *C-t* measurements to investigate deep-level centers at the SiO_2/GaN interface.

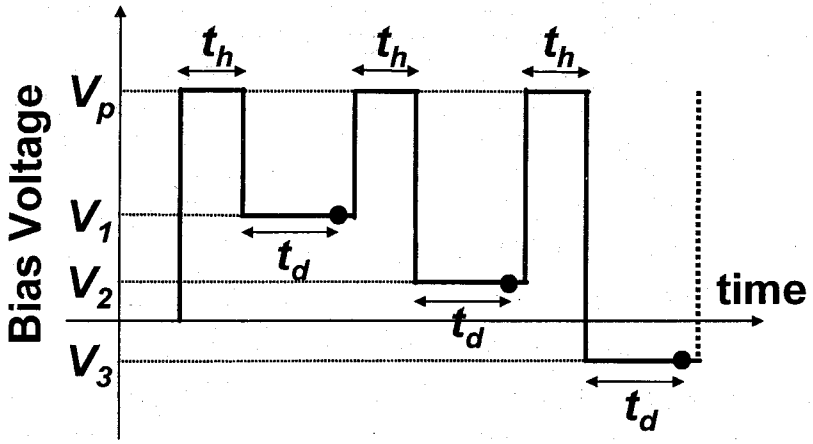

FIG. 5.2. The pulse pattern of the bias voltage on pulsed *C-V* measurements.

5.2.2 Results and Discussion

Figure 5.3 shows room-temperature *I-V* characteristics for the fabricated SiO_2/GaN MOS diodes. The reverse breakdown and the forward turn-on voltages are -35.7 and 13.6 V, respectively. From the gate SiO_2 thickness of ~100 nm, the corresponding forward breakdown field is calculated to be ~1.4 MV/cm effectively.

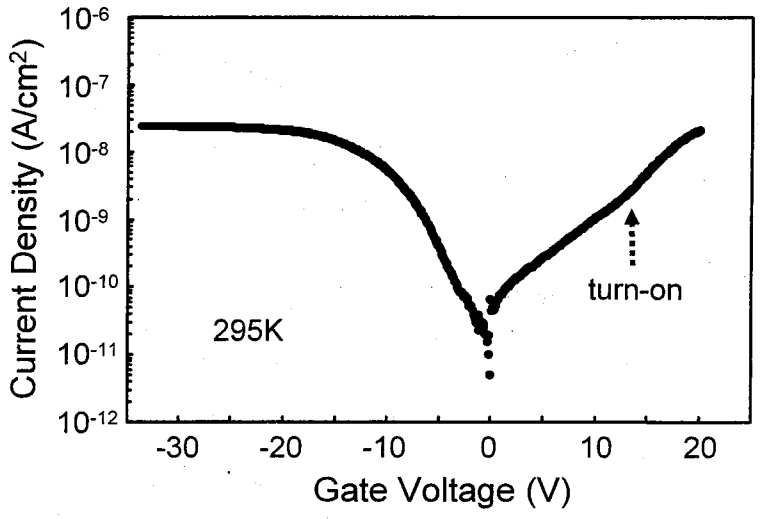

FIG. 5.3. Room-temperature I-V characteristics for the fabricated SiO_2/n-GaN MOS diodes.

Figures 5.4 (a) and 5.4 (b) respectively show typical room-temperature normal and pulsed *C-V* curves for the fabricated SiO_2/GaN MOS diodes at t_d of 1, 5 and 30 s. Ideal *C-V* curves with inversion mode are also shown. Bias voltage was swept from +20 (accumulation) to -30 V (depletion) and then back to +20 V. In both curves, the capacitance tends to be saturated in deep depletion where the reverse voltage is larger than 15 V. In the strict sense, the capacitance in deep depletion is clearly saturated regardless of t_d in the normal *C-V* curves, whereas the t_d dependence of the capacitance is seen in the pulsed *C-V* curves; the capacitance in deep depletion slightly increases to the saturation capacitance of the normal *C-V* characteristics with an increase of

t_d. This capacitance transient is caused by thermal emission of carriers from the SiO_2/GaN interface in accordance with applying the reverse voltage (> 15 V). In addition, the capacitance transient seems to have a long time constant of the order of several seconds at room temperature, indicating that the observed capacitance saturation is associated with deep interface states energetically far away from the conduction band edge of GaN. Thus, the pulsed *C-V* method is an effective tool to evaluate time dependence of

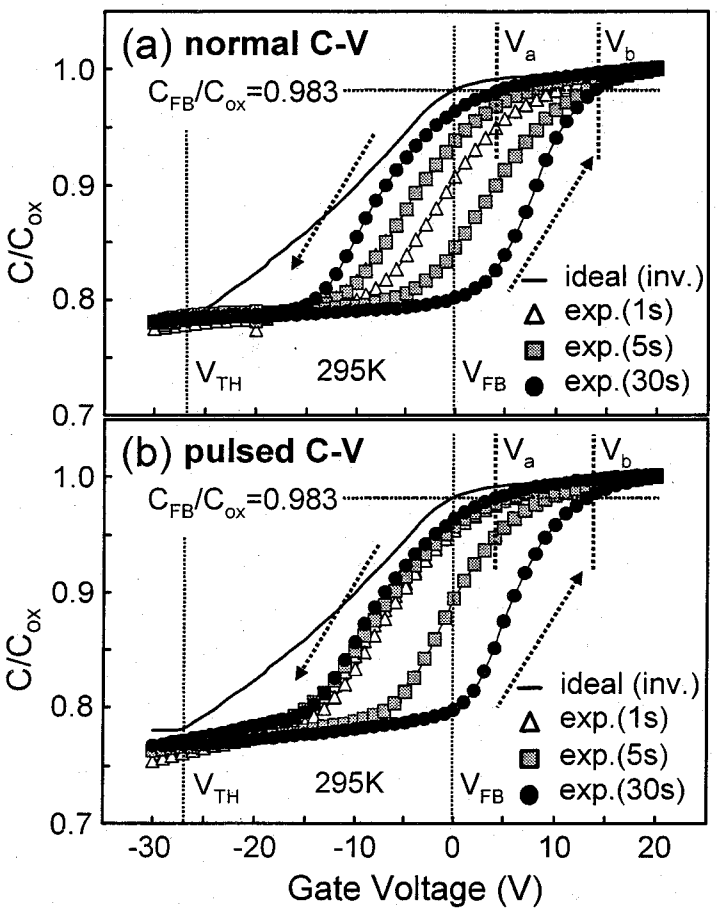

FIG. 5.4. (a) Normal *C-V* and (b) pulsed *C-V* curves at room temperature for the fabricated SiO_2/n-GaN MOS diodes as the bias voltage is swept from +20 to -30 V and then back to +20 V at t_d of 1, 5, and 30 s, together with ideal *C-V* data.

charging and discharging at the SiO_2/GaN interface. Here, in the ideal *C-V* curve, the flatband capacitance, C_{FB}/C_{ox}, is calculated to be 0.983. In both curves of Figs. 5.4 (a) and 5.4 (b), slight hysteresis is observed at t_d of 1 s, whereas a much larger increase of hysteresis windows is seen with increasing t_d. The hysteresis windows show a tendency to be saturated at around t_d of 30 s. This hysteresis behavior indicates charge exchange between the deep interface states and the bulk GaN. Here, V_a is the flatband voltage V_{FB} when the bias voltage goes from accumulation to deep depletion and V_b is that when the voltage sweeps from deep depletion to accumulation. In case of the normal *C-V* characteristics, the V_a is +4.9 V at t_d of 30 s, as shown in Fig. 5.4 (a). This flatband voltage shift (ΔV_{FB}) to the positive side gives a fixed oxide charge density N_f of ~1.1×10^{12} $eV^{-1}cm^{-2}$ with net negative charges distributed in the SiO_2. In addition, compared with the *C-V* data at t_d of 1 s, the V_a and V_b shift toward negative and positive voltages, respectively, at t_d of 30 s. This implies the presence of numerous residual negative charges at the SiO_2/GaN interface. These interface states can be attributed to acceptor-like interface electron traps. $|V_a - V_b|$ is the total hysteresis window at flatband. The large window at t_d of 30 s is ~9.1 V in the normal *C-V* characteristics, which corresponds to a total interface state density N_{ss} of at least ~2.2×10^{12} $eV^{-1}cm^{-2}$. The N_f and N_{ss} calculated from the pulsed *C-V* method are in agreement with those from the normal *C-V* method, respectively.

Figure 5.5 (a) shows typical temperature dependence of the pulsed *C-V* curves at t_d of 30 s for the fabricated SiO_2/GaN MOS diodes. The bias voltage was scanned back and forth between +20 and -30 V. The capacitance saturation in deep depletion becomes clear with the rising of temperature. The hysteresis window becomes small with increasing temperature even at t_d of 30 s. Figure 5.5 (b) shows typical t_d dependence of the pulsed *C-V* curves at 373 K for the fabricated SiO_2/GaN MIS diodes. The capacitance transient in deep depletion can be clearly seen even at 373 K; the capacitance in deep depletion gradually increases up to a saturation value with an increase of t_d. These results also indicate the observed capacitance saturation is probably concerned with localized deep-level traps at the SiO_2/GaN interface.

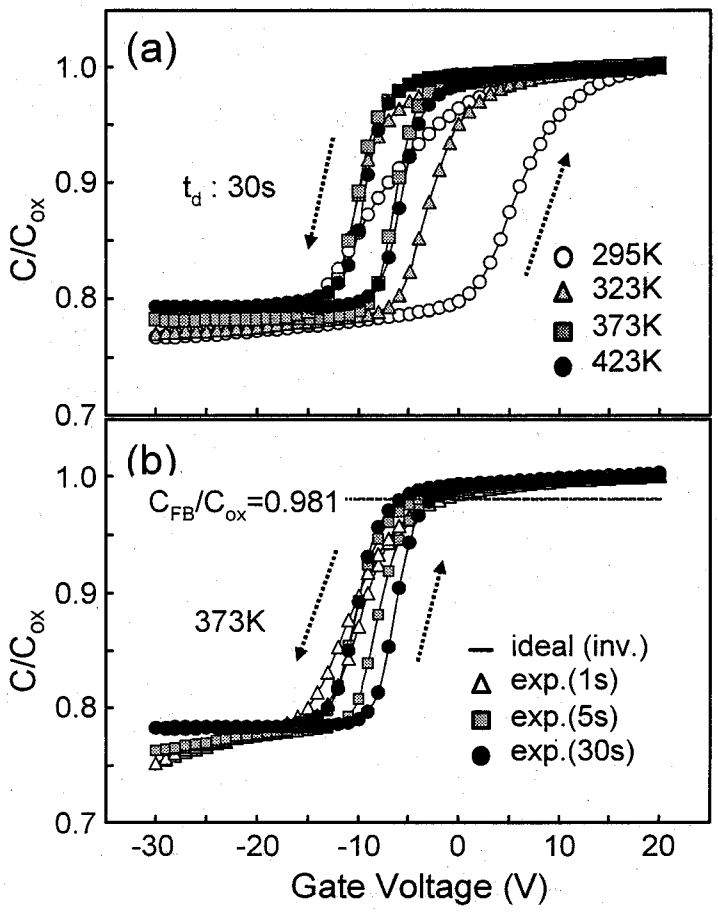

FIG. 5.5. (a) Temperature dependence of pulsed *C-V* curves at t_d of 30 s as the bias voltage is swept from +20 to -30 V and then back to +20 V.
(b) t_d dependence of pulsed *C-V* curves at 373 K as the bias voltage is swept from +20 to -30 V and then back to +20 V.

To clarify the interface trap generation in the fabricated SiO_2/GaN MOS diodes, photo *C-V* measurements were carried out at room temperature. Figure 5.6 shows typical room-temperature normal and pulsed *C-V* curves at t_d of 5 s with and without the white light illumination. In both *C-V* methods, a significant difference between with and without the photo illumination can be clearly seen in deep depletion

of the measured *C-V* characteristics. The capacitance in deep depletion largely increases up to a saturation value by the continuous photo illumination, indicating a significant increase of charge density in the inversion region which leads to a reduction of the depletion region width. That is, exposing the SiO_2/GaN MOS diodes to the white light produces hole-electron pairs only at the GaN surface where the gate metal (gate electrode) is not present. Sequentially, the SiO_2/GaN interface at the edge of the gate electrode reaches inversion and can act like an n^+ source. In this case, the capacitance should approach a value expected when an inversion layer is formed. In addition, the capacitance in deep depletion gradually decreases when the white light is removed. This result directly implies the presence of numerous interface states, i.e. the capacitance value decays due to hole-capture process by the interface states. Thus, the photo induced charges may correspond to the sum of the inversed charges and the interface trapped charges. Conversely, the interface states are considered to induce surface Fermi level pinning at the SiO_2/GaN interface, which leads to the capacitance saturation in deep depletion of the dark *C-V* characteristics instead of actual hole inversion [32,33]. Therefore, the interface state density should be reduced in order to achieve inversion mode in the SiO_2/GaN MOS structures.

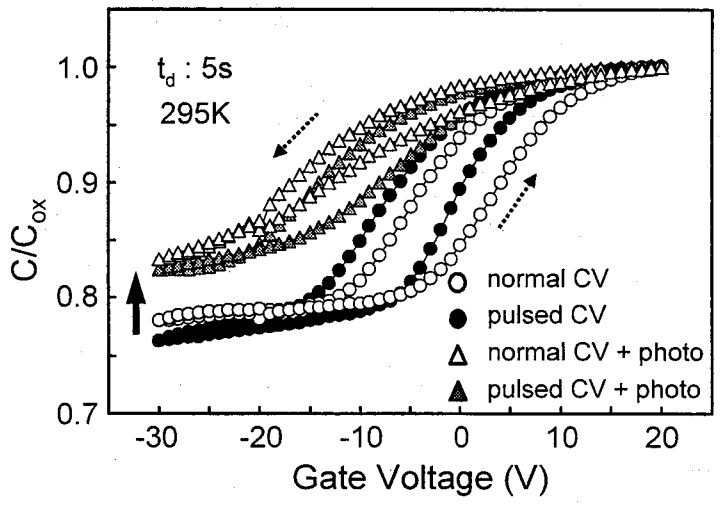

FIG. 5.6. Room temperature of normal and pulsed *C-V* curves at t_d of 5 s with and without white light illumination for the SiO_2/n-GaN MOS diodes fabricated as the bias voltage is swept from +20 to -30 V and then back to +20 V.

To examine the capacitance transient observed in deep depletion, *C-t* measurements were performed in the dark by means of the pulsed *C-V* technique as mentioned above. Figure 5.7 (a) shows typical bias voltage dependence of the capacitance transient at room temperature for the fabricated SiO_2/GaN MOS diodes. C_{fin} means final capacitance. Two capacitance transients are clearly seen, which is labeled *G* and *I*, as shown in this figure. By combining with the measured *C-V* characteristics as stated above, both capacitance transients correspond to thermal emissions of carriers from the SiO_2/GaN interface [18].

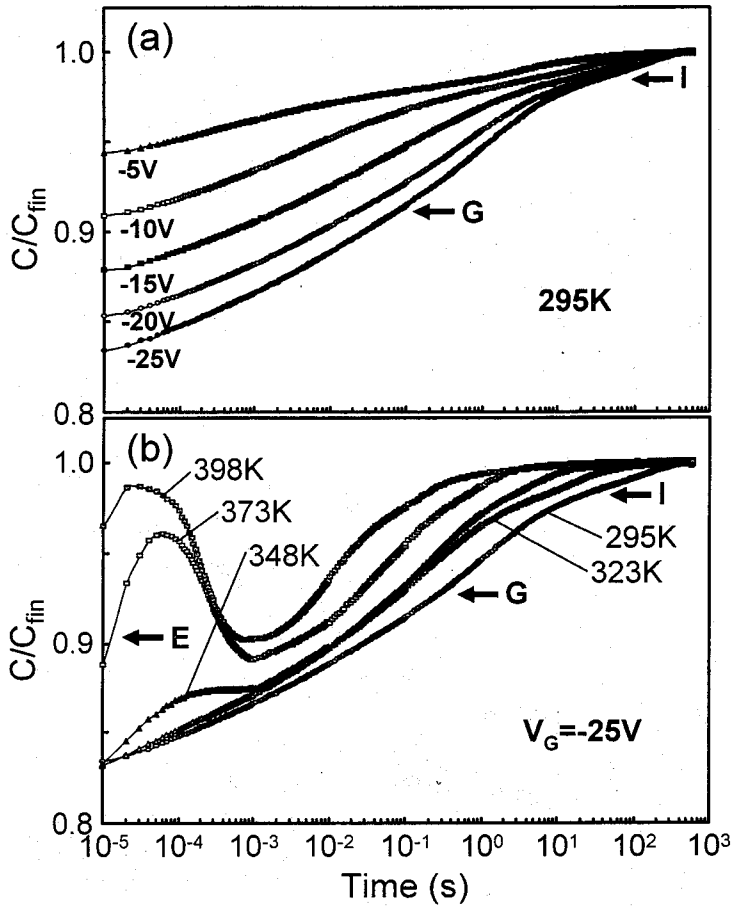

FIG. 5.7. (a) Bias voltage and (b) temperature dependence of capacitance transient for the fabricated SiO_2/n-GaN MOS diodes after applying the bias voltage of -25 V.

The capacitance significantly increases with an increase of reverse voltage for the capacitance transient *G*, whereas the capacitance variation remains small independent of reverse voltage for the slow capacitance transient *I*. The relaxation time for both capacitance transients *G* and *I* becomes longer with increasing the reverse voltage, which is a typical characteristic of interface states. In particular, the capacitance transient *G* seems to be associated with the capacitance saturation observed in the *C-V* characteristics as stated in Figs. 5.4 (a) and 5.4 (b) in view of a relaxation time. Figure 5.7 (b) shows typical *C-t* curves after applying the bias voltage of -25 V for the fabricated SiO_2/GaN MOS diodes at 295 (room temperature), 323, 348, 373 and 398 K, respectively. The relaxation time for both capacitance transients *G* and *I* becomes shorter in accordance with the rising of the temperature, which is in reasonable agreement with the theory of thermal carrier emission based on the Shockley-Read-Hall (SRH) statistics. In addition, a capacitance transient *E* with a fast relaxation time of ~10^{-5} s shows up in the *C-t* curves at temperatures higher than ~330 K.

To estimate the activation energies for the carrier emissions of the capacitance transients, DLTS measurements were performed under the same condition as the *C-t* measurements as stated above. Figure 5.8 shows typical DLTS spectra measured on the fabricated SiO_2/GaN MOS diodes at various rate windows t_1/t_2. The DLTS signal, $|C(t_1) - C(t_2)|$, is displayed for the rate windows t_1 (ms)/t_2 (ms) = 4/8, 5/10, 8/16, and 10/20; the carrier emission rates are 173.3, 138.6, 86.6, and 69.3 s^{-1}, respectively. The spectra reveal three peaks at around 330, 430, and 460 K, which correspond to the capacitance transients *E*, *G*, and *I* in Fig. 5.7 (b), respectively. These peaks shift toward higher temperatures with an increase of the carrier-emission rate, which indicates that both peaks are assigned to deep-level centers at the SiO_2/GaN interface. In particular, the thermal activation energy for the carrier emission from the dominant deep center *G*, was determined by an Arrhenius analysis of the emission rate, as shown in the inset of Fig. 5.8. The activation energy is estimated to be ~0.77 eV for the *G* center from the slope of the lines fitted to these plots, which value is in good agreement with that reported in our previous study [34]. This energy is substantially that for electron emission into conduction band. Considering that the capacitance transient *G* is related to the capacitance saturation in the measured *C-V* characteristics as mentioned above, this interface trap may dominantly induce

the surface Fermi level pinning effect at the SiO_2/GaN interface upon applying reverse voltages (> 15 V), which results in the capacitance saturation observed in the *C-V* characteristics.

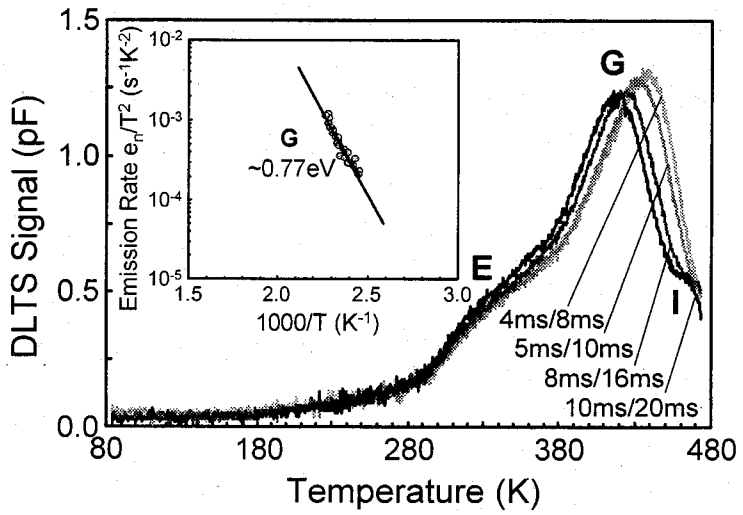

FIG. 5.8. Typical DLTS spectra at various rate windows t_1/t_2 for the fabricated SiO_2/n-GaN MOS diodes after applying the bias voltage of -25 V. The inset shows Arrhenius plots of electron-emission rate.

In summary, the interface properties of the SiO_2/n-GaN MOS diodes have been investigated by using *C-V* and capacitance transient techniques. The MOS diodes have a total interface state density of ~2.2×10^{12} $eV^{-1}cm^{-2}$. The capacitance in deep depletion tends to be saturated upon applying the reverse voltage (> 15 V). The photo *C-V* measurements reveal the interface trap generation. The dominant interface trap is found to be located at ~0.77 eV below the conduction band as determined by DLTS measurements. Therefore, this interface trap is considered to induce the surface Fermi level pinning at the SiO_2/GaN interface upon applying reverse voltages, which results in the capacitance saturation in the measured *C-V* characteristics.

5.3 Thermally Oxidized n-GaN MOS Structures

5.3.1 Experimental

The epitaxial GaN films in these experiments were grown by atmospheric pressure MOCVD on a-plane sapphire substrates. First a 20 nm AlN buffer layer was deposited at 400 °C, and then Si-doped 3-μm-thick GaN layer was grown at 1050 °C as an active layer. The GaN active layer had free electron concentrations of ~$7.6x10^{17}$ cm^{-3} and mobilities of ~440 cm^2/Vs as determined by room-temperature Hall-effect measurements. The Si concentration was also confirmed to be ~$6.8x10^{17}$ cm^{-3} by SIMS measurements. After growth, lateral dot-and-ring GaN MOS diodes were fabricated by a thermal oxidation technique, as shown in Fig. 5.9. First a 500-nm-thick Si layer was selectively deposited on the top surface of the GaN sample as a mask material for thermal oxidation by RF sputtering at nominal room temperature. This sample was then thermally oxidized at 880 °C for 6h in dry oxygen ambient. The formation of monoclinic β-Ga_2O_3 was confirmed by x-ray diffraction (XRD). After removing the Si mask by a HF-HNO_3 solution (HF:HNO_3=20:3) for ohmic contact directly on the GaN active layer, Al metal was evaporated through a shadow mask to provide gate and ohmic electrodes. The dot gate electrode was 500 μm in diameter, and was surrounded by the ring ohmic electrode with a 50 μm gap. After metallization, the MOS samples were

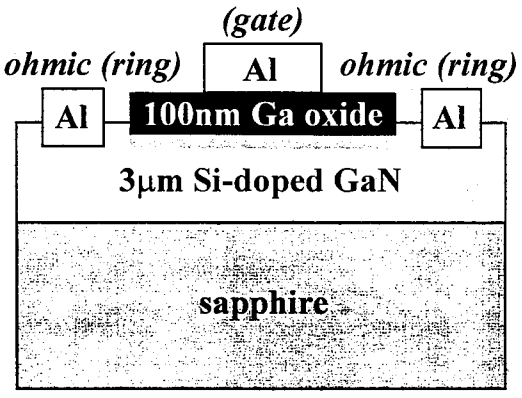

FIG. 5.9. Schematic cross-section of a thermally oxidized β-Ga_2O_3/n-GaN MOS structure.

annealed at 450 °C for 30 min in nitrogen ambient. As a reference, sputtered SiO_2/n-GaN MOS diode samples were also prepared with the SiO_2 thickness of ~100 nm using conventional methodology, as described in section 5.2.

The MOS capacitors were characterized by using high-frequency *C-V* and *C-t* techniques to evaluate time dependence of charging and discharging at the MOS interface. The measurements were performed in the dark at a frequency of 1 MHz with an ac modulation of 30 mV. On both measurements, one unit of the pulse pattern consists of two stages. After applying a 1 ms pulsed voltage of +20 V to approach an accumulation region temporarily, bias voltage is sequentially applied and the capacitance is measured after a delay time t_d. The bias voltage and t_d are independently varied. *I-V* measurements were performed in the dark at a voltage step of 0.1 V under a conventional dc mode. The surface morphology and structure of the thermally oxidized GaN samples were analyzed by atomic force microscopy (AFM) and cross-sectional transmission electron microscopy (XTEM), respectively.

5.3.2 Results and Discussion

Figure 5.10 shows SIMS profiles of Ga, N, and O atoms in the thermally oxidized GaN sample. A pure Ga oxide containing no N atoms can be clearly seen in the surface region of ~100 nm where the GaN has been completely oxidized. This layer is probably identical with the monoclinic β-Ga_2O_3 layer, as confirmed by XRD. In addition, ambiguous broad oxide/GaN interface is also seen, indicating the formation of an intermediate Ga-oxynitride layer with graded compositions in the depth region of 100 - 400 nm from the surface. This Ga-oxynitride layer is found to be formed inevitably under any thermal oxidation conditions. Thus, the thermal oxidation of GaN may be dependent on the combined effect of the interfacial reaction and diffusion mechanism.

Figures 5.11 (a) and 5.11 (b) show typical AFM and XTEM images of the thermally oxidized GaN sample. From the AFM image, the surface morphology is found to become very rough with a mean

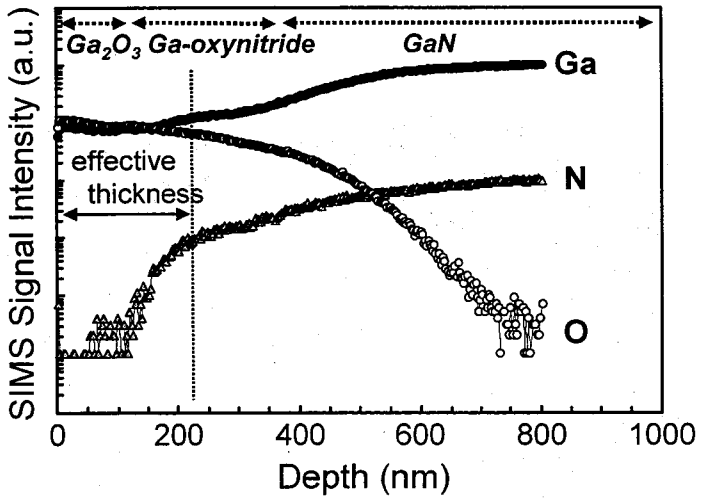

FIG. 5.10. SIMS profiles of Ga, N, and O atoms in the thermally oxidized β-Ga_2O_3/n-GaN structure.

roughness R_{ms} of ~23.3 nm by thermal dry oxidation. This non-uniform morphology indicates that the dry oxidation of GaN may be enhanced at dislocations. The thermally oxidized layer is ~200 nm thickness from the XTEM images, which value is in reasonable agreement with the effective thickness of the gate insulator estimated from *C-V* data, as discussed later. In addition, porous polycrystalline shapes can be observed in the thermally grown β-Ga_2O_3 layer.

Room-temperature *I-V* characteristics are shown in Fig. 5.12. Compared to the referenced SiO_2/GaN MOS structure, the β-Ga_2O_3/GaN MOS structure shows large leakage currents in both the accumulation and depletion regions. In particular, in the accumulation region, the gate leakage current of the β-Ga_2O_3/GaN MOS structure is two orders of magnitude larger than that of the SiO_2/GaN MOS structure fabricated, which is probably associated with the decrease in effective thickness of the β-Ga_2O_3 layer due to its porous structure, as stated herein. Thus, thermally grown β-Ga_2O_3 layer has some disadvantage in view of gate characteristics.

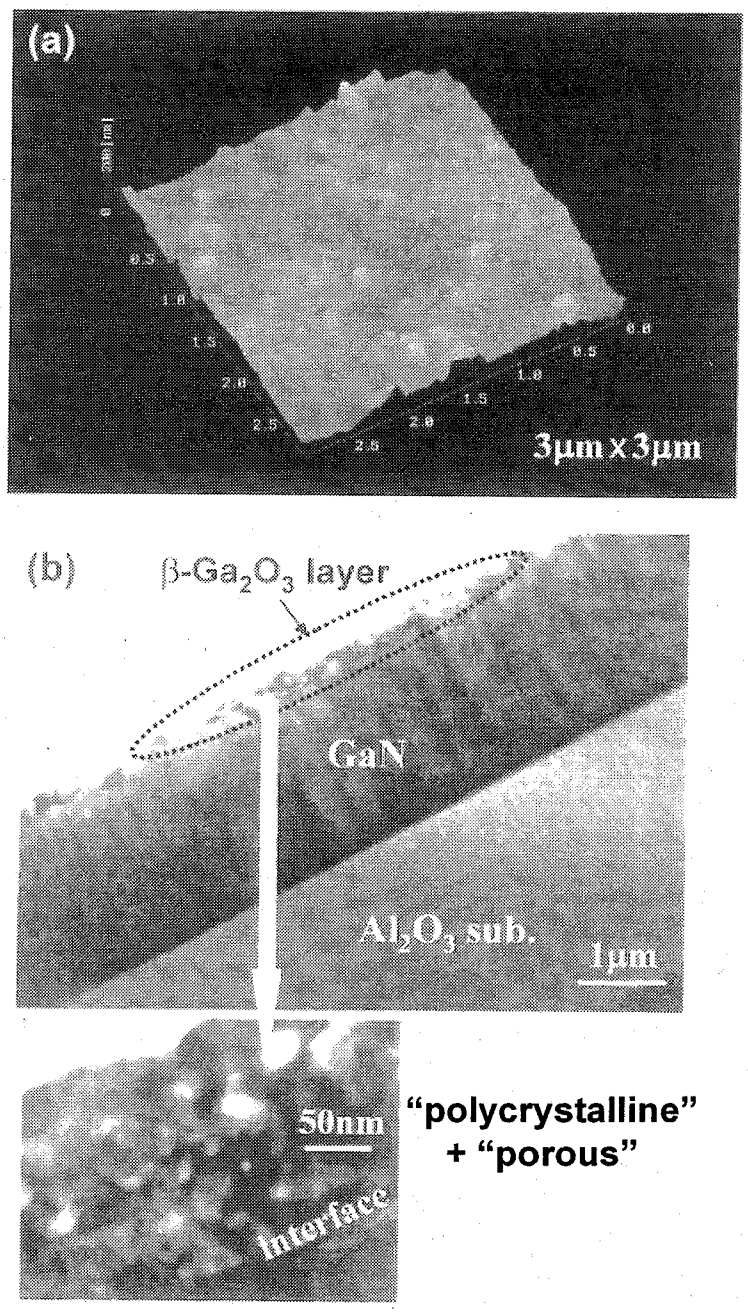

FIG. 5.11. (a) AFM and (b) XTEM images of the thermally oxidized β-Ga_2O_3/n-GaN structure.

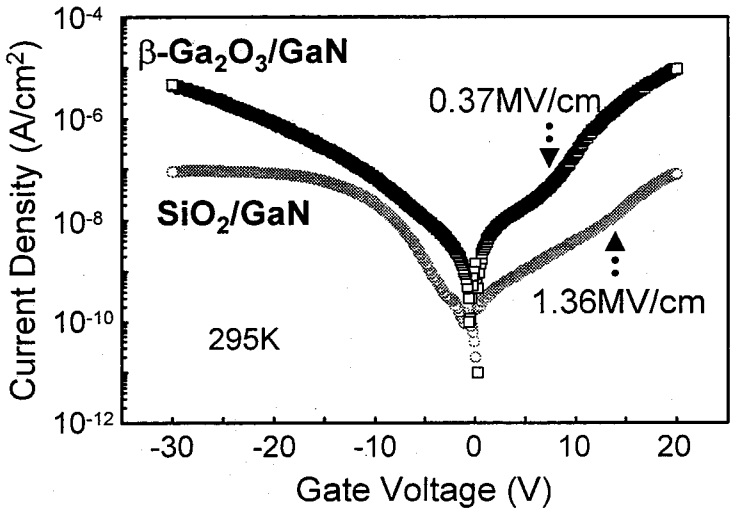

FIG. 5.12. Room-temperature *I-V* characteristics of the thermally oxidized β-Ga_2O_3/n-GaN MOS structure, together with that of the referenced SiO_2/GaN MOS structure.

Figure 5.13 (a) shows typical room-temperature *C-V* curves for the thermally oxidized MOS capacitors at t_d of 1, 5, and 30 s, respectively. An ideal *C-V* curve with an inversion mode is also shown. Bias voltage was swept from +20 (accumulation) to -30 V (depletion). By using a dielectric constant of ε_{Ga2O3}=14, an effective thickness of insulator was estimated to be ~220 nm from the capacitance in the accumulation region, which value is considerably thicker than that of β-Ga_2O_3 layer. The t_d dependence of the measured *C-V* curves is hardly ever seen; a little t_d-dependence of capacitance is observed in the weak depletion region. Additionally, a deep depletion feature can be observed in the depletion region regardless of t_d, which is significantly different from a situation of sputtered SiO_2/n-GaN MOS system as stated in the previous section 5.2. In the ideal *C-V* curve, the flatband capacitance, C_{FB}/C_{ox}, is calculated to be 0.978. The flatband voltage (V_{FB}) which is the corresponding voltage of the C_{FB}/C_{ox}, gives a value of ~6.1 V from the measured *C-V* curve at t_d of 30 s. Thus, the flatband voltage shift (ΔV_{FB}) gives a fixed oxide charge density (N_f) of ~6.7×10^{11} $eV^{-1}cm^{-2}$. Figure 5.13 (b) shows typical room-temperature *C-V* hysteresis curves for the

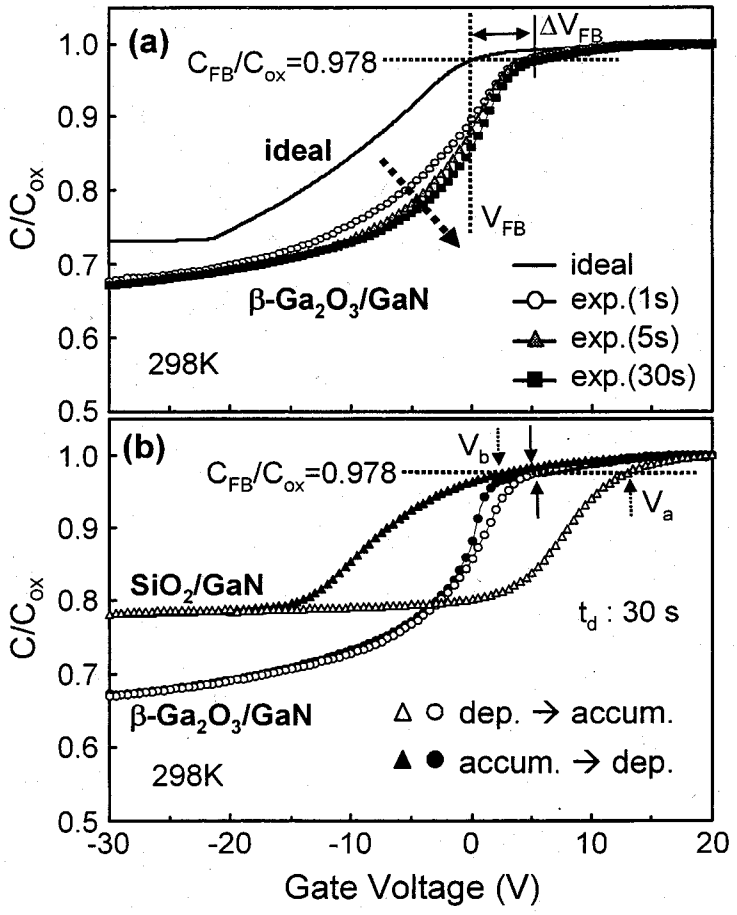

FIG. 5.13. (a) High-frequency *C-V* curves at room temperature for the thermally oxidized β-Ga_2O_3/GaN MOS structure as the bias voltage is swept from +20 to -30 V at t_d of 1, 5, and 30 s, together with an ideal *C-V* curve. (b) High-frequency *C-V* hysteresis curve at room temperature for the thermally oxidized β-Ga_2O_3/GaN MOS and the sputtered SiO_2/n-GaN MOS structures as the bias voltage is swept from +20 to -30 V and then back to +20 V at t_d of 30 s.

thermally oxidized MOS and the referenced SiO_2/GaN MOS capacitors at t_d of 30 s, respectively. Bias voltage was scanned back and forth between +20 and -30 V. Large hysteresis is observed for the SiO_2/GaN MOS capacitor fabricated, while a small hysteresis window is seen for the thermally oxidized MOS one.

This hysteresis indicates charge exchange between the deep interface states and the bulk GaN. Here, V_a is the V_{FB} when the bias voltage goes from accumulation to deep depletion and V_b is that when the voltage sweeps from deep depletion to accumulation. In both the capacitors, to a greater or less extent, the V_a and V_b shift toward negative and positive voltages, respectively, with an increase of t_d. This implies the presence of residual negative charges at the MOS interface. These interface states can be attributed to acceptor-like interface electron traps. $|V_a - V_b|$ is the total hysteresis window at flatband. The hysterisis windows for the thermally oxidized and the SiO_2/GaN MOS capacitors at t_d of 30 s are ~0.5 and ~9.1 V, which correspond to a total interface state density of at least ~5.5×10^{10} and ~2.2×10^{12} $eV^{-1}cm^{-2}$, respectively. The thermally oxidized MOS sample is found to have an incredibly lower interface state density than the sputtered MOS one. Thus, the deep depletion feature observed in the *C-V* characteristics is due to this much low density of interface states for the thermally oxidized MOS sample, which is largely different from a situation of the sputtered MOS sample where a large number of interface traps may induce surface Fermi level pinning at the MOS interface, resulting in the capacitance saturation observed in the deep depletion region of the *C-V* curve.

Figure 5.14 shows typical *C-t* curves after applying the bias voltage of -25 V for the thermally oxidized MOS samples at 298 (room temperature), 323, 373, and 423 K, respectively. A *C-t* curve for the sputtered MOS sample at 298 K is also shown. C_{fin} means final capacitance. In the referenced MOS sample, we can observe some fast and slow capacitance transients (*E*, *G*, and *I*) corresponding to the thermal emissions of carriers from the MOS interface states, as stated in the previous section 5.2. On the other hand, in the thermally oxidized MOS sample, small fast capacitance transient with the opposite code is seen, which seems to reflect the t_d-dependence of the *C-V* characteristics, as stated above. In addition, temperature-independent of the capacitance transient is seen, which implies that it is not the typical character of interface states. Thus, this small capacitance transient may be related to the presence of the intermediate Ga-oxynitride layer at the MOS interface. That is, this phenomenon is considered to be caused by the time delay swelling of the depletion layer in the intermediate layer with graded compositions upon applying reverse voltages.

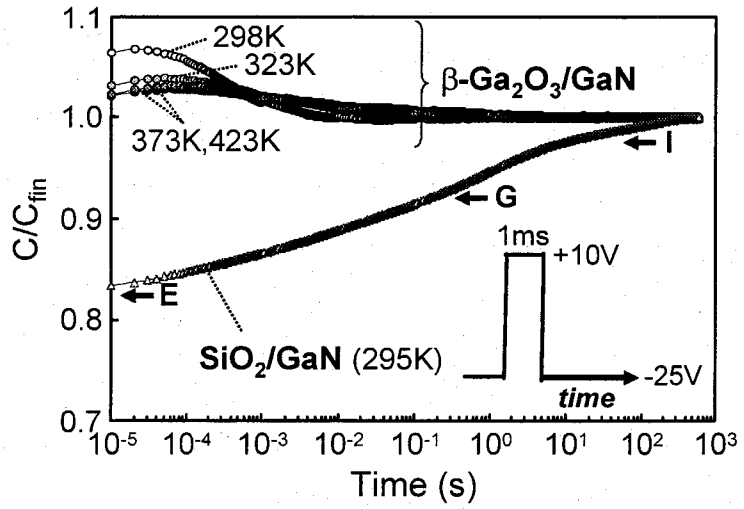

FIG. 5.14. Temperature dependence of capacitance transient for the thermally oxidized β-Ga_2O_3/GaN MOS structure after applying the bias voltage of -25 V. Room-temperature capacitance transient is also shown for the sputtered SiO_2/n-GaN MOS structure.

Figure 5.15 shows typical DLTS spectra measured on the thermally oxidized and the sputtered MOS samples. Here, the DLTS signal, $|C(t_1) - C(t_2)|$, is displayed for the rate windows t_1 (ms)/t_2 (ms) = 10/20; the carrier emission rate is 69.3 s^{-1}. In the referenced SiO_2/GaN MOS sample, some DLTS peaks are detected at around 300 - 480 K, which correspond to the capacitance transients *E*, *G*, and *I* in Fig. 5.14, respectively. In particular, a main deep interface trap *G* is located at ~0.77 eV below the conduction band, from an Arrhenius analysis of the emission rates for the *G* peak. This interface trap probably induced the Fermi level pinning effect at the SiO_2/GaN interface upon applying reverse voltages, as stated above. On the other hand, in the thermally oxidized MOS sample, no DLTS peaks can be detected. This result implies that there are no effective deep traps at the thermally oxidized MOS interface. Therefore, the surface Fermi level is considered to be probably unpinned in the thermally oxidized MOS structures, which is significantly different from the situation of sputtered SiO_2/n-GaN MOS sample. These distinguished interface properties may be probably associated with the presence of the interfacial Ga-oxynitride layer.

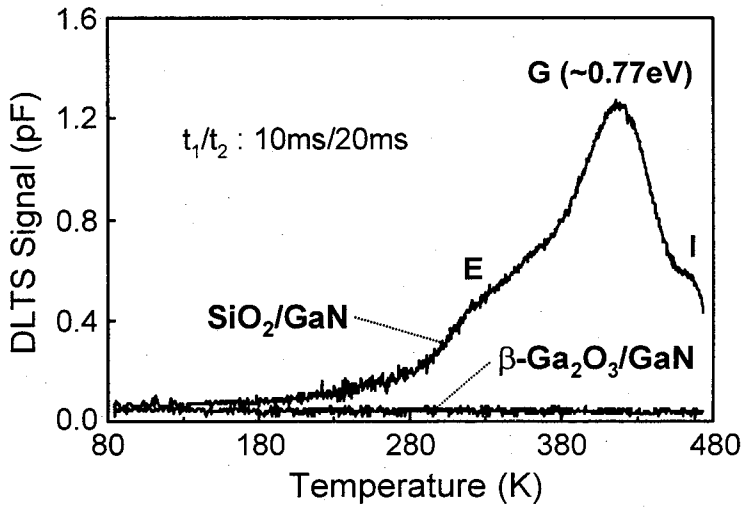

FIG. 5.15. Typical DLTS spectra at a rate window t_1/t_2 of 10 ms/20 ms for the thermally oxidized β-Ga_2O_3/GaN MOS and the sputtered SiO_2/n-GaN MOS structures after applying the bias voltage of -25 V.

In summary, the interface properties of the thermally oxidized GaN MOS capacitors have been investigated electrically by using *C-V* and capacitance transient techniques. From the *C-t* and DLTS measurements, no deep interface trap can be observed, which is in good agreements with the deep depletion feature and the low interface state density of ~5.5×10^{10} $eV^{-1}cm^{-2}$ determined by the *C-V* measurements. Therefore, the surface Fermi level is probably unpinned in the MOS structures fabricated by a thermally oxidation technique.

5.4 Characteristics of SiO_2/n-GaN Interfaces with β-Ga_2O_3 Interlayers

5.4.1 Experimental

The epitaxial GaN films used in these experiments were grown by atmospheric pressure MOCVD on a-plane sapphire substrates. First a 20 nm AlN buffer layer was deposited at 420 °C, and then Si-doped

4-μm-thick GaN layer was grown at 1130 °C as an active layer. The GaN active layer had free electron concentrations of 9.9×10^{17} cm^{-3} and mobilities of 263 cm^2/Vs as determined by room-temperature Hall-effect measurements. The Si concentration was also confirmed to be ~1×10^{18} cm^{-3} by SIMS measurements. After growth, lateral dot-and-ring SiO_2/β-Ga_2O_3/GaN MOS capacitors were fabricated by thermal oxidation and SiO_2 deposition techniques. A schematic of the complete SiO_2/β-Ga_2O_3/GaN MOS capacitor is shown in Fig. 5.16. First a 500-nm-thick Si layer was selectively deposited on the top surface of the GaN sample as a mask material for thermal oxidation by RF sputtering at room temperature. The GaN samples were then thermally oxidized at 800 °C for 6 h in dry oxygen ambient. The formation of monoclinic β-Ga_2O_3 was confirmed by XRD. After removing the Si mask by a HF-HNO_3 solution (HF:HNO_3=20:3), 100-nm-thick SiO_2 layer was deposited on the top surface of the GaN samples as a gate dielectric by RF sputtering using an SiO_2 target. This SiO_2 layer was selectively removed by wet etching using a photolithographic technique and then Al metal was evaporated through a shadow mask to provide gate and ohmic electrodes. The dot gate electrode was 500 μm in diameter, and was surrounded by the ring ohmic electrode with a 50 μm gap. After metallization, the stacked SiO_2/β-Ga_2O_3/GaN MOS samples were

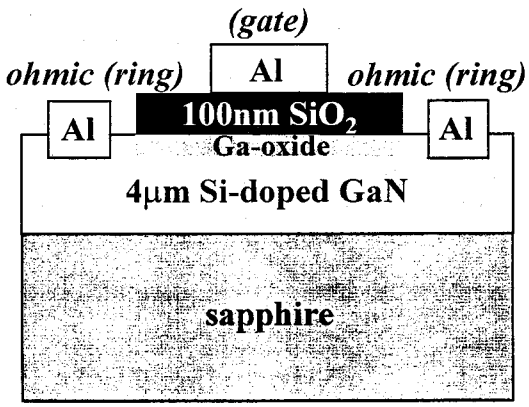

FIG. 5.16. Schematic cross-section of the complete SiO_2/β-Ga_2O_3/GaN MOS structure.

annealed at 400 °C for 20 min in nitrogen ambient. As a reference, conventional SiO_2/n-GaN MOS samples without any β-Ga_2O_3 interlayers were also prepared with the SiO_2 thickness of 100 nm by using conventional methodology [19].

The material properties of thermally oxidized GaN samples were analyzed by XRD, SIMS, and AFM measurements. The MOS capacitors that we fabricated were assessed by *I-V*, *C-V*, *C-t*, and DLTS techniques. The *I-V* measurements were carried out in the dark at a voltage step of 0.1 V under a conventional dc mode. The *C-V* measurements were also performed in the dark at a frequency of 1 MHz and a voltage step of 0.01 V with various delay time t_d. On the *C-t* measurements, the time dependence of the capacitance under a reverse voltage was measured after applying a 1-ms-pulsed voltage of +10 V to approach an accumulation region temporarily. The DLTS measurements were carried out at temperatures between 80 and 475 K under the same condition as the *C-t* measurements.

5.4.2 Results and Discussion

Figure 5.17 shows SIMS profiles of Ga, N, and O atoms in a thermally oxidized GaN sample before SiO_2 deposition. A pure Ga oxide containing no N atoms is seen in the surface region of ~15 nm, where the GaN has been completely oxidized. This layer probably corresponds to the monoclinic β-Ga_2O_3 layer as confirmed by XRD. In addition, in the deeper lying region of 15 - 50 nm from the surface, the β-Ga_2O_3 is transformed into the GaN, that is, ~35-nm-thick intermediate Ga-oxynitride layer with composition gradient is seen.

Figures 5.18 (a) and 5.18 (b), respectively, show typical AFM images of GaN samples before and after thermal dry oxidation. A clear difference can be seen between them. Before thermal dry oxidation, smooth surface morphology with a number of growth steps is clearly observed, where the mean roughness R_{ms} is ~0.35 nm. In addition, some dark points that we can see correspond to threading dislocations. In sharp contrast, the surface morphology is seen to become very rough with R_{ms} of ~13.6 nm by thermal dry oxidation, indicating non-uniform oxidation of GaN. In a narrow sense, polycrystalline shapes with small

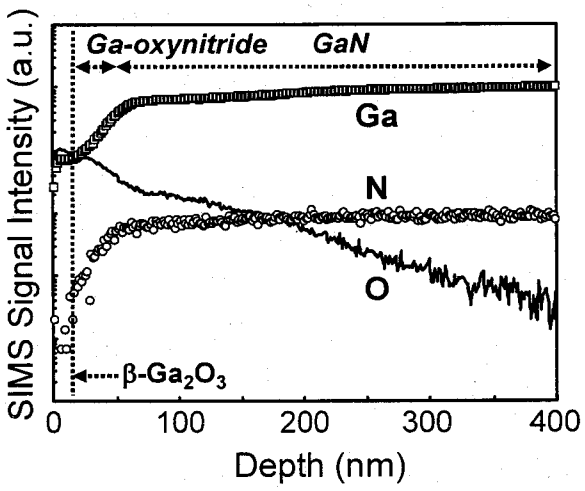

FIG. 5.17. SIMS profiles of Ga, N, and O atoms in a thermally oxidized n-GaN sample before SiO_2 deposition.

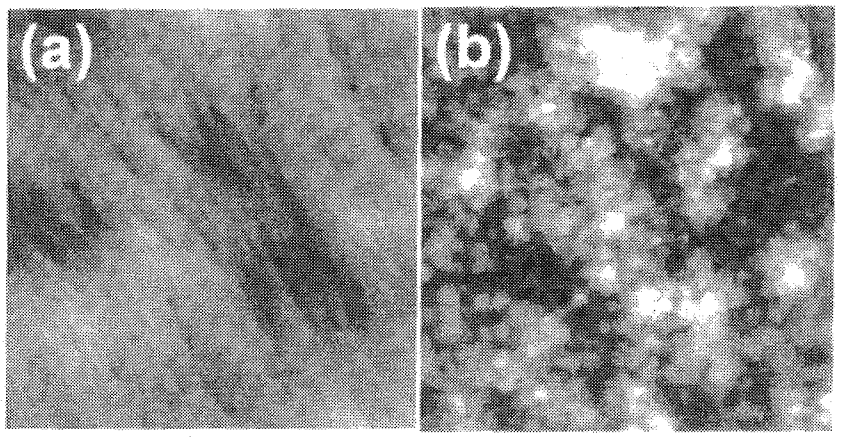

FIG. 5.18. AFM images of n-GaN samples (a) before and (b) after thermal dry oxidation. Both images are 5x5 μm^2.

grain size of ~10 nm can be clearly observed in the oxide surface, which suggests that the oxidation occurs preferentially at dislocation sites. In particular, a higher degree of roughness at the oxide surface can be attributed to the process features of thermal dry oxidation.

Room-temperature forward *I-V* characteristics of SiO_2/GaN MOS samples with and without β-Ga_2O_3 interlayer are shown in the inset of Fig. 5.19. The *I-V* data of the 100-nm-thick β-Ga_2O_3/n-GaN MOS sample that we have previously fabricated are also shown [18]. The SiO_2/β-Ga_2O_3/GaN sample shows a relative large leakage current of 1.2 μA/cm^2 at a gate voltage of +20 V, compared to 4.3 nA/cm^2 of the conventional SiO_2/GaN sample. This increase in forward leakage current by the presence of the β-Ga_2O_3 interlayer is probably caused by a reduction in effective thickness of SiO_2 layer due to the rough oxide surface, as shown in Fig. 5.18 (b). From the surface roughness R_{ms} of the β-Ga_2O_3 interlayer, the effective thickness of the SiO_2 layer is estimated to be ~73 nm. However, the SiO_2/β-Ga_2O_3/GaN sample displays a leakage current by less than one order of magnitude compared to that of the β-Ga_2O_3/GaN MOS sample. In addition, both samples show high oxide breakdown voltages of ~4 MV/cm regardless of the presence of the β-Ga_2O_3 interlayer.

Figure 5.19 shows typical room-temperature C-V hysteresis curves for SiO_2/GaN MOS samples with and without β-Ga_2O_3 interlayer at t_d of 30 s, respectively. Their corresponding ideal *C-V* curves with an inversion mode are also shown, considering the thinning effect of the SiO_2 layer, as stated above. Bias voltage was scanned back and forth between -30 (depletion) and +20 V (accumulation). A deep depletion feature can be clearly observed in the depletion region for the SiO_2/β-Ga_2O_3/GaN sample, whereas capacitance saturation is seen for the SiO_2/GaN sample. In addition, a large hysteresis is observed for the SiO_2/GaN sample, while a very small hysteresis window is seen for the SiO_2/β-Ga_2O_3/GaN sample. These hysteresis windows should reflect charge exchange between the deep interface traps and the bulk GaN. Thus, these results suggest that the SiO_2/β-Ga_2O_3/GaN sample has much lower interface traps than the SiO_2/GaN sample, which probably results in unpinning the surface Fermi-level at the β-Ga_2O_3/GaN interface. Here, in their ideal *C-V* curves, the flatband capacitance (C_{FB}/C_{ox}) is calculated to be 0.944 and 0.980 for the SiO_2/GaN MOS samples with and without the β-Ga_2O_3 interlayer, respectively. V_{FB}^f is the flatband voltage V_{FB} when the bias voltage goes from deep depletion to accumulation and V_{FB}^b is that when the voltage sweeps from accumulation to deep depletion. $|V_{FB}^f - V_{FB}^b|$ is the total hysteresis window at flatband. The

hysteresis windows for the SiO_2/GaN MOS samples with and without the interlayer are ~0.15 and ~15.8 V, which correspond to a total interface state density of at least ~$3.9x10^{10}$ and ~$4.5x10^{12}$ $eV^{-1}cm^{-2}$, respectively. Thus, the SiO_2/β-Ga_2O_3/GaN sample is found to show an incredibly lower interface trap density than the SiO_2/GaN sample, which is the same level as that of the β-Ga_2O_3/GaN MOS sample that we have previously reported in section 5.3 [18].

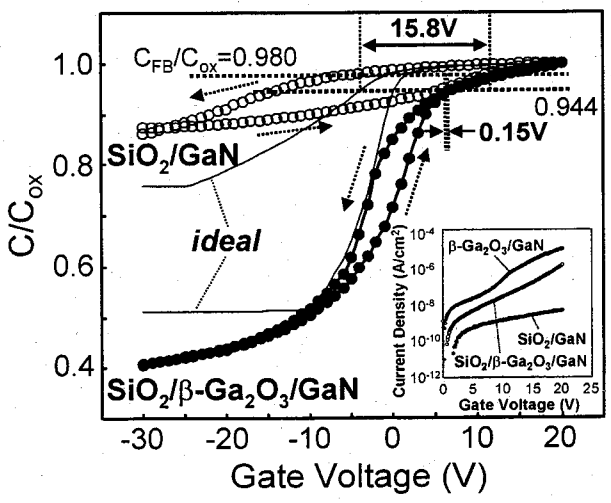

FIG. 5.19. High-frequency hysteresis *C-V* curves at room temperature for SiO_2/β-Ga_2O_3/n-GaN and SiO_2/n-GaN samples as bias voltage is swept from -30 to +20 V and then back to -30 V at t_d of 30 s, together with respective ideal *C-V* curves. Inset shows forward *I-V* characteristics of SiO_2/β-Ga_2O_3/n-GaN and SiO_2/n-GaN samples, together with those of 100nm-thick β-Ga_2O_3/n-GaN MOS sample.

In addition, to evaluate time dependence of charging and discharging in deep depletion at the oxide/GaN interface, conventional *C-t* measurements were performed. Figure 5.20 shows typical room-temperature *C-t* curves after applying a gate voltage of -25 V for SiO_2/GaN MOS samples with and without β-Ga_2O_3

interlayer. C_{fin} means final capacitance. A large capacitance transient *J* with the time constant τ of ~20 ms is seen for the SiO_2/GaN sample, whereas two kinds of small capacitance transients with the opposite codes are seen for the SiO_2/β-Ga_2O_3/GaN sample; one is a fast capacitance transient *H* with the τ of ~0.1 ms and the other is a slow capacitance transient *I* with the τ of 0.1 s. The τ for all the capacitance transients tends to become longer with increasing the reverse voltage, which indicates a typical characteristic of the oxide/GaN interface. However, the fast capacitance transient *H* is independent of temperature, which implies that it is not a typical character of interface traps. This capacitance transient *H* may be caused by the time delay swelling of the depletion layer in the intermediate Ga-oxynitride layer upon applying reverse voltages [18]. The other capacitance transients *I* and *J* with relatively long τ correspond to the thermal emission of carriers from the interface traps at oxide/GaN interface, because they show the strong dependence of τ on temperature. Furthermore, DLTS measurements were carried out under the same condition as the *C-t* measurements to

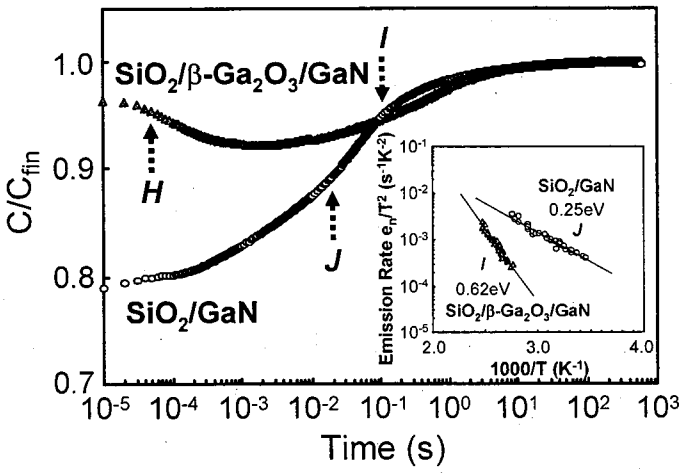

FIG. 5.20. Capacitance transients for SiO_2/β-Ga_2O_3/n-GaN and SiO_2/n-GaN samples after applying bias voltage of -25 V. Inset shows Arrhenius plots of emission rates from DLTS measurements of SiO_2/β-Ga_2O_3/n-GaN and SiO_2/n-GaN samples.

investigate deep-level centers at the oxide/GaN interface. In both samples, to a greater or less extent, respective DLTS spectra show a dominant peak, which corresponds to the capacitance transients, *I* and *J* at room temperature. From Arrhenius plots of the emission rates e_n/T^2 as shown in the inset in Fig. 5.20, the thermal activation energies for the carrier emission from the dominant interface traps are estimated to be ~0.62 and ~0.25 eV for the SiO_2/GaN MOS samples with and without the β-Ga_2O_3 interlayer, respectively. Thus, the SiO_2/β-Ga_2O_3/GaN sample has a deep interface trap level at 0.62 eV below the conduction band at the β-Ga_2O_3/GaN interface. However, the surface Fermi level is considered to be probably unpinned because of the extremely low interface trap density, as determined by the *C-V* measurements. This behavior is significantly different from a situation of the SiO_2/GaN sample without the β-Ga_2O_3 interlayer, in which a number of interface traps induce the surface Fermi-level pinning effect at the SiO_2/GaN interface upon applying reverse voltages. These distinguished interface properties of the SiO_2/GaN sample with the β-Ga_2O_3 interlayer may be probably associated with the presence of the intermediate Ga-oxynitride layer.

In summary, we have demonstrated that the stacked SiO_2/β-Ga_2O_3 insulator improves both the electrical interface properties and the gate dielectric characteristics of the n-GaN MOS structures. The total interface state density was estimated to be 3.9×10^{10} $eV^{-1}cm^{-2}$. The forward gate leakage current was ~1.2 μA/cm^2 for a gate voltage of +20 V.

5.5 Thermally Oxidized p-GaN MOS Structures with n^+ Source Regions

5.5.1 Experimental

The epitaxial Mg-doped GaN (GaN:Mg) films used in these experiments were 2.5 μm thick. They were grown on a-plane sapphire substrates by atmospheric pressure MOCVD at 1130 °C, with a pre-deposited 20 nm AlN buffer layer grown at 420 °C. The Mg concentration of the as-grown GaN:Mg layers was determined to be ~5×10^{18} cm^{-3} by SIMS measurements. After growth, activation annealing was performed at 700 °C for 10 min in flowing N_2, resulting in the free hole concentration of ~2.5×10^{16} cm^{-3} as confirmed by room-temperature Hall-effect measurements. Then, thermally oxidized p-GaN MOS diodes

with n^+ source regions were fabricated as follows. A schematic of the complete MOS diode is shown in Fig. 5.21. Prior to Si+N co-implantation, a 1-μm-thick Ni layer was selectively deposited as a mask material for the implantation on the top surface of the samples by electron-beam evaporation. The GaN samples were implanted using pure N_2 and SiF_4 gases as the sources of the $^{14}N^+$ and $^{28}Si^+$ species, respectively, to create the n^+ source regions in GaN:Mg. First, multiple step N^+ implantation was performed; the N^+ ions were implanted at 240, 180, 120, 60, and 20 keV with dosages of $1.8x10^{14}$, $6x10^{13}$, $8x10^{13}$, $7.5x10^{13}$, and $3x10^{13}$ cm^{-2}, respectively, to produce a mean N concentration of $1x10^{19}$ cm^{-3} to a depth of ~0.35 μm from the GaN surface. Multiple Si^+ implantation was then performed; the Si^+ ions were implanted at 360, 200, 120, 60, and 30 keV with dosages of $2.5x10^{14}$, $9x10^{13}$, $5.3x10^{13}$, $2.8x10^{13}$, and $1.4x10^{13}$ cm^{-2}, respectively, to produce a mean Si concentration of $1x10^{19}$ cm^{-3} to a depth of ~0.35 μm. Here, the N/Si ratio was kept ~1 for an optimum doping [28,29]. All the implants were carried out at room temperature, with an incident angle 7° off the surface normal. After implantation, the Ni layer was removed and then a 500-nm-thick SiO_2 capping layer was deposited on the top surface of the implanted samples by RF sputtering at room temperature to provide an encapsulation cap for the subsequent implant activation annealing. All the samples were annealed at 1300 °C for 5 min in flowing N_2 gas. From the room-temperature Hall effect measurements, the free electron concentration of the n^+ source regions was confirmed to be ~$4.7x10^{18}$ cm^{-3}. After removing the SiO_2 capping layer, a 500-nm-thick Si layer was selectively deposited on the top surface of the GaN samples as a mask material for thermal oxidation by RF sputtering at room temperature. The GaN samples were then thermally oxidized at 880 °C for 5 h in flowing dry O_2 gas. The formation of monoclinic β-Ga_2O_3 layer was confirmed by XRD and its thickness was ~100 nm from SIMS measurements. After removing the Si mask by a HF-HNO_3 solution (HF:HNO_3=20:3), Al metal was selectively evaporated through a shadow mask to provide gate electrodes. The dot gate electrode was 500 μm in diameter. After metallization, the MOS samples were annealed at 500 °C for 30 min in flowing N_2 gas. Finally, In metal was deposited at 200 °C directly on the GaN:Mg active layer and the n^+ source for ohmic electrodes. As a reference, thermally oxidized p-GaN MOS structures without any n^+ source regions were also fabricated by

using the same methodology as stated above.

The MOS structures that we fabricated were characterized by using *C-V* measurements at room temperature. The *C-V* measurements were performed under a grounded source contact condition in the dark with an ac modulation level of 30 mV and frequencies ranging from 100 Hz to 10 MHz. On these *C-V* measurements, gate bias voltage is applied and the capacitance is measured after a delay time t_d [18,34]. The bias voltage and t_d are independently varied.

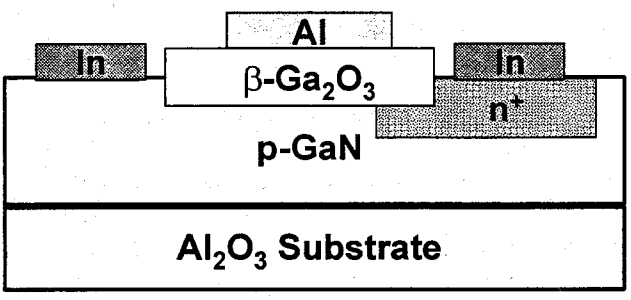

FIG. 5.21. Schematic cross-section of a thermally grown β-Ga_2O_3/p-GaN MOS diode with an n^+ source region.

5.5.2 Results and Discussion

Figure 5.22 (a) shows room-temperature *C-V* curves at a frequency of 1 MHz for a thermally grown β-Ga_2O_3/p-GaN MOS sample with an n^+ source region at t_d of 1 and 30 s, respectively. An ideal *C-V* curve is also shown. Gate bias voltage was scanned back and forth between -5 and 5 V. In the ideal *C-V* curve, the flatband capacitance (C_{FB}/C_{ox}) is calculated to be 0.855 by using a dielectric constant of 10.2. The flatband voltage (V_{FB}) which is the corresponding voltage of the (C_{FB}/C_{ox}), gives a value of ~0.56 V from the

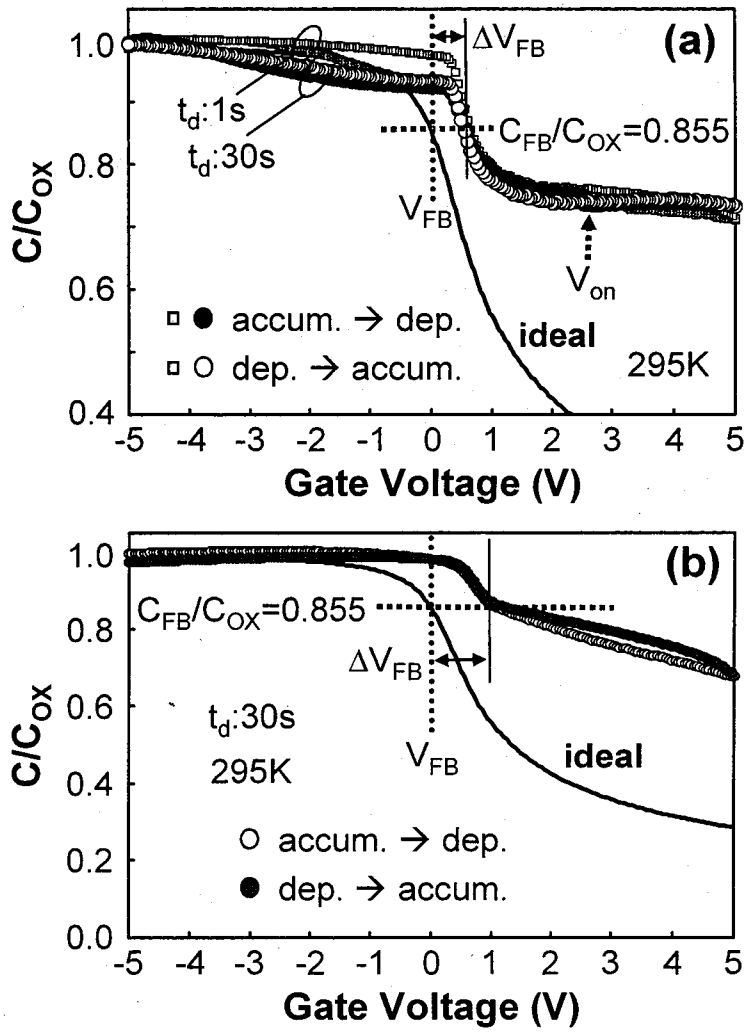

FIG. 5.22. High-frequency *C-V* hysteresis curves at room temperature for thermally grown β-Ga_2O_3/p-GaN MOS diodes (a) with and (b) without an n^+ source region as the gate bias voltage is swept from -5 to +5 V and then back to -5 V at t_d of 1 and 30 s, together with an ideal *C-V* curve.

measured *C-V* curve at t_d of 30 s. Thus, the flatband voltage shift (ΔV_{FB}) gives a negative fixed oxide charge density (N_f) of 1.3×10^{10} $eV^{-1}cm^{-2}$. In addition, the t_d dependence of the measured *C-V* curves is hardly observed in the flatband and depletion regions. That is, the total hysteresis window at the flatband is found to be very small for the measured *C-V* curves under different sweep directions, regardless of t_d. Even

though the frequency dependence of the accumulation capacitance is considered, the total interface state density is estimated to be less than $1x10^{10}$ $eV^{-1}cm^{-2}$ [16,17]. Furthermore, the measured *C-V* curves show capacitance saturation in the depletion region and present a large deviation from the ideal *C-V* curve. Additionally, the referenced MOS sample without any n^+ source region is found to show a deep-depletion like feature [35], as discussed later (Fig. 5.22 (b)). These results indicate that the capacitance saturation is probably associated with the surface inversion induced by the injection of minority carriers from the n^+ source region. Thus, we can say that the capacitance saturation observed is a typical feature of the surface inversion in the high-frequency *C-V* characteristics. A sudden and small capacitance drop is also observed at ~2.5 V in the measured *C-V* curves when the bias voltage is swept from accumulation to depletion, as shown in Fig. 5.22 (a). This value may be an onset voltage V_{on} of the surface inversion for this MOS diode. On the other hand, the accumulation capacitance of the measured *C-V* characteristics seems to depend on the t_d and sweep direction. A large hysteresis is observed in the accumulation region of the measured *C-V* curves at t_d of 1 s under different sweep directions. This hysteresis dwindles away and the accumulation capacitance becomes slightly smaller than a value expected from the ideal *C-V* curve with an increase of t_d. These results indicate the observed variation in accumulation capacitance may be related to the presence of defects inside of the β-Ga_2O_3 layer, which is in reasonable agreement with those discussed previously in section 5.3.

Figure 5.23 (a) shows representative room-temperature *C-V* curves at frequencies of 1, 2, 3, and 10 kHz for a thermally grown β-Ga_2O_3/p-GaN MOS sample with an n^+ source region at t_d of 30 s, respectively. Gate bias voltage was swept from -4 V (accumulation) to +10 V (depletion). An increase in capacitance can be clearly seen when the bias voltage is applied towards the depletion region, regardless of measurement frequency. This phenomenon is a typical behavior of the surface inversion in the low-frequency *C-V* characteristics. As shown in Fig. 5.23 (b), the inversion capacitance is found to increase significantly with decreasing measurement frequency. This is probably caused by the incomplete ionization of Mg dopants in

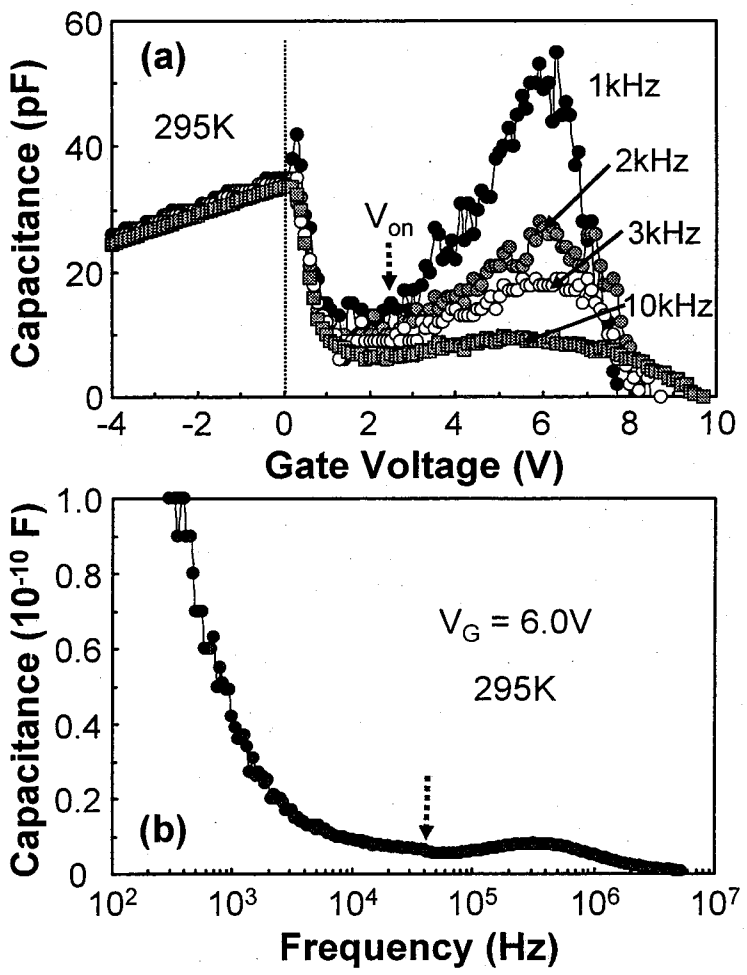

FIG. 5.23. (a) Room-temperature *C-V* curves at frequencies of 1, 2, 3, and 10 kHz for thermally grown β-Ga_2O_3/p-GaN MOS diode with an n^+ source region as the gate bias voltage is swept from -4 to +10 V at t_d of 30 s. (b) Frequency dependence of inversion capacitance at bias voltage of 6 V at room temperature for thermally grown β-Ga_2O_3/p-GaN MOS diode with an n^+ source region.

the GaN:Mg active layer, as stated in chapter 3 [36-41]. That is, as the measurement frequency is decreased, the Mg deep acceptors can follow the frequency voltage modulation, resulting in an improvement of the minority carrier injection from the n^+ source region. This inversion behavior could be seen even at 200 °C.

The V_{on} of the surface inversion is ~2.5 V, which value seems to be independent of measurement frequency. The V_{on} of the low-frequency *C-V* characteristics is also in good agreement with that of the high-frequency characteristics as stated above. The *C-V* characteristics are likely to be classified into low- and high-frequency features at a frequency of ~40 kHz, which characteristic frequency may correspond to the impurity transition frequency f_t of the Mg deep acceptors in the GaN:Mg active layer, as shown in Fig. 5.23 (b) [36-41]. In addition, a decrease of capacitance in the accumulation region is due to the poor ohmic contact to the GaN:Mg layer.

The effective V_{on} of the surface inversion is estimated to be ~2 V from the ΔV_{FB}. This V_{on} obtained in this study is apparently much smaller than the values in the previous literature [16,17]. This reduction in V_{on} is considered to be caused by the enhanced implantation-doping characteristics attained by the Si+N co-implantation and subsequent activation annealing at high temperatures in addition to the extremely low interface trap density at the β-Ga_2O_3/p-GaN MOS interface. Here, in the Si+N co-implanted region, the sheet carrier concentration n_s and the electron mobility μ_e are 1.66×10^{14} cm^{-2} and 63.4 cm^2/Vs, respectively, from room-temperature Hall-effect measurements. Thus, effective Si activation efficiency, n_s/n_{Si}, of the n^+

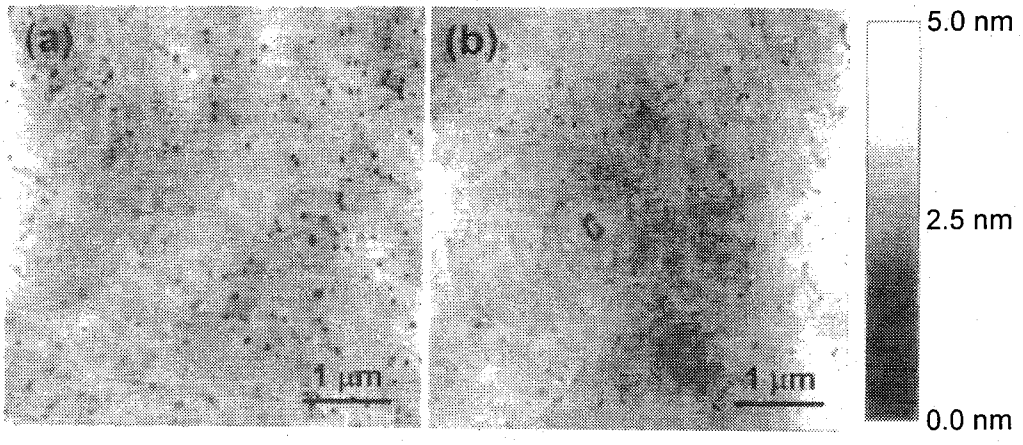

FIG. 5.24. AFM images of Si+N co-implanted p-GaN (a) before and (b) after annealing at 1300 °C. Both images are 5x5 μm^2.

source region is estimated to be ~38 % from the total implanted Si dosage n_{Si} of 4.35×10^{14} cm^{-2}. This value is in reasonable agreement with our previously reported value [28]. In addition, smooth surface morphology can be seen in the AFM images (Figs. 5.24 (a) and 5.24 (b)) before and after activation annealing at 1300 °C, although the activation annealing induces the out-diffusion of the Si atoms towards the GaN surface from SIMS measurements as shown in Fig. 5.25. As a consequence, an improvement in characteristics of the n^+p junction under the β-Ga_2O_3 layer gears up for the minority carrier injection from the n^+ source region. Moreover, the results obtained in this study suggest that the thermally grown β-Ga_2O_3/p-GaN MOS structure is a promising candidate for inversion-mode MOSFETs.

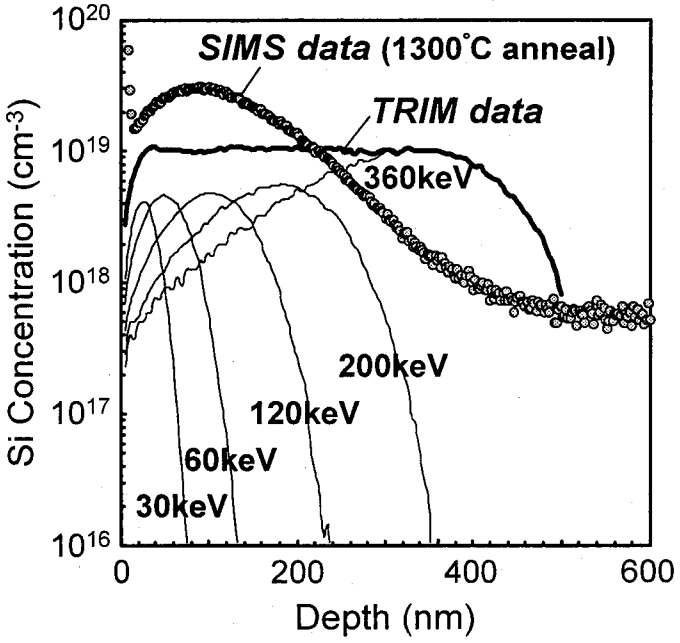

FIG. 5.25. SIMS profiles of implanted Si atoms in p-GaN after annealing at 1300 °C, together with TRIM data.

The characteristics of thermally grown β-Ga_2O_3/p-GaN MOS structures without any n^+ source regions are also investigated electrically. As shown in Fig. 5.22 (b), the V_{FB} gives a value of ~1.05 V from the measured *C-V* curve. Thus, the ΔV_{FB} gives a negative fixed oxide charge density N_f of 2.4×10^{10} $eV^{-1}cm^{-2}$. In addition, the t_d dependence of the measured *C-V* curves is hardly observed, which is identical with the situation of β-Ga_2O_3/p-GaN MOS structure with an n^+ source region. The sweep direction induced total hysteresis window $|V_{FB}^f - V_{FB}^b|$ at the flatband is found to be ~0.02 V even at long time t_d of 30 s, which small value corresponds to a low interface state density of ~1×10^{10} $eV^{-1}cm^{-2}$. This value is also the same level as that of β-Ga_2O_3/n-GaN MOS structure with an n^+ source region. Furthermore, the measured *C-V* curves present a large deviation from the ideal *C-V* curve in the depletion region. Bearing in mind that the surface inversion generally results in the capacitance saturation on the high-frequency *C-V* characteristics and that the MOS sample fabricated has low interface traps as mentioned herein, the observed behavior is likely to show both deep depletion and surface inversion features in the depletion region.

Figure 5.26 (a) shows typical *C-V* curves at frequencies of 1, 3 and 10 kHz for a thermally grown β-Ga_2O_3/p-GaN MOS sample without any n^+ source region, respectively. First, relatively small capacitance in the accumulation region is found due to the poor ohmic contact to the GaN:Mg layer, which results in inaccurate accumulation capacitance. Hereafter, low-frequency *C-V* characteristics are qualitatively stated. An increase in capacitance can be clearly seen when the bias voltage is applied towards the depletion region, regardless of measurement frequency. This peculiar behavior of capacitance is analogous to the low-frequency *C-V* characteristics that have previously reported to be observed in the gate controlled MOS diodes with n^+ source regions [16,17]. Thus, this phenomenon probably seems to correspond to a typical feature of the surface inversion in the low-frequency *C-V* characteristics. The GaN MOS structures without any n^+ source regions are generally known to show no surface inversion at room temperature, because the generation rate of the minority carriers is extremely low. Taking account of the high-frequency *C-V* characteristics as stated earlier, we can say that the surface inversion occurs at room temperature in the p-GaN MOS sample without any n^+ source regions. The surface inversion observed may result from characteristics

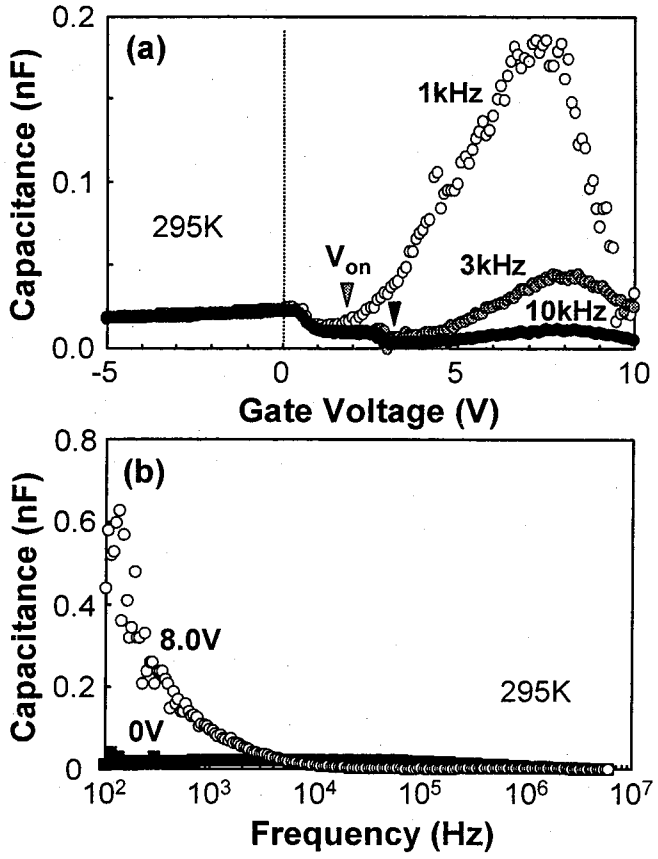

FIG. 5.26. (a) Room-temperature *C-V* curves at frequencies of 1, 3, and 10 kHz for thermally grown β-Ga_2O_3/p-GaN MOS diode without any n^+ source region as the gate bias voltage is swept from -5 to +10 V. (b) Frequency dependence of inversion capacitance at bias voltage of 8 V at room temperature for thermally grown β-Ga_2O_3/p-GaN MOS diode without any n^+ source region.

of thermally grown β-Ga_2O_3/p-GaN interface. As shown in Fig. 5.26 (b), the inversion capacitance at gate voltage of 8 V is found to increase significantly with decreasing measurement frequency. This is probably caused by the incomplete ionization of Mg dopants in the GaN:Mg active layer [36-41], as stated herein. The onset voltage V_{on} of the surface inversion seems to depend on measurement frequency; the V_{on} decreases

gradually with decreasing measurement frequency. The V_{on} obtained in this MOS structure without any n^+ source region is apparently much smaller than the values previously reported in the literature [16,17]. This reduction in V_{on} is considered to originate from the presence of efficient generation centers for minority carrier injection in addition to the low interface traps at the β-Ga_2O_3/p-GaN MOS interface as stated above. From the fact that threading dislocations in GaN act as recombination centers [42,43], the origin of the observed surface inversion may be related to the dislocations characteristic of heteroepitaxial GaN. Thus, the results obtained in this MOS structure without any n^+ source region probably suggest that the dislocations in p-GaN help to provide an external source of minority carriers instead of n^+ source regions, resulting in the partial formation of the surface inversion at the β-Ga_2O_3/p-GaN MOS interface.

In summary, the thermally grown β-Ga_2O_3/p-GaN MOS structures with the n^+ source regions have been fabricated by combining Si+N co-implantation and thermal dry oxidation techniques. From the frequency dependence of *C-V* characteristics at room temperature, the surface inversion with the V_{on} of ~2.5 V can be clearly seen. This small V_{on} is considered to be attained by the enhanced implantation-doping characteristics and the extremely low interface state density less than $1x10^{10}$ $eV^{-1}cm^{-2}$ at the β-Ga_2O_3/p-GaN MOS interface.

5.6 Conclusion

We have investigated interface properties of GaN MOS structures equipped with SiO_2 and/or β-Ga_2O_3 as a gate insulator by using high-frequency *C-V* and capacitance transient techniques. From the *C-V* measurements, the β-Ga_2O_3/n-GaN MOS structure shows a low interface state density of $\sim5.5x10^{10}$ $eV^{-1}cm^{-2}$, while the SiO_2/n-GaN MOS structure displays capacitance saturation in deep depletion (> 15 V) and a total interface state density of $\sim2.2x10^{12}$ $eV^{-1}cm^{-2}$. Thus, the surface Fermi level is probably unpinned at the β-Ga_2O_3/GaN interface, which may be probably associated with the presence of the interfacial Ga-oxynitride layer. In addition, the stacked SiO_2/β-Ga_2O_3/n-GaN MOS structure is found to improve both the electrical interface properties and the gate dielectric characteristics. Furthermore, we have studied electrical properties of the β-Ga_2O_3/p-GaN MOS structure with an n^+ source region fabricated on sapphire substrates. The n^+

regions were selectively produced in Mg-doped GaN by Si+N co-implantation and subsequent annealing at 1300 °C, and then 100-nm-thick β-Ga_2O_3 was grown by dry oxidation at 880 °C for 5 h. Room-temperature *C-V* measurements display a surface inversion feature with an onset voltage of ~2.5 V and show an extremely low interface state density less than $1x10^{11}$ $eV^{-1}cm^{-2}$. These results suggest that the thermally grown β-Ga_2O_3/p-GaN MOS structure is a promising candidate for inversion-mode MOSFETs.

References

[1] H. Morkoç, S. Strite, G. B. Gao, M. E. Lin, B. Sverdlov and M. S. Burns, J. Appl. Phys. **76**, 1363 (1994).

[2] T. P. Chow and R. Tyagi, IEEE Trans. Electron Devices **41**, 1481 (1994).

[3] J. Han, A. G. Baca, R. J. Shul, C. G. Willison, L. Zhang, F. Ren, A. P. Zhang, G. T. Dang, S. M. Donovan, X. A. Cao, H. Cho, K. B. Jung, C. R. Abernathy, S. J. Pearton, and R. G. Wilson, Appl. Phys. Lett. **74**, 2702 (1999).

[4] M. A. Khan, X. Hu, A. Tarakji, G. Simin, J. Yang, R. Gaska, and M. S. Shur, Appl. Phys. Lett. **77**, 1339 (2000).

[5] F. Ren, M. Hong, S. N. G. Chu, M. A. Marcus, M. J. Schurman, A. Baca, S. J. Pearton, and C. R. Abernathy, Appl. Phys. Lett. **73**, 3893 (1998).

[6] J. W. Johnson, B. Luo, F. Ren, B. P. Gila, W. Krishnamoorthy, C. R. Abernathy, S. J. Pearton, J. I. Chyi, T. E. Nee, C. M. Lee, and C. C. Chuo, Appl. Phys. Lett. **77**, 3230 (2000).

[7] H. Hong, K. A. Anselm, J. Kwo, H. M. Ng, J. N. Baillargeon, A. R. Kortan, J. P. Mannaerts, A. Y. Cho, C. M. Lee, J. I. Chyi, and T. S. Lay, J. Vac. Sci. Technol. B **18**, 1453 (2000).

[8] H. Kim, S. Park, and H. Hwang, J. Vac. Sci. Technol. B **19**, 579 (2001).

[9] H. Kawai, M. Hara, F. Nakamura, and S. Imanaga, Electron Lett. **34**, 592 (1998).

[10] H. C. Casey, Jr, G. G. Fountain, R. G. Alley, B. P. Keller, and S. P. Denbaars, Appl. Phys. Lett. **68**, 1850 (1996).

[11] P. Chen, W. Wang, S. J. Chua, and Y. D. Zheng, Appl. Phys. Lett. **79**, 3530 (2001).

[12] S. Arulkumaran, T. Egawa, H. Ishikawa, T. Jimbo, and M. Umeno, Appl. Phys. Lett. **73**, 809 (1998).

[13] W. P. Li, R. Zhang, Y. G. Zhou, J. Yin, H. M. Bu, Z. Y. Luo, B. Shen, Y. Shi, R. L. Jiang, S. L. Gu, Z. G. Liu, Y. D. Zheng, and Z. C. Huang, Appl. Phys. Lett. **75**, 2416 (1999).

[14] L. W. Tu, P. H. Tsao, K. H. Lee, I. Lo, S. J. Bai, C. C. Wu, K. Y. Hsieh, and J. K. Sheu, Appl. Phys. Lett. **79**, 4589 (2001).

[15] T. Rotter, D. Mistele, J. Stemmer, F. Fedler, J. Aderhold, J. Graul, V. Schwegler, C. Kirchner, M. Kamp, and M. Heuken, Appl. Phys. Lett. **76**, 3923 (2000).

[16] J. Kim, R. Mehandru, B. Luo, F. Ren, B. P. Gila, A. H. Onstine, C. R. Abernathy, S. J. Pearton, and Y. Irokawa, Appl. Phys. Lett. **80**, 4555 (2002).

[17] J. Kim, R. Mehandru, B. Luo, F. Ren, B. P. Gila, A. H. Onstine, C. R. Abernathy, S. J. Pearton, and Y. Irokawa, Appl. Phys. Lett. **81**, 372 (2002).

[18] Y. Nakano and T. Jimbo, Appl. Phys. Lett. **82**, 218 (2003).

[19] Y. Nakano and T. Jimbo, J. Vac. Sci. Technol. B **21**, 1364 (2003).

[20] H. H. Tippins, Phys. Rev. **140**, 316 (1965).

[21] D. J. Fu, Y. H. Kwon, T. W. Kang, C. J. Park, K. H. Baek, H. Y. Cho, D. H. Shin, C. H. Lee, and K. S. Chung, Appl. Phys. Lett. **80**, 446 (2002).

[22] J. W. Seo, C. S. Oh, H. S. Jeong, J. W. Yang, K. Y. Lim, C. J. Yoon, and H. J. Lee, Appl. Phys. Lett. **81**, 1029 (2002).

[23] Y. Nakano, T. Kachi, and T. Jimbo, Appl. Phys. Lett. **82**, 2443 (2003).

[24] C. Lee, H. Chen, H. Lee, Appl. Phys. Lett. **82**, 4304 (2003).

[25] R. Therrien, G. Lucovsky, and R. F. Davis, Phys. Stat. Sol. (a) **176**, 793 (1999).

[26] J. W. Johnson, B. P. Gila, B. Luo, K. P. Lee, C. R. Abernathy, S. J. Pearton, J. I. Chyi, T. E. Nee, C. M. Lee, C. C. Chuo, and F. Ren, J. Electrochem. Soc. **148**, G303 (2001).

[27] Y. Nakano, T. Kachi, and T. Jimbo, Appl. Phys. Lett. **83**, 4336-4338 (2003).

[28] Y. Nakano and T. Jimbo, J. Appl. Phys. **92**, 3815 (2002).

[29] Y. Naknao and T. Kachi, Appl. Phys. Lett. **79**, 1468 (2001).

[30] Y. Naknao and T. Kachi, J. Appl. Phys. **91**, 884 (2002).

[31] T. Yoshimura, N. Fujimura, D. Ito, and T. Ito, J. Appl. Phys. **87**, 3444 (2000).

[32] L. G. Meiners, Appl. Phys. Lett. **33**, 747 (1978).

[33] Y. Mochizuki and M. Mizuta, Appl. Phys. Lett. **69**, 3051 (1996).

[34] Y. Nakano and T. Jimbo, Appl. Phys. Lett. **80**, 4756 (2002).

[35] Y. Nakano, T. Kachi, and T. Jimbo, J. Vac. Sic. Technol. B **21**, 2220 (2003).

[36] D. Seghier and H. P. Gislason, Appl. Phys. Lett. **88**, 6483 (2000).

[37] N. D. Nguyen, M. Germain, M. Schmeits, B. Schineller, M. Hueken, J. Appl. Phys. **90**, 985 (2001).

[38] Y. Nakano and T. Kachi, Appl. Phys. Lett. **79**, 1631 (2001).

[39] Y. Nakano and T. Jimbo, J. Appl. Phys. **92**, 5587 (2002).

[40] Y. Nakano and T. Jimbo, Appl. Phys. Lett. **81**, 3990 (2002).

[41] Y. Nakano, T. Kachi, and T. Jimbo, Appl. Phys. Lett. **82**, 2082 (2003).

[42] S. J. Rosner, E. C. Carr, M. J. Ludowise, G. Girolami, and H. I. Erikson, Appl. Phys. Lett. **70**, 420 (1997).

[43] Z. Z. Bandić, P. M. Bridger, E. C. Piquette, and T. C. McGill, Appl. Phys. Lett. **72**, 3166 (1998).

Chapter 6

Conclusions and Future Trends

6.1 Conclusions of this Work

This dissertation has focused on the development and understanding of requisite processing technologies such as n- & p-type implantation doping and gate insulators of GaN to facilitate the fabrication of advanced inversion-mode GaN metal-oxide-semiconductor field-effect transistors (MOSFETs). Here, we summarized this dissertation as follows.

In Chapter 1, the state-of-the-art GaN power MOSFETs that might be expected to replace the Si power devices in high-power switching applications for near-future EV electronics, were discussed and some requisite basic technologies such as n- & p-type implant doping and gate insulators of GaN were chosen.

In Chapter 2, we reported on n-type implant doping of GaN by using Ge, Si, and O dopants. First, we have investigated the doping characteristics and structural defects of Ge+N co-implanted GaN. N-type regions were produced in undoped GaN films by Ge and Ge+N implantation and subsequent annealing with an SiO_2 encapsulation layer at 1300 °C. Improved Ge-doping characteristics were achieved for GaN by Ge+N co-implantation, attaining activation efficiencies of ~44 %, whereas in the case of conventional Ge implantation, the activation efficiency was low due to the lack of N atoms for maintaining the GaN stoichiometry. From transmission electron microscopic observations, the damage induced by the co-implantation was entirely restored by annealing at 1300 °C. However, positron annihilation spectroscopic measurements revealed the creation of new vacancy-type defects with markedly different characteristics in the electrically activated regions by the annealing of both Ge- and Ge+N-implanted samples. Second, Si-doping characteristics have been systematically investigated for Si+N co-implanted GaN. N-type regions were produced in undoped GaN films by the co-implantation and subsequent annealing with

an SiO_2 encapsulation layer at high temperatures. The sheet carrier concentration was seen to be precisely controllable between $3x10^{12}$ cm^{-2} and $5x10^{14}$ cm^{-2} with Si activation efficiencies of ~50% when the samples were annealed at 1300 °C. From atomic force microscopic observations, the co-implanted sample showed smooth surface morphology identical with that before implantation, whereas Ga islands were found to be formed in surface region by the activation annealing in the case of conventional Si implantation. Therefore, the Si+N co-implantation technique turned out to be an effective method to enhance electrical and structural properties in view of GaN stoichiometry. However, implantation-induced micro-defects remained even after the high-temperature annealing process for both Si- and Si+N-implanted GaN samples. Furthermore, doping characteristics of O-implanted GaN have been investigated systematically from a viewpoint of annealing temperature. The implanted O atoms became electrically active as an n-type dopant after annealing above 1050 °C, but with a low activation efficiency of only 1.1 %. From variable temperature Hall-effect measurements, O-implanted GaN displayed a shallow ionization level of ~18.3 meV after 1100 and 1200 °C anneals. In addition, secondary ion mass spectrometry measurements showed no measurable redistribution of the O atoms by the annealing. These results indicated poor probability of the O atoms occupying an N-lattice site in GaN.

In Chapter 3, we focused on the electrical characterization of p-type GaN in advance of p-type implant doping. First, current deep-level transient spectroscopy (*I*-DLTS) technique has been applied to the investigation on acceptor levels in Mg-doped GaN grown by metal-organic chemical-vapor deposition (MOCVD). For activation of the Mg dopant, rapid thermal annealing was performed with an SiO_2 encapsulation layer at 850 °C in N_2. *I*-DLTS measurements on the fabricated Schottky diode revealed a discrete deep level located at ~112 meV above the valence band, corresponding to the energy level measured by the conventional thermal admittance spectroscopy (TAS). This energy level was also in good agreement with the frequency dependence of capacitance in view of the characteristic frequency. Therefore, this energy level is most probably attributed to the Mg acceptor state itself. Second, TAS and *I*-DLTS techniques have been applied to the Schottky diodes fabricated on Mg-doped GaN grown by MOCVD to

investigate the dependence of the Mg acceptor levels on the annealing temperature. Both measurement techniques revealed two deep acceptor levels with activation energies at ~135 and ~160 meV above the valence band. The former level was only seen when the samples were annealed at temperatures between 650 and 700 °C, and its presence corresponded with a significant increase in effective acceptor concentration, as confirmed by low-frequency capacitance-voltage (*C-V*) measurements. Therefore, this acceptor level was considered to dominate the electrical activation of Mg in GaN.

In Chapter 4, we dealt with p-type implant doping of GaN by using Be dopant. First, we have electrically investigated the acceptor levels that were present in Be-implanted GaN. Slight p-type conductivity was attained in undoped GaN films by Be implantation and subsequent annealing at 1050 °C with an SiO_2 encapsulation layer. Capacitance-frequency measurements showed a typical dispersion effect characteristic of deep acceptors in the Schottky diodes fabricated. TAS measurements revealed a discrete deep level located at ~231 meV above the valence band. This energy level was in reasonable agreement with the frequency dependence of the capacitance in view of the impurity transition frequency. Therefore, this energy level was most probably assigned to a Be-related deep acceptor. Second, p-type regions were produced in undoped GaN films by Be and Be+O implantation and subsequent annealing at temperatures between 1000 and 1050 °C. From TAS measurements, the activation energy of the Be acceptor level was found to decrease from ~240 to ~163 meV by the implantation of additional O atoms, which was in reasonable agreement with the improvement in p-type doping characteristics, as determined by room-temperature Hall-effect measurements. These results indicated that the Be+O co-implantation reduced the depth of the Be acceptor level based on a site-competition effect. Therefore, these acceptor levels were most probably attributable to Be atoms at interstitial and Ga-lattice sites, respectively.

In Chapter 5, we reported on some kinds of gate insulators of GaN. First, we have investigated the interface properties of SiO_2/n-GaN MOS structures by using *C-V* and capacitance transient techniques. The MOS diodes were fabricated by SiO_2 sputtering onto n-GaN epitaxial layers grown by atmospheric pressure MOCVD on sapphire substrates. *C-V* characteristics showed a total interface state density of ~2.2×10^{12}

$eV^{-1}cm^{-2}$ and displayed capacitance saturation in deep depletion (> 15 V). The capacitance in deep depletion was found to significantly increase by incident white light. A capacitance transient was also seen after applying reverse voltages, reflecting thermal emission of carriers from the SiO_2/GaN interface. DLTS measurements revealed a dominant interface trap with an activation energy of ~0.77 eV from the conduction band, corresponding to the capacitance transient. Therefore, this interface trap was considered to induce surface Fermi-level pinning, which resulted in the capacitance saturation in the measured *C-V* characteristics. Second, we have investigated the interface properties of thermally oxidized n-GaN MOS structures fabricated on sapphire substrates. 100-nm-thick β-Ga_2O_3 was grown by dry oxidation at 880 °C for 6 h. From secondary ion mass spectrometry measurements, an intermediate Ga-oxynitride layer with composition gradient was clearly observed at the β-Ga_2O_3/GaN interface. *C-V* measurements showed a deep depletion feature and a low interface state density of ~$5.5x10^{10}$ $eV^{-1}cm^{-2}$. Additionally, no discrete interface traps could be detected by DLTS measurements. These results indicated that the surface Fermi level was unpinned at the β-Ga_2O_3/GaN interface, which was probably associated with the presence of the interfacial Ga-oxynitride layer. Third, we have investigated the interface properties of SiO_2/n-GaN MOS structures with Ga-oxynitride interlayers. β-Ga_2O_3 15 nm thick was grown by dry oxidation at 800 °C for 6 h, and 100-nm-thick SiO_2 was then deposited by sputtering. From secondary ion mass spectrometry measurements, 35-nm-thick Ga-oxynitride had composition gradient and O atoms diffused into deeper lying region than the β-Ga_2O_3/GaN interface besides the β-Ga_2O_3 layer. *C-V* measurements showed a low interface state density of ~$3.9x10^{10}$ $eV^{-1}cm^{-2}$, resulting in an unpinning of the surface Fermi-level. These characteristics were clearly different from those without the interlayer. These stacked SiO_2/β-Ga_2O_3/n-GaN MOS structures were found to be equipped with both the outstanding interface properties and the good gate dielectric characteristics. Furthermore, we have studied the electrical properties of thermally oxidized p-GaN MOS structures with n^+ source regions fabricated on sapphire substrates. The n^+ regions were selectively produced in Mg-doped GaN by Si+N co-implantation and subsequent annealing at 1300 °C, and then 100-nm-thick β-Ga_2O_3 was grown by dry oxidation at 880 °C for 5 h. Room-temperature *C-V*

measurements displayed a surface inversion feature with an onset voltage of ~2.5 V and showed an extremely low interface state density less than $1x10^{10}$ $eV^{-1}cm^{-2}$. These results suggested that the thermally grown β-Ga_2O_3/p-GaN MOS structure was a promising candidate for inversion-mode GaN MOS field-effect-transistors.

6.2 Suggestions for Future Works

In this work, we have developed some requisite processing technologies to facilitate the fabrication of advanced inversion-mode GaN MOSFETs. Several important results can be obtained, as stated above, whereas there are many problems remaining.

As for n-type implantation doping of Ge and Si, good doping characteristics can be obtained by using a co-implantation technique of additional N atoms, regardless of there being a number of implantation-induced defects remaining even after activation annealing. In their doping process, however, high-temperature annealing (> 1200 °C) is found to be required to activate the implanted dopant atoms. This annealing temperature is much higher than the growth temperature (~1100 °C), which indicates that thermal stability of GaN-based materials may be a concern in the high-temperature annealing process. In fact, we find that N-deficiency from GaN-lattice starts to occur at temperatures above 900 °C. Thus, an n-type implantation-doping technique that enables relatively low-temperature activation is more desirable. From this point of view, O-implantation doping becomes a promising option. In this case, however, effective activation efficiency of the implanted O atoms is too poor. Therefore, the implantation-doping technique should be better improved to be compatible with the low-temperature activation and the high activation efficiency. Additionally, in advance of the fabrication of real GaN MOSFET devices, a satisfactory level of contact resistivity for ohmic contacts to n-type implanted GaN should be assessed and then be feedbacked to the implant activation efficiency.

P-type GaN layers have to be formed selectively to realize power device structures that enable a normally-off operation for EV electronic applications. Thus, p-type implantation doping is a most attractive

processing technology. In particular, the Be+O co-implantation technique is found to reduce the depth of the Be acceptor level based on a site-competition effect. However, the present doping level is inadequate to fabricate these power devices. A significant increase in effective acceptor concentration is needed in connection with a decrease in acceptor energy level to improve p-type activation efficiency. To that end, we will have to optimize an O/Be ratio and annealing conditions for the Be+O co-implantation process. Furthermore, ohmic contacts to p-type implanted GaN should be assessed.

Regarding gate insulators, a low interface state density, a low leakage current, and a high breakdown voltage need to be obtained. From this point of view, the combination of thermal dry oxidation and SiO_2 deposition is considered to be a powerful tool to overcome troublesome issues of GaN MOS structures. A stacked SiO_2/β-Ga_2O_3/GaN MOS structure is found to improve both the electrical interface properties and the gate dielectric characteristics; the β-Ga_2O_3 interlayer provides good electrical interface properties and the SiO_2 layer reduces gate leakage currents and enhances oxide breakdown voltages, respectively. To enhance these characteristics, a photoelectrochemical oxidation technique which yields very smooth thin oxide surface and a high-temperature SiO_2 deposition technique which improves gate characteristics, become promising practical options. In addition, gate metals should be assessed for real GaN MOSFET devices.

At present, available GaN epitaxial layers have poor crystal quality, compared to Si and GaAs. They have high dislocation densities on the order of 10^6 - 10^{10} cm^{-2}. In accordance with an advance in the GaN growth technique, the crystal quality will be improved remarkably. Thus, the present characteristics of the ion-implantation doping and the gate insulators will be better improved with a rise of GaN crystal quality. In addition, these processing technologies should be combined to fabricate real GaN MOSFET devices. In this case, some thermal management may be an open issue. In particular, the difference of annealing temperatures between n- and p-type implant activation may be a bottleneck when both implantation-doping techniques are simultaneously applied to the realization of their device design.

Furthermore, physical source of deep levels in GaN and related materials are not known in general. Particularly, any correlation between defects and electronic properties in GaN has not been well understood,

because there are a large number of different types of defects may be present; dislocations, point defects, complexes, extrinsic & intrinsic defects. Among them, electronic defects, especially implantation-induced defects probably seem to limit performance of FETs. Therefore, we will have to pay much more attentions to point defects in GaN in the near future. In particular, electrical characterization of process-induced point defects will gear up for the establishment of basic technologies for GaN power devices.