MOCVD Growth and Evaluation of GaAs on p^+n-Si and n^+p-Si Substrates

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This paper describes the MOCVD growth of GaAs on p^+n-Si and n^+p-Si substrates in GaAs/Si monolithic tandem solar cell technology. A GaAs epilayer with an etch pit density (EPD) of less than $5\times10^6cm^{-2}$ was achieved by inserting a GaP buffer, GaP/GaAsP and GaAsP/GaAs strained layer superlattices (SLS's) between the GaAs epilayer and Si substrate, and combining in-situ thermal cycle (TC) and post-growth thermal cycle. The samples with 4 μm-thick GaAs epilayer on p^+n-Si and n^+p-Si were evaluated by molten KOH etching at 350°C and cross-sectional TEM images. Electron-beam induced current (EBIC) shows that in the case of p^+n-Si substrate, the p-n junction of Si is destroyed due to diffusion of P and As. On the other hand, in the case of n^+p-Si substrate the p-n junction of Si remained with some modification after the growth of GaAs. The efficiency of an n^+p-Si solar cell filtered by 4μm GaAs is 5.2%.

1. Introduction

In recent years, there have been significant increses in the growth of GaAs on Si substrate, and a lot of kind of devices have been fabricated. A GaAs on Si solar cell of 19.2% conversion efficiency at AMO one sun ($1\times1cm^2$) has been demonstrated [1] . The Si has characteristics of light weight, low cost and tough compared to GaAs. GaAs solar cell has characteristics of high conversion efficiency and radiation resistance, but the cost is high. The GaAs/Si tandem structure solar cell which combines the advantages of Si and GaAs will produce large area, high efficiency, light weight and low cost. The GaAs is transparent for infrared light of the wavelength longer than 0.87 μm, and the infrared light can not be converted to electric power. If the Si substrate also has a p-n junction, this GaAs/Si monolithic tandem type solar cell will have wide spectral sensitivity and about 30% conversion efficiency [2] .

We will discuss the improvements of GaAs growth on p^+n-Si and n^+p-Si substrates which have led to GaAs epilayer with an etch pit density (EPD) of less than $5\times10^6cm^{-2}$. This etch pit density is low enough to get GaAs/Si solar cell of 17% efficiency [3] . These improvements were achieved by inserting GaP buffer layer, GaP/$GaAs_{0.5}$ $P_{0.5}$ and $GaAs_{0.5}$ $P_{0.5}$/GaAs strained layer superlattices (SLS's) between the GaAs epilayer and Si substrate, and performing in-situ thermal cycle (TC) and post-growth TC. And we will discuss the modification of p-n junction in Si substrates before and after GaAs growth in order to develop the fabrication technique of GaAs/Si tandem solar cell.

2. Growth procedure

2. 1 Sample preparation

The wafers of 0.02 Ω-cm (100) 2° off n-Si and 2 Ω-cm (100) 2° off p-Si are used. First of all, a p-n junction was formed in Si substrate by thermal diffusion. In the case of n-Si wafer, B_2O_3 emulsion diffusant was spin-coated on clean Si wafer and p-n junction of 1 μm depth and the hole concentration of $1\times10^{19}cm^{-3}$ was made at 1000°C for 15 minutes. In the case of p-Si wafer, a p-n junction of 1 μm depth and the electron concentration of $8\times10^{18}cm^{-3}$ was formed at 900°C for 25 minutes. Diffusant is P_2O_5 emulsion.

2. 2 Growth procedure of GaAs

The structure of GaAs/Si monolithic tandem solar cell and the structure of our experimental sample are shown in Fig. 1 and Fig. 2, respectiviely.

A conventional metalorganic chemical vapor deposition (MOCVD) system consisting of horizontal reactor was used for GaAs layer growth. Trimethylgallium, arsine and phosphine are the source gases. Hydrogen selenide and diethylzinc are used for n and p type dopants. The oxide film formed

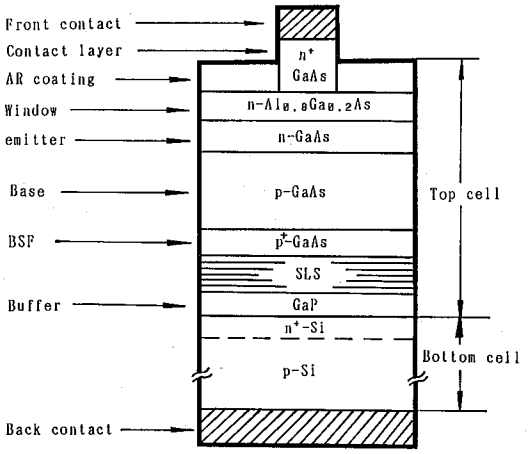

Fig. 1 Structure of GaAs/Si monolithic tandem solar cell

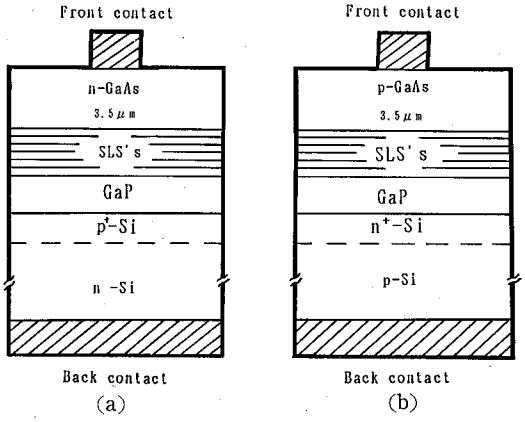

Fig. 2 Structure of experimetal samples
(a) n-GaAs on p^+n-Si substrate
(b) p-GaAs on n^+p-Si substrate

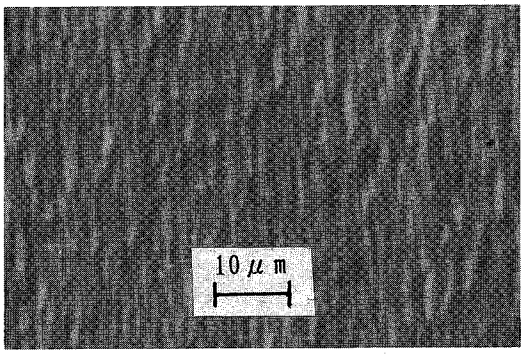

Fig. 3 As grown surface micrograph of GaAs on p^+ n-Si

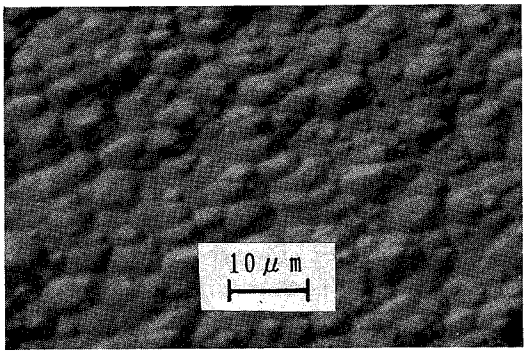

Fig. 4 Molten KOH etched surface micrograph of GaAs on p^+n-Si

by thermal diffusion was etched off from Si substrates before putting wafer into the reactor. Thermal cleaning of Si wafer was performed in atmospheric pressure H_2 at 1000°C for 15 minutes before GaP growth to eliminate the antiphase domain (APD) [4] . Next, 0.5 μm GaP, two SLS's and 3.5 μm GaAs were grown. The GaP is relatively lattice matched to Si, and the SLS's are composed of GaP/$GaAs_{0.5}$ $P_{0.5}$ and $GaAs_{0.5}$ $P_{0.5}$/GaAs. The growth temperature of GaP, SLS's and GaAs are 900°C, 800°C and 750°C, respectively. In-situ thermal cycle (TC) and post-growth theramal cycle are performed to improve quality of GaAs crystal.

3. Results of GaAs epilayer

As-grown GaAs has a mirror surface as shown in Fig. 3. The 4 μm-thick film was etched with molten KOH at 350°C to reveal etch pit for determination of etch pit density (EPD). A typical etched surface is shown in Fig. 4. Characteristically aligned pits indicate that the GaAs epilayer is single-domain crystal. These pits are supposed to correspond to threading dislocation. On the occasion of same growth process, GaAs layer EPD of p^+n-Si substrate and n^+p-Si substrate are about same. On the occasion of various process, EPD is various. EPD of GaAs on Si grown by the conventional growth is order of $10^8 cm^{-2}$, and when the thickness of epilayer exceeds 3 μm, cracks appears in the GaAs on Si due to the difference in the thermal expansion coefficients. Thus, the reduction of dislocation density is necessary. The GaP and two SLS's are inserted between the GaAs epilayer and Si substrate, and thermal cycle (TC) are performed, then quality of GaAs crystal is improved. The typical sequences of growth and thermal cycle are shown in

Fig. 5, and the resulting EPD numbers are summarized in Table 1.

The procedures of growth and thermal cycle are : (a) conventional growth ; (b) post-growth annealing at 900°C for 15 minutes ; (c) one in-situ thermal cycle between 200°C and 900°C followed by GaAs growth ; and (d) one thermal cycle between 200°C and 900°C followed by GaAs growth, and one thermal cycle between 200°C and 900°C after growth (in-situ TC 1 + post-growth TC 1). The total thickness of epilayer here was fixed at about 4 μm (the total GaAs layer thickness was about 3.5 μm). The effect of EPD reduction is largest for (d), and decrease for (c), (b) and (a), in order.

Comparing (b) and (c), it is obvious that TC is more effective than post annealing. The process of thermal anneal and thermal cycle is efficient at temperatures higher than GaAs growth teperature. According to the results of in-situ TC experiments, the optimum thermal cycle layer thickness of GaAs is about 1.5～2 μm for 3.5～4 μm total epilayer. In the experiment, in-situ TC is performed at about 2 μm -thick GaAs epilayer. The as-grown surface and molten KOH etched surface micrographs of GaAs on n^+p-Si in the cases (d) and (c) are shown in Fig. 6 and Fig. 7. Comparing (d) and (c), the surface

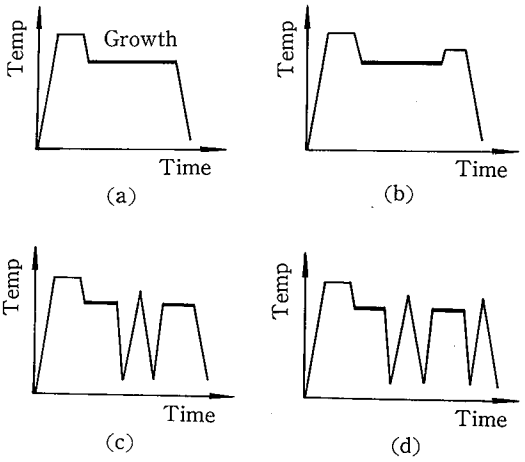

Fig. 5 Schematic diagrams of growth procedures
(a) Conventional growth
(b) Post growth annealing
(c) In-situ TC
(d) In-situ TC and post-growth TC

Table 1 Growth procedure and EPD

Growth procedure	EPD (cm^{-2})
(a) Conventional growth	$\sim 1\times10^8$
(b) Post growth annealing (900°C, 15min)	1.2×10^7
(c) In-situ TCl (200°C～900°C)	7.2×10^6
(d) In-situ TCl+Post TCl (200℃～900℃)	4.3×10^6

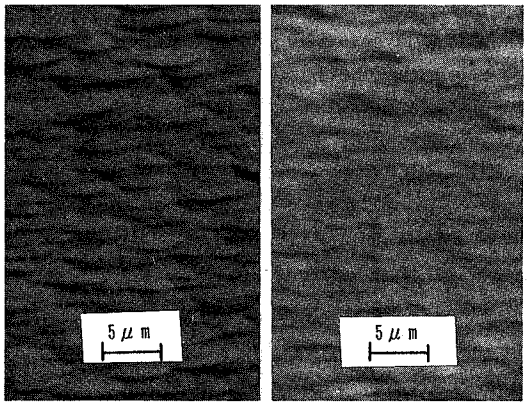

Fig. 6 As-grown surface micrographs of GaAs on n^+p-Si
(a) in-situ TC
(b) in-situ TC and post-growth TC

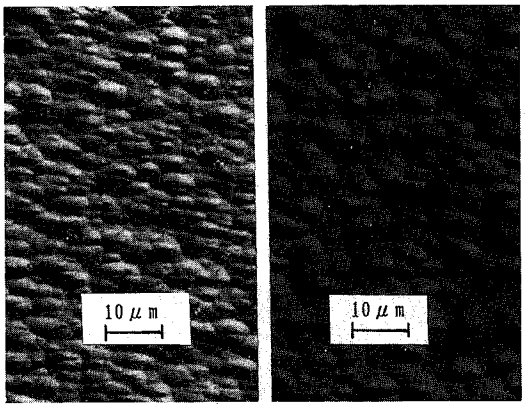

Fig. 7 Molten KOH etched surface micrographs of GaAs on n^+p-Si
(a) in-situ TC
(b) In-situ TC and post-growth TC

morphology of GaAs on n^+p-Si with in-situ TC and Post-growth TC is smoother than that with in-situ TC only. The EPD of GaAs epilayer was reduced to $3.5\sim5\times10^6cm^{-2}$ by in-situ TC, and post-growth TC. In the case of in-situ TC, the EPD of GaAs epilayer was $7.2\times10^6cm^{-2}$.

The 4 μm-thick GaAs on p^+n-Si substrate with in-situ TC and post-growth TC was evaluated by cross-sectional TEM image. A TEM image is shown in Fig. 8. Because the GaP buffer is relatively lattice matched to Si, dislocation density is not high. The stress put repeatedly in the GaP/GaAsP and GaAsP/GaAs SLS's bend threading dislocations and let the dislocations run away [5] . During the in-situ TC and post-growth TC, the dislocations move, combine and disappear due to thermal stress. As a result, the EPD of GaAs layer is reduced.

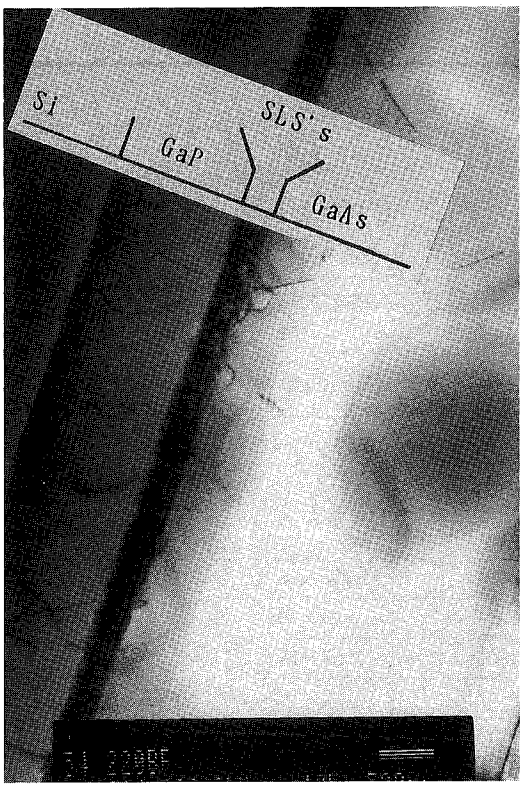

Fig. 8 TEM image of GaAs on n^+p-Si using in-situ TC and post-growth TC

4. P-n junction characteristics of p^+n-Si and n^+p-Si substrates

Electron-beam induced current (EBIC) profile of n-GaAs/p^+n-Si sample and p-GaAs/n^+p-Si sample are shown in Fig. 9 and Fig. 10, respectively. The EBIC signal in Fig. 9 has two weak peaks ; one is at the heterointerface of GaAs and GaP, another is at the heterointerface of GaP and Si. But there is no peak in the Si region. This shows that in the case of GaAs growth on p^+n-Si substrate, the p-n junction was destroyed due to P and As doping to Si substrate during the long high temperature growth process. Fig. 10 shows, on the other hand, in the case of n^+p-Si substrate, there is one strong peak at about 3 μm from Si/GaP interface and the p-n junction of Si substrate has remained after growth of GaAs.

Four-point probe and Hall measurements were performed on the samples after etching off the epilayer on Si substrates. The results also show that p type layer in n-Si substrate has changed to n type, and n type layer in p-Si substrate still remains after GaAs growth. The characteristics of the n^+p-Si solar

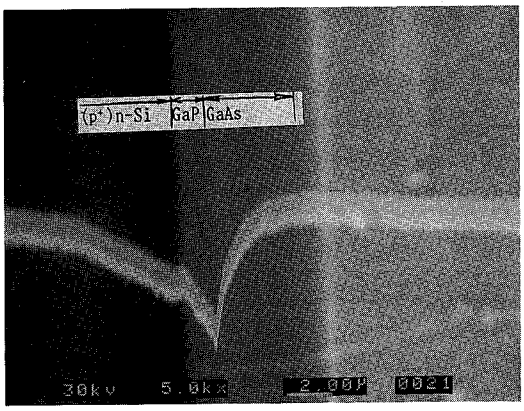

Fig. 9 EBIC profile and secondary electron image of GaAs on p^+n-Si substrate

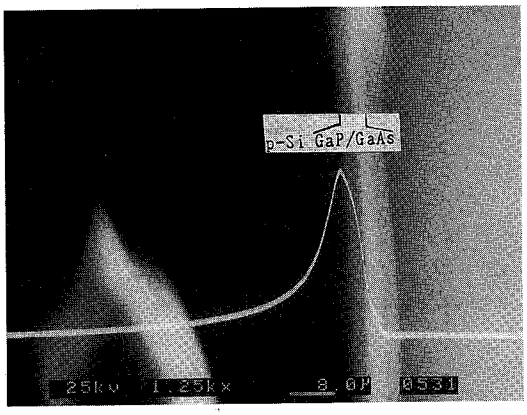

Fig. 10 EBIC profile and secondary electron image of GaAs on n^+p-Si substrate

Table 2 Characteristics of n^+p-Si cell before and after GaAs growth (AMO, 1Sun, 27°C, 0.5×0.5cm²)

	Voc (mV)	Jsc (mA/cm²)	η total (%)	N_D (cm^{-3})	X_j (μm)
before growth of GaAs	580	39.9	14.0	8×10^{18}	1.0
4 μm GaAs epilayer filtered	468	17.6 (Without AR coating)	5.2	5×10^{18}	~3.0

cell filtered by 4 μm GaAs epilayer and n^+p-Si before growing GaAs epilayer are listed in Table 2.

Table 2 shows that the modification of impurity concentration N_D is small before and after growth because P and As are donor dopants in Si and the electron concentration of n type layer in Si substrate is replenished during growth of GaAs. The modification of junction depth x_j is serious. The x_j is 1 μm and 3 μm before and after growth. The conversion efficiency of n^+p-Si cell filtered by 4 μm GaAs is 5.2%. This low efficiency is due to x_j modification and the light absorption by GaAs epilayer.

5. Conclusion

In the MOCVD growth of GaAs on Si substrate with p-n junction, the combination of the GaP buffer, GaP/GaAsP and GaAsP/GaAs SLS's, in-situ TC and post-growth TC can reduce EPD of GaAs epilayer effectively. Although the p-n junction in n-Si substrate has been detsroyed, the p-n junction in p-Si substrate has remained with some modification after growth of GaAs. The efficiency of 4 μm GaAs filtered n^+p-Si solar cell is 5.2%. Taking into account of change of Si junction and optimizing GaAs growth process and tandem solar cell structure, GaAs/Si monolithic tandem solar cell of high efficiency is expected.

6. References

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