バル　シング　チャウダリ
氏　　名　BAL SINGH CHAUDHARI

学位の種類　博士（工学）
学位記番号　博第1325号
学位授与の日付　2024年3月31日
学位授与の条件　学位規則第４条第１項該当　課程博士

学位論文題目　MOVPE Growth and Characterization of CdTe Epilayers Grown Directly on Si Substrates
（MOVPE法によるSi基板上CdTe層の直接成長と評価）

論文審査委員　主査　教授　Niraula Madan
教授　市村　正也
准教授　岸　直希
教授　青木　徹
（静岡大学）

論文内容の要旨

Epitaxial growth of single-crystal CdTe on large-area Si substrates for the development of X-ray and gamma ray detectors was studied. The direct growth of CdTe on Si substrates is challenging because of large differences in lattice mismatch and thermal expansion coefficient between these two materials. To overcome this, a specialized Si substrate pre-treatment method was employed to achieve the direct growth of CdTe single crystals on Si substrates. Subsequently, detectors were fabricated in a p-CdTe/n-CdTe/n^+-Si heterojunction diode structure. The detector evaluation, however, revealed that the detector suffered from a large dark current that severely degraded its gamma detection capability. It was confirmed that the primary source of the dark current was the high density of dislocations in the crystal. These dislocations were not only localized at the n-CdTe/n^+-Si heterointerface but also extended deeply into the epilayer, penetrating the depletion region formed between p-CdTe/n-CdTe, resulting generation of excessive dark currents. Similarly, the suboptimal transport characteristics of photon-generated charge carriers constituted another factor constraining the detector's property. It was discovered that the incomplete depletion of the thick p-CdTe layer, where charge carriers are primarily generated from the incident photons, led to carrier recombination during transport. To address these challenges, the following topics were explored to enhance the detector's performance. Firstly, growth of a thick and heavily doped n-CdTe layer was investigated to ensure the depletion region fully extends towards the p-CdTe layer, thereby

enhancing the transport of carriers. Secondly, methods for reducing dislocations were explored by the optimization of growth techniques and the incorporation of thermal annealing techniques. The thesis is structured into seven chapters, with the content of each chapter outlined below.

Chapter 1 presents the introduction and motivation of this work.

Chapter 2 includes a brief discussion of the experimental procedure used in this work for the growth and characterization of CdTe epilayers.

Chapter 3 describes the growth and iodine doping of CdTe layers grown on (211) Si by MOVPE. A high growth rate of 2.6 μm/h and high electron density of 10^{18} cm^{-3} were obtained by optimizing the growth temperature and flow-rate ratio of Te/Cd source materials. This made the growth of highly doped thick n-CdTe possible.

Chapter 4 evaluates dislocation density distribution in the CdTe epilayer and their correlation with the device dark currents. Thin devices had a high dislocation density, which decreased as the device thickness increased. However, even in a 35 μm thick device, a high threading dislocation (TD) density in the order of 10^6 cm^{-2} persisted. The detector's dark current showed a strong correlation with the density of dislocations that propagated and penetrated the depletion region formed at the n-CdTe/p-CdTe. It was determined that the dislocation density in the epilayer should be reduced well below the order of 10^6 cm^{-2} for effective detector applications.

Chapter 5 investigates dislocation density reduction in CdTe/Si epilayer using a technique called post-growth patterning and annealing. We created square island patterns with dimensions of 60 μm x 60 μm on a typically 10 μm thick CdTe epilayer using photolithography. The patterned samples were then annealed ex-situ in a flowing hydrogen environment at various temperatures. It was found that the sample annealed at 600 °C, 5 min showed the lowest TD density of 2.9 x 10^5 cm^{-2}, nearly an order of magnitude lower than the TD density of the of the whole wafer samples subjected to similar annealings. This confirmed the effectiveness of patterning and annealing in the dislocation reduction. However, regrowth of CdTe on the patterned and annealed samples to make thick films resulted very rough surface and needs further investigations.

Chapter 6 explores the optimizations of ex-situ annealing conditions for dislocations reduction and its implementation during the device fabrications. Typically, 5μm thick CdTe layers were used, where the temperatures, durations, and number of annealing cycles were varied. Afterward, n-CdTe layers were first annealed using the optimized conditions, 870 °C, 60s and 3 cycles, followed by growth of thick p-CdTe layers to fabricate devices in a p-CdTe/n-CdTe/n+-Si heterojunction structure. The TD density of these thick devices was lower than 10^5 cm^{-2}. They exhibited lower dark currents and improved gamma detection properties when compared to similar devices that did not undergo annealing during their fabrication.

Chapter 7 summarizes the entire work and provides recommendations for future research.

論文審査結果の要旨

CdTe半導体は室温動作可能なX 線、ガンマ線検出器用材料として注目されており、すでにバルク結晶成長法によるCdTe単結晶を用いた小型検出器が作製されている。しかし、バルクCdTe 結晶は均一かつ良好な電気特性を持つ大面積結晶の成長が極めて困難であるため、大面積かつ高性能の検出器の実現は困難な状況にある。この問題点をMOVPE法による大面積 Si 基板上の厚膜 CdTe 単結晶成長層を用いることにより解決が期待できる。しかし、本方法による CdTe 成長層を用いた検出器では暗電流の低減、さらに放射線によって発生されたキャリアの輸送特性向上などにより検出器高性能化の課題があった。

本研究ではまず、p-CdTe/n-CdTe/n^+-Si ヘテロ接合ダイオード型放射線検出器の評価を行い、キャリアの輸送特性向上には p-CdTe層全体に空乏層を広げる必要があり、そのため n-CdTe層の高電子密度化と厚膜化が必要であることを見だした。 ここでは、MOVPE法による (211) Si基板上の n-CdTe 層の成長時にCdとTeの原料供給比、成長温度およびドーパント（エチルヨウ素）供給量の最適化を行い、従来のn-CdTe層に比べて成長速度は約５倍（2.6 μm/h）、また、電子密度は１から２桁ほど高く(10^{18} cm^{-3})の成長条件を確立した。これにより厚膜化と高電子密度化の両立が可能となった。

続いて、検出器の暗電流の評価を行い、暗電流発生メカニズムを解明した。SiとCdTeの格子不整合の原因による高密度の転位は、n-CdTe/p-CdTe接合で形成される空乏層内まで伝播し、検出器暗電流を増加させるとともに、深い準位（キャリアトラップ）として活動し、検出特性劣化させることを確認した。CdTe 成長層の低転位密度化に向けて、成長層に島状のパターンを形成し熱処理により転位の運動を促進させ、パターンの自由表面に逃がす方法（PHP法）を用いて、その有効性を検証した。膜厚が10 μm程度の試料を用いて検討を行った結果、本PHP法により転位密度は従来のパターン形成せずに熱処理行う法に比べて有効であることを示した。しかし、検出器の作製に必要とする膜厚の厚い試料ではパターン形成は難しく、また、パターンを形成後再び成長を行った場合成長表面は不均一となり、本PHP法を今後さらなる検討が必要であることも確認した。

最後に、検出器作製に向けて、厚膜層の成長時に成長早期段階で成長を一度中断して熱処理行い、その後再成長行う方法について検討行った。熱処理条件の最適化を行い作製した 40 μm 程度の成長層では転位密度を~10^5 cm^{-2}となり、熱処理を行わず同条件で作製した試に比べて一桁ほど減少した。さらに、作製したデバイスでは暗電流の低減および放射線検出特性の向上も見られた。

以上、本検討により得られた結果は成長層の高品質化とデバイス特性の向上に有効であると考えられる。またこれらの研究成果は４編の審査あり学術論文として公表されている。よって、本研究の業績は博士の学位を授与するに十分であると評価できる。