MOVPE Growth and Characterization of CdTe Epilayers Grown Directly on Si Substrates

(MOVPE 法による Si 基板上 CdTe 層の直接成長と評価)

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Abstract

Epitaxial growth of single crystal CdTe on large-area Si substrates for the development of X-ray, gamma ray detectors was studied. The direct growth of CdTe on Si substrates is very difficult because of large differences in lattice mismatch and thermal expansion coefficient between these two materials. To overcome this, a specialized Si substrate pre-treatment method was applied to achieve the direct growth of CdTe single crystals on Si substrates. Subsequently, detectors were fabricated in a p-CdTe/n-CdTe/n^+-Si heterojunction diode structure. The detector evaluation, however, revealed that the detector suffered from a large dark current that severely degraded its X-ray, gamma ray detection capabilities. It was confirmed that the primary source of the dark current was the high dislocations in the crystal generated due to mismatch between the epilayer and the substrate. These dislocations were not only localized at the n-CdTe/n^+-Si heterointerface but also extended deeply into the epilayer, penetrating the depletion region formed between p-CdTe/n-CdTe, resulting generation of excessive dark currents. Furthermore, the suboptimal transport characteristics of photon-generated charge carriers constituted another factor degrading the detector's property. It was found that the incomplete depletion of the thick p-CdTe layer, where charge carriers are primarily generated from the incident photons, led to carrier recombination during their transport. To address these challenges, the following topics were studied to enhance the detector's performance. Firstly, growth of a thick and highly doped n-CdTe layer was investigated to ensure the depletion region fully extends towards the p-CdTe layer, thereby enhancing the transport of carriers. Secondly, methods for reducing dislocations were explored by

the optimization of growth technique and the incorporation of thermal annealing techniques. The thesis is structured into seven chapters, with the content of each chapter given below.

Chapter 1 presents the introduction and motivation of this work.

Chapter 2 includes a brief discussion of the experimental procedure used in this work for the growth and characterization of CdTe epilayers.

Chapter 3 describes the growth and iodine doping of CdTe layers grown on (211) Si by MOVPE. A high growth rate of 2.6 μm/h and high electron density of 10^{18} cm^{-3} were obtained by optimizing the growth temperature and the flow-rate ratio of Te/Cd source materials. This made the growth of highly doped thick n-CdTe possible.

Chapter 4 evaluates dislocation distribution in the CdTe epilayer and their correlation with the device dark currents. Thin devices had a high dislocation density, which decreased as the device thickness increased. However, even in a 35 μm thick device, a high threading dislocation (TD) density in the order of 10^6 cm^{-2} persisted. The detector's dark current showed a strong correlation with the density of dislocations that propagated and penetrated the depletion region formed at the n-CdTe/p-CdTe. It was determined that the dislocation density in the epilayer should be reduced well below the order of 10^6 cm^{-2} for effective detector applications.

Chapter 5 investigates dislocation density reduction in CdTe/Si epilayer using a technique called post-growth patterning and annealing. We created square island patterns with dimension of 60 μm x 60 μm on a typically 10 μm thick CdTe epilayer using photolithography. The patterned samples were then annealed ex-situ in a flowing hydrogen environment at various temperatures for 5 min. It was found that sample annealed at 600 ^{0}C showed the lowest TD density of 2.95 x 10^5 cm^{-2}, nearly an order of

magnitude lower than the TD density of the whole wafer samples subjected to similar annealings. It was suggested that annealing enhances the dislocation glide towards the sidewalls of island where they terminate, hence their densities are reduced on the island surfaces. This confirmed the effectiveness of this technique. However, regrowth of CdTe on the patterned and annealed samples to make thick epilayers resulted very rough surface, requiring further investigations.

Chapter 6 explores the optimizations of ex-situ annealing conditions for dislocation reduction and its implementation during the device fabrications. Typically, 5 μm thick CdTe layers were used, where temperatures, durations, and the number of annealing cycles were varied. The lowest TD density of 2 x 10^6 cm^{-2} was obtained in the sample annealed at 870 ºC, 60 s for 3 cycles. Using this annealing condition, the devices were fabricated in a p-CdTe/n-CdTe/n^+-Si heterojunction structure, where n-CdTe layers were first annealed, followed by growth of 40 μm thick p-CdTe layers. The TD density of these thick devices was lower than 10^5 cm^{-2}. They exhibited lower dark currents and improved gamma detection properties when compared to similar devices that did not undergo annealing during their fabrication.

Chapter 7 summarizes the entire work and provides recommendations for future research.

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Chapter 1

Introduction

1.1 Radiation Detectors

Radiation detectors are being used in various fields, including nuclear physics, industry, security, space astronomy and medical imaging. Several types of radiation detectors such as scintillators and semiconductor-based silicon (Si) and germanium (Ge) are available for spectroscopy and imaging applications. However, scintillator detectors are slow in response and exhibit poor energy resolution. On the other hand, semiconductor-based detectors such as silicon (Si) and germanium (Ge) exhibit good energy resolution, high-quality imaging [1,2]. However, due to the low atomic number, Si detector has a low photon absorption efficiency and is not suitable for high energy radiations exceeding 30 keV. Ge, on the other hand, has a small band gap, hence a cryogenic cooling is required during the operation to reduce the detector leakage currents. In order to solve these problems several alternative detector materials such as CdTe or CdZnTe, GaAs, HgI_2, TlBr, are being explored [3-7]. Among them, compound semiconductors such as CdTe, CdZnTe are considered highly superior material for the room temperature X-ray, gamma ray detector development that does not need cryogenic cooling. **Table 1.1** compares the material properties of CdTe with that of well-established detectors such as Si and Ge. CdTe has a high average atomic number (Z_{Cd}=48, Z_{Te}=52) and high density 5.85 g/cm^3 that give CdTe a high absorption coefficient for the incident photons. Besides its wide energy band gap of 1.48 eV makes it suitable for the room

temperature operation. CdZnTe, on the other hand, which is obtained by adding a few percentages of Zn on CdTe during the crystal growth, possesses almost similar material properties to that of CdTe, except than the higher energy bandgap.

Table 1.1 Properties of semiconductor materials

Material	CdTe	Si	Ge
Atomic number	48,52	14	32
Density [g/cm^{-3}]	5.85	2.33	5.33
Band gap [eV]	1.48	1.12	0.67
Resistivity [Ωcm]	10^9	~10^4	50
Electron mobility [cm^2/v.s.]	1100	1400	3900
Hole mobility [cm^2/v.s.]	100	480	1900
Electron lifetime [μs]	3	>1000	>1000
Hole lifetime [μs]	2	2000	2000

Figure 1.1 compares the detection efficiencies of 1mm thick Si, Ge and CdTe detectors for various photon energies from 1 to 1000 keV. The detection efficiencies were calculated using equation (1.1), where the absorption coefficient (μ) was calculated from X-Ray Mass Attenuation Coefficients data base available on homepage of NIST [8].

$$\text{Detection efficiency} = (1 - e^{-\mu t}) \text{ x } 100\% \qquad (1.1),$$

where μ is the absorption coefficient and t is the detector thickness

The result shows, compared to other materials, CdTe has a high detection efficiency for the whole range of photon energies. The high detection efficiency coupled with the

possibility of room temperature operation make CdTe most promising materials for detector fabrication. However, current detector-grade CdTe, CdZnTe crystals are mainly grown by melt-growth technique [9-13]. Presently, these melt-grown crystal contains numerous defects, and in some cases exhibit polycrystallinity that lead to poor electrical transport properties and inhomogeneity, which limit the detector size to small dimensions [11,12,14]. This significantly hampers the development of large area detectors with high energy resolution [11,12,14]. Hence there is a strong need for growth of large area and high-quality crystal with uniform material properties.

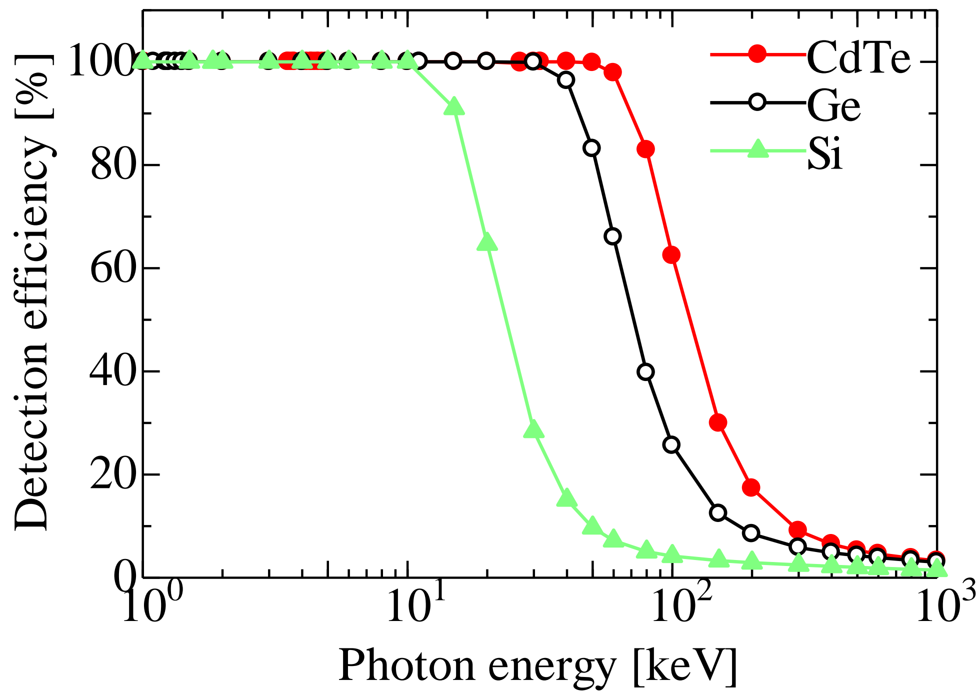

Fig. 1.1 Calculated detection efficiency for 1mm thick Si, Ge and CdTe detectors as a function of photon energy.

1.2 Motivation and purpose of this work

CdTe and CdZnTe are the promising materials that show the great potential for the development of room temperature X-ray, gamma ray detectors. Present CdTe or CdZnTe crystals for radiation detector fabrication are grown using travelling heater method (THM)-based melt growth process [9-13,15,16]. High energy resolution, small area detectors are being developed using melt-grown bulk CdTe or CdZnTe crystal. However, the growth of uniform and large-area bulk crystal is very difficult. So, the development of large-area imaging arrays has been a major challenge. Also, the production cost of bulk crystal is high, and handling of the crystals is difficult due to crystal fragility. The grown crystal has various defects such as non-uniform and polycrystalline that lead to poor electrical transport properties. One of the ways to alleviate those challenges is to employ heteroepitaxial growth technique. The heteroepitaxial growth of thick and detector-grade single crystal CdTe films on large area substrates such as GaAs or Si is a promising way for achieving large-area crystal with uniform material properties. This epitaxial growth technique not only provides the required uniform large area crystals, but also offers strict control of electrical property of the crystal by adjusting the growth parameters as well as impurity dopings during the growth. This results in additional flexibilities in the detector design. Several growth techniques, including hot wall epitaxy (HWE) [17-19], molecular beam epitaxy (MBE) [20-22] and metalorganic vapor phase epitaxy (MOVPE) [23-25] have been investigated to grow epitaxial layers. MBE is a highly effective technique for the growth of high-quality CdTe epilayers [20-22], however, growth rate in MBE is low and it will be very difficult to grow thick films. For example, about 180 μm thick CdTe layers are needed for developing X-ray, gamma ray detectors to detect 60 keV photons with a detection efficiency of 50%. Besides, a thin ZnTe or Ge buffer layer is grown prior

to the CdTe growth to facilitate single crystal growth of CdTe on Si substrates [26,27]. This technique is very effective for devices that operate in lateral direction such as infrared (IR) detectors [28-30]. However, it is not suitable for vertical devices, such as X-ray or gamma ray detectors, where photon-generated charge carriers travel vertically across the heterointerface and are collected at respective electrodes. To overcome these challenges, we have investigated growth of high quality and thick single crystal CdTe epilayers directly on the Si substrates using metalorganic vapor epitaxy (MOVPE) [31-34]. Using our growth technique, single crystal CdTe of thicknesses up to 260 μm could be achieved [35]. Subsequently, these epitaxially grown CdTe epilayers were used to fabricate detectors in a p-CdTe/n-CdTe/n+-Si in a heterojunction structure. Evaluation of detector properties revealed that the detector suffered from a large dark current that severely degraded its gamma detection capability. It was found that crystal defects such as dislocations resulted due to the large differences in lattice mismatch and thermal expansion between the CdTe and Si was the major sources of detector dark currents. Furthermore, it was also found that the transport properties of photon-generated charge carriers were affected because of the incomplete depletion of the thick p-CdTe layer, resulting recombination of carriers during their transport. This constituted another factor constraining the detector's property.

The aim of this study was to reduce the defects present in CdTe epilayers and to improve the detector's charge carrier properties. For this, we first studied growth of thick and heavily doped n-CdTe layers so that the depletion layer fully extends towards the p-CdTe layer, which will enhance the transport properties of photon-generated charge carriers. Subsequently, we investigated on dislocations distribution on CdTe layers and found that dislocations were not only localized at the n-CdTe/n+-Si heterointerface but also extended

deeply into the epilayer, penetrating the depletion region formed between p-CdTe/n-CdTe, resulting generation of excessive dark currents. To address this challenge, we investigated on dislocation density reduction methods such as post-growth patterning and thermal cycle annealing while growing thick CdTe layers. Thermal annealing enhances the dislocation-dislocation glide motion so that they may annihilate or coalesce, as a result their number can be reduced in the CdTe epilayer [35]. Ex-situ annealing was performed on outside of the growth chamber, interrupting the growth, on the whole wafer or on the patterned samples by varying annealing parameters (such as temperature, time and cycle) in a flowing hydrogen environment. Finally, gamma ray detectors were fabricated applying these methods to evaluate their effectiveness in improving the detection properties.

1.3 Organization of the thesis

The growth of undoped p-type CdTe layers, heavily doped thick n-type CdTe layers on Si substrate, as well as investigation on the dislocation reduction techniques and their application in device fabrication and evaluation, are described in detail in this thesis. The thesis is structured into seven chapters, with the content of each chapter outlined below.

Chapter 1 presents the introduction and motivation of this work.

Chapter 2 includes a brief discussion of the experimental procedure used in this work for the growth and characterization of CdTe epilayers.

Chapter 3 describes the growth and iodine doping of CdTe layers grown on (211) Si by MOVPE.

Chapter 4 evaluates dislocation distribution in CdTe epilayer and their correlation with the device dark currents.

Chapter 5 investigates dislocation density reduction in CdTe/Si epilayer using a technique called post-growth patterning and annealing. After that, regrowth on the patterned annealed samples was studied to achieve thicker CdTe epilayers.

Chapter 6 investigates optimization of dislocation reduction in an MOVPE-grown CdTe/Si epilayer by ex-situ annealing, followed by regrowth of thick CdTe epilayer and its implementation on device fabrications.

Chapter 7 Summarize the whole work and provides recommendations for the future work.

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Chapter 2

Experimental procedure

2.1 Introduction

CdTe epilayers were grown on Si substrate using the metalorganic vapor phase epitaxy (MOVPE) growth technique, where a special Si substrate pretreatment was employed to achieve single crystal growth of CdTe directly on the Si substrates. The thermal annealing of the grown epilayers was performed ex-situ in a separate chamber in a flowing hydrogen environment to reduce the defects in the crystal. The samples were characterized with optical microscopy, x-ray diffraction (XRD), dislocation decoration etch pit method, current-voltage, and gamma detection tests. The details about these techniques are presented in this chapter.

2.2 Growth of CdTe using MOVPE technique

2.2.1 Growth system

In this work, the growth was carried out in a custom-built vertical growth reactor equipped with a load-lock system. The reactor is operated at atmospheric pressure during the growth. A schematic diagram of the MOVPE reactor is shown in **Fig. 2.1**. The growth reactor is made of stainless steel, and it can accommodate max 4-inch size wafer. The wafer is placed on a specially designed graphite-coated carbon susceptor, which is heated by the resistive heating system. The wafers are loaded into the reactor using the load-lock system. The susceptor is rotated at a speed of 6.0 rpm during the growth. The source materials and the dopants are transported to the reactor using dedicated flow lines, where

highly pure hydrogen is used as a carrier gas. Their flow rate is controlled using the mass-flow controller. Near the reactor entrance, these flow lines merged as shown in **Fig.2.1**, which are then branched into multiple feedlines (supply lines A-C) to cover the whole area of the large-sized wafer. Each supply line has a needle valve for the further control of the source flow. Only middle supply line A was used throughout this study. The distance between the outlet of this supply line and the susceptor is about 30 mm.

2.2.2 Source materials and substrate

Dimethylcadmium (DMCd) and diethyltelluride (DETe) were used as the group II and group VI source materials for the growth of undoped CdTe, whereas ethyl-iodine (EI) was used as a dopant for the n-CdTe growth.

In this study, (211)-oriented Si substrates measuring 24 mm x 24 mm were used to obtain single-crystal growth of CdTe. Typically, two substrates were used per growth run. In previous studies conducted in our laboratory, both (100) Si and (211) Si substrates were investigated for CdTe growth. However, CdTe grown on (100) Si substrates exhibited polycrystalline characteristics, with the CdTe layer containing both (100) and (111) domains [1]. On the other hand, growth on the high-index (211) Si substrates resulted in twin-free, single-domain CdTe with an orientation parallel to the substrates [1]. The stepped nature of the high-index (211) Si surface plays an important role in suppressing twinning and other structural defect formation during growth [2-4].

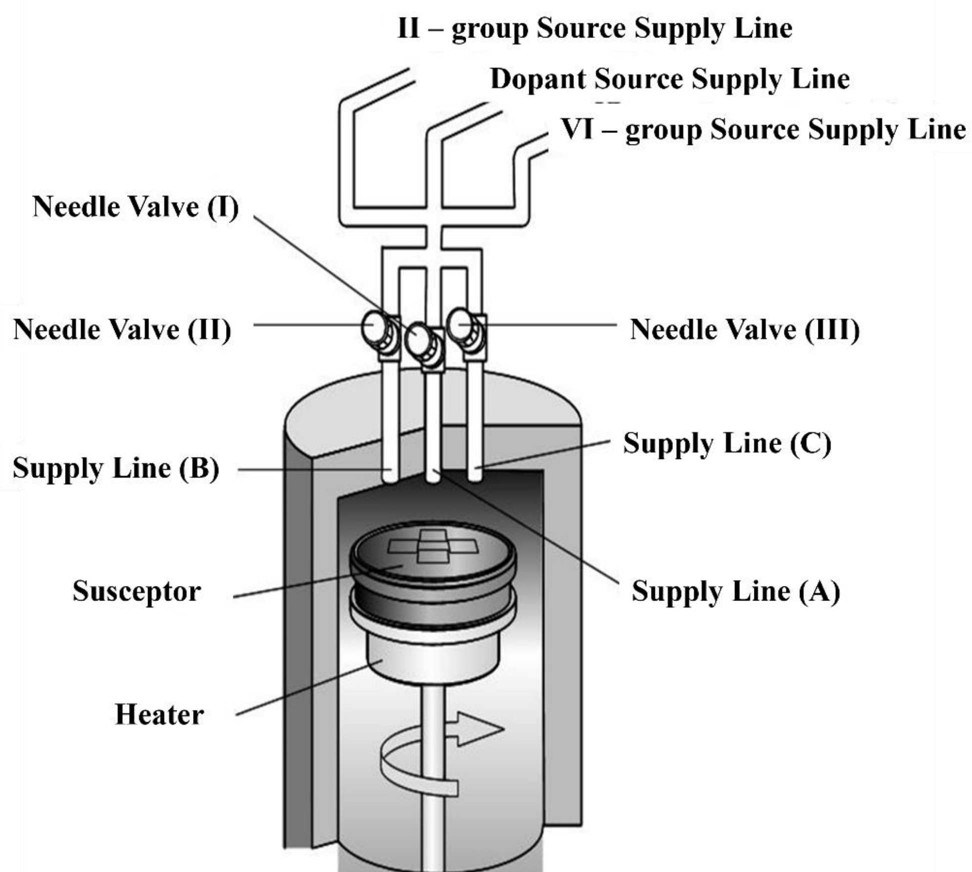

Fig. 2.1 Schematic diagram of MOVPE reactor.

2.3 Growth procedure

2.3.1 Substrates cleaning

(a) Si substrates cleaning

(1) Si substrates were boiled in acetone for 3 min to remove organic materials.

(2) Rinsed with deionized water for 3 min.

(3) Cleaned with H_2SO_4: H_2O_2 = 1:1 to remove organic materials.

(4) Washed in running deionized water for 3 min.

(5) Etched with HF: H_2O = 1:50 for 1 min. to remove oxide from surface.

(6) Lastly, washed with deionized water for few seconds.

(7) Dried using a nitrogen gas blow.

(b) GaAs substrates cleaning

(1) Small pieces of GaAs were boiled in acetone for 3 min. to remove organic materials.

(2) Rinsed with deionized water for 3 min.

(3) Cleaned with H_2SO_4 for 1 min.

(4) Etched with H_2SO_4: H_2O_2: H_2O = 5: 1:1 for 5 min.

(5) Washed in running deionized water for 5 min.

(6) Dried using a nitrogen gas blow.

2.3.2 Si substrates pretreatments

The growth of CdTe directly on Si substrates is extremely difficult because of large differences in lattice constants (19.3%) and thermal expansion coefficients between these two materials. Without a special substrate pretreatment, the grown layers become polycrystalline and easily peel-off from the substrate. In this study, we addressed this

challenge by applying a previously developed Si substrate pretreatment method in our laboratory, where the Si substrates are coated with a very thin layer of GaAs prior to CdTe growth to promote the single crystal growth [5-7]. We call this technique as "GaAs treatment".

The GaAs treatment of the Si substrates was conducted in a separate chamber as shown schematically in **Fig. 2.2.** It consists of a horizontal quartz tube, a heater with multi-channel temperature controller which surrounds the quartz tube and can be moved horizontally over the tube, gas handling system and an exhaust system. The quartz tube is 175 cm long with a diameter of 5 cm. High purity hydrogen and nitrogen were used as process gas, their flow rate was controlled by mass flow controller. Pressure inside the quartz tube was monitored by pressure gauge and a rotary pump was used for evacuation. The GaAs treatment process is as follows.

Before introducing the Si and GaAs substrates, the quartz tube was baked at 700~900 ºC for 30 min. in a hydrogen environment.

(1) Purge the quartz tube with nitrogen.
(2) Introduce the chemically cleaned Si and GaAs substrates inside the quartz tube, their positions were separated by about 40 cm, as in **Fig. 2.2.**
(3) Purge the quartz tube with hydrogen.
(4) Adjust the pressure inside the quartz at 0.1 to1 Torr.
(5) Maintain the temperatures of GaAs and Si substrates at 800 ºC and 900 ºC respectively, heat them in a flowing hydrogen environment for 120 min.
(6) Stop heating the Si substrates and then allow it to cool down for 60 minutes.

(7) Take out the Si substrates and GaAs from quartz tube.

(8) Load the Si substrates immediately into the MOVPE growth chamber for the CdTe growth.

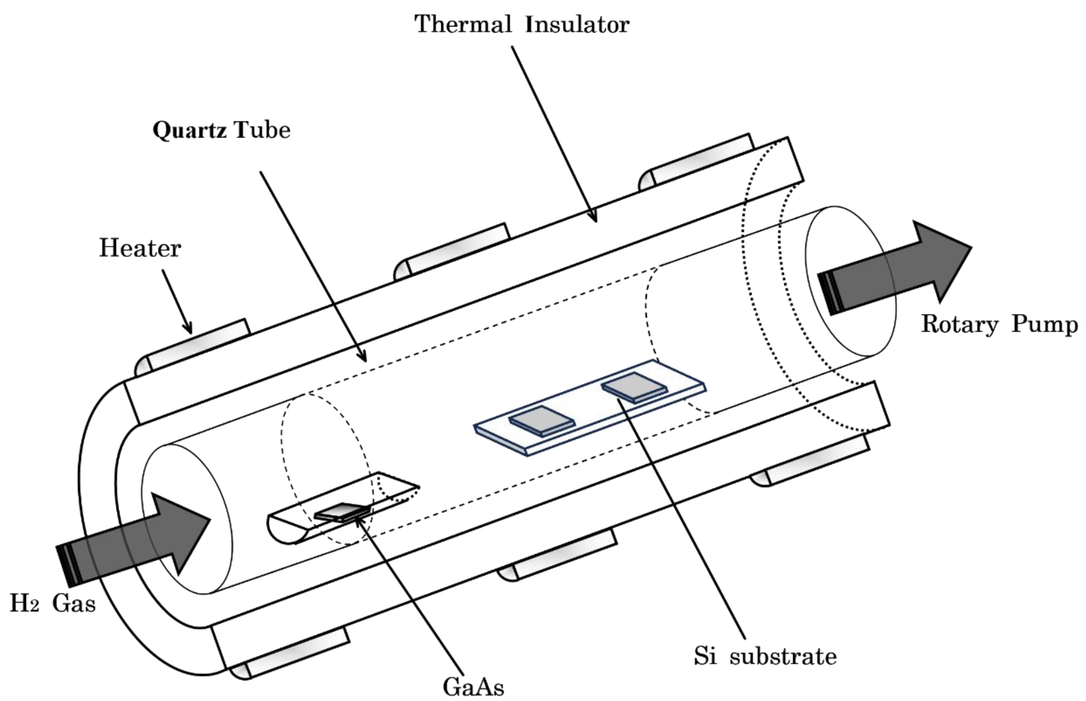

Fig. 2.2 Schematic diagram of GaAs treatment setup.

2.4 Growth conditions

The GaAs-treated Si substrates were loaded into the vertical MOVPE reactor, working at atmospheric pressure. The growth was carried out at substrate temperatures varying from 325 ^{o}C to 560 ^{o}C. The growth conditions for the n-CdTe and undoped p-CdTe are listed in **Table 2.1**. Iodine was used as a dopant to achieve the n-CdTe layers, however, layers grown without intentional doping exhibited high resistivity and a p-type property [8].

Table 2.1 Typical Growth conditions of CdTe epilayers on Si substrates

	n-CdTe	p-CdTe
Carrier gas supply (l/min)	65	65
DMCd (mol/min)	3.12×10^{-5}	3.92×10^{-5}
DETe (mol/min.)	7.56×10^{-6}	1.17×10^{-4}
DETE/DMCd (VI/II) flow ratio	0.25	3.0
EI (mol/min.)	4.28×10^{-8}	undopped
Growth temperature (^{o}C)	325	450 ~ 560

2.5 Post growth thermal annealing

Post growth thermal annealing was performed in a separate setup outside the growth chamber, using the same apparatus that was employed for the “GaAs-treatment”. The annealing was performed placing one sample over the another (face to face) in a hydrogen environment, as schematically shown in **Fig. 2.3**. This face-to face configuration was chosen to suppress Cd evaporation from the sample surface due to its high vapor pressure. Before initiating the experiment, the heater was set to desired temperature. Once the

temperature is settled, the annealing was started by moving the heater over to the sample position, kept there for the fixed anneal time for each cycle, and then moved away. In this study, the anneal temperatures were varied from 550 to 1000 ºC, whereas anneal duration was from 1 to 5 min. and the number of anneal cycles was varied from 1 to 7. After annealing, hydrogen inside of quartz tube was evacuated, the tube purged with nitrogen and then samples were removed from the quartz tube. Annealed samples were then characterized using various characterization techniques detailed below.

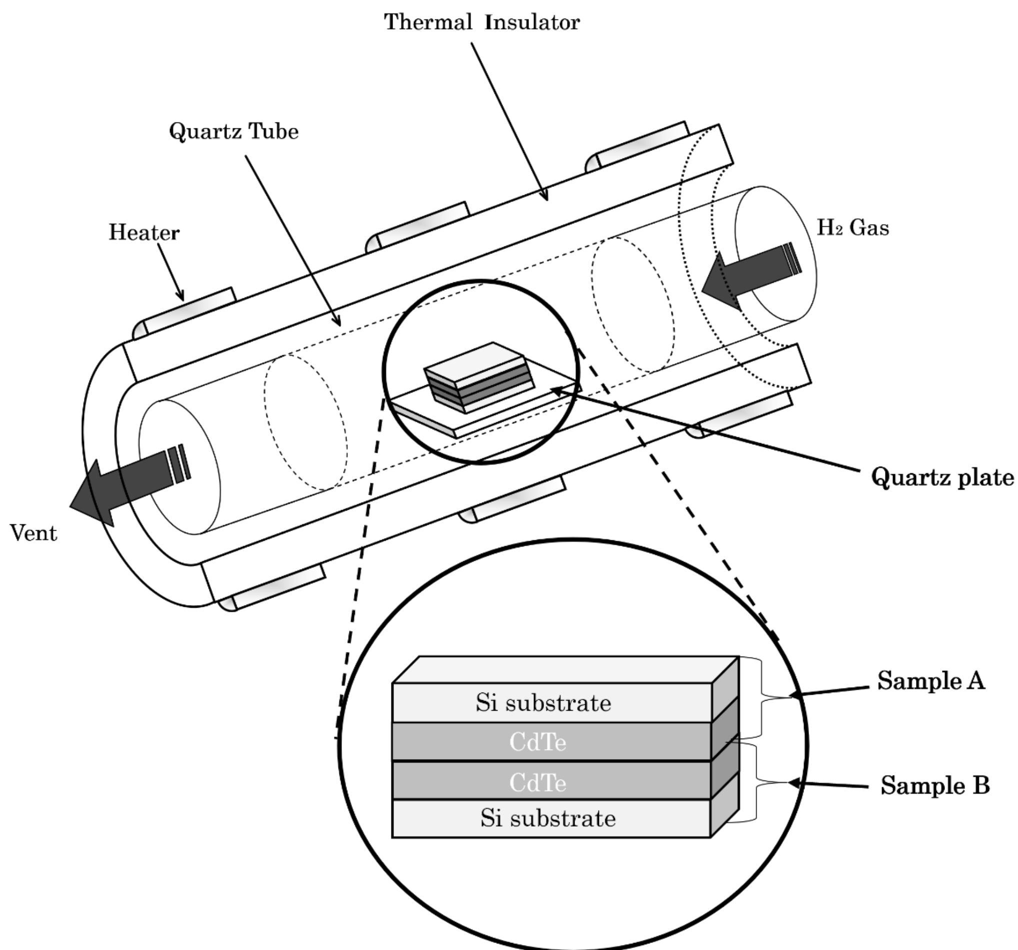

Fig. 2.3 Schematic diagram of the set up used for the face-to-face annealing.

2.6 Evaluation of dislocation in CdTe

Dislocation densities in CdTe epilayers were evaluated by wet chemical etching process that reveals the locations of dislocations on the surface as pits. The standard etch pit density (EPD) etches that are used for CdTe are Schaake etch [9], Everson etch [10] and Benson etch [11,12]. In this work, we used Everson etching method, as it forms clear pits on the CdTe (211) B face. The composition of Everson etch consists of lactic acid : nitric acid : hydrofluoric acid = 25 : 4 : 1 in volumetric ratios [10]. All the samples were etched for the same etching time of 2 minutes. The samples were rinsed with deionized water after each etch and then blown with pure dry N_2 gas. Pits formed on the sample surface were counted using an optical microscope and dislocation density was estimated.

2.7 Detector fabrication

The detectors were fabricated in a p-CdTe/n-CdTe/n^+-Si heterojunction diode structure by growing n-CdTe and undoped p-CdTe successively on the n^+-Si substrates. Gold electrode was evaporated on the p-CdTe side and on the back side of n+-Si substrate as an ohmic contact. Before the gold deposition, the back side of n+-Si substrate was mechanically roughened with sandpaper. This process was necessary to achieve the ohmic contact. After the contact deposition, the samples were annealed briefly in nitrogen environment at 140 °C to improve the contact property. The ohmic behavior of gold contact on both undoped p-type CdTe layers and the n+-Si substrates was confirmed by current-voltage measurements separately [13]. Annealed samples were then cut into 1mm x 1mm sizes. No other surface passivation techniques were applied. The detectors were mounted on a TO-5 metal can package and wire bonded as schematically shown in **Fig. 2.4.**

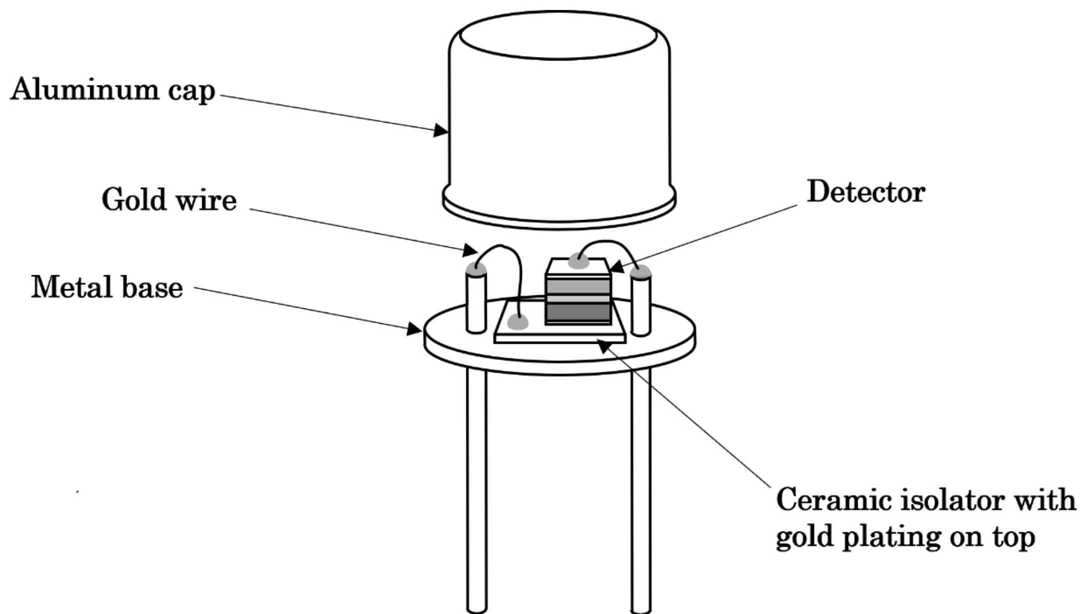

Fig. 2.4 Schematic diagram of the detector mounted on a TO-5 metal can package.

2.8 Characterization techniques

2.8.1 Optical microscopy

In this study, the surface morphology of Everson-etched CdTe samples were examined using Optical microscope (KEYENCE VH-2500). This microscope can be used in both reflectance and transmittance mode. We evaluated the sample surface in the reflectance mode with magnification varying from 500 x to 5000 x. The surface morphology of the as-grown samples were also examined using Nomarski interference contrast microscopy.

2.8.2 X-ray diffraction (XRD)

XRD is a nondestructive technique for characterizing crystalline and polycrystalline materials. It gives information about structure, crystal orientation, crystallinity, grain size, strain etc. The crystallinity of the CdTe grown layer was evaluated by double-crystal rocking curve (DCRC) full width half maximum (FWHM) value from the CdTe (422) reflection plane using Cu K_α as X-ray source.

2.8.3 Photoluminescence (PL)

The photoluminescence was performed at 4.2 K by immersing the samples in liquid He, where semiconductor laser of wavelength 488 nm. (Stradus488-150 (VORTRAN) was used as the excitation source. The emitted spectra were collected with a liquid-nitrogen cooled Si-CCD detector (Symphony CCD Detection System (HORIBA JOBIN YVON) connected to a computer.

2.8.4 Hall Measurement

The carrier density, mobility and resistivity were measured with ECOPIA HMS-3000 Hall effect measurement system, which is based on the van der Pauw method. Measurements were performed on the 5 mm x 5 mm sized samples cut from the whole 25 mm x 25 mm sample. Before the measurement, indium electrode was deposited on four corners of the sample for the ohmic contact.

2.8.5 Current-voltage (I-V) characterization

Current-voltage (I-V) measurement was performed at room temperature using a pico-ammeter 6517A (KEITHLEY), varying the applied voltage in the range from -100

to +100 V. Furthermore, the temperature dependent I-V measurement was performed using a power device analyzer B1505A equipped with a temperature controlling device. With this device, it is possible to measure the I-V characteristics controlling the sample temperatures from -30 to + 60 ºC.

2.8.6 Gamma radiation detection test

Figure 2.5 shows the schematic configuration of gamma detection test setup. It consists of a preamplifier, shaping amplifier and a multichannel analyzer, which was then connected to the computer. The fabricated detector was mounted on a sample holder and connected to a pre-amplifier. A positive bias was applied on the detector to operate it in a reverse bias mode and an ^{241}Am radioisotope gamma source was placed in front of the detector. The signal generated by the gamma radiation in the detector was collected and analyzed.

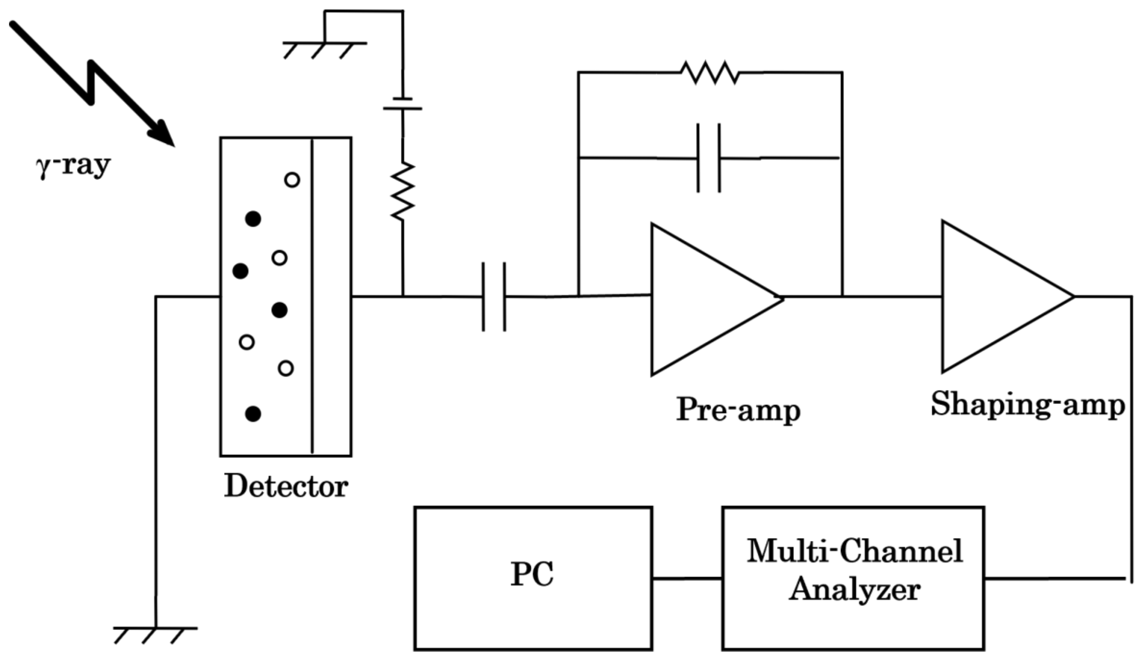

Fig. 2.5 Schematic diagram of radiation detection measurement apparatus.

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Chapter 3

Growth and n-type doping of CdTe layers on (211) Si substrates

3.1 Introduction

The growth of thick single-crystal CdTe epitaxial layers on large-area Si substrates is a promising way for the development of large-area X-ray, gamma ray imaging detectors [1-3]. In the previous works at our laboratory, detectors were fabricated in a p-CdTe/n-CdTe/n^+-Si heterojunction diode structure, where the p-CdTe and n-CdTe layers were typically 100 μm and 5 μm, respectively [4]. Those detectors could detect gamma radiations and measure their energies when operated in a pulse mode by applying reverse bias voltage. However, their gamma detection capabilities were not adequate. It was found that large dark currents coupled with the suboptimal charge transport properties of photon-generated charge carriers constituted major factor constraining the detector's property. The crystal defects such as dislocations were found responsible for the increased detector dark currents. The details will be presented in next chapter. The carriers' charge transport properties, on the other hand, were affected because of the incomplete depletion of the thick p-CdTe layer, resulting recombination of carriers during their transport. To overcome this problem, it is necessary to increase the carrier concentration and thicknesses of the n-CdTe layers, so that the depletion layer will fully extend towards the p-CdTe, away from the highly dislocated n-CdTe/n^+-Si interface. However, previous studies of the n-CdTe growth were limited, and the maximum electron density and the

growth rate were around 10^{17} cm^{-3} and 0.5 μm/h, respectively [5,6]. It was not feasible to grow thick n-CdTe layers, and there was a need to increase of the electron density further. In this study, we performed growth of iodine-doped n-CdTe layers at higher substrate temperatures, as well as at various Te/Cd precursor ratio in the vapor phase (VI/II ratio) to achieve both higher growth rates and the high electron density. Growth details, electrical properties of these iodine-doped CdTe layers as well as possible doping mechanism are presented in this chapter.

3.2. Experimental procedure

CdTe layers were grown on 25 x 25 mm^2 sized (211) n^+-Si substrates using MOVPE technique. Dimethylcadmium (DMCd) and diethyltelluride (DETe) were used as group II and VI precursors. Ethyl-iodine (EI) was used as dopant for the growth of n-CdTe. The growth temperatures were varied from 325 ºC to 450 ºC and VI/II flow rate ratio from 0.05 to 0.3. The DETe flow rate was fixed while the DMCd flow rate was adjusted to vary the VI/II ratios. First, a 10 μm thick high resistivity undoped CdTe buffer layer was grown on the Si substrates. Afterwards, doped layers were grown on these buffered substrates.

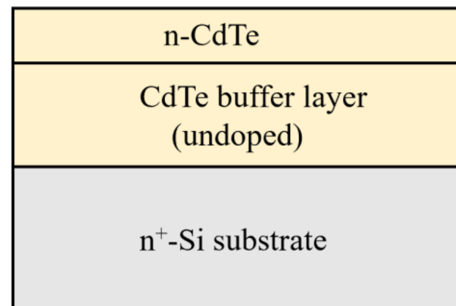

Fig. 3.1 Schematic structure of sample used in this study.

Figure 3.1 shows the schematic structure of the sample used in this study. All n-CdTe growth was performed for the same length of time. The grown layers were evaluated by room-temperature Hall measurement (van der Pauw method), 4.2 K photoluminescence measurement, as well as double crystal x-ray rocking curve (DCRC) measurement. The surface morphology was examined using a Nomarski microscope. The high resistivity CdTe buffer layer, whose resistivity is several orders of magnitude higher than that of n^+-Si substrate, was inserted in order to minimize the effect of substrate (i. e. to electrically isolate the doped layer from the substrate) during the Hall measurement. Indium electrodes were evaporated on the four corners of the sample to make Ohmic contacts.

3.3. Results and discussion

Figure 3.2 shows dependence of growth rate of iodine-doped n-CdTe epilayers as a function of substrate temperature. The growth was performed at VI/II ratio of 0.25. The result shows that the growth rate increases with the substrate temperature increase. This result shows expected pattern where growth is dominated by thermal decomposition of DETe [7]. The decomposition rate of DETe increases with the substrate temperatures increase, leading to a higher growth rate. A maximum growth rate of 2.6 μm/h is obtained at 425 °C, which is more than 5 times higher than the growth rates of our pervious n-CdTe layer on Si substrates [5,6]. This high growth rate makes growth of thick n-CdTe possible. However, the growth rate slightly decreases after reaching the maximum value.

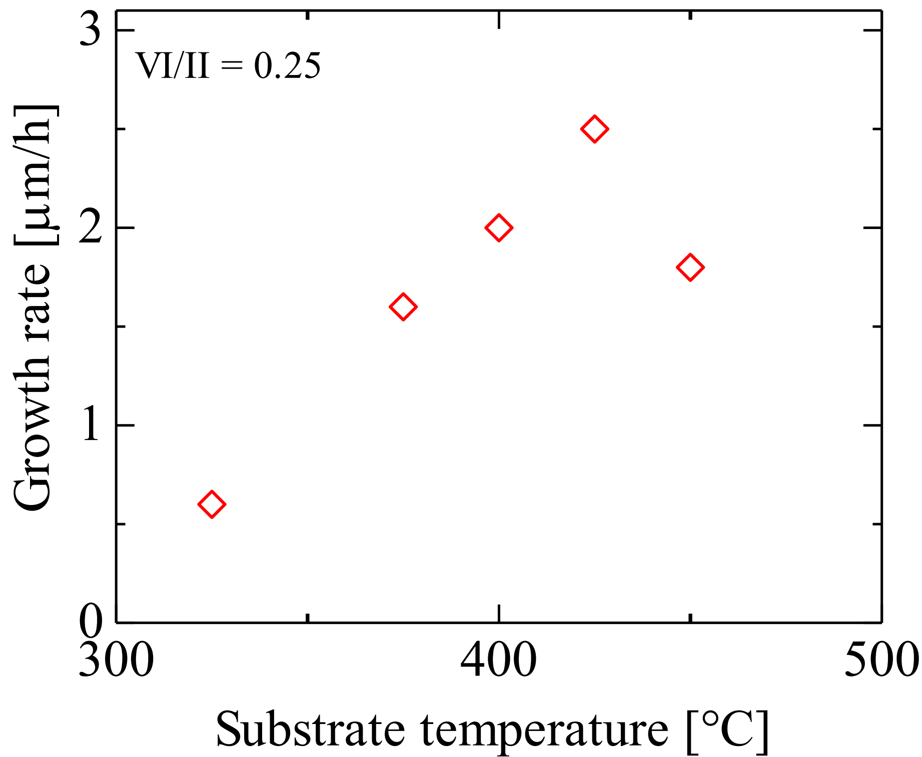

Fig. 3.2 Growth rate of iodine-doped n-CdTe epilayers as a function of substrate temperature.

Figure 3.3 shows the room-temperature electron density and mobility values of the n-CdTe layers grown at different substrate temperatures. No clear variation in carrier concentration or mobility was observed with substrate temperature within this substrate temperature range studied. The exact reason is not known. It may be due to limited incorporation of dopant onto the growth surface due to a high surface coverage rate of Te. However, it needs further verification. The doping properties in CdTe has been reported due to the compensation effect [5,8,9]. The cadmium vacancy in the crystal forms the cadmium vacancy-donor complex, which acts as an acceptor like defect, and neutralize the donor in the following way [9]. It has been reported that a low-temperature growth is

effective to resolve this dopant compensation problem [5,10,11]. However, the results in **Fig. 3.3** suggests that growth parameters other than substrate temperature are playing more important role.

$$[V_{\mathrm{Cd}}^{--} \qquad I_{\mathrm{Te}}^{+}]^{-} + I_{\mathrm{Te}}^{+} \tag{3.1}$$

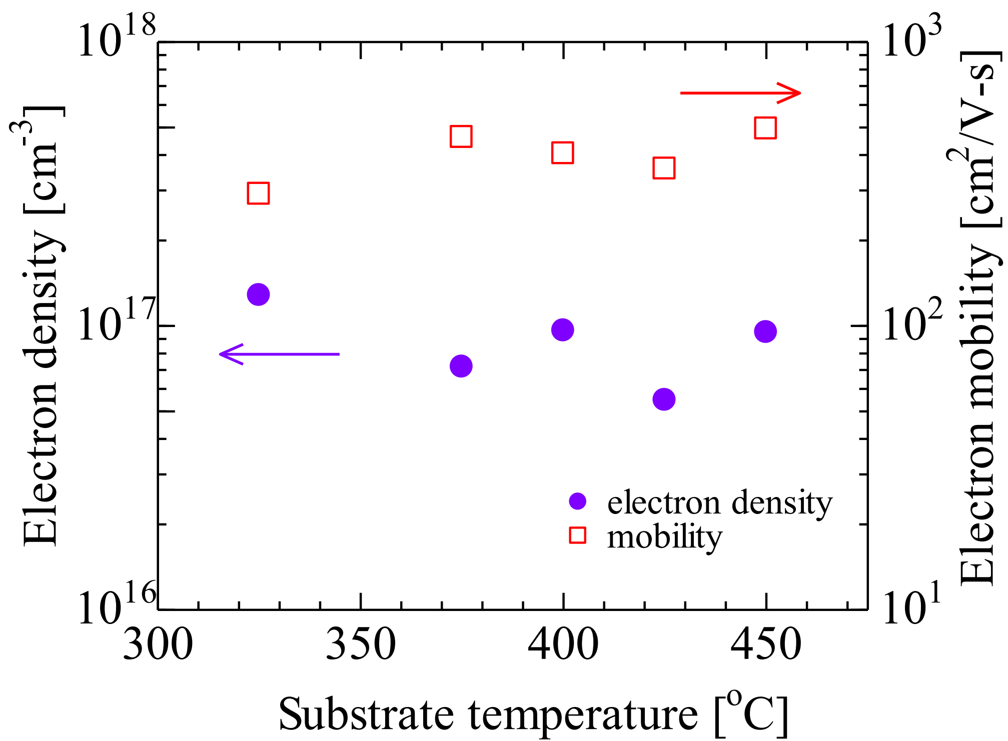

Fig. 3.3 Room temperature electron density and mobility values of n-CdTe layers grown at different substrate temperatures.

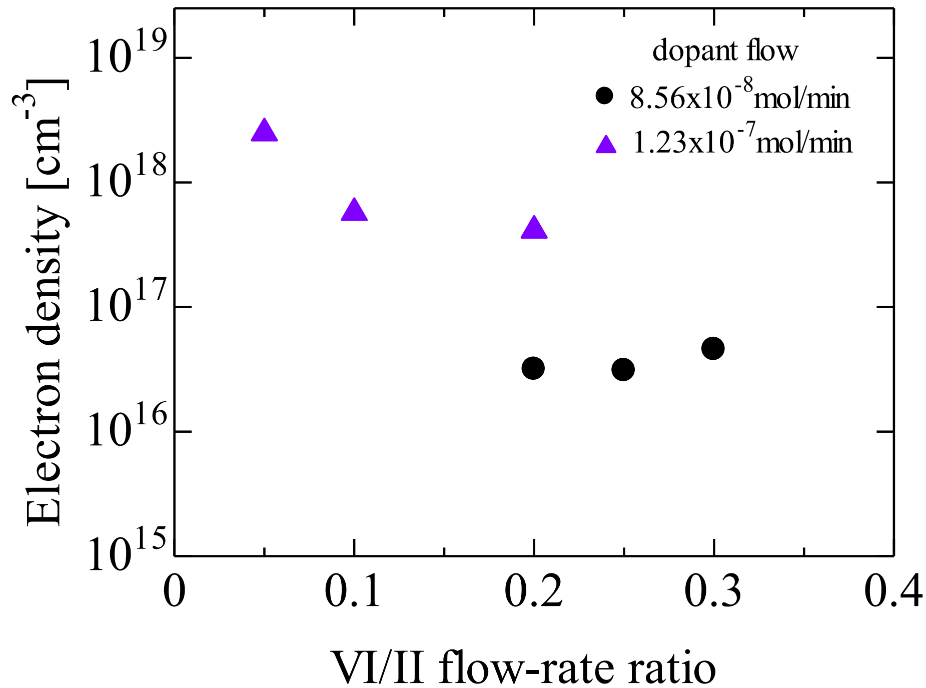

Fig. 3.4 The variation of room temperature electron density with VI/II flow-rate ratio for epilayers grown with different dopant flow rates.

Figure 3.4 shows room-temperature electron density as a function of VI/II flow-rate ratio at two different dopant flow rates. The substrate temperature during the growth was 400 ºC, and the DMCd flow-rate was adjusted to vary the VI/II ratios. The n-CdTe layer thickness remained almost constant (typically 5μm), when the substrate temperature was kept constant, and the VI/II ratio varied at fixed DETe flow, as DETe is the growth rate controlling species. The results in **Fig. 3.4** show that the electron density gradually increases with decreasing VI/II ratio, and the highest electron density of 2.5×10^{18} cm^{-3} was obtained with a VI/II ratio of 0.05 [8,10-13]. This could be explained due to decrease

of donor compensation with decreasing VI/II ratio, as this growth condition suppresses the formation of Cd vacancies. On the other hand, increasing the VI/II ratio makes the growth less Cd-rich, hence the compensation increases. Also shown in **Fig. 3.4,** for a fixed VI/II ratio and with these small dopant flow rates, the electron density increases with the increase of dopant flow rates as dopant incorporation in the crystal increases. However, further increase of dopant flow rates (above $1.3x10^{-7}$ mol/min), the electron density starts to decrease (not shown here) due to onset of donor compensation [5]. These results suggest there exists an optimum supply of dopants governed by growth conditions that produce epilayers with high electron densities.

X-ray diffraction measurements were performed on these CdTe layers grown at different VI/II ratios. The θ-2θ scan showed a single diffraction peak corresponding to CdTe (422) reflection. The rocking curve measurement revealed the FWHM values were 540, 405, and 447 arcsec for layers grown with VI/II ratio of 0.1, 0.25 and 0.3, respectively. These results suggest structural quality of crystal slightly degrades when VI/II ratio is lowered to 0.1. Surface morphology of the layers grown at two different VI/II ratios is shown in **Fig. 3.5**. Both images show dense characteristic hillock structures, which may be the result of Cd-rich growth. The morphology is somewhat smoother for layer grown at VI/II ratio of 0.3 when compared to that of 0.1.

(a) 0.1 and (b) 0.3.

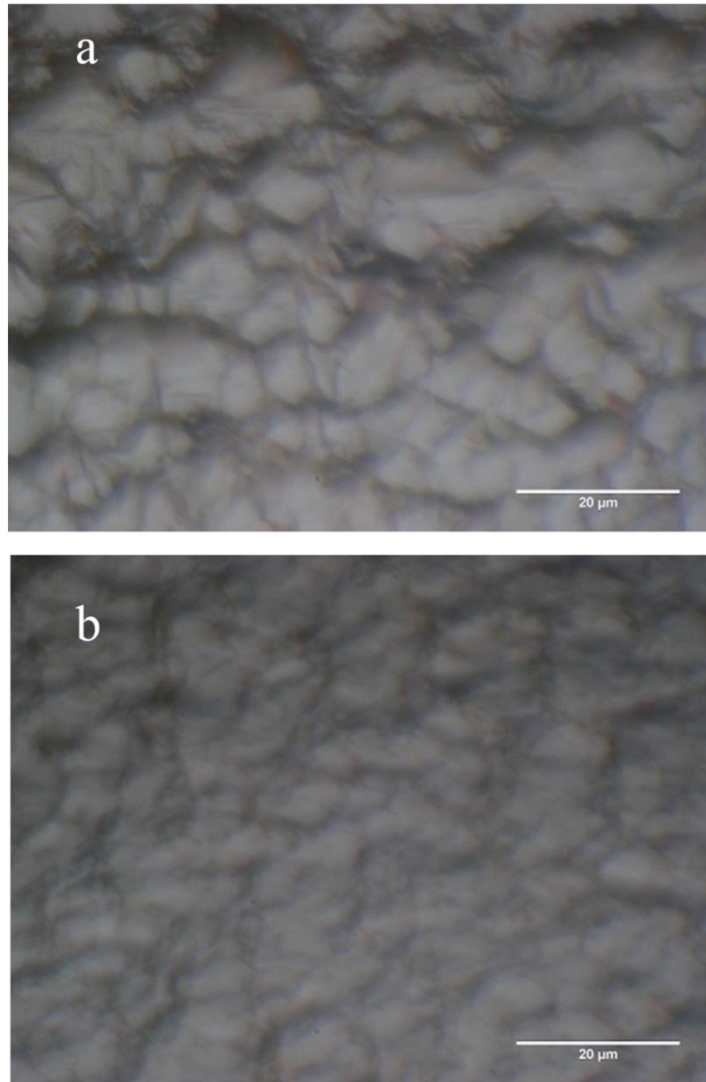

Fig. 3.5 Surface morphology of n-CdTe layers grown at 400 °C at different VI/II ratio of (a) 0.1 and (b) 0.3.

Photoluminescence spectra of iodine-doped n-CdTe layers grown at a substrate temperature of 400 °C, with different VI/II ratios are shown in **Fig. 3.6**. The PL spectrum of the layer grown with a VI/II ratio of 0.1 (**Fig. 3.6a**), shows distinct edge-emission peak and broad donor-acceptor pair (DAP) emission peak, accompanied with LO-phonon replicas. Also, there is a distinct peak near 1.5 eV. The edge-emission peak is attributed to an exciton bound to neutral I donor, whereas the emission peak near 1.5 eV could be due to the iodine donor recombining with residual acceptor impurities [14]. The broad band DAP emission is related to A-center (V_{Cd}-I_{Te}) acceptor and isolated I donors (I_{Te}) [5,14,15], though dislocation related peaks also appear at this region. This is the characteristics PL spectrum of an iodine-doped CdTe, where electrical compensation of dopant is low [16]. However, the bound-exciton emission peak decreases drastically, the 1.5 eV peak mostly disappears, while the DAP emission becomes broad and the phonon replicas become less prominent for the layers grown with higher VI/II ratios as in **Fig. 3.6 (b), (c)**, which is an indicative of the onset and increase of electrical compensation [16]. As discussed above, growth at a low VI/II ratio (i.e. Cd-rich condition) helps to suppress the formation of $V_{cd,}$ leading to small donor compensation as formation probability of iodine A-center decreases. Hence, free electron carrier densities increases as in **Fig. 3.4,** and distinct bound-exciton emission appears in the PL spectrum (**Fig. 3.6a**). However, V_{Cd} increases when the growth is performed at higher VI/II ratios, resulting increased donor compensation, and hence free electron carrier density decreases.

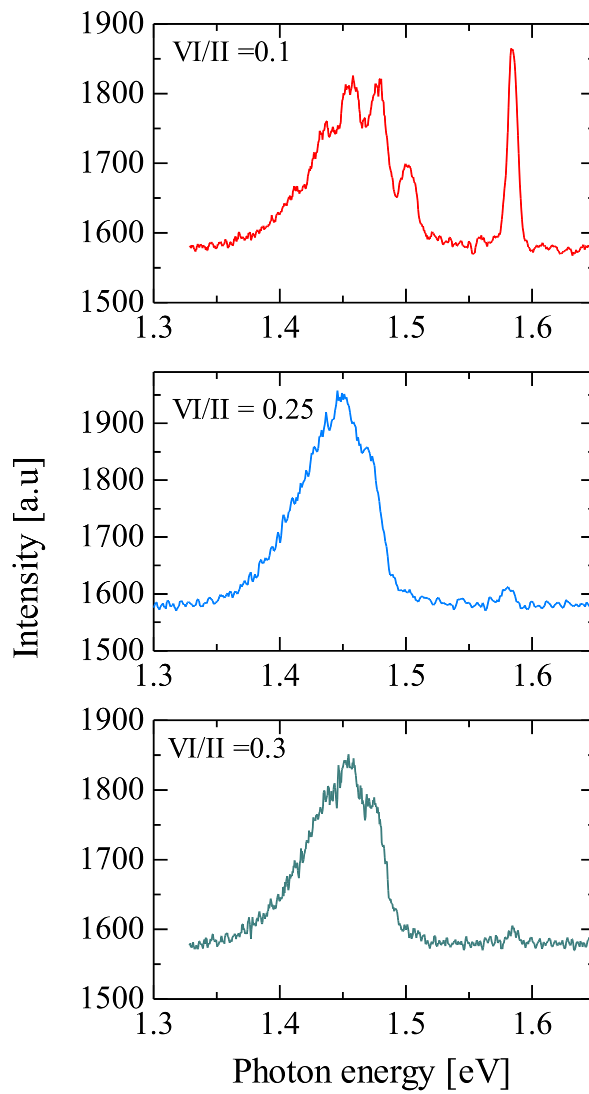

Fig. 3.6 The 4.2 K PL spectra of iodine-doped n-CdTe layers grown at a substrate temperature of 400 ºC, with different VI/II flow-rate ratios.

3.4. Conclusions

Iodine doping of CdTe layers grown on (211) Si substrates by metalorganic vapor phase epitaxy at high substrate temperatures has been studied. The growth rate increased with the substrate temperature increase, reaching a maximum growth rate of 2.6 μm/h at a substrate temperature of 425 ºC. The room temperature free electron density, on the other hand, showed strong dependence with VI/II flow ratio during the growth. The electron density increased while decreasing the VI/II ratio. A maximum electron density of 2.5×10^{18} cm^{-3} was obtained by growing the epilayers at a substrate temperature of 400 ºC, and the VI/II ratio was 0.05. We discussed the improvement of electron density is due to the result of suppression of cadmium vacancy formation, which in turn decreases the donor compensation effect. It was found that VI/II flow-rate ratio has more pronounced effect in controlling the cadmium vacancy formation than the substrate temperature in the temperature range investigated in this work. The results obtained here can be implemented in the device fabrication, which will lead to improved carrier charge transport properties by extending the depletion layer fully towards the thick p-CdTe side. Hence, improvement in the detector's gamma detection properties can be expected.

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Chapter 4

Study of dislocation distributions in CdTe/Si and their effects in device properties

4.1 Introduction

In chapter 3, we studied the growth of thick and heavily doped n-CdTe layer, where maximum growth rate of 2.6 μm/h and highest electron density of 2.5 x 10^{18} cm^{-3} were obtained at the substrate temperature 400 °C and Te/Cd flow-rate ratio of 0.05. This opened possibilities to fabricate detectors, where the depletion layer will fully extend towards the thick p-CdTe layer. This, in turn, will help to improve the transport properties of photon-generated charge carriers, and hence the detector performances. However, the dark current of this p-CdTe/n-CdTe/n^+-Si diode type detector was another major issue, which severely degrade the gamma detection properties [1-3]. One of the major sources of dark current was the dislocations present in CdTe crystal. As described in earlier chapters, the n-CdTe/n^+-Si interface contains a large number of misfit dislocations generated due to the large lattice constants and thermal expansion coefficients mismatches between these two materials. These misfit dislocations further propagate as threading dislocations deep into the epilayer, and act as a major source for the generation of device dark currents [1-3]. In this chapter, we investigate how far these dislocations propagate and distribute into the CdTe epilayer and how they affect the device properties. For this, we first fabricated a thick p-CdTe/n-CdTe/n^+-Si detector and then successively etched it from the p-CdTe side to make devices of different thicknesses. We then

examined the threading dislocation (TD) density as well as measured the dark currents in those devices of different thicknesses. It was found that the TD density was higher in thin devices which decreased as the device thickness was increased. A strong co-relation was observed between the TD density and the detector dark current which increased with increasing the TD density. The dark current generation mechanism also changes depending on the TD density present in the device.

4.2 Experimental procedure

4.2.1 Dislocation density analysis

Figure 4.1 shows the schematic structure of p-CdTe/n-CdTe/n^+-Si device used in this investigation. The device was fabricated by growing an iodine-doped n-CdTe and an undoped p-CdTe layer subsequently on 25 mm x 25 mm sized (211) n^+-Si substrates by using metalorganic vapor phase epitaxy (MOVPE) growth. The n-CdTe and the p-CdTe layers were grown at 350 ^{o}C and 450 ^{o}C respectively, and were typically 5 μm and 35 μm in thickness. All samples studied here were grown at the same growth-run.

After the growth, the samples were then diced into several small pieces of dimension 6 mm x 6mm, which were then repeatedly etched and polished from the p-CdTe side with a 2% Br-Methanol solution to make samples of different total CdTe thicknesses varying from 6 to 35 μm. In all samples studied, the n-CdTe thickness remained intact at 5 μm, whereas, the p-CdTe thickness was varied. One set of samples was then etched with dislocation decorated Everson etching solution with volumetric ratios of lactic acid: nitric acid: hydrofluoric acid of 25:4:1. The Everson etch reveals the point of emergence of a dislocation as a pit on the CdTe surface [4]. The etching time was fixed at 2 minutes which was optimized in this study to reveal clear pits formation, followed by rinsing in deionized

(DI) water. Pits formed on CdTe surface were counted using an Optical microscope. Moreover, the crystal quality was also examined by using X-ray diffraction (XRD) rocking curve for each sample before subjecting to EPD etching.

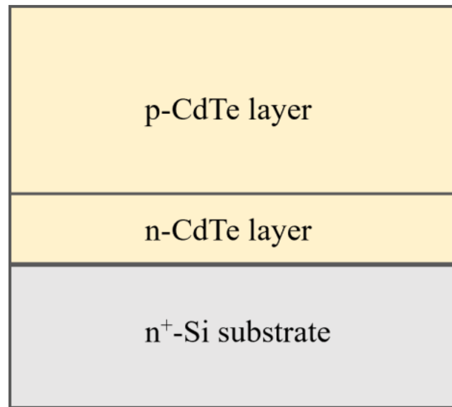

Fig. 4.1 Schematic diagram of sample structure used in this study.

4.2.2 Device fabrication and analysis

Detectors were fabricated using another set of samples with different total CdTe thicknesses. Gold electrodes were evaporated on the p-CdTe side and then on the back side of n^+-Si substrate after proper surface treatments to make ohmic contacts [5,6]. Finally, these devices were cut into 1 mm x 1 mm chip and current-voltage (*I*-*V*) measurements were performed at room temperature and also by varying the temperature from -40 ºC to 40 ºC to evaluate temperature dependence of dark current and its generation mechanism. The detector dark current was measured by applying a positive bias on back side contact on n+-Si substrate (reverse bias mode). Gamma detection tests were also studied using two selected samples of different thicknesses.

4.3 Results and discussion

Figure 4.2 shows the surface images of four samples of different CdTe thickness of 35, 20, 12 and 6 μm after Everson etching. Triangular shape pit that are observed in Everson etched (211) CdTe B-face are clearly visible [4]. However, the density of the pits is different depending on the sample thickness. The 35 μm thick sample as in **Fig. 4.2 (a)**, shows lowest number of pits. The pit density increases when the sample thickness was decreased. This observation supports that misfit dislocations generated at the heterointerface, propagate deep into the CdTe epilayer as TDs and while propagating these TDs sometimes annihilate or coalesce and their density reduces as the epilayer thickness increases [7-10]. From the EPD counts, we calculated dislocation density in the samples, as the pit corresponds to the point of emergence of dislocations. The results are plotted in **Fig. 4.3** as a function of epilayer thickness. The data in **Fig. 4.3** shows that dislocation density first decreases rapidly with sample thickness, nonetheless, the decrement somewhat slows down when the device of thickness increases above 20 μm. A previous study on dislocation depth analysis in CdTe epilayers has reported similar trend, however, for thinner epilayers that were grown on GaAs substrates [7,11,12].

Figure 4.4 shows the plot of DCRC FWHM value of samples as a function of the sample thickness. The result shows the FWHM value was 300 arcsec for the thickest sample of thickness 35 μm, which increased to around 600 arcsec when the sample thickness was reduced to 6 μm. This could be considered due to x-ray rocking curve broadening in the epilayers consisting of higher dislocation density.

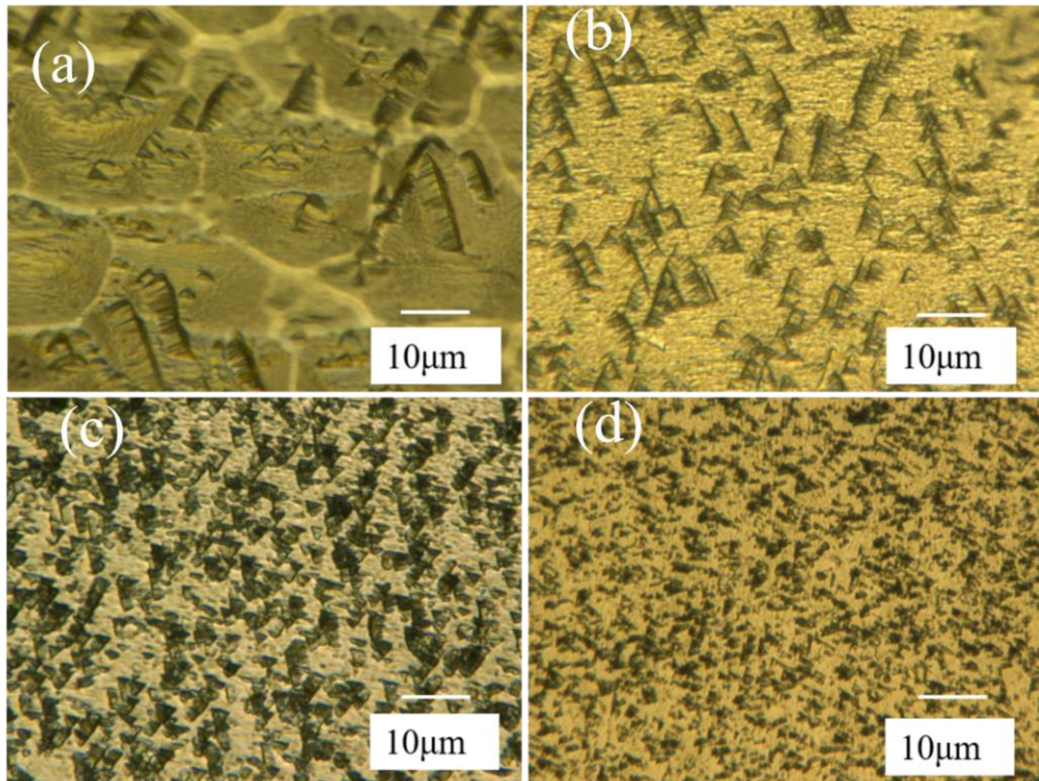

Fig. 4.2 Optical images of sample surface after Everson etching. The sample thickness was (a) 35 μm, (b) 20 μm, (c) 12 μm and (d) 6 μm.

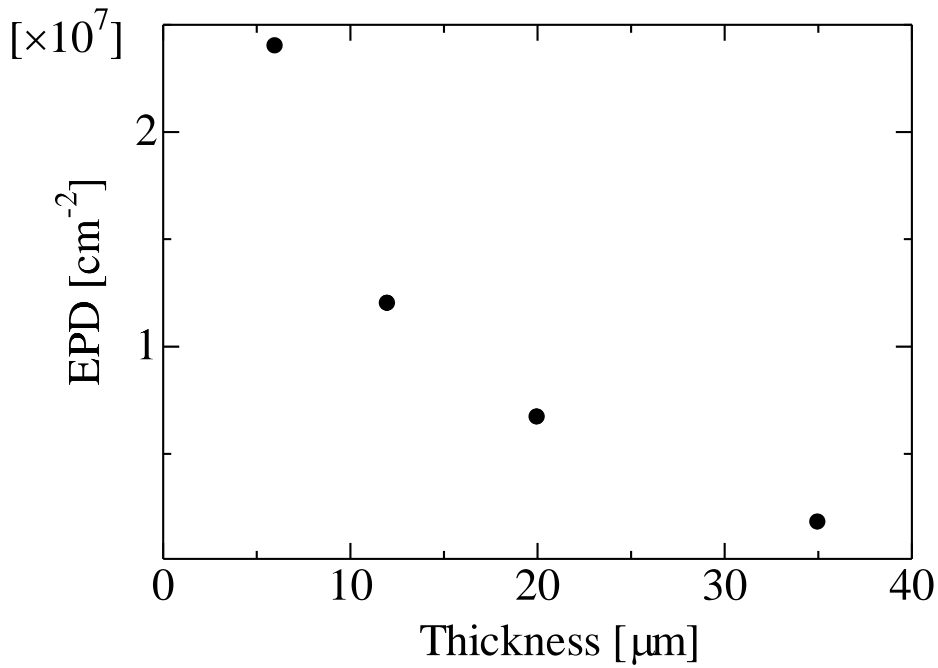

Fig. 4.3 Variation of EPD with CdTe epilayer thickness.

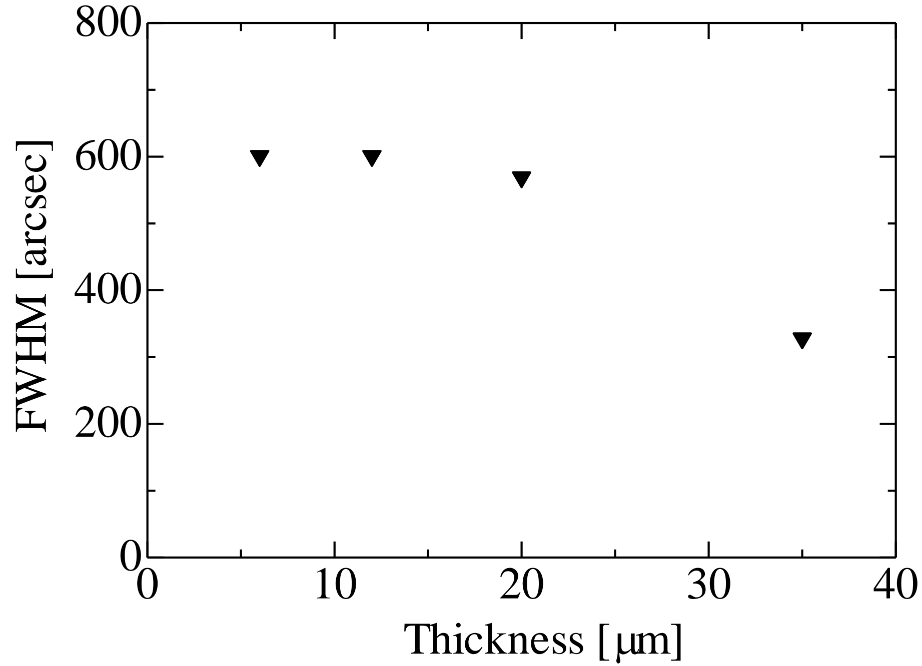

Fig. 4.4 DCRC FWHM value of the samples as a function of sample thickness.

Furthermore, the dislocation density of these samples was calculated from the DCRC FWHM values using the following equation [13-15], and plotted in **Fig. 4.5**. For comparison, the TD densities evaluated from the EPD counts are also replotted in the same Figure. The results show the TD densities calculated from the FWHM values were higher compared to the TD densities evaluated from the EPD counts. This may be due to penetration of x-ray into the epilayer whereas only dislocations reaching the sample surface that form pit are counted in EPD, or due to rocking curve broadening by other factors. However, it needs further verifications.

$$\text{TD density} = \frac{\beta^2}{4.36 \times |b|^2} \qquad (4.1)$$

a_0: Lattice constant = 6.48 Å , b: Burger vector = 4.5821 x10^{-8} cm

β : FWHM [rad]

Next, we investigated the dependence of device dark current on TD density, using devices of different thickness. As explained earlier in **Fig. 4.3** thin device contains large TD density, which decreases when the device thickness increased. **Figure 4.6** shows the reverse bias current-voltage (*I-V*) characteristics of the devices measured at room temperature. We tested several devices of different total CdTe thickness, and the results were similar. All devices exhibit bias–dependent dark current. The thinnest device of total thickness of 6 μm shows largest dark current, and it shows early breakdown. The thickest device, on the other hand, exhibited lowest dark current. Moreover, as in **Fig. 4.6**, for all device the dark current varies with square root of applied reverse bias in lower bias range, but dependence soon goes toward linear and power dependence.

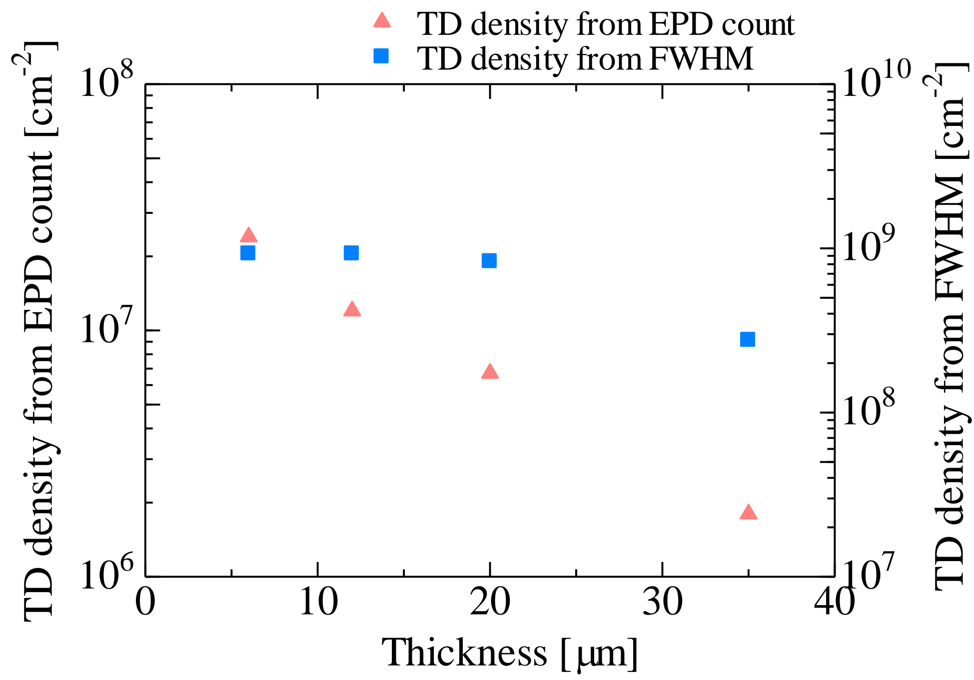

Fig. 4.5 TD density of sample of different thicknesses evaluated from EPD counts and FWHM value.

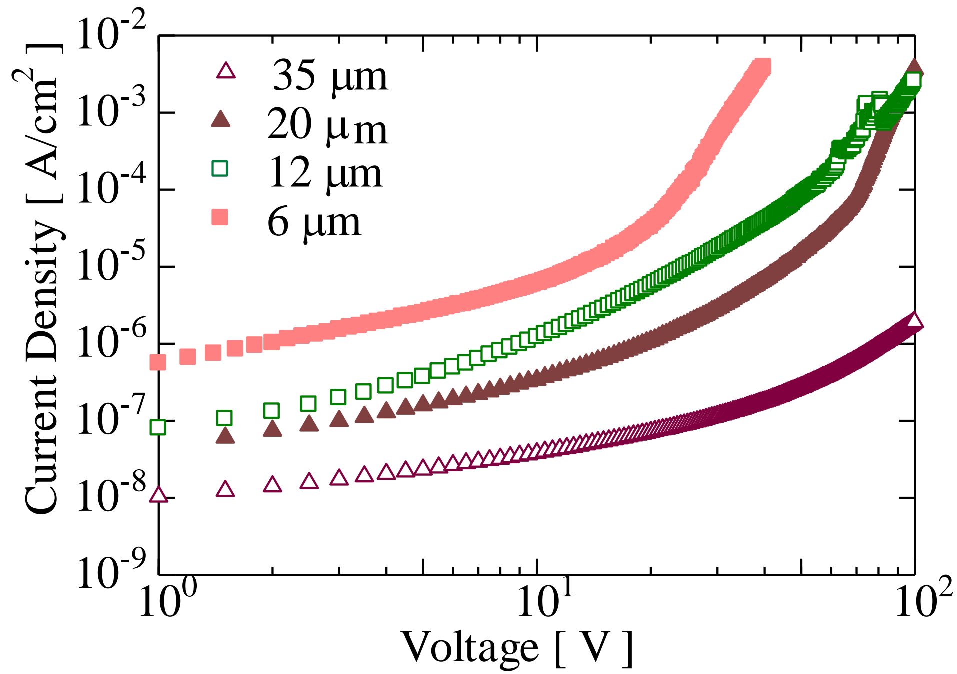

Fig. 4.6 I-V characteristics of detectors with different thickness measured at room temperature.

We replotted the dark current as a function of TD density at two different reverse bias voltages as shown in **Fig. 4.7**. As expected, the dark current increases with increasing TD density at each voltage, however, a linear relationship was not observed. The dark current shows a large variation when the TD density increases above 10^7 cm^{-2}. In order to study mechanism behind the observed dark current, temperature dependent current-voltage (*I-V*) measurement was performed in the temperature range from – 40 ºC to 40 ºC. **Figure 4.8** shows an Arrhenius plot of the dark current for devices of different thicknesses for an applied reverse bias voltage of 40 V. The 6 µm thick device shows weak temperature dependence when compared to thicker devices (20 ~35 µm) in all temperature range. On

the other hand, thicker devices exhibit temperature dependence of dark currents, however the dependence became less temperature sensitive when the temperature decreased below 260 K. The nearly temperature independent dark currents observed in 6 μm thick device, though it shows a nearly exponential bias dependence, suggests the dominant the dark current mechanism is due to tunneling [16,17]. This result can be explained in the following way. Dislocations produce trap centers which contribute to detector dark current. Thin device has a large number of TD which intersect the p-n junction and produce traps that are effective for trap-assisted-tunneling (TAT) [16,17]. Since no thermally activated process are involved, the dark current is nearly temperature independent. However, the number of TD intersecting the p-n junction decreases as device thickness is increased. Hence, besides TAT current component, the dislocation induced generation-recombination (G-R) limited current also plays a definite role. This explains the bias and moderate temperature dependence of dark currents observed in thicker devices.

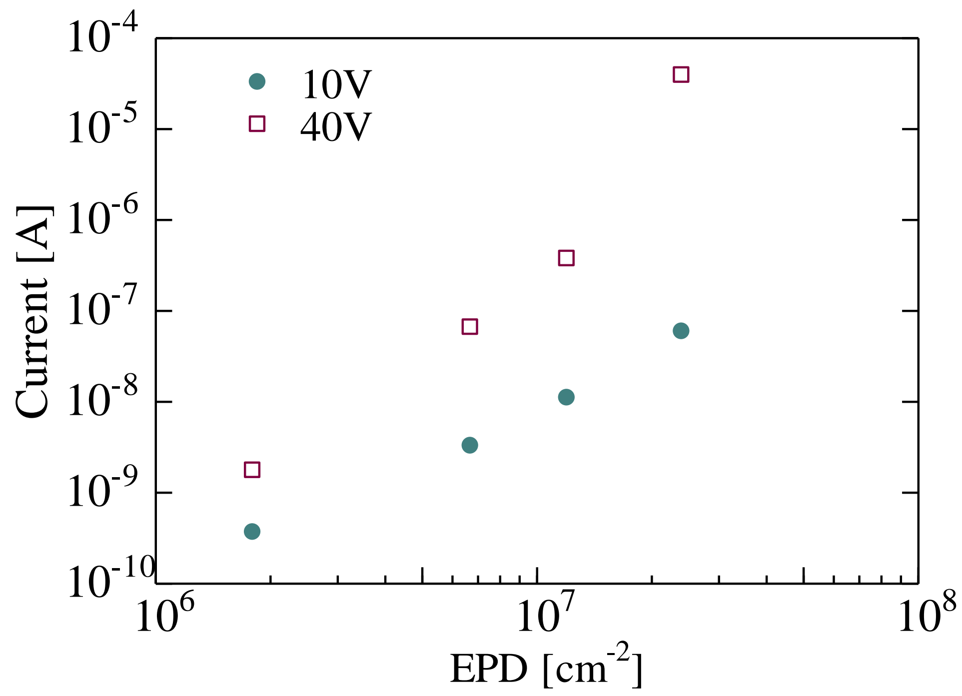

Fig. 4.7 Device dark current as a function of TD density at two different reverse bias voltages.

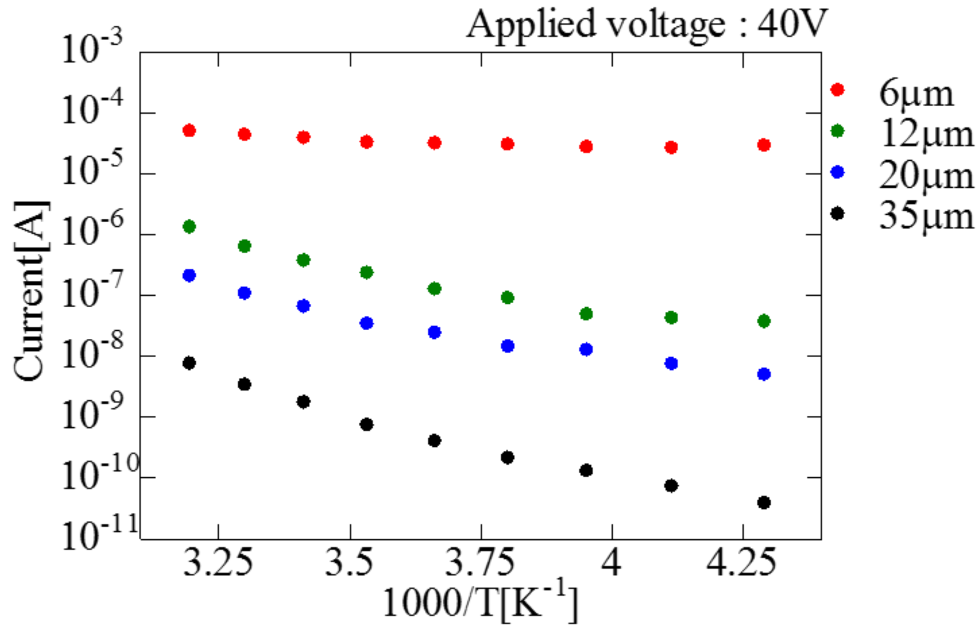

Fig. 4.8 Arrhenius plot of dark current as a function of inverse temperature for different thickness.

Now we discuss on the gamma detection properties of our devices. **Figure 4.9** shows the gamma spectrum of the ^{241}Am radioisotope obtained at room temperature by the detectors of thicknesses (a) 35 μm and (b) 12 μm. The thickest device of total CdTe thickness of 35 μm could resolve 59.5 keV main gamma peak from the ^{241}Am radioisotope, however, the spectrum is broad and the energy resolution is not good. The detection property is strongly controlled by the device dark currents [18-20]. On the other hand, no energy peaks could be detected from thinner devices of thickness 12 μm. We consider this is because of insufficient absorption of gamma radiation in the devices coupled with their large dark currents. This confirms that in order to improve the gamma detection property we need thicker devices with maximum dislocation densities not exceeding low 10^6 cm^{-2} range.

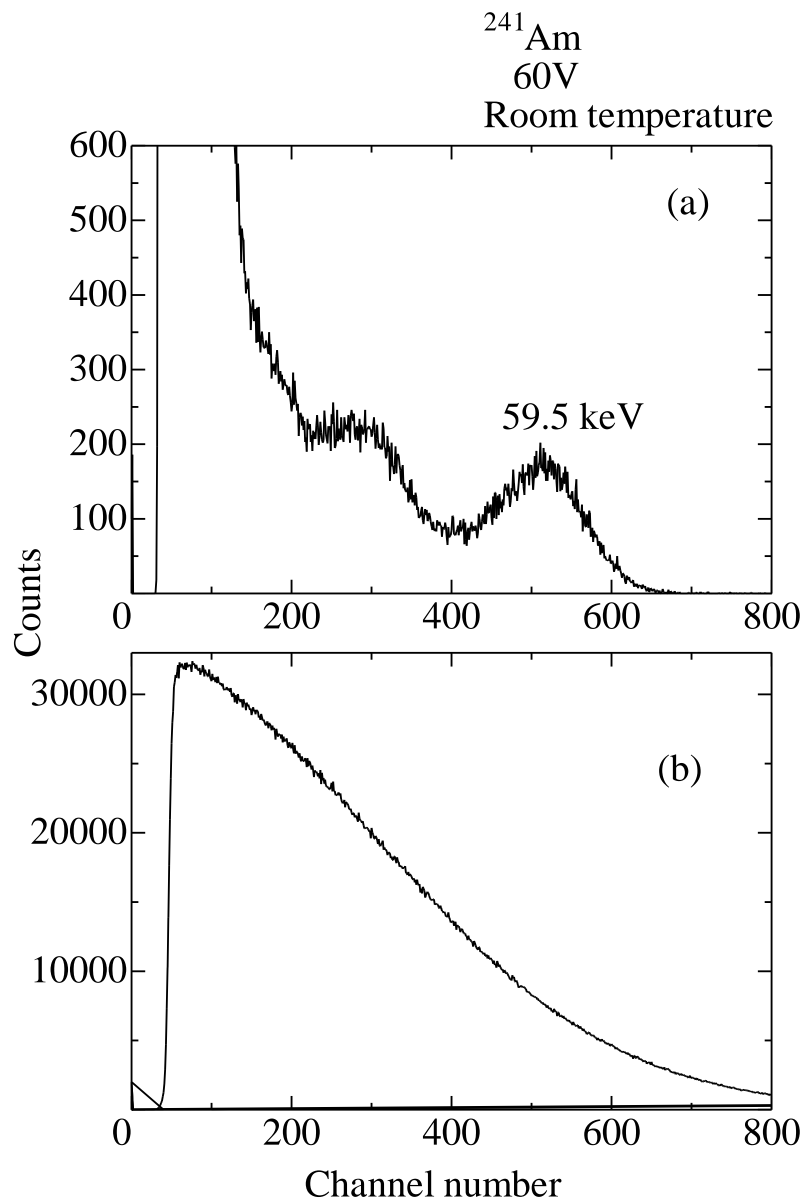

Fig. 4.9 Spectrum of the ^{241}Am gamma source obtained from the detectors with thicknesses (a) 35 μm and (b) 12 μm.

4.4 Outlook

It was confirmed that the reverse bias dark current of CdTe/Si device was strongly influenced by the dislocation density present in the CdTe epilayer. The dislocation density and hence the device dark current decreased when the CdTe epilayer thickness was increased. A large dark current was observed in the thin device when the dislocation density intersecting the p-n junction formed by the n-CdTe/p-CdTe increases. Hence, it can be suggested that by reducing the TD density as well as suppressing them from intersecting the p-n junction would be necessary to reduce the detector dark currents in epitaxially grown CdTe/Si based vertical diode-type detectors. TD density can be reduced by subjecting the eilayers to thermal cycle annealing [21]. Moreover, the number of dislocations intersecting the p-n junction can be suppressed by moving the p-n junction away from the substrate-epilayer interface where the density of the dislocation would be minimum. This could be achieved by making n-CdTe epilayer thicker than 20 μm, the critical thickness in our device structure beyond which the dislocation density decreases slowly.

4.5 Conclusions

Dislocation density and their distribution as well as their effect on device dark current were studied using a p-CdTe/n-CdTe/n^+-Si diode type device structure. Thin device showed a high dislocation density which decreased with increasing the device thickness. For devices of total CdTe thickness up to 20 μm, the dislocation density decreased rapidly, but above this the decrement slowed down. The device dark currents exhibited a strong dependence with threading dislocation (TD) density, where the dark current increased excessively with the increase of the TD density. A thin device of total

CdTe thickness of 6 μm showed very large and nearly temperature independent dark currents which could be explained due to trap-assisted-tunneling (TAT) mechanism, resulting from a large number of dislocations intersecting the p-n junction. Thicker devices, on the other hand, showed temperature as well as field dependent dark currents which could be explained due to the contributions from both generation recombination (G-R) currents and TAT currents. With this study it was revealed that for the detector applications thicker devices with dislocation densities well below than the 10^6 cm^{-2} range are needed.

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Chapter 5

Dislocation reduction in CdTe epilayer grown on (211) Si substrates

5.1 Introduction

As discussed in previous chapters, CdTe/Si junction contains large number of misfit dislocations resulting from the large differences in lattice mismatch and thermal expansion coefficients between these two materials. These misfit dislocations further propagate into the CdTe epilayer as threading dislocations. In chapter 4, we investigated how these dislocations propagate and distribute into the CdTe layer. Furthermore, we examined their effect on device properties. It was found that, dislocation density decreases slowly when the epilayer thickness is increased, but even a 35 μm thick epilayer had a high dislocation density in the 10^6 cm^{-2} range. The dark currents of the device exhibited a strong dependence on dislocation density, substantially degrading the device properties. In order to reduce dislocations in CdTe epilayers, in this chapter, we applied post-growth patterning and annealing technique, which was previously applied in ZnSe/GaAs or CdTe/Si grown by molecular beam epitaxy (MBE) [1-7]. We initially assess the suitability of this technique in our MOVPE-grown CdTe/Si with relatively thin epilayers. Subsequently, we investigated the regrowth of thick CdTe epilayers on these patterned and annealed samples to attain the increased thickness required for detector development. We found a lower threading dislocation (TD) density on the patterned samples, indicating the effectiveness of this technique in reducing dislocations. The

subsequent growth of thicker CdTe layers on these patterned and annealed samples, however, led to rough epilayers, requiring further optimization.

5.2 Experimental procedure

CdTe layers with typical thicknesses of 10 μm were grown on (211) Si substrates by MOVPE. The grown CdTe/Si samples were cut into several 6 mm x 6 mm pieces. One set of samples was patterned using photolithography to make island patterns of dimension 60 x 60 μm^2, and then etched in a mixture of HBr: Br: H_2O= 17:1:34 to remove the CdTe film in between the patterns. Another set was used as it is without making any pattern. The two types of samples studied are named as (a) whole wafer and (b) post-growth patterned and are shown schematically in **Fig. 5.1**.

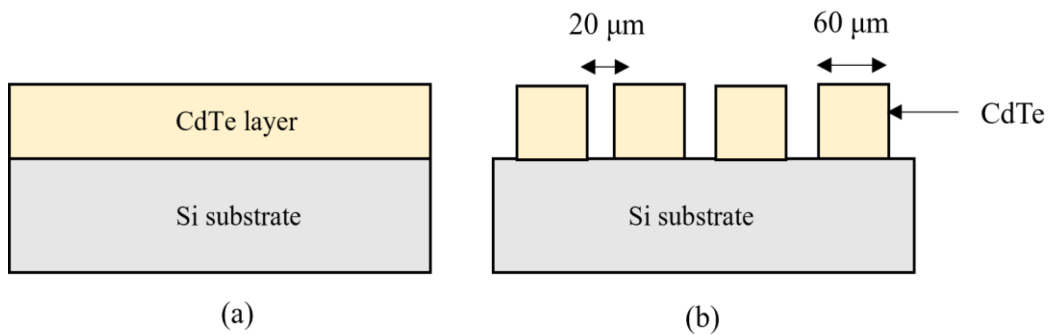

Fig. 5.1 Schematic structure of sample studied (a) whole wafer and (b) post-growth pattern.

Annealing was performed ex-situ in a horizontal quartz tube by placing two samples face to face in a flowing hydrogen environment, as explained in chapter 2. For this study, the anneal temperature was varied from 550 ºC to 800 ºC, whereas the anneal duration and the number of anneal cycles were typically fixed at 5 minutes and single cycle. However, for comparison, a limited number of samples were also subjected to three cycles anneal, keeping the anneal temperature and anneal time fixed. After annealing, both types of samples were subjected to dislocation decorating etching using Everson solution with volumetric ratios of lactic acid: nitric acid: hydrofluoric acid of 25:4:1 for a fixed etching time of 2 minutes [8]. The triangular pits formed on the surface were counted using an optical microscope. The EPD were calculated on different locations on the whole wafer sample, different islands on patterned samples and the average values were taken. Another set of samples cut from the same wafer and subjected to same anneal conditions as in the EPD evaluation was used for the X-ray diffraction (XRD) rocking curve measurements for crystallinity evaluation. The thicknesses of the samples were measured using the Dektak surface profiler and the surface morphology was investigated using an optical microscope.

5.3 Results and discussion

Figure 5.2 shows the double crystal rocking curve (DCRC) full-width half maximum (FWHM) values of the (422) CdTe rocking curves for both whole wafer and post-growth patterned samples as a function of annealing temperatures. Both types of samples show the DCRC FWHM values decrease with annealing, indicating overall improvement in crystallinity due to annealing. The FWHM values of the whole wafer samples decrease rapidly from the no-anneal value and attains a lowest value at anneal

temperature of 700 °C, however, the FWHM value increases when the anneal temperature is raised to 800 °C. This may be due to surface roughening resulting from higher anneal temperature. This will be discussed in **Fig. 5.3**. The DCRC FWHM values of the post-growth patterned samples also decreased with the anneal temperature, however, showed higher values compared to the whole wafer sample before annealing as well as throughout most of the anneal temperatures.

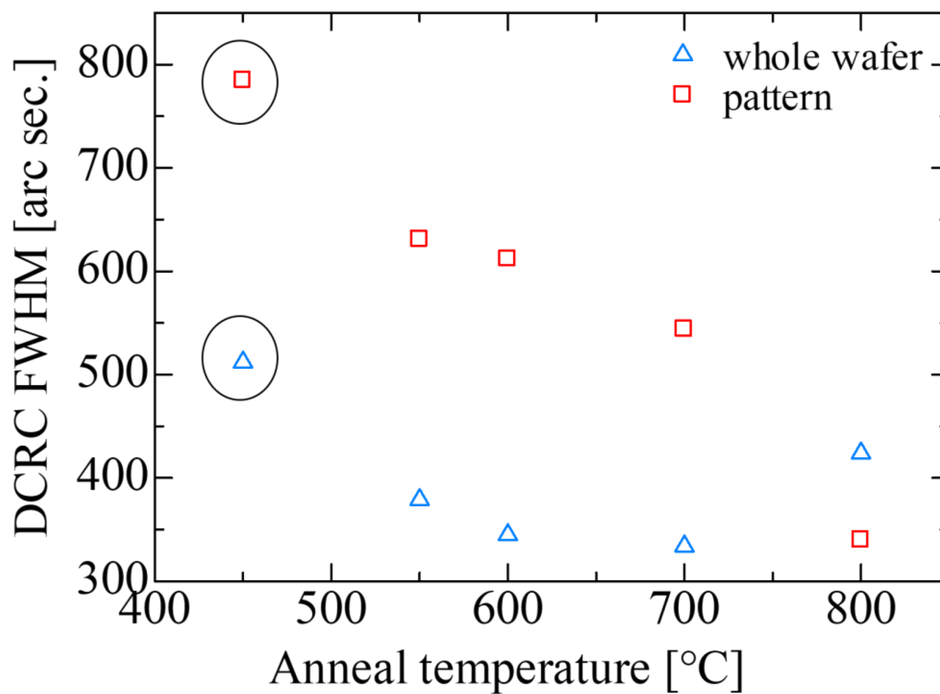

Fig. 5.2 DCRC data of CdTe layers as a function of annealing temperatures. Points enclosed with circles correspond to no anneal values.

Figure 5.3 shows the surface morphology of as-grown, post-growth patterned, post-growth patterned annealed at temperature 600 °C and 800 °C. At higher anneal temperature 800 °C, sample surface is rough compared to as-grown or low anneal temperature. From the Dektak surface profiler measurement, thickness had also decreased 1~2 μm at this high annealing temperature (800 °C).

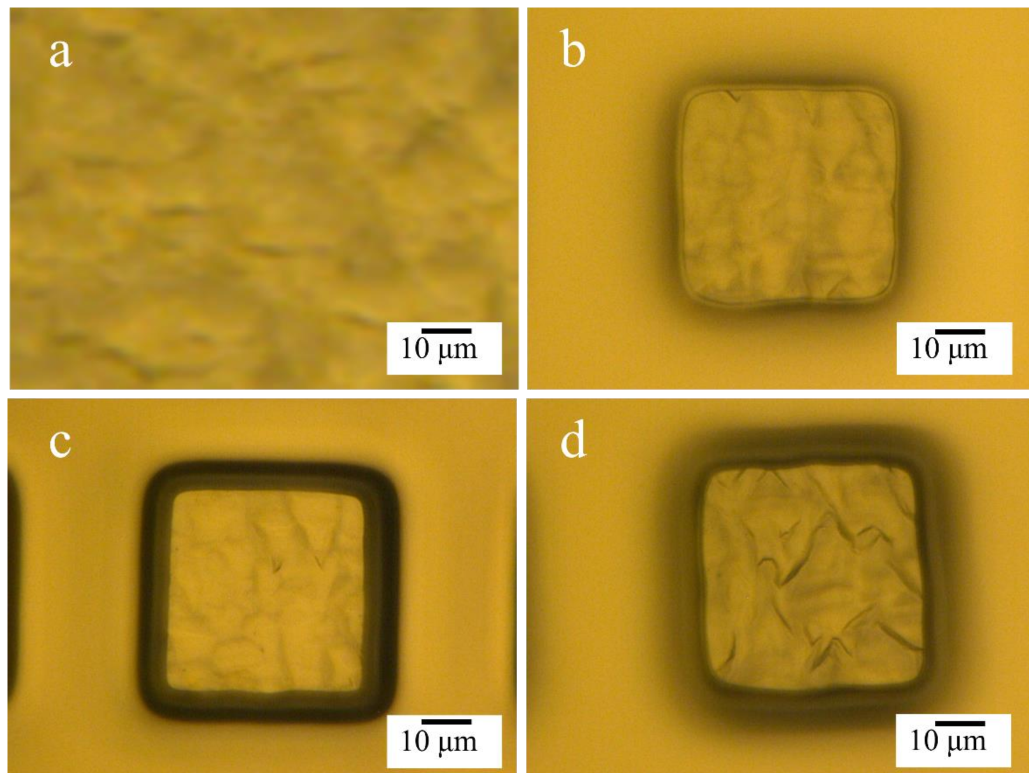

Fig. 5.3 Sample morphology of (a) as-grown, (b) post-growth patterned samples before annealing, (c) PHP sample annealed at 600 °C and (d) 800 °C for fixed anneal duration 5 minutes, single cycle, annealing at 800 °C made the sample surface rough and the thickness was also decreased.

Figure 5.4 shows the surface morphology of Everson etched whole wafer samples that were subjected to different annealing temperatures. Triangular pits corresponding to CdTe (211) B face are clearly observed. From this observation, we counted the pits formed on the surface and plotted them as a function of annealing temperatures as in **Fig. 5.5**. The number of pits formed on the sample surface decreased after annealing when compared to non-annealed sample. The EPD decreases monotonously with annealing temperature up to 700 °C but then slightly increases at 800 °C because of surface degradation at this temperature, which may be due to a similar reason as discussed in **Fig. 5.3**. Annealing at 700 °C resulted an EPD value of 1.02 x 10^6 cm^{-2}, which is about a 52% reduction with respect to the non-annealed whole wafer sample's EPD value.

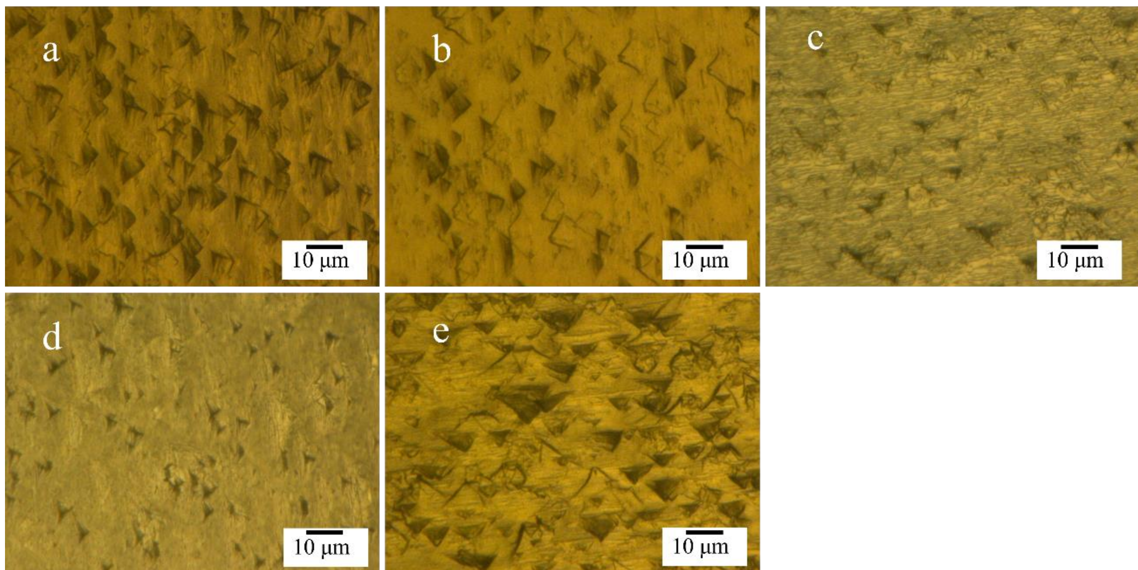

Fig. 5.4. Optical images of whole wafer sample surface after Everson etching (a) no anneal and annealed at (b) 550 °C, (c) 600 °C, (d) 700 °C, and (e) 800 °C.

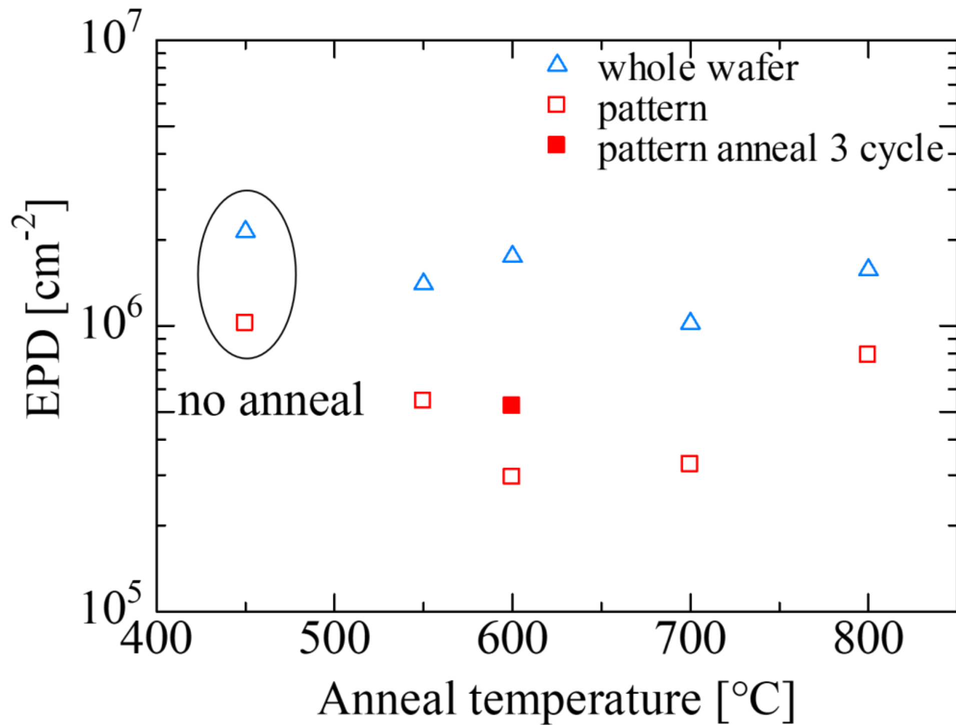

Fig. 5.5 EPD of CdTe layers as a function of annealing temperatures. All anneal were performed for 5 min, single cycle except data point shown by red solid square when 3 cycle anneal was used.

Figure 5.6 shows the surface morphology of post-growth patterned and annealed samples after Everson etching. The samples were subjected to different temperature anneal. It clearly shows smaller number of pits formed on the surface when compared to the whole wafer samples subjected to the similar anneal. The number of pits formed on the island surface were counted and were also plotted in **Fig. 5.5**. It shows the EPD value decreases rapidly when compared to the whole wafer sample and attains a minimum value around anneal temperature of 600 °C. At this anneal temperature, a lowest EPD value of

2.95×10^5 cm^{-2} was obtained, which is well below the value obtained for the whole wafer surface. This may be due to enhancement of dislocation glide motion, which then exit at the edges of the island. For comparison, we also studied three cycles annealing on the patterned sample at 600 °C, keeping anneal duration 5 minutes fixed per cycle. The surface morphology of this sample is also shown in **Fig. 5.6**, whereas the EPD count result is also plotted in **Fig. 5.5**. The number of pits formed on the surface slightly increased giving a higher EPD value than the single cycle anneal. This confirms patterning and annealing is very useful in dislocation reduction in MOVPE grown CdTe/Si. However, in patterned samples also, as in the whole wafer sample, the EPD shows an increasing trend when the anneal temperature is raised to 800 °C. The reason may be similar to that explained for the whole wafer sample. On the other hand, though a limited investigation, no improvement in TD reduction was achieved using higher cycle anneal. The EPD values we obtained in this investigation are comparable to that of the state-of-art MBE grown materials (low 10^5 cm^{-2}) or MOVPE grown materials [7,9-11]. However, those reported values were for CdTe layers grown on Si substrates with intermediate ZnTe buffer layers (to reduce the lattice mismatch), whereas our CdTe layers do not have intermediate ZnTe buffer layers. This confirms effectiveness of the post growth pattern and annealing technique.

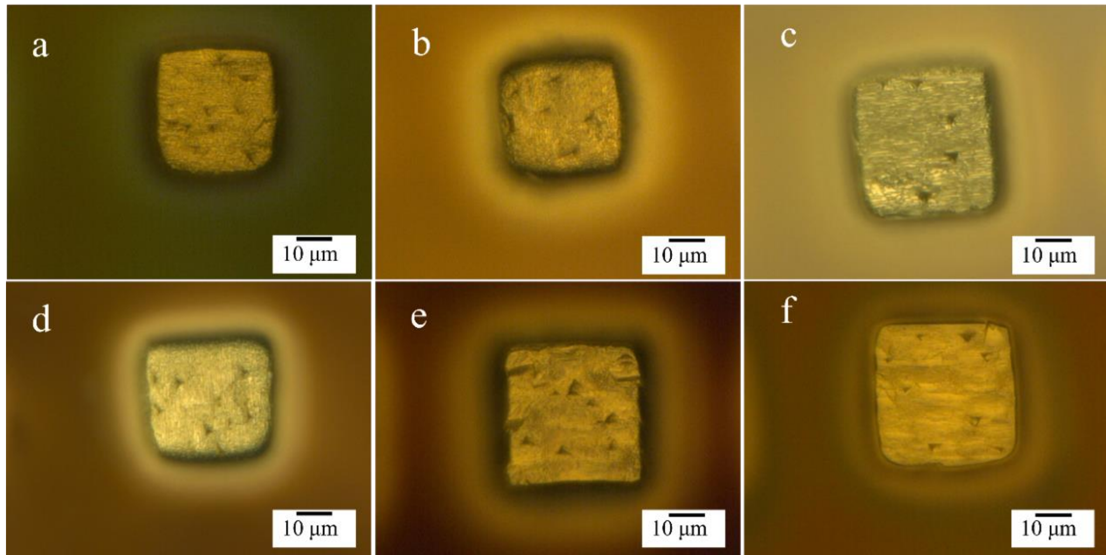

Fig. 5.6 Optical images of post-growth pattern sample surfaces (a) no anneal and anneal at (b)550 °C, (c) 600 °C, (d) 700 °C, (e) 800 °C and (f) 600 °C, 3cycles after Everson etching.

5.4 Regrowth on the patterned annealed CdTe samples

In this study, we used patterned and annealed CdTe samples, where the CdTe layer thickness was varied from 0.4 – 10 μm. These samples were annealed ex-situ at 500 °C, 5 min, in hydrogen environment as described above. Subsequently, regrowth of CdTe epilayers of different thicknesses were performed at temperatures varying from 325 °C to 500 °C on these samples. Typical surface morphology of regrown CdTe layer on the patterned and annealed sample is shown in **Fig. 5.7**. The patterned sample, in **Fig. 5.7 (a),** has about 2 μm thick CdTe layer. Shown in **Fig. 5.7 (b)** is the sample morphology after the regrowth, where the thickness of the CdTe layer is about 10 μm. The result shows CdTe growth occurred not only on the islands, but also between them, resulting in a rough and uneven surface not suitable for device fabrication. Regrowth on the patterned and

annealed samples of different thicknesses also exhibited similar rough surfaces. This could be due to the large pattern sizes, their heights, and the larger gaps between them. Hence, optimizations of pattern dimensions and growth conditions are needed to achieve smooth surfaces and selective epitaxy exclusively on the CdTe islands.

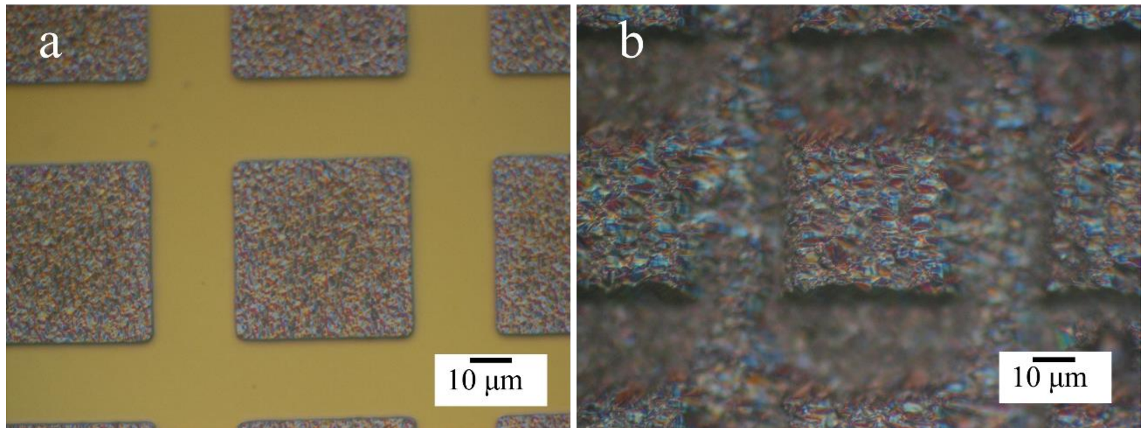

Fig. 5.7 Optical images of sample surfaces: (a) Patterned annealed sample, where the CdTe thickness is about 2 μm, and (b) sample surface after the regrowth, where the CdTe thickness is about 10 μm.

5.5 Discussion and Outlook

It was confirmed that patterning and annealing was effective for TD reduction in thin CdTe/Si. In this study, we used CdTe with typical thicknesses of 10 μm. However, for the gamma ray detector development thicker layers of several hundreds of μm will be needed for efficient gamma ray absorption. Patterning is difficult on such thick layers. To achieve thicker epilayers, we further studied regrowth on the post-growth patterned and annealed CdTe/Si samples. We studied regrowth by varying both the regrown CdTe layer thicknesses as well as the initial thicknesses of the CdTe layers on the patterned samples.

However, all studies on the regrowth on these patterned and annealed samples resulted in very rough layer, which was not suitable for the device application. So, while this technique effectively reduces dislocations in thin epilayers, it cannot be applied for gamma detector development in its current state. Further optimization of pattering and regrowth techniques is needed.

5.6 Conclusions

Threading dislocation density (TD) reduction in MOVPE grown CdTe layers on Si substrates using post-growth patterning and annealing was studied. After growth, the samples were patterned with photolithography to make 60-μm-wide square islands and annealed ex-situ in a flowing hydrogen environment at temperatures varying from 550 ºC to 800 ºC for a fixed anneal duration of 5 minutes. It was found that post-growth patterning and annealing was more effective for TD reduction. Patterned samples annealed at 600 ºC showed lowest TD density of 2.95×10^5 cm^{-2}, which is nearly an order of magnitude lower than the TD density of whole wafer samples subjected to similar annealing treatment. It is concluded that in pattern samples, annealing promotes dislocation glide towards the sidewalls of the islands, hence their densities are reduced at the island surface. To achieve thick films for detector fabrications, we further studied regrowth on the post-growth patterned and annealed CdTe/Si epilayer. The regrowth on the patterned sample, however, resulted in very rough layer, not suitable for the device application. Further optimizations of patterning and regrowth techniques are needed to obtain the thick and smooth CdTe layers selectively on the islands for the detector developments.

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Chapter 6

Optimizations of ex-situ annealing and its implementation during gamma ray detectors fabrication in a p-CdTe/n-CdTe/n^+-Si heterojunction structure

6.1 Introduction

As discussed in earlier chapters, dislocation in the epilayer was the major issue that severely degraded the device's property. In Chapter 5, we studied on post-growth patterning and annealing techniques in CdTe/Si epilayer for dislocation density reduction, where a lowest dislocation density of 2.95 x 10^5 cm^{-2} was obtained on a 10 μm thick patterned sample. Though such dislocation densities are acceptable for our device applications, however, this technique at the current state cannot be applied for gamma ray detector fabrication. For the detector development, thick layers ranging from several tens to hundreds of micrometers are required, depending on the gamma ray energies [1-3]. Patterning on such thick layers are not possible. On the other hand, regrowth on the thin patterned and annealed samples to obtain thicker epilayer resulted in very rough layers not suitable for the device applications. Hence, to achieve suitable dislocation reduction technique which can be implemented easily in the device fabrication, in this chapter, we studied optimizations of ex-situ annealing conditions using whole wafer CdTe samples. Annealing temperatures, durations and number of cycles were varied to optimize the

annealing conditions. Here, modified annealing conditions were employed by varying the number of annealing cycles and duration per each cycle, different from those studied in chapter 5. Gamma ray detectors were fabricated by subjecting the optimized annealing conditions during CdTe growth, and the annealing effects on the device performances were evaluated. It was found that annealing was helpful in improving the device's performance.

6.2 Experimental procedure

6.2.1 Ex-situ annealing study

CdTe layers with thicknesses of typically 5 μm were grown on (211) Si substrates using metalorganic vapor phase epitaxy (MOVPE). The substrate temperature for CdTe growth in this study was kept constant at 450 ºC. All samples studied were grown in the same growth run. The grown CdTe/Si samples were cut into several 6 mm x 6 mm pieces. Rapid thermal annealing was performed ex-situ in a hydrogen environment by placing two samples face to face inside a horizontal quartz tube as explained in chapter 2. The anneal temperature was varied from 600 to 1000 ºC, whereas the anneal duration was fixed at 60 s and the number of anneal cycles was varied from 1~7. Here, we modified the annealing conditions than that studied in last chapter by incorporating the effect of annealing cycles, and duration per each cycle. For comparison, a limited number of samples were also subjected to a single cycle, 5 minutes of annealing at temperatures of 600 and 700 ºC. After annealing, samples were subjected to dislocation decorating etching using Everson solution with volumetric ratios of lactic acid: nitric acid: hydrofluoric acid of 25:4:1 for a fixed etching time of 2 minutes [4]. The dislocation density on the sample surface was estimated by counting pits formed on the surface using

an optical microscope. Based on the lowest etch pit density (EPD) obtained, the best annealing condition was established.

6.2.2 Device fabrication and characterization

Two types of devices were fabricated in this study to examine the effectiveness of annealing in the device's properties. The details of the devices were as follows: Device (D1) was fabricated by growing an iodine-doped n-type CdTe layer on the (211) n^+-Si substrates and then an un-doped CdTe layer, which shows a p-type property on the top [5]. The thickness of the n-CdTe and the p-CdTe layers were typically 5 μm and 40 μm. The n-CdTe layer was grown at 325 ºC whereas the p-CdTe layer was grown at 450 ºC. Device (D2) was similarly fabricated, however, after the n-CdTe growth, it was subjected to ex-situ anneal at 870 ºC, 3 cycles, 60 s which was the best annealing condition established in this study. After that, the annealed sample was placed back into the growth chamber and then the p-CdTe layer was grown on the top. The thickness of the n-CdTe and p-CdTe layers was kept similar to that of the D1 device. These samples were further cut into small pieces. One set of samples was subjected to dislocation decorating Everson etching for EPD evaluation [4]. Another set of samples was used for device fabrication. For this, gold electrodes were deposited on the p-CdTe side and then on the back side of the n^+-Si surface to make ohmic contacts [6,7]. **Figure 6.1** shows the schematic cross-section of the device fabricated. Finally, the devices were cut into 1 x 1 mm^2 chip and mounted in a chip carrier. The device properties were evaluated by the current-voltage (*I-V*) and the gamma-ray detection measurements at room temperature.

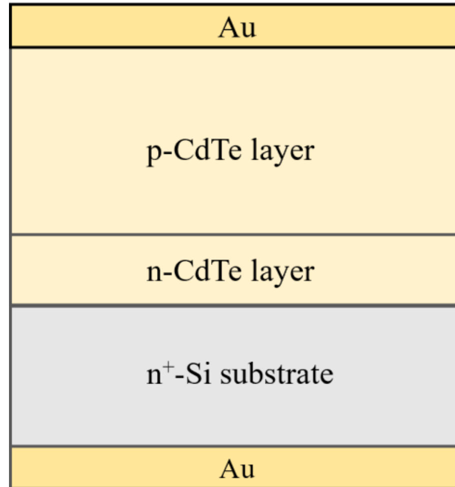

Fig. 6.1 Schematic cross-section of the device fabricated. Device D1 was fabricated by continuously growing n-CdTe and p-CdTe layers, whereas n-CdTe layer was subjected to ex-situ anneal in D2 sample, prior to p-CdTe growth.

6.3 Results and discussion

6.3.1 Ex-situ annealing and EPD analysis

We first studied the effect of annealing temperature. No significant effect of annealing was observed at lower temperatures of 600 or 700 °C, 60 s anneal. It could be due to the small annealing temperature and time, which is not sufficient for dislocations' motion and their interaction. Effect of annealing was observed only when the annealing temperature was increased above 800 °C. **Figure 6.2** shows the surface morphology of the Everson etched CdTe sample which was subjected to different annealing conditions. The samples were annealed at 870 °C, 60 s, where the number of cycles was varied. Triangular pits corresponding to CdTe (211) B face are clearly observed. Pits formed on the surfaces were counted using an optical microscope and plotted in **Fig. 6.3**, where results from other

annealing experiments were also included. The EPD of samples annealed at 870 ºC decreases when the annealing cycle is increased from 1 to 3. However, a further increase in anneal cycle results higher EPD value which shows a saturation tendency. This could be due to the roughening of the sample surface due to the increased surface temperature of the sample due successive cycles. On the other hand, samples annealed at temperatures 820 ºC and 1000 ºC showed less desirable results. To examine the effect of annealing duration, we further studied a single cycle anneal at temperatures of 600 and 700 ºC by increasing anneal duration to 5 min. The EPD values of samples annealed at these temperatures are also shown in **Fig. 6.3**, which are found similar to that of the EPD values of the as-grown samples. Hence, the annealing effect was not observed even though the annealing duration was increased at lower annealing temperatures. These EPD values are slightly different than those reported in chapter 5 for whole wafer samples. This difference is due to the differences in the sample thicknesses. This confirms that the annealing condition of 870 ºC, 60 s, 3 cycles was best, where the lowest EPD value of 2×10^6 cm^{-2} was obtained.

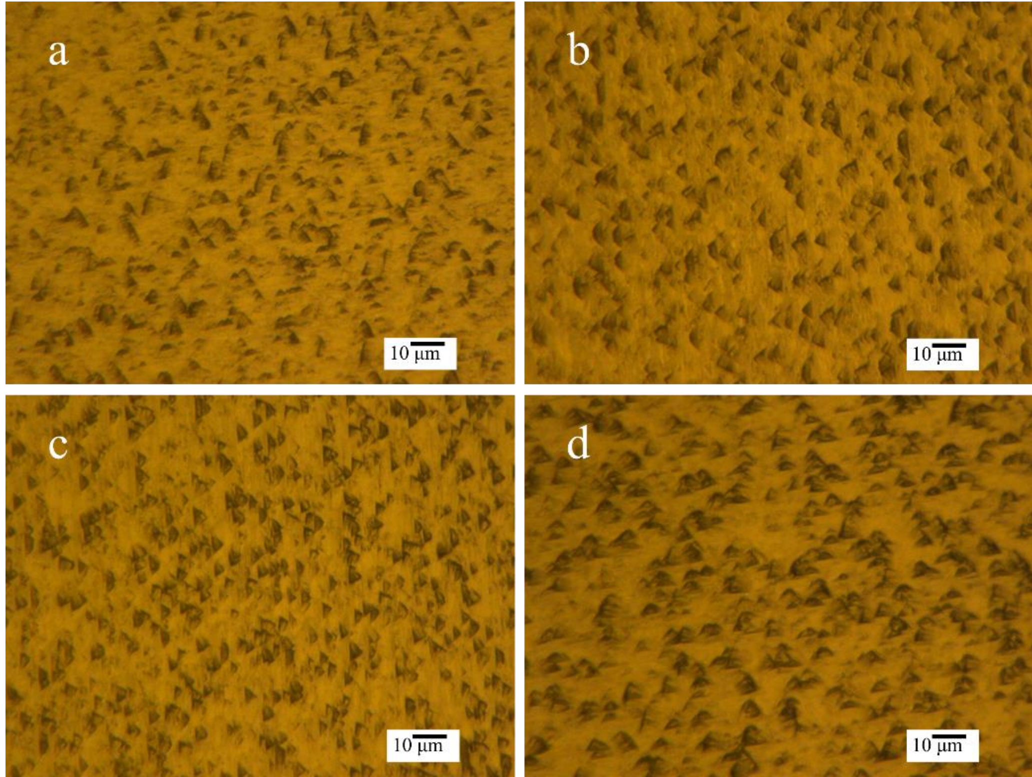

Fig. 6.2 Optical images of sample surface after Everson etching. The samples were annealed at 870 ºC for (a) 1, (b) 3, (c) 5, (d) 7 cycles, keeping the anneal duration 60 s per cycle.

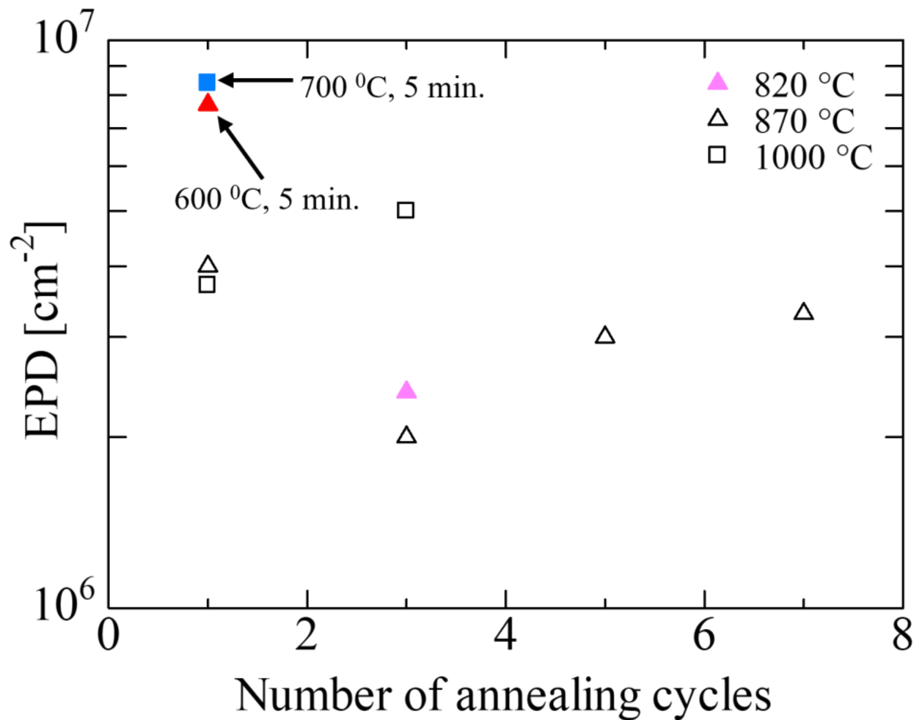

Fig. 6.3 EPD as a function of annealing temperature and cycles. The annealing duration was kept at 60 s per cycle for all samples except than the samples annealed at 600 and 700 °C.

6.3.2 Device fabrication and evaluation

Figure 6.4 shows the optical images of the D1 and D2 sample's surface after Everson etching. For comparison samples grown at different growth runs are also shown. The number of pits formed was lower in D2 when compared to D1. The pits were counted and plotted in **Fig. 6.5**. The annealed sample D2 shows an average of 33% lower pits than the unannealed sample D1, where the lowest EPD value of 5 x 10^4 cm^{-2} was obtained. This confirms that annealing was effective for dislocation reduction and improvement in crystal quality. **Figure 6.6** shows the reverse bias current-voltage (I-V) characteristics of

the device measured at room temperature. The unannealed sample D1 showed a larger dark current compared to the annealed sample D2. Both samples show a square-root dependence of current on applied bias at lower bias range, then the dependence turns to linear. The deviation, however, was earlier for the D1 samples, which may be the effects of the higher dislocations.

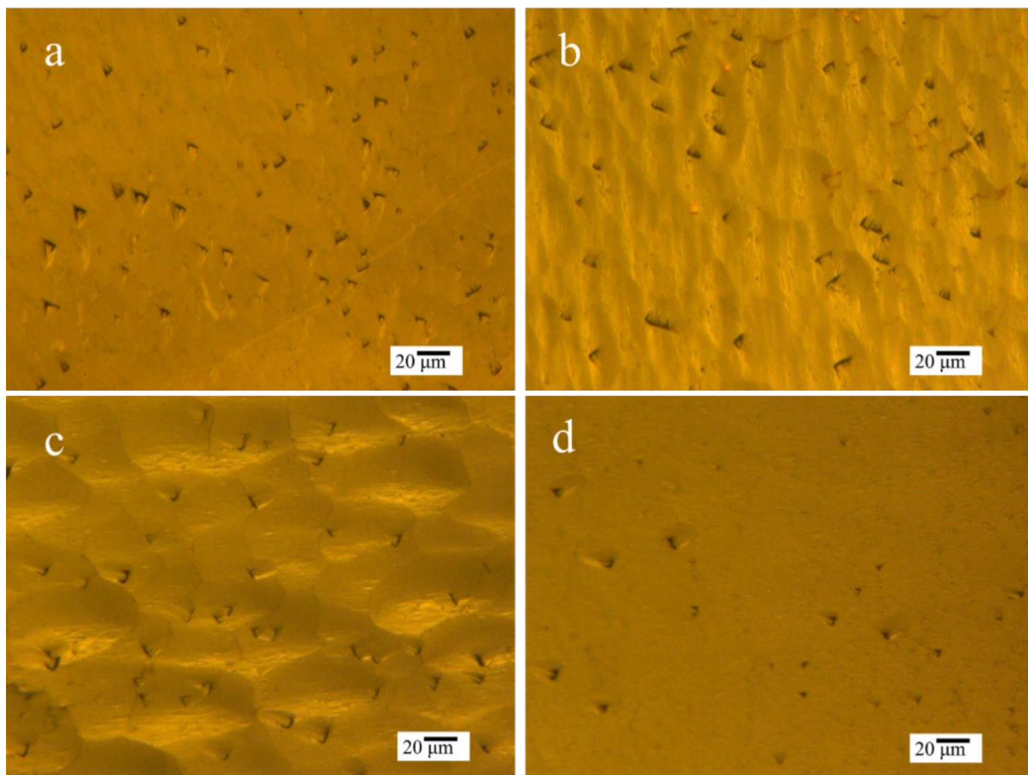

Fig. 6.4 Optical images of D1 sample (a,c) and D2 sample (b,d) after Everson etching.

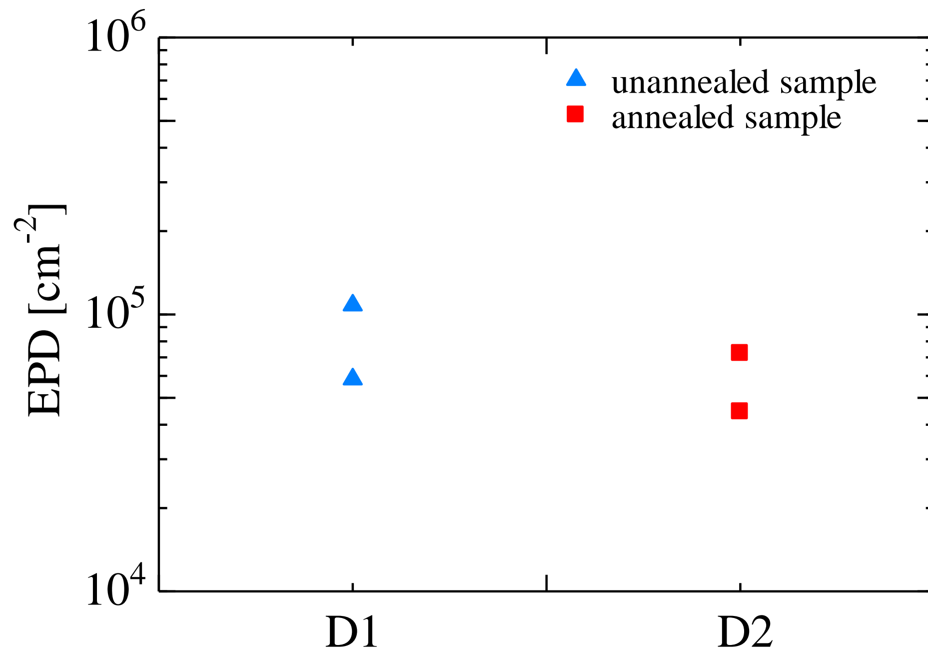

Fig. 6.5 EPD of samples D1 and D2

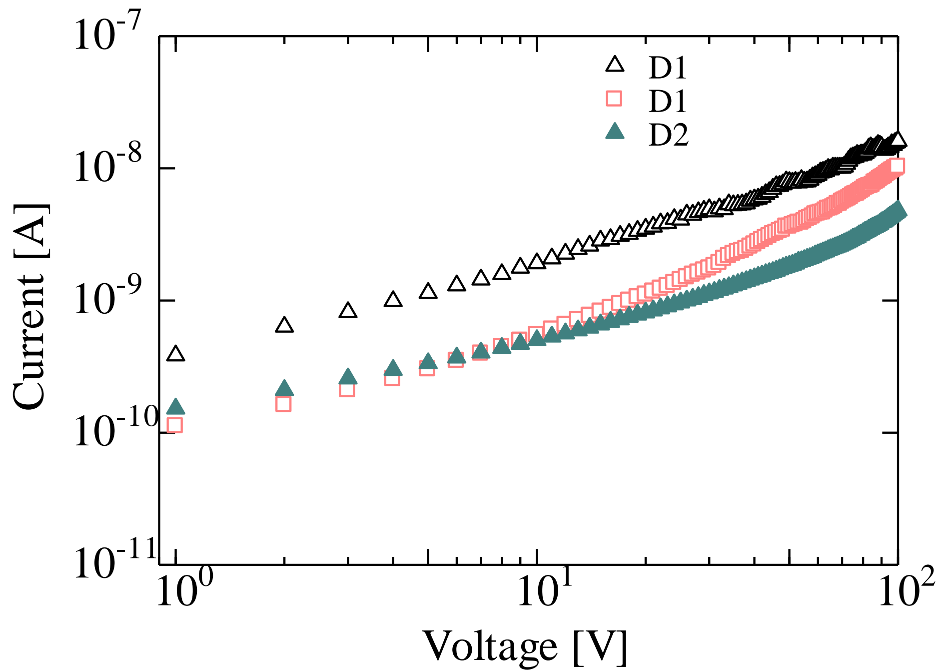

Fig. 6.6 Reverse bias characteristics of the diode-type detectors measured at room temperature.

Finally, we measured the gamma detection properties of the detectors. For this measurement, the detectors were mounted on a customized sample holder, as described in chapter 2, which was then directly connected to a pre-amplified. A positive bias was applied on the detector to operate it in a reverse bias mode and an ^{241}Am radioisotope was placed in front of the detector. The signal generated by the gamma radiation in the detector was passed through the pre-amplifier, shaping amplifier, and a multichannel analyzer connected to a computer. All measurements were performed under similar conditions at room temperature. **Figure 6.7** shows the gamma spectrum of the ^{241}Am radioisotope recorded by the detectors. The 59.5 keV main gamma peak and other lower energies were

clearly identified from all detectors [1,8]. However, the spectrum recorded by D1 detectors shows lower energy tailing at 59.5 keV peak and the other low energy peaks are also broad and less resolved. However, no such effects were observed for D2 detectors. This indicates the charge transport properties of the D2 detector are better when compared to the D1 detectors, confirming cycle annealing helps to improve detector performances. Still, both detectors suffer from high leakage current that has affected their performance. Other than dislocation-related current, surface leakage current which increases at higher applied biases should be reduced.

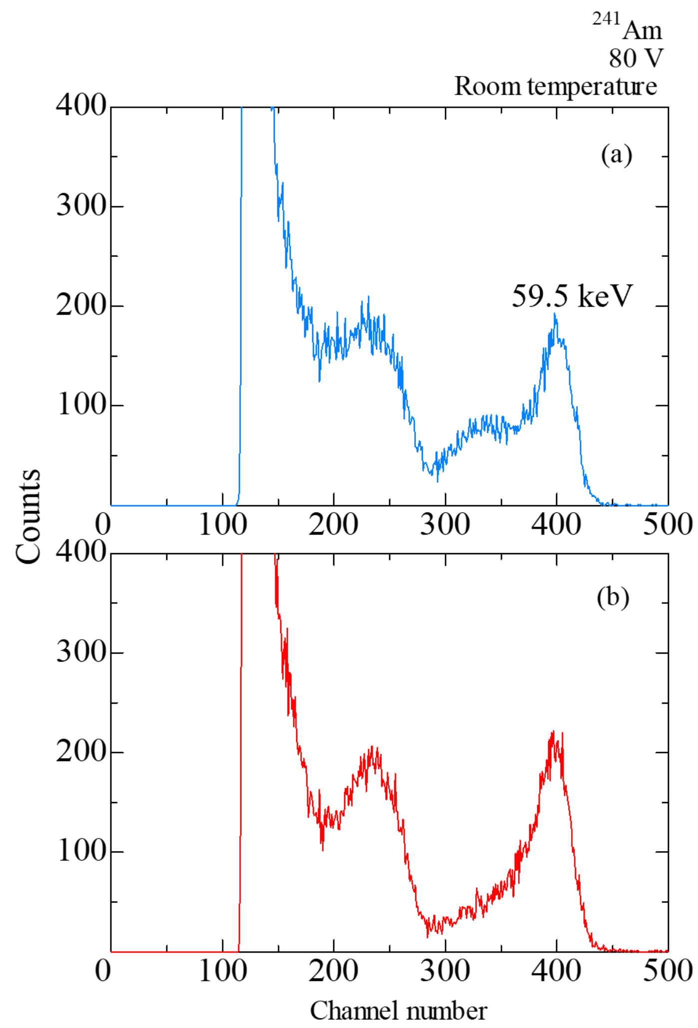

Fig. 6.7 Pulse height spectrum of the ^{241}Am gamma source obtained from the detectors D1 (a) and D2 (b).

6.4 Conclusions

Dislocation density reduction in MOVPE-grown CdTe layers on Si substrates using ex-situ cycle annealing technique was studied. The grown samples were annealed at temperatures varying from 600 ~ 1000 ºC for different anneal duration and cycle. The lowest dislocation density was obtained on a CdTe layer annealed at temperature 870 ºC, 60 s for 3 cycles. Further, we fabricated devices in a p-CdTe/n-CdTe/n^+-Si diode type detector using this best annealing condition. Gamma detection property and device dark current were evaluated and it was confirmed that annealing improves the device performances.

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Chapter 7

Conclusions and Future works

7.1 Overall conclusions

The MOVPE growth of single-crystal CdTe on large area Si substrates is a promising way to obtain large area crystals that are required for X-ray, gamma ray detector development. However, the direct growth of CdTe on Si substrates is very challenging because of large differences in lattice mismatch and thermal expansion coefficient between these two materials. To overcome this, a specialized Si substrates pre-treatment method, developed previously in our laboratory, was employed to achieve the direct growth of CdTe single crystals on Si substrates. Subsequently, detectors were fabricated in a p-CdTe/n-CdTe/n^+-Si heterojunction diode structure. The detector evaluation, however, revealed that there was a need for the gamma detection property improvement. It was found that detector suffered from a large dark current that degraded its gamma detection property. The dislocation-related defects in the crystal were primary source of the dark current. The dislocations generated at the n-CdTe/n^{+-}Si heterointerface were not only localized there but also extended deep into the epilayer, penetrating the depletion region formed between p-CdTe/n-CdTe, resulting excessive dark currents. Furthermore, the suboptimal transport property of photon-generated charge carriers was another factor affecting the detector's detection property. It was found that the incomplete depletion of the thick p-CdTe layer, led to recombination of photo-generated charge carriers during their transport. The objective of this work was to improve the detector properties by

reducing the dislocation in the crystal as well as to optimize the device structure so that the depletion region fully extends towards the p-CdTe layer. To achieve this goal, dislocation reduction by the application of thermal annealing as well as growth conditions of highly doped thick n-CdTe layer were studied in this work. The main results obtained are summarized below.

In chapter 3, we studied properties of iodine-doped CdTe layer grown on (211) Si substrates by varying the substrate temperatures and the flow-rate ratios of the Te/Cd source materials. Higher substrate temperatures than our previously studied values were investigated to achieve a higher growth rate. The maximum growth rate of 2.6 μm/h was obtained at a substrate temperature 425 °C. The highest electron density of 2.5×10^{18} cm^{-3} was obtained for CdTe epilayers grown at substrate temperature 400 °C and VI/II ratio of 0.05. It was confirmed that VI/II flow rate play an important role to improve the electron density by suppressing the Cd vacancy rather than the substrate temperature range investigated in this work. The growth rate is nearly five times higher, and the electron density is nearly an order higher than the previous growth rate that was used in our laboratory. This made the growth of highly doped thick n-CdTe layer possible.

In chapter 4, we investigated dislocation distribution in the CdTe epilayer and their correlation with the device dark current using devices with structure of p-CdTe/n-CdTe/n^+-Si heterojunction diode. Devices with different p-CdTe thicknesses were investigated. It was found that thin devices had a high dislocation density, which decreased as the device thickness increased. However, even in a 35 μm thick device had a high threading dislocation (TD) in the order of 10^6 cm^{-2}. The device dark currents showed a strong dependence on TD density that reached up to the p-CdTe layer, penetrating the depletion region formed at the n-CdTe/p-CdTe. Dislocation density higher

than 10^7 cm^{-2} made the device unsuitable by generating excessive currents. The dark current in those devices were due to the trap assisted tunneling resulting from the large number of dislocations intersecting the p-n junction. It was found that dislocation density should be reduced well below the order of 10^6 cm^{-2} for effective detector applications.

In chapter 5, we applied an approach for dislocation density reduction in CdTe/Si epilayer using post-growth patterning and annealing technique. Typically, 10 μm thick CdTe layers were patterned using photolithography to make square islands with dimensions of 60 μm x 60 μm. The patterned samples were then annealed in a flowing hydrogen environment at temperatures varying from 550 ~ 800 °C for a fixed anneal duration of 5 min. The sample annealed at 600 °C showed the lowest TD density of 2.95 x 10^5 cm^{-2}, nearly an order of magnitude lower than the TD density of the whole wafer sample subjected to similar annealings. This confirmed the effectiveness of this technique in dislocation reduction, however, this technique in current state could not be applied for the gamma detector fabrication. Because for the gamma ray detector development thicker epilayers of several tens of μm are needed for efficient gamma ray absorption. Patterning is difficult on such thick layers. To achieve thicker layers, we further studied regrowth of CdTe on the patterned and annealed samples. CdTe layers of various thicknesses were regrown on patterned and annealed samples that had different initial CdTe thicknesses varying from 0.4 μm to10 μm. However, the regrown layers exhibited very rough surfaces, and they were not suitable for the device applications. This indicates further optimizations of this is needed.

In chapter 6, we studied optimizations of ex-situ annealing conditions on whole wafer CdTe layers for dislocation reductions and its implementation during the device fabrications. Typically, 5 μm thick CdTe layers were used, and they were annealed by

varying the temperatures from 600 ~ 1000 ºC, anneal duration of 1 ~ 5 min. and cycles 1 ~ 7. The lowest TD density of 2 x 10^6 cm^{-2} was obtained on a CdTe layer annealed at 870 ºC, 60 s for 3 cycles. Using this annealing condition, the devices were fabricated in a p-CdTe/n-CdTe/n^+-Si heterojunction structure for gamma ray detection, where n-CdTe were first annealed, followed by growth of 40 μm thick p-CdTe layers. TD density of these thick devices was lower than 10^5 cm^{-2}. Devices subjected to annealing showed lower dark current and improved gamma detection property when compared to the devices that were not subjected to annealing during their fabrications. This confirms that annealing was effective for dislocation density reduction and for improvement of gamma detection property.

7.2 Future works

As discussed throughout this work, CdTe is a promising material for X-ray, gamma ray detector development. In addition to works described in this thesis, the following additional works are suggested to improve the detector performances further.

Further optimizations of the growth parameters and substrate pre-treatment process will help to obtain high-quality single crystal CdTe required for the detector development. Subsequently, defects in the CdTe layer, mainly dislocations, can be reduced further by optimizing annealing parameters. Besides this, during the ex-situ annealing, the sample should be carefully transported into the annealing apparatus because contamination with atmosphere degrades sample surfaces. On the other hand, as discussed in chapter 5, patterned and regrowth was highly effective in dislocation reductions. However, to effectively utilize this technique in detector fabrication further optimization of pattern dimensions and growth conditions are needed. We found that regrowth on the patterned

and annealed sample resulted very rough CdTe layers. This could be due to large-sized pattern used, where the patterns were 60 µm x 60 µm in size and the gap between them was 20 µm. This resulted CdTe regrowth not only on the island surface but also between them. To avoid this, pattern sizes and the gap between them should be reduced to nano sizes. Also, the thickness of the CdTe layer before subjecting to patterning (pattern height) should be investigated further, probably should be reduced well below than investigated in chapter 5. Hence, by further optimizing of patterning and regrowth techniques, thick and smooth CdTe regrown layer can be obtained, which can be used for the detector development. Furthermore, optimization of device fabrication technique is needed. The use of different contact materials and their deposition methods should be investigated. Likewise, techniques for surface processing of CdTe crystal before the electrode deposition, detector passivation techniques should be studied further to achieve detectors with better performances.

List of the Publications

1. M. Niraula, K. Yasuda, R. Tori, Y. Higashira, R. Tamura, **B. S. Chaudhari**, T. Kobayashi, H. Goto, S. Fuji, and Y. Agata, “Properties of Iodine-Doped CdTe Layers on (211) Si Grown at High Substrate Temperatures by MOVPE” J. Electron. Mater. 49, 6996 (2020).

2. **B. S. Chaudhari**, H. Goto, M. Niraula, and K. Yasuda, **“**Analysis of dislocations and their correlation with dark currents in CdTe/Si heterojunction diode-type x-ray detectors” J. Appl. Phys. 130, 055302 (2021).

3. **B. S. Chaudhari**, M. Niraula, Y. Takagi, R. Okumura, K. P. Sharma, T. Maruyama, **“**Dislocation Density Reduction in MOVPE-Grown (211) CdTe/Si by Post-Growth Patterning and Annealing” J. Electron. Mater. 52, 3431 (2023).

4. **B. S. Chaudhari**, M. Niraula, R. Okumura, T. Maruyama, **“**Dislocation reduction in an MOVPE-grown CdTe/Si epilayer by ex-situ annealing and its effect on the performances of gamma ray detectors fabricated” Phys. Scr. 99, 015931 (2024).

List of the Conferences

1. **B. S. Chaudhari**, Hayata Goto, Madan Niraula, Kazuhito Yasuda, “Evaluation of dislocation densities and their distribution in epitaxial (211) CdTe/Si”, (oral), JSAP 68th Spring Meeting, Mar. 16-19, 2021.
2. **B. S. Chaudhari**, Yutaka Takagi, Ryo Okumura, Madan Niraula, “Investigation on threading dislocation reduction on CdTe/Si epitaxial layer using post-growth patterning and annealing technique”, (oral), JSAP 83rd Autumn Meeting, Sep. 20-23, 2022.
3. **B. S. Chaudhari**, Yutaka Takagi, Ryo Okumura, Madan Niraula, “Study of dislocations distribution in (211) CdTe/ Si epitaxial layer and their reduction methods”, (oral), International Conference on Thin Films and Nanotechnology – Knowledge, Leadership and Commercialization (ICTN-KLC), Indian Institute of Technology Madras, India, July 6-8, 2023.