The Application of Optoelectronic Devices to Pattern Recognition through Neural Networks

Masayoshi UMENO* and Alessandro ZIMMER and Takashi JIMBO*

Department of Electrical and Computer Engineering

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In this paper we present possibilities for the implementation of neural networks using digital, analog, optical and hybrid device architectures currently under research. We also demonstrate the viability of the implementation of an "artificial retina" able to recognize a set of inputs by the use of monolithically integrated optoelectronic devices, which receive weights and compute the input/weights product in a VSPD (variable-sensitivity photodetector) array, then pass the results through an analog threshold element.

1 Introduction

Lately it has been noticed a great effort to understand the mechanisms that are present in our main processing unit, the brain. Trough better understanding of those processes we could be able to develop models that try to immitate, by learning processes, some of the inherent abilities of the human being, like pattern recognition and the recall of distorted information.

Some models were already created, including works of Grossberg, Parker, Rumelhart and others, and are well known for having a very good capability of generalization and mapping of space features. The main problem here is that those models require a fully parallel processing scheme that, if simulated by even the fastest serial computer would take an inconceivable time.

For this reason new device architectures have being developed to cope with the need of paralelism and consequent speed increase.

2 Digital Neuro-Devices

As an example we have a digital hardware implementation of a feed forward back-propagation artificial network by Naizeih et al in. [1] It was realized a circuit with FPGAs (Field Programmable Gate Arrays). Each node of the 5×4×2 (input-hidden-output) network used two FPGAs and eight 1K EPROMs. The learning is realized off-chip, with the circuit receiving weights and biases from a digital computer responsible for the simulations, and producing an output without the error signals. The main problem with this architecture is the size of the circuitry, since each node is performed by 10 chips, excluding control elements. Usually the only-digital neural circuits do not present in-situ learning due to the size of the circuitry needed.

To solve the problem of storing the weights, Thakoor et al.[12] cite the development of a programable binary synaptic matrix CMOS chip. It was built of nMOSFETs each functioning as a binary resistive connection. Each synapse consisted of a 1-bit shift register cell and a long channel nMOSFET. The disadvantage is that the long channel required for large resistances restricts the number of synaptic connections that can be put onto a single chip.

Another solution to the problem was presented as a film resistive network, where programmable read-only thin film synaptic test arrays based on memory switching in hydrogenated amorphous silicon have been fabricated. At each node of the matrix is a normally OFF microswitch of hydrogenated amorphous silicon in series with a current limitting resistor. By applying a short voltage pulse of a certain sufficient amplitude, the microswitch is permanently switched ON and the resistance is determined by the current limiting resistor. Although the connection strength is binary, it is possible to obtain a limited number of bits by simply combinning a number of connection matrices with the appropriate binary weighted current limmiting resistors.

* Research Center for Micro-Structure Devices.

3 Analog Neuro-Devices

Circuits with electrical properties changed after the processing of a certain number of signals, called self-learning neuron circuits, with both excitatory and inhibitory synapses were proposed by Hiroshi in [6] with each circuit composed by a MISFET with a ferroelectric gate insulator film. The source-drain resistance of the FET changes gradually by applying signal pulses with negative and positive pulses being interpreted as excitatory and inhibitory synapses.

Another work, presented by Brion et al., [2] includes simulations of on-chip learning forward and backward computations using analog components. The network learns how to compensate the deficiencies of analog circuits, such as limited voltage range, instability and lack of precision, and at the same time produces the desired computations. The additions required by the back-propagation algorithm are performed by summing currents on a wire. The multiplications are be performed by the use of analog multipliers (wide-range Gilbert multipliers). They are also used to perform the subtractions and to generate the threshold sigmoid functions.

In order to store the weights it was built an electronic neural network composed by a 22×22 array of micro-fabricated resistive synapses. [5] Since very small resistors could be fabricated, the overall substract area was smaller than the usual area required if transistors were used instead.

Another works about analog neuro-devices can be found at. [11),13)]

4 Hybrid Neuro-Devices

Mos of the work done on hybrid circuits are based on the use of transistors and memories. Song. [4] utilizes electrically-controllable MOSFET resistances, with the synaptic multiplication being done by the switching transistor. The system is connected to a computer control interface.

Thakoor et al. [12] utilizes high-density random access digital memories to store a large quantity of information associated with the synaptic weights while retaining high speed analog neurons for the signal processing. The neurocircuit consists of a block of digital RAMs for storing the binary data, a linear array of analog switches each connected in series to a current limiting resistor, an array of threshold amplifiers functioning as neurons, and a single feedback channel with a current summing amplifier. The operation of the circuit is controlled by clock signals.

5 Optical Neuro-Devices

Kyuma et al. in [7] presents an array of VSPD (variable sensitivity photodetectors) that is able to compute the matrix vector multiplication needed for neural networks calculations. The signal is then modulated by an external neural network. The circuit is said to be able to execute a great number of operations over the input pattern, as well as recognition of new patterns.

A bipolar optical neural network was presented by Cleber et al. [3]. The Hebbian rule can be achieved by optically comparing the states of two FLC (ferroelectric liquid crystals) cells, representing two bipolar neurons, and by driving a third cell with a voltage that changes according to the result of the comparison. The state of this third cell will switch according to the polarity of its voltage and therefore it becames equivalent to a clipped version of the corresponding connection strenght.

Waveguides were used by Junichi et al. [9] to emulate the Hopfield model, by considering that the waveguide has a parabolic index distribution in lateral direction and Gaussian index distribuition in the depth direction.

6 Intelligent Artificial Retina

As can be noticed, up to now there is no circuit able to to optical/digital or optical/analog computations in one single chip. Our interest is to show how it can be done, initially for one device with few processing possibilities, but monolithically integrated. This device would be a multi-layer neural network chip, with the optical interface serving to input the data as well as a front-end processor responsible for the first input/weights multiplication. The output would be generated and passed to the analog circuit responsible for realizing the threshold of the signal, and the subsequent multiplication of the second-layer weights, thresholding it again and finally outputing the final result. The system would be initially with an 36×1 feedfoward layer architecture described below.

6.1 Input Layer

As the first processing (hidden) layer an array of VSPD [7] is used. Each element of the array has two electrodes. One-sided electrodes are mutually interconnected at and among every row. The weights of the layer are individually set by external bias. When the light is distributed over the chip (equivalent to the input signal), the photocurrent is summed up over all rows of the two-dimensional array.

The total photocurrent of the rows will be equal to a vector multiplication between the light power output by the VSPD and its quantum efficiency corresponding to the synaptic interconnection strength. All rows would be connected in order to produce a single output to the next layer, so that the total output of the N × N array can be written as :

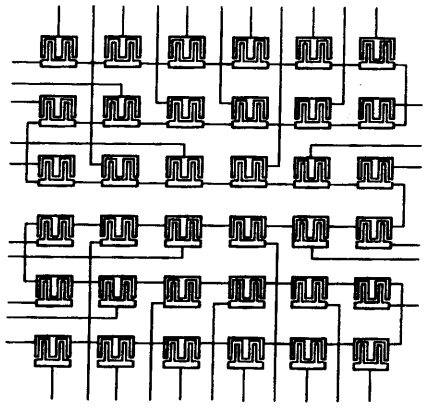

Fig 1. Photodetectors Array.

$$o = \sum_{i=1}^{N} \sum_{j=1}^{N} \eta_{ij} \upsilon_{ij}$$

with υ_{ij} being the input (light power) of each neuron, and η_{ij} the weight biases (quantum efficiency) of the first layer. Since, in the case of VSPD, the quantum efficiency can be modulated by the applied bias voltage[10], we can dinamically modify the weights of the network.

The processed output from the array must be thresholded by a non-linear function. This can be done by the use of a multiplier circuit (see 6.3).

6.2 Output Layer

The single output from the hidden layer needs to be multiplied by the output layer bias weight. This is done by the use of a wide-range Gilbert multiplier, which can perform analog-valued multiplications in four quadrants. In the wide-range version the ranges of input [8] voltages are independent from the output ones.

A four quadrant multiplier takes the difference between two voltages (V_1 and V_2) and multiply by a difference between two other voltages (V_3 and V_4), giving :

$$I_{out} = (I_b \tanh \kappa (V_1 - V_2)/2)(\tanh \kappa (V_3 - V_4)/2)$$

For both $(V_1 - V_2)$ and $(V_3 - V_4)$ less than $\frac{kT}{qk}$, the $\tanh x$ is approximately equal to x, producing then the desired product.

6.3 The Threshold Function

Both values produced by the hidden and output layer should be then thresholded by a non-linear element, usually a derivative of a sigmoid function ($s'(\cdot)$). This derivation can be approximated by $1 - s(\cdot)^2$, with s being the output of the sigmoid. The process can be executed by the wide-range Gilbert multiplier by making its inputs ($V_1 \sim V_4$) respectivelly equal to $1, s(\cdot), s(\cdot)$ and -1.

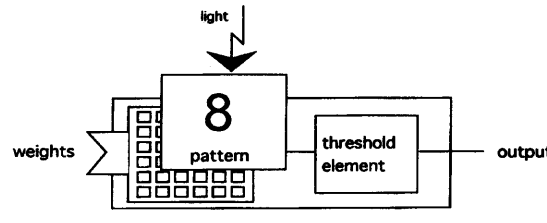

Fig 2. Neuro-Circuit.

7 Conclusion

We have shown that a simple "inteligent" artificial multilayer neural-network can be implemented by the use of an VSDP array and a few analog devices. A feedfoward network simulated through backpropagation learning rule was able to recognize up to 90% of printed digits bitmaps.

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