Studies on Deep Level Characterization and Optoelectronic Device Application of Rapidly Thermal-Processed GaAs

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ABSTRACT

The nature and distribution of the electrically active defects in rapidly thermal-processed (RTP) GaAs have been investigated. The conductive GaAs layers formed by Si implantation on the semi-insulating (SI) substrates and molecular beam epitaxy (MBE) are characterized by a deep level transient spectroscopy (DLTS) and an electro-chemical C-V method. The liquid encapsulated Czochralski (LEC) SI materials are characterized by the X-ray topography and the contactless measurement of a reflectance microwave prove method (RMP) using optically injected excess carrier. In LEC and horizontal Bridgman GaAs the most dominant deep level is known to be the EL2 center which has the near-infrared optical absorption band. Furthermore, in the present study the detection of EL2 by RMP method has been demonstrated by the numerical calculation. This technique does not have a good spectroscopic nature, however, this is a practical and useful technique to characterize the distribution of EL2 in SI GaAs wafers.

In the Si-implanted layers (250 keV, 2×10^{13} cm^{-2} dose), the residual defects produced by Si implantation are annealed by RTP over 800 °C, and two deep levels of NI2 (Ec - 0.55 eV) and EL2 (Ec - 0.78 eV) are detected.

In the MBE n-type layers, native defects in as-grown layer are annealed out during RTP at 800 - 900 °C. On the other hand, two deep levels of N1 (Ec - 0.5 ∿ 0.7 eV) and EL2 (Ec - 0.82 eV) are produced by RTP. The in-plane distributions of these deep levels are determined by DLTS and RMP method.

These distribution patterns of EL2 and N1 in MBE layers and LEC SI GaAs, which are produced by RTP at 800 °C, indicates that the spatial variations of deep levels are caused by the thermal stress developed as a result of small temperature gradient across the wafer. It is found that when the thermal stress are effectively suppressed by the guard ring preventing the heat transfer from the periphery of the wafer sample, the EL2 distributed uniformly in the wafer and N1 is not produced by RTP.

RTP is also applied to dope Zn acceptor from Zn-doped oxide film to n-type GaAs. The p^+n junction photodiodes fabricated by RTP were characterized by the analysis of spectral response curves and DLTS. The spectral response of photodiodes formed by RTP strongly depends on the heating rate. The diffusion length of minority carrier in the n-type bulk region is degraded by RTP with the rapid heating rate over 70 °C/s.

Consequently, if the temperature gradient is suppressed carefully by the use of the guard ring placed on the wafer edge, and the milder heating and cooling rates are employed to prevent the thermal stress, RTP at 800 °C or so is appropriate for the GaAs device processing, such as the activation of ion implants, defect annealing, and impurity diffusion to form shallow p^+n junctions.

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I. INTRODUCTION

The characterization of electrically active layers in GaAs and semi-insulating (SI) substrates, using some electrical and optical evaluation techniques is the most important subject to advance the GaAs device processing and to understand this material. This study deals with the characterization of the electrical properties on the conductive GaAs layers formed by the Si implantation, molecular beam epitaxy (MBE) and Zn diffusion, and the SI GaAs wafers grown by the liquid encapsulated Czochralski (LEC) method. In particular, this study shows how properties of these GaAs are changed during rapid thermal processing (RTP).

Recently, substantial attention has been given to RTP using halogen lamps, and the advantages of RTP over the conventional furnace annealing have led to a great deal of research activity in exploiting this technology.[1-12] The significant advantages of this thermal processing for the device fabrication are produced by facilitating very short thermal treatment for few seconds.[13-16] For example, (1) it is expected that the dopant and background impurity diffusion are minimized during annealing implantation damage and activation of implanted dopants. It has been reported that rapidly thermal-annealed GaAs shows the high electrical activation and electron mobility without noticeable dopant diffusion and surface decomposition, and metal-semiconductor field-effect transistors fabricated on the active layer formed by RTP show good drain and gate characteristics and high transconductance.[17,18]

(2) A poisonous gas such as AsH_3 may not be necessary for capless annealing, to prevent the desorption of As from the GaAs surface. It has been reported that Si-implanted GaAs at dose of about 10^{13} cm^{-2} after RTP at temperatures between 850 and 975 °C in either Ar or Ar-H_2 atmospheres shows essentially identical electric characteristics as compared to 30-min conventional furnace annealing under optimum conditions at 850 °C using the controlled atmosphere technique, and surface degradation was minimal for rapid thermal annealing with face-to-face configuration, as compared to exposed SiO_2 encapsulated surfaces.[16)]

(3) Large annealing systems can be constructed by increasing the number and the length of halogen lamps. (4) The diffusion of modulation-doped impurity of GaAs/AlGaAs heterostructures into the pure GaAs can be suppressed. In the application to short channel modulation-doped field-effect transistor, the mobility and sheet carrier concentration decreases associated with RTP below 850 °C are negligible.[19)] In addition, (5) it is expected that the depth of the shallow pn junctions is exactly controlled by RTP-conditions, such as diffusion temperature, hold time, heating or cooling rates.[20)]

RTP, however, involves rapid heating and cooling processes, so that there is a possibility that some native defects and those complex are introduced or annihilate in substrates and active layers during RTP.[21-26)] Since the deep levels relating to those defects in semiconductors act as generation-recombination-trapping centers,[27)] and generally have profound influence on

device performance,[28,29] the effects of RTP on deep levels should be paid attention.[30-55]

In this thesis, the experimental results and discussions are divided into four parts (Chap.II - V) from the points of view of the experimental techniques and device application, as follows.

In Chap. II, the electrical characteristics of deep levels in active layer and the distributions of deep levels in the wafer sample are given for Si-implanted and RTP-GaAs.

The thermal stability and the distribution of deep levels during RTP in Si-doped n-type GaAs layers grown by MBE are shown in Chap. III. In this chapter, the RTP-induced thermal stress in the GaAs wafer is also discussed and the distributions of its intensity are calculated using the elastic model in order to inspect the origin for spatial distribution of deep levels across the wafers.[56-62] The concentration and thermal ionization energy of deep levels can be determined by deep level transient spectroscopy (DLTS).[63] DLTS is commonly used to represent the investigation of deep levels, because this method is very convenient for determining the parameters of deep levels : electron and hole capture rates and emission rates, their energy level positions, and their concentrations, which completely characterize the carrier recombination properties.[64-66] Furthermore, it is spectroscopic, sensitive, and rapid and easy to analyze. However, it is difficult to characterize the deep levels in SI materials, because DLTS is applied to pn junctions, Schottky-barriers, which may be on the superlattice, or metal-insulator-semiconductor structure.[67-70] SI GaAs crystal is gaining favor as a direct ion implantation substrate in the

fabrication of high-frequency field-effect transistors (FET) and integrated circuits (IC).[17,18,69,71] The FET threshold voltage depends on both the carrier concentration and the thickness of the active layer. Thus, the in-plane uniformity of electrical activation efficiency, which is fluctuated by the distribution of the dislocation and point defects, should be controlled precisely to realize GaAs IC with high yield.[72-78]

In Chap. IV, the dominant mid gap defect in SI GaAs wafers are characterized by the contactless measurement of reflectance microwave probe method using optically injected carrier.[79,80] The optical injection of carriers in GaAs by the below-gap excitation is discussed.

The diffusion of Zn with the use of RTP is applied to form the p^+n junctions. The spectral responses of p^+n photodiodes fabricated by RTP are analyzed, and the relation between depth profiles of impurity concentration and spectral responses of photodiodes is discussed in Chap. V.

Finally, conclusions and suggestions for possible extensions of the study are given in Chap. VI.

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II. CHARACTERISTICS OF DEEP LEVELS IN Si-IMPLANTED GaAs LAYERS ACTIVATED BY RAPID THERMAL PROCESSING

2.1 Introduction

Characteristics of deep levels in donor ion-implanted semi-insulating (SI) GaAs substrates have been reported by several investigators,[1-5] since ion implantation into SI substrates has been widely used for fabrication of GaAs metal-semiconductor field-effect transistors and integrated circuits. In these reports, the conventional furnace processing (FP) has been performed at temperatures of 800-860 °C for 20 min for dopant activation.[1,2,4] However, it has been reported that the redistribution of the implanted ions[6] and the compensation deep centers Cr acceptor and EL2 donor[7-9] is caused by FP.

Recently, rapid thermal processing (RTP) has been successfully used to activate implanted impurities in GaAs and has been reported to have several advantages over conventional furnace processing.[3,10,11] Kohzu, Kuzuhara, and Takayama[10] have shown that n-type GaAs activated by RTP (100 keV, 5×10^{12} cm^{-2} dose) has higher peak carrier concentration and steeper carrier profile than the FP sample. For n^+-type GaAs (150 keV, 5×10^{13} cm^{-2} dose), they have reported that carrier concentration and mobility profiles for the RTP sample are almost the same as those for the FP sample. It is inevitable to characterize deep levels in ion-implanted and rapidly thermal-annealed SI GaAs, since the rapid heating and cooling during the RTP may produce some defects which are different from those in FP samples.[12]

Dhar, Seo, and Bhattacharya[3] have previously reported the results of deep level transient spectroscopy (DLTS) measurements for traps present in Si-implanted GaAs activated with RTP using halogen lamps by adopting a two-step annealing procedure. In this chapter, The results of a study on deep level traps present in Si-implanted GaAs activated by RTP using halogen lamps are presented. In particular, we have studied the dependence of the trap concentration upon the RTP temperatures and upon the Cr impurity in the substrates. Furthermore, the stability of midgap electron trap (EL2) is discussed. Comparison is also made between RTP and FP samples.

2.2 Experimental techniques

The substrates used in this study were (100)-oriented undoped and Cr-doped (0.17 ppm) liquid-encapsulated Czochralski (LEC) SI-GaAs. The wafers were chemically etched before implantation to remove any polishing damage. The implanted ion was $^{28}Si^{+}$ at an energy of 250 keV with a dose of 2×10^{13} cm^{-2} at room temperature. The present implanted dose and energy were appropriate for n^{+}-type layers. Furthermore, this higher dose enabled to evaluate traps near the surface by DLTS. After implantation, each 2-in. wafer was quartered and both sides of the individual pieces were coated with $\sim$3500 Å SiO_2 encapsulant. These were placed on a Si wafer susceptor in a quartz tube with the implanted side facing up and irradiated by cylindrical array of tungsten halogen lamps in flowing N_2. The RTP was performed

at 700, 800, and 900 °C for 6 s. The heating rate was fixed at 50 °C/s, and the sample was cooled down unintentionally. For comparison, conventional furnace processing was performed at 800 °C for 20 min with SiO_2 encapsulation.

After annealing, SiO_2 encapsulant was removed. Before the contact formation the annealed substrates were carefully cleaned by organic solvents and distilled deionized water. The carrier concentration profiles were obtained by electro-chemical C-V profiling system[13)] (POLARON PN4200). DLTS measurements with a bipolar rectangular weighting function[14)] were made on Au Schottky barrier diodes deposited by vacuum evaporation on the Si-implanted GaAs surfaces. The ohmic contacts were made on the same surface by alloying Au-Ge. These diodes were characterized by near-unity ideality factors in I-V characteristics.

2.3 Carrier concentration profiles in active layers

Carrier concentration profiles by electrochemical C-V measurements[13)] for n-type Si-implanted GaAs layers annealed at 800 °C are shown in Figs. 2-1(a) and 2-1(b). The peak carrier concentration is 1 - 2 x 10^{17} cm^{-3} for all samples investigated in this study.

Kohzu and co-workers[10)] have shown the dependence of electrical activation on RTP temperature for Si implants in Cr-doped SI GaAs by measuring sheet carrier concentration. In this study, the dependence of carrier concentration profile on annealing temperature from 700 to 900 °C is not clearly observed.

Carrier concentration profiles for RTP samples are almost

the same as those for the FP samples, as shown in Figs. 2-1(a) and 2-1(b). The similar carrier concentration profiles between Cr-doped and undoped samples is observed. This mutual agreement of the carrier profile for FP and RTP samples is consistent with the result in the case of implantation with high dose (5 x 10^{13} cm^{-2}) reported by Kohzu and co-workers.[10] On the other hand, it has been reported that the difference of the carrier concentration profiles between the RTP and FP samples is conspicuous in the case of implantation with the doses lower to our condition. It is supposed that impurities, such as Cr and Si, redistribute in different ways under thermal treatment at high temperatures in the case of low-dose conditions in comparison with higher-dose conditions above 2 x 10^{13} cm^{-2}.[15]

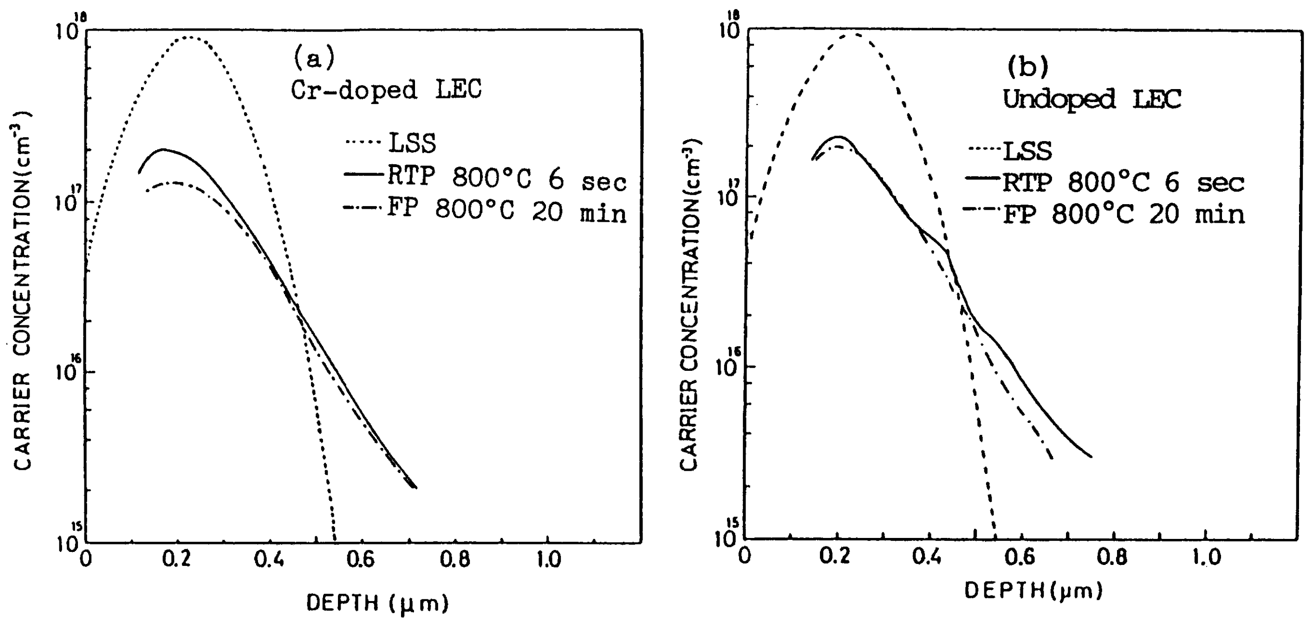


Fig.2-1. Carrier concentration profiles for Si-implanted GaAs layers after RTP and FP on (a) Cr-doped substrate, and (b) undoped one.

2.4 Deep levels in implanted layers

Figure 2-2 represents DLTS spectra for Si-implanted GaAs activated by RTP at 700 °C for 6 s. DLTS spectra in the upper half and the lower half of this figure show the signal from a Cr-doped sample and an undoped sample, respectively. The positive-going peaks indicate thermal emission from electron traps. The negative-going peaks in both DLTS spectra around 150 K are observed, although these signals are caused by using a majority-carrier pulse.[16] Hence, it can be suspected that the reverse current-voltage characteristics for these Schottky barrier diodes on the active layers by RTP at 700 °C are not ideal.[17] Actually, the reverse leakage current and the series resistance for these diodes are larger than those for the diodes made by RTP at 800 and 900 °C. Consequently, the activation of Si impurities is occurring by RTP at 700 °C for 6 s with residual implantation damage contained in the layers.

Three electron traps labeled NI1, NI4, and EL2 are observed in the Cr-doped sample, while three electron traps labeled NI1, NI3, and EL2 are observed in the undoped sample. These electron traps NI1, NI3, and NI4 are observed only in the RTP samples at 700 °C. On the other hand, the electron trap EL2 is observed in all present samples. The energy levels and capture cross sections for these traps are listed in Table 2-I. These values are calculated from the Arrhenius plots assuming that the capture cross sections are independent of temperatures. The trap concentrations are also shown in Table 2-I. These trap concentrations are averages of measured values for 7-10 diodes. These have been calculated from DLTS signals at $\sim 0.2\ \mu m$ below the surface.

Table 2-I. Characteristics of electron traps in Si-implanted GaAs.

Trap	Energy level (eV)	Capture cross section (cm^2)
NI1	Ec - 0.53 (± 0.02)	5.4×10^{-14} (±∿150%)
NI2	Ec - 0.55	5.1×10^{-15}
NI3	Ec - 0.47	1.1×10^{-16}
NI4	Ec - 0.63	1.0×10^{-14}
EL2	Ec - 0.78 (*)	5.0×10^{-14}

	Trap concentration (10^{15} cm^{-3}) Cr-doped				undoped			
Trap	700	800	900	FP	700	800	900	FP
NI1	2.4	-	-	-	2.1	-	-	-
NI2	-	14	180	150	-	1.4	8.4	14
NI3	-	-	-	-	1.2	-	-	-
NI4	22	-	-	-	-	-	-	-
EL2	6.7	21	5.2	1.0	13	5.6	14	1.7

* The energy level and capture cross section for trap EL2 in this Table is different from the values for EL2 in Table 3-II (p.35). However, the midgap levels in Si-implanted GaAs and molecular-beam-epitaxial GaAs are identified with EL2 level, since the photocapacitance quenching effect[21] (p.17,18) is observed in both samples. Various possible candidates to explain the differences between these trap paramaters are considered as followes. 1) The Schottky barrier height can be affected by the surface conditions.[35] The some errors in the trap paramaters may be caused by the low Schottky barrier height on Si-implanted GaAs.
2) The differences of the DLTS phenonena can be correlated with the reactions between metals and semiconductors.[36]
3) The EL2 state is perturbed by the other defects or donor impurity in Si-implanted GaAs layers.

Bhattacharya et al.[18] have reported an electron trap at Ec - 0.53 eV in the n-type VPE GaAs after Si implantation and FP. Furthermore, Rhee, Bhattacharya and Koyama[4] have reported that the same electron trap is observed in n-type layers formed by Si implantation and FP on Cr-doped SI substrates. They regarded this electron trap to be an ion implantation induced defect. An electron trap C (Ec - 0.53 eV) in Si-implanted GaAs MESFET on undoped and Cr-doped LEC SI substrates has been reported by Sriram and Das.[2] The trap NI1 is identical with these traps reported by Bhattacharya et al.,[18] Rhee and co-workers,[4] and Sriram and Das,[2] and it is considered that these traps are produced by ion implantation.

The trap NI3 is observed in the undoped samples and not observed in the Cr-doped samples. These are no reports about an electron trap corresponding to the trap NI3, to our knowledge. However, the trap NI3 is not detected in Si-doped n-type LEC GaAs prepared by RTP at 700 °C for 6 s by the same apparatus as the present experiment.[19] Hence, NI3 is not due to any contamination during RTP or the fabrication of Schottky barrier diodes, but it is considered that NI3 is also caused by ion implantation.

The trap NI4 is observed in the Cr-doped samples and not observed in the undoped samples, and the concentration of the trap NI4 is about 2×10^{16} cm^{-3}. Therefore, it can be considered that the trap NI4 is related to Cr impurity. Stievenard and Bourgoin[20] have reported an electron trap I2 (Ec - 0.62 eV) in S-doped CZ materials irradiated by electron beam, and have

concluded that the trap I2 is an impurity complex defect, involving interstitial As (As_i). The Arrhenius plot of thermal emission rate for the trap NI4 coincides with that of the trap I2. Therefore, this trap NI4 is probably the same as the trap I2. These traps are related to Cr impurity and a lattice defect. The thermal emission rate for the trap H (Ec - 0.57 eV) reported by Dhar, Seo, and Bhattacharya[3)] approximates to that for the trap NI4 in the measured temperature range. However, the activation energy and capture cross section for the trap H are smaller than that for the trap NI4. Furthermore, the spatial variation of the concentration across the wafer is not observed for the trap NI4, but the notable variation has been reported for the trap H. Therefore, we consider that the trap H is different from the trap NI4.

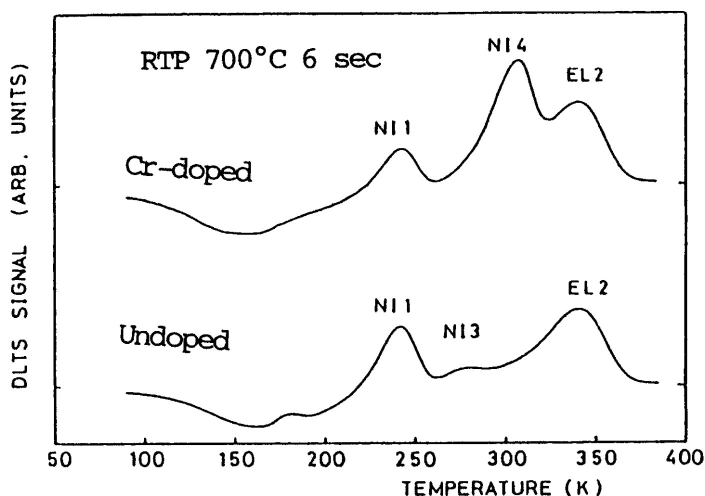


Fig.2-2. DLTS spectra of electron traps in RTP samples at 700 °C.

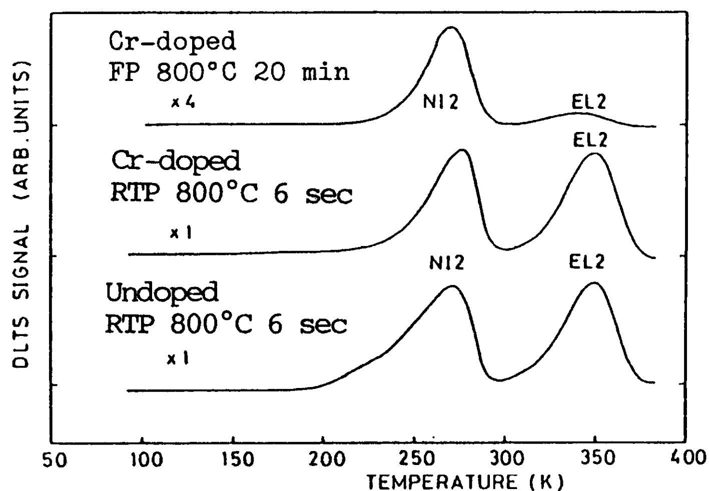


Fig.2-3. DLTS spectra obtained in FP and RTP samples at 800 °C.

Figure 2-3 shows the representative DLTS spectra for the samples after Si implantation and annealing at 800 °C. The traps NI1, NI3, and NI4 are annealed out, but the trap NI2 appears in RTP and FP samples at 800 °C. The dominant trap is NI2 or EL2 in the samples after Si implantation and RTP at 800 °C for 6 s. On the other hand, in FP samples at 800 °C for 20 min, the trap NI2 is the dominant deep level. This result is identical with that in RTP samples at 900 °C for 6 s. These results do not depend on whether Cr-doped or undoped substrates. DLTS signals for the trap EL2 in both FP samples on Cr-doped and undoped substrates are very small.

We observe a photoquenching effect[21] in the photocapacitance at liquid-nitrogen temperature in the RTP sample, as shown in Fig. 2-4, but did not in the FP sample, where the EL2 concentration is low. The energy level and capture cross section for EL2 in the present samples are slightly smaller than those for the trap labeled EL2, according to the trap labeling by Martin, Mitonneau, and Mircea[22] (E_c - 0.82 eV, 1.2×10^{-13} cm^2). Namely, EL2 in GaAs after Si implantation and RTP is one of the "EL2 family"[23] characterized by the photoquenching effect. The photoquenching effect has been attributed to a configurational instability, which was described with the help of configuration coordinate diagrams.[22] While this approach is helpful in visualizing the defect properties in an empirical way, the nature of the electron-lattice interaction, which provides the driving force for configurational change, is not well defined. Several attempts have been made to explain the existence of the metastable state by introducing a new atomic configuration for

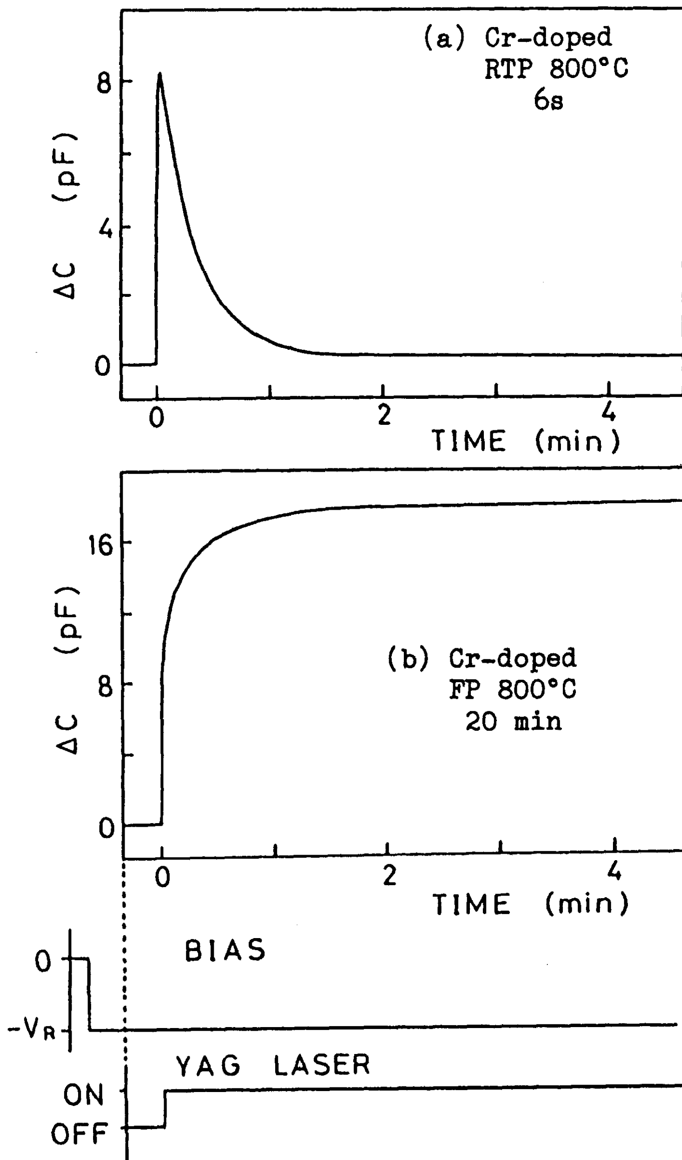


Fig.2-4. Photocapacitance signals for EL2 level after a direct electrical pulse under YAG laser illumination (1.17 eV) in (a) RTP sample and (b) FP sample.

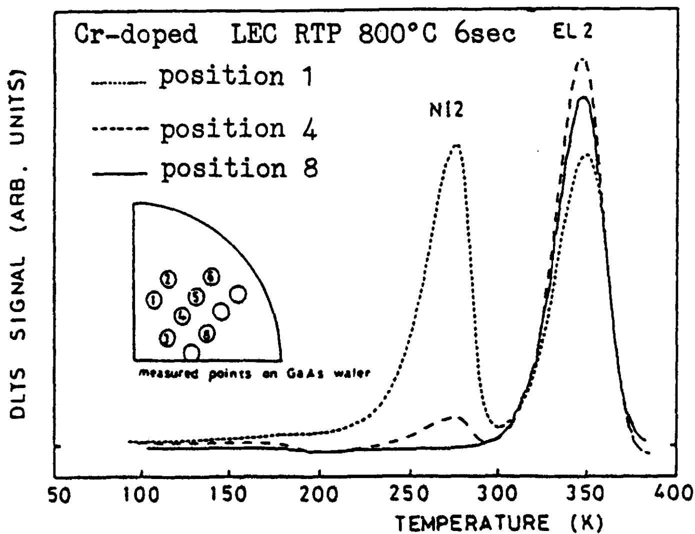


Fig.2-5. A spatial variation of DLTS signals across the Cr-doped GaAs wafer after Si implantation and RTP at 800 °C.

EL2.[23-25] Bourgoin and Bardeleben have suggested that the metastable behaviors can be understood without the need to introduce distorted atomic configurations.[26] The nature of the photoquenching effect will be able to be explained by the study of atomic structure of EL2.

The trap NI1 is observed in the Cr-doped and undoped samples, but not detected on all diodes (or all positions on a wafer). A spatial distribution of DLTS signals for the trap NI2 and the trap EL2 across the Cr-doped GaAs wafer after RTP at 800 °C is shown in Fig. 2-5. The inset in Fig. 2-5 shows the position of diodes on the quartered wafer. The variation of the trap EL2 peak height is not pronounced, but the variation of the trap NI2 peak height is notable. However the specified tendency of the spatial distribution of the trap NI2 is not observed. The above results for the trap NI2 and the trap EL2 is also true for case of undoped substrates. The energy level and capture cross section for the trap NI2 are listed in Table 2-I. The trap concentrations for the trap NI2 are also shown in Table 2-I. These trap concentrations for the trap NI2 are maximum values among the NI2 concentrations for measured diodes on the each RTP and FP samples, which are calculated from DLTS signals at the depth of ~ 0.2 μm, because of the variation of the NI2 concentration across the wafer.

The measured DLTS spectra of the trap NI2 are broader than a curve calculated from measured activation energy and the capture cross section. Four DLTS signals from discrete states can be separated from measured NI2 signal by means of curve fitting for a DLTS spectrum. These four DLTS peaks are labeled NI2a, NI2b,

NI2c, and NI2d, and are shown in Fig. 2-6, respectively. The energy levels and capture cross sections for these traps are listed in Table 2-II. The trap NI2 in Table 2-I coincides with the trap NI2a whose DLTS signal forms a main peak in the spectrum for the trap NI2. In all samples involving the trap NI2, the DLTS half width of whole NI2 signal is fixed at 27 K when the time constant is 152 ms. Therefore, relative intensities of DLTS signals for the traps NI2a - NI2d are constant among the samples investigated and the trap densities normalized by the NI2a concentration are shown in Table 2-II. This result supports the idea that the traps NI2a - NI2d are due to the same origin. The qualitative characteristics for the trap NI2 can be listed as follows. (1) The traps NI2a - NI2d are produced by Si

Table 2-II. Characteristics of the trap NI2a - NI2d separated from NI2 spectrum.

Trap	Energy level (eV)	Capture cross section (cm^2)	N_t/[NI2a]
NI2a	Ec - 0.55	5.1×10^{-15}	1.0
NI2b	Ec - 0.67	6.4×10^{-12}	0.065
NI2c	Ec - 0.60	1.4×10^{-12}	0.17
NI2d	Ec - 0.55	1.1×10^{-12}	0.066

implantation and FP or RTP above 800 °C. (2) The traps NI2a - NI2d are due to the same origin. (3) The spatial variation of the trap NI2 across the wafer is notable, but the specified tendency of the spatial distribution for the trap NI2 is not observed. (4) The concentration of the trap NI2 is comparable to the carrier concentration, occasionally.

Dhar and co-workers[3] have reported an electron trap H (Ec - 0.57 eV) in undoped LEC GaAs after Si implantation and RTP. The activation energy of this trap H is close to that of the main trap NI2a in NI2. However, the above characteristics (2) and (3) are different from the characteristics of the trap H. They have mentioned the concentration of the trap H follows the dislocation defect profile across the substrate and it is therefore considered that the segregation of implanted damage around dislocation forms electrically active defects after annealing. The characteristics (1) and (4) are similar to that of the trap H. Hence, it is considered that the trap H and the trap NI2 are not the same defect, but are similar to each other. The trap NI2 is related to an implantation induced damage, since NI2 trap is not detected in the rapid-thermal-processed Si-doped n-type LEC GaAs from 700 to 900 °C for 6 s, as reported previously.[19] The spatial variation of the trap NI2 across the wafer is related to the variation of defects across the original substrate. Therefore, it is reasonable to consider that the NI2 trap is created by the association of defects in the original substrate and implantation induced damage during high-temperature (>800 °C) annealing. It seems that the difference in characteristics between the trap NI2 and the trap H corresponds to the difference of defects between the substrate used by us and by Dhar and co-workers.[3] On account of the characteristics (3) and (4), it is possible that the trap NI2 and the trap H cause an extraordinary characteristic of devices such as FET. However, as the above discussion, it is probably possible that this subject is settled by improvement in a perfection of a bulk crystal.

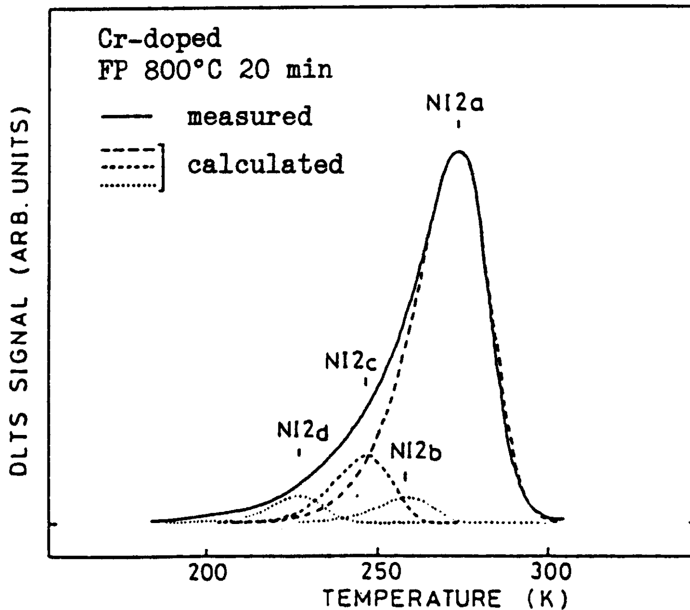


Fig.2-6. DLTS spectra of the trap NI2 and calculated signals NI2a-NI2d separated from the NI2 signal.

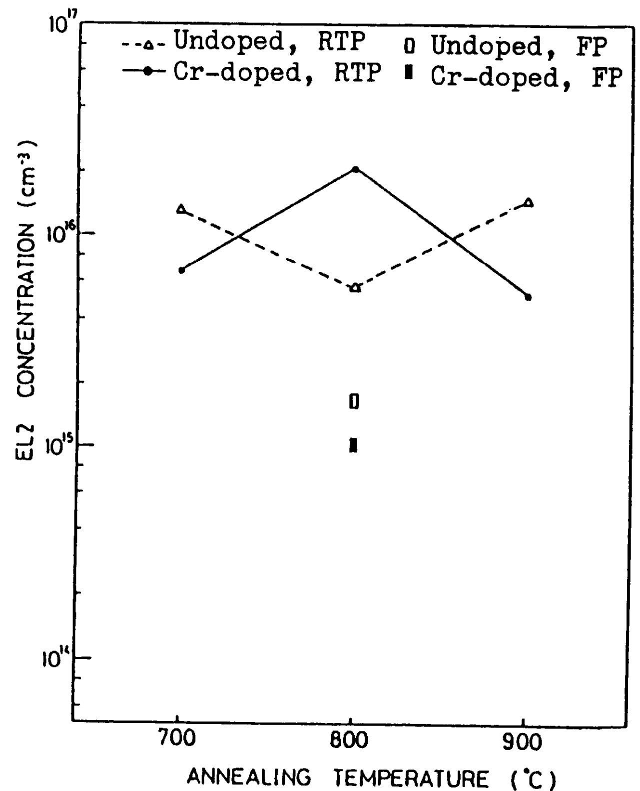


Fig.2-7. The dependence of the trap EL2 concentration on RTP temperature.

2.5 The thermal stability of the trap EL2

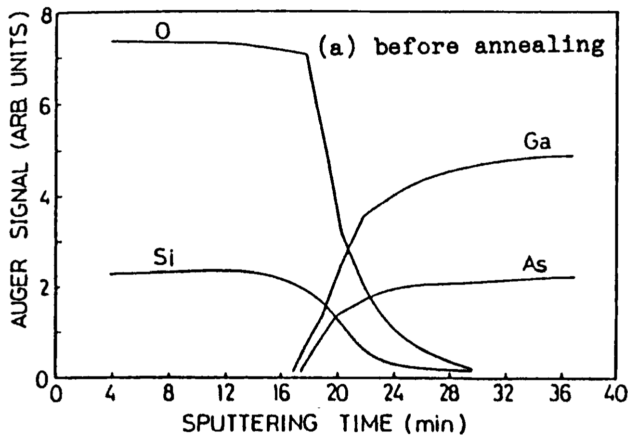
The variations of the trap EL2 concentration with RTP temperatures are shown in Fig. 2-7 for Cr-doped and undoped substrates, respectively. These EL2 concentrations are the mean values listed in Table 2-I. The EL2 concentration in RTP samples is about 10^{16} cm^{-3}, while that in FP samples is about 10^{15} cm^{-3}. It can be believed that the low EL2 concentration in FP samples on the undoped substrate is due to the out-diffusion of it similarly to bulk n-type GaAs.[27] Figures 2-8(a), 2-8(b) and 2-8(c) show the depth profiles of Auger signals (ULVAC-PHI ESCA/AES/SIMS 558A) for Ga, As, O, and Si for SiO_2/GaAs

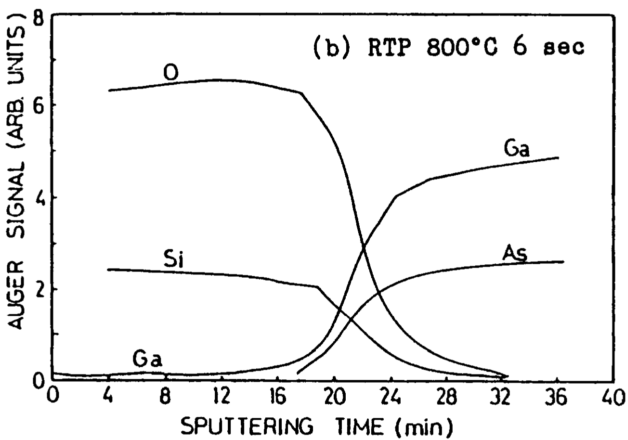
structures before annealing, after RTP at 800 °C for 6 s and after FP at 800 °C for 20 min, respectively. It is observed that Ga diffuses into SiO_2 film even for RTP samples as well as for FP samples in spite of its short annealing time. In Figs. 2-8(a) and 2-8(b), comparatively abrupt SiO_2/GaAs interfaces are found for these components. An interface is not abrupt in Fig. 2-8(c). It is expected that a transition region is formed between SiO_2 and GaAs by FP,[28] and the Ga and As diffuse into this transition region from the bulk GaAs in FP sample. The contribution of an excessive As to the formation of the trap EL2 has been reported.[29] The result of the above Auger depth profiling gives suggestions about the origin of the difference of the EL2 concentration between RTP samples and FP samples, as follows. It is expected that the Ga out-diffusion in both RTP and FP samples and the formation of the transition region at the SiO_2/GaAs interface in FP samples occur, so the difference of the EL2 concentration between RTP samples and FP samples can correspond to the existence of the transition region. Some Ga vacancies (V_{Ga}) formed by the Ga out-diffusion produce Si donors in the Ga lattice sites. Other V_{Ga}, As interstitials (As_i) and antisite As (As_{Ga}) must be related to the formation of the trap EL2. In the FP samples the Si donors in the Ga lattice sites are the same concentration as that in the RTP samples, as seen from Fig. 2-1. On the other hand, a large amount of As contributes to the formation of the transition region in FP samples, therefore excessive As in the implanted and furnace annealed layers is likely insufficient in comparison with that in RTP samples. Hence, it is believed that the decrease of the trap EL2 in the FP

samples must be related to the decrease of excess As atoms. Namely, the interaction between SiO_2 encapsulant and GaAs is smaller for RTP than that for FP. Therefore, the surface of GaAs is relatively stable during RTP. This stability is merits of the RTP method over the FP method in regards to GaAs device fabrication.

In the Si-doped molecular-beam epitaxial (MBE) n-type GaAs layers, which are free from the EL2, we have reported that the trap EL2 is produced by RTP at 800 °C.[30] Furthermore, we have the close relation between the EL2 concentration and distance of the measured diodes from edge of the RTP sample. The EL2 concentration increases by about two orders of magnitude for the RTP sample toward the edge from the center, that is, a larger amount of EL2 is produced near the edge of the sample by RTP.

Figure 2-9 shows that the EL2 concentration at $\sim$0.2 μm below the surface across the sample after Si implantation and RTP at 800 °C using the quartered one of an undoped substrate, where the distance from the edge x is the smallest one of each measured diode from the edge of the quartered wafer on the undoped substrate. However, the peculiar spatial variation of the trap EL2 concentration is not observed over the measured range of x. Furthermore, the EL2 concentration have been plotted toward the radial direction across the 2-in. wafer after Si implantation and RTP. However, a symmetry or peculiar shape of the EL2 concentration along <110> and <100> direction, the so-called W shape,[31] is not found in a range of 7 - 21 mm from the center of the wafer. The spatial variation of the EL2 concentration across





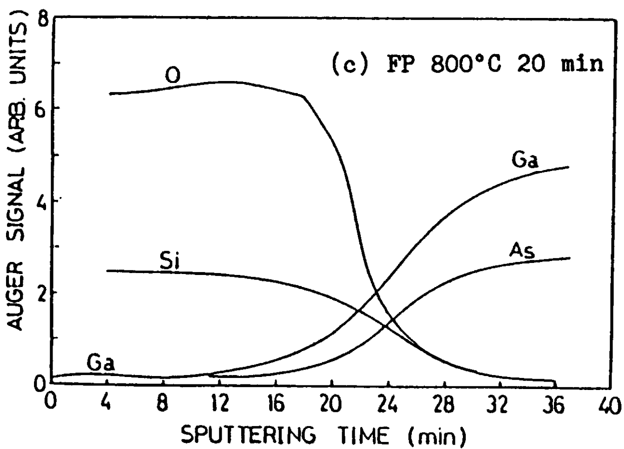


Fig.2-8. Auger depth profiles for Si-implanted GaAs (a) before annealing, (b) after RTP at 800 °C for 6 s, and (c) after FP at 800 °C for 20 min.

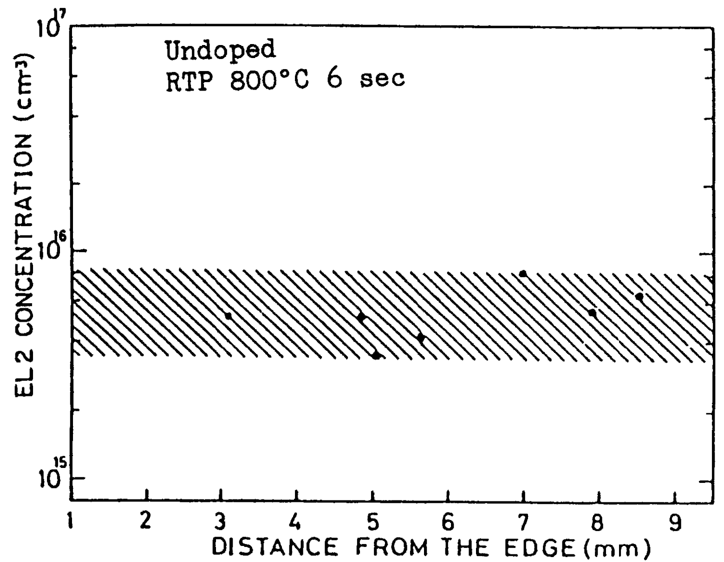


Fig.2-9. Spatial distribution of the EL2 in Si-implanted layer activated by RTP on the undoped substrate.

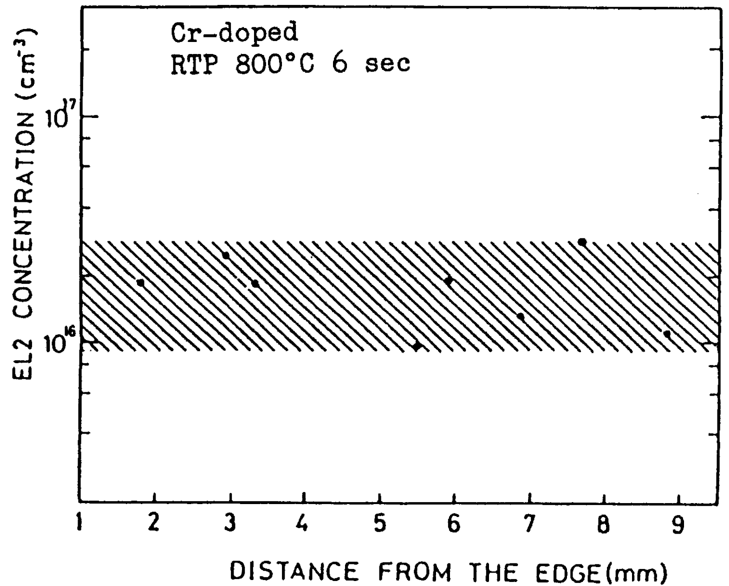


Fig.2-10. Spatial distribution of the EL2 in Si-implanted layer activated by RTP on Cr-doped substrate.

the 3-in. wafer has been optically mapped by Dobrilla and Blakemore[32] in the LEC undoped and In-doped SI GaAs wafers. These mapping show the W-shaped spatial distribution for the trap EL2. It seems that the shape of spatial distribution for EL2 after Si implantation and RTP does not correspond to that of SI GaAs measured by Holmes and Chen[31] over the measured range of the radial distance. It has been reported that the formation of the trap EL2 is related with ion implantation.[33,34] Probably, the EL2 concentration in the RTP sample is sum of the concentration of the trap EL2 caused by the Si implantation and RTP, and that existing in the substrate, so the W-shaped spatial distribution of the EL2 concentration is disturbed by Si implantation and RTP. Therefore, we believed that the EL2 concentration is not determined mainly by the EL2 concentration in the original substrate. The variation of EL2 concentration likely depends on the conditions of Si implantation. However, in a very low-dose condition the EL2 concentration may be determined on RTP condition or the EL2 concentration in the as-grown substrates, since in this condition the EL2 concentration by ion implantation is relatively low.

Figure 2-10 shows the spatial distribution of EL2 for the Cr-doped sample. The EL2 concentration in Cr-doped LEC SI substrates has not been measured accurately. The role of the trap EL2 in Cr-doped SI substrates is different in semi-insulating mechanism from that in undoped SI substrates. However, we believe that the phenomenon for production or diffusion of the trap EL2 in Cr-doped samples during Si implantation and RTP or FP is the same as the phenomenon in

undoped samples. Therefore, it seems that the distribution of the trap EL2 for Cr-doped samples is determined by the same origin in the undoped RTP sample as discussed earlier.

2.6 Summary

Deep level traps present in Si-implanted and rapidly thermal-annealed GaAs have been characterized with DLTS. It is found that the trap NI2 (Ec - 0.55 eV) or EL2 (Ec - 0.78 eV) is the dominant electron trap in RTP samples above 800 °C, but in FP samples at 800 °C for 20 min, the EL2 concentration is decreased and the trap NI2 is dominant. The notable spatial variation of the NI2 concentration is observed across the wafer. It is proposed that the trap NI2 is created by the association of defects in the original substrate and implantation induced damage during high temperature (>800 °C) annealing. On the other hand, the peculiar spatial distribution of the EL2 concentration is not observed across the RTP sample. Furthermore, the dependence of the EL2 concentration on RTP temperatures is not observed in Si-implanted layer.

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III. EFFECTS OF RAPID THERMAL PROCESSING ON DEEP LEVELS IN MOLECULAR-BEAM-EPITAXIAL GaAs

3.1 Introduction

RTP is applied for the activation of ion implants as a simple and powerful technique, and previously has been reported to have several advantages over conventional furnace processing for fabrication of GaAs metal-semiconductor field effect transistors.[1] Furthermore, in recent years, it has been known that RTP is suitable for the fabrication of high-speed devices,[2] and significantly improve the crystalline quality of GaAs grown on Si substrates.[3] Therefore, it is an important subject to characterize the rapid-thermal-processed epitaxial layers, with the advance of epitaxial growth such as molecular-beam epitaxy (MBE) and metalorganic chemical vapor deposition (MOCVD).

We have reported that RTP produces electron traps EL2 (E_c - 0.82 eV) and N1 (E_c - 0.72 eV) in MBE n-type GaAs layers,[4] and an electron trap ED1 (E_c - 0.26 eV) in LEC n-GaAs.[5] Kuzuhara and Nozaki[6] have reported the trap EN1 (E_c - 0.20 eV) produced by RTP in bulk n-type GaAs. These results for the RTP samples have been in contrast with the results for FP samples at the same temperature, that is, the electron traps ED1 and EN1 have not been produced by FP.[4-6] In addition to the production of these traps, the spatial variation of the EL2 concentration across the RTP layer has been observed.[4]

In this chapter, I will discuss the electron traps present in RTP MBE n-type GaAs layers by DLTS. MBE GaAs layers before

RTP are free from the electron trap EL2, which electrically plays a crucial role in undoped semi-insulating GaAs. In particular, we have tried to clear spatial distributions of the trap EL2 and N1 produced by RTP.

3.2 Experiment

The epitaxial GaAs layers with thickness of 2 μm and doped with Si to about 10^{17} cm^{-3} were grown by MBE on Cr-doped horizontal Bridgman (HB) semi-insulating (100) GaAs substrates in a V. G. Semicon V80H system. The substrate temperature, the growth rate, and the As_4/Ga flux ratio was maintained at 600 °C, 1 μm/h, and 3, respectively. These GaAs samples were cleaved in a few pieces and the individual pieces were sandwiched by two GaAs wafers without any encapsulant, so that the epitaxial layers face GaAs wafers (proximity capping method). These were placed in a quartz tube and irradiated by a cylindrical array of tungsten halogen lamps in flowing N_2. RTP conditions and labels of layers are listed in Table 3-I. For comparison, FP was performed at 800 °C for 15 min with the proximity capping technique. This sample is labeled FP-800. The layers labeled OP-800L, M, N, and H were made by RTP in order to investigate the heating rate dependence of the trap EL2 concentration. For the "CL-800" layer, RTP was performed at 800 °C for 6 s with the cleaved edge around the sample kept in contact with GaAs pieces in order to improve the temperature nonuniformity and to prevent the thermal stress during RTP (as seen from the inset in Fig. 3-

Table 3-I. RTP and FP conditions.

Sample	Temperature (°C)	Hold time (s)	Heating rate (°C/s)	Edge of the sample
OP-700	700	6	50	open
OP-800	800	6	50	open
OP-800L	800	6	10	open
OP-800M	800	6	30	open
OP-800N	800	6	50	open
OP-800H	800	6	70	open
OP-800-20	800	20	50	open
OP-900	900	6	50	open
CL-800	800	6	50	close
FP-800	800	Furnace 20 min	--	open

6), but for the layers "OP-number" and "FP-800", heat treatment was performed with the edge around the sample open (see the inset in Fig. 3-5).

DLTS measurements with a bipolar rectangular weighting function[7)] were made on Au Schottky-barrier diodes deposited by vacuum evaporation on these processed epitaxial layers. The ohmic contacts were made on the same surface by alloying Au-Ge.

3.3 Defect production by RTP

Figure 3-1 shows typical DLTS spectra for the RTP samples OP-800H, OP-900, and the as-grown samples. In as-grown MBE GaAs, three electron traps are observed. These traps are commonly present in as-grown MBE GaAs layers, and identified with traps M1, M3, and M4 as reported by Lang and co-workers[8)] and others.[9-]

[11] The thermal activation plots of electron emission for M1, M3, and M4, and the lines by a least-squares fit are presented in Fig. 3-2, where the results reported by DeJule and co-workers[11] are also shown as broken lines. In Fig. 3-2 our result for the trap M1 is slightly different from the result reported by DeJule and co-workers.[11] This difference is ascribed to the effect of the field-assisted electron emission, since the thermal emission rate of an electron for M1 is changed by the quiescent reverse bias during DLTS measurement.[10]

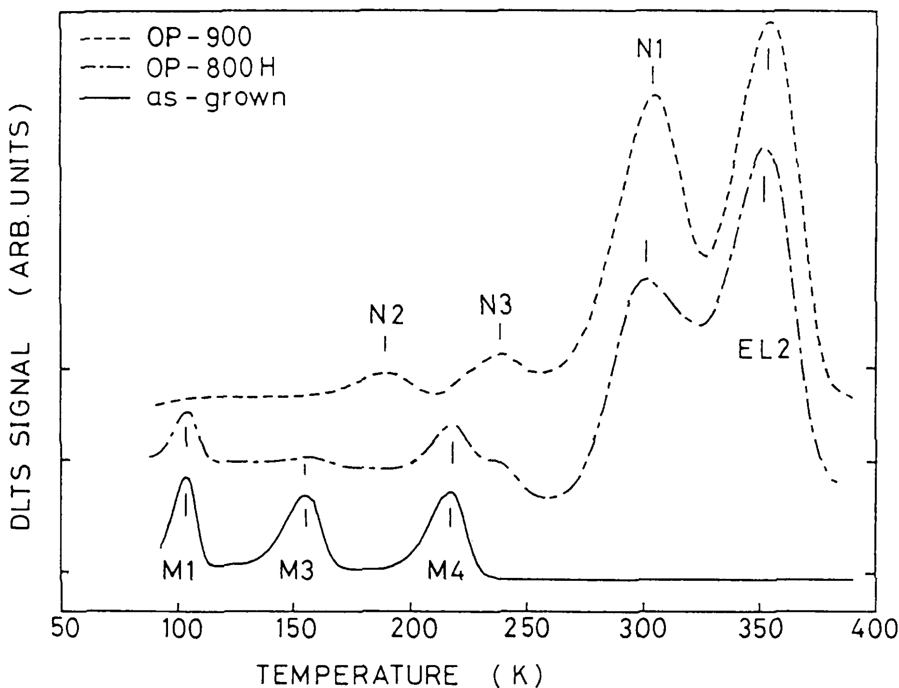


Fig.3-1. DLTS spectra for the rapid-thermal-processed MBE GaAs at 800 and 900 °C and the as-grown one.

On the other hand, five electron traps are observed in RTP samples at 800 °C,[4] which are also observed in RTP 700 °C samples. Three electron traps in the low-temperature side of a DLTS spectrum for RTP sample at 700 and 800 °C are the same as those in the as-grown MBE GaAs layers, and two electron traps in the high-temperature side of the spectrum are produced by RTP,

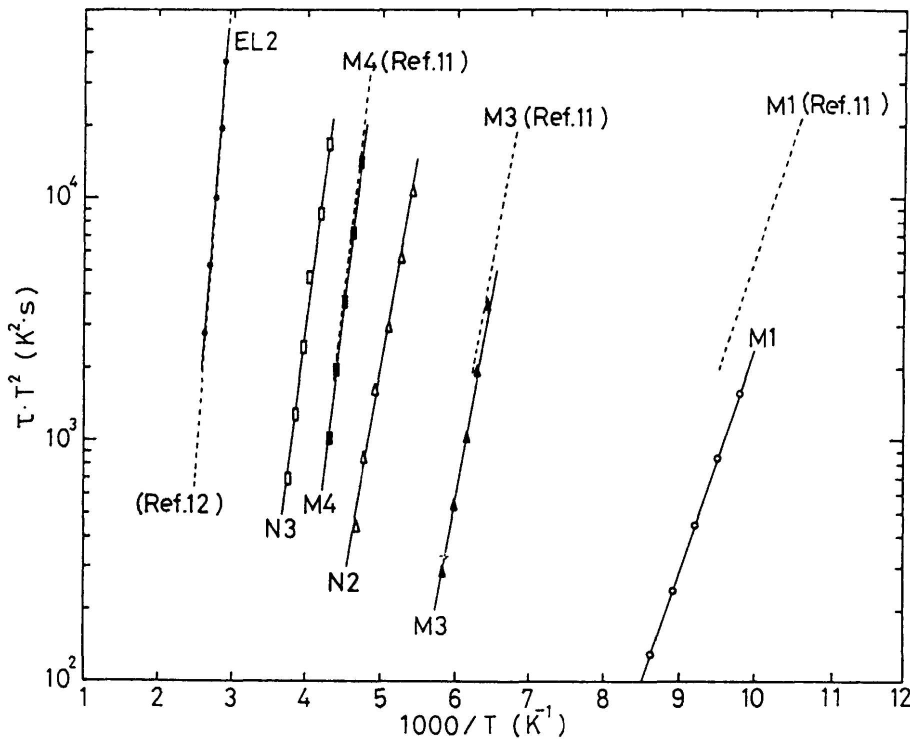


Fig.3-2. Arrhenius plots of $T^2\tau$ for M1, M3, M4, N2, N3, and EL2. The broken lines are extracted from data reported in Refs. 11 and 12.

and dominant in RTP samples. One of these two electron traps has been identified with the deep donor EL2,[4] from the comparison of the reported temperature dependence[12] of the EL2 as seen from Fig. 3-2. Furthermore, we observed a photoquenching effect in the photocapacitance[13] in the RTP sample. Another one of them is named N1. Figure 3-1 also represents the DLTS spectrum for the OP-900 sample. Electron traps termed N2 and N3 are observed in this sample besides the traps N1 and EL2, but the traps M1, M3, and M4 disappear. The energy levels and capture cross sections for these traps M1, M3, M4, N1, N2, N3, and EL2 are listed in Table 3-II. These values are calculated from the Arrhenius plots in Fig. 3-2 assuming that the capture cross sections are independent of temperatures.

The DLTS peak temperature and signal intensity for the trap N1 changes as the DLTS measurements are repeated. In addition, the peak position and peak height for N1 depend on the measured

Table 3-II. Characteristics of electron traps in rapidly thermal-processed MBE n-GaAs.

Trap	Energy level (eV)	Capture cross section (cm^2)
M1	Ec - 0.18 ± 0.02	3.2×10^{-15} (±∿150%)
M3	Ec - 0.33	7.6×10^{-14}
M4	Ec - 0.51	5.8×10^{-13}
N1	Ec - 0.5 ∿ 0.7	$2 \sim 100 \times 10^{-15}$
N2	Ec - 0.36	3.0×10^{-15}
N3	Ec - 0.49	1.08×10^{-14}
EL2	Ec - 0.82	1.30×10^{-13}

RTP layers and these variation are also observed across each one of the RTP layers. This variation of N1 signal is attributed to temperature induced, bias-controlled metastability. Hence, the parameters of this level is not determined with accuracy. The extent of the energy level and capture cross section is shown in Table 3-II. Buchwald, Johnson, and Trombetta[14)] have reported that the metastable defect, labeled M2, with an emission activation energy of 0.64 eV is observed in MOCVD layers after RTP at 900 °C and above with Si_3N_4 encapsulant. The bias-controlled metastability of the defect is explained by the transformation between defect configurations which are driven by Coulombic attraction and is completely reversible. These characteristics and models of the configurational transformation kinetics were discussed in detail in Refs. 15 - 17. The trap N1 is consistent with the trap M2 reported by Buchwald, Johnson, and Trombetta, as regards "metastability" and the range of the

activation energy. However, the trap N1 is different from the metastable defect M2 with regard to the consecutive variation of DLTS peak temperature for the N1 signal. This may be explained as follows. The N1 signal is caused by a defect which has several configurations and of which the structures can electrically change, that is, multistable or defect clusters.

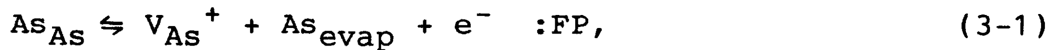
The energy level for the trap N3 is the same as that for the trap ED2 reported by Katayama et al.[5] However, the capture cross section for N3 is larger than that for ED2 by about one order. It seems that the production of the trap N2 and N3 are not due to the diffusion of defects or impurities from the substrate, since the energy levels and the capture cross sections of the traps N2 and N3 are inconsistent with those of the traps in HB GaAs substrates.[18] Hence the traps N2 and N3 are new electron traps induced by RTP at 900 °C and related to inherent impurities or defects which are absent from bulk GaAs.

3.4 Annealing behavior of traps by RTP

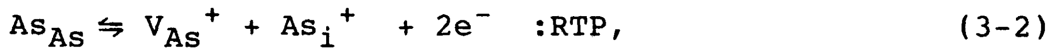
Figure 3-3 shows the variations of the traps M1, M3, M4, N2, and N3 by RTP for 6 s. The traps M1 and M4 are stable during RTP at 700 °C, but the concentration of these decrease with the RTP temperature above 800 °C and are below the detection limit of DLTS after RTP at 900 °C. It is noted that the decrease of the traps M1 and M4 concentration is coincident with the increase of the N2 and N3 concentration. The concentrations of the traps M1 and M4 in the as-grown layer are nearly equal to those of the traps N2 and N3 in the RTP layer at 900 °C. The production of

traps N2 and N3 in the RTP layer at 900 °C. The production of the traps N2 and N3 may be related to the annealing of the traps M1 and M4 through the transform between them.

It has been reported that the formation of native deep levels are dependent on the surface stoichiometry during MBE growth.[19] The origins of M1 and M4 may be related to arsenic vacancies (V_{As}). The following reactions with respect to As evaporation near the surface region during high-temperature annealing was presented in Ref. 6:



$$As_{As} \leftrightharpoons V_{As}^{+} + As_{evap} + e^{-} \quad :FP, \qquad (3\text{-}1)$$



$$As_{As} \leftrightharpoons V_{As}^{+} + As_{i}^{+} + 2e^{-} \quad :RTP, \qquad (3\text{-}2)$$

where As_i are arsenic interstitials and As_{evap} is evaporated As. If the origin of the trap M1 and M4 is V_{As} by itself, the trap M1 and M4 must increase during FP according to reaction (3-1). However, it is observed that the concentrations of M1 and M4 also decrease by FP at 800 °C for 15 min. Therefore, it is not reasonable that the origin of M1 and M4 is the V_{As} by itself. Blood and Harris[10] have suggested that these deep levels are related to defect-unknown impurity complexes involving V_{As}. Assuming that the origins are V_{As}-impurity complex defects, the decrease of M1 and M4 concentration by RTP is related to the production of the traps N2 and N3 through the formation reaction of arsenic divacancy-impurity complex defects which is possible during RTP and FP according the reactions (3-1) and (3-2). A similar connection between EL2 or N1 and M1 or M4 cannot be made, since a larger amount of the trap EL2 is produced by RTP at 700 °C and M1 and M4 do not decrease during RTP at 700 °C.

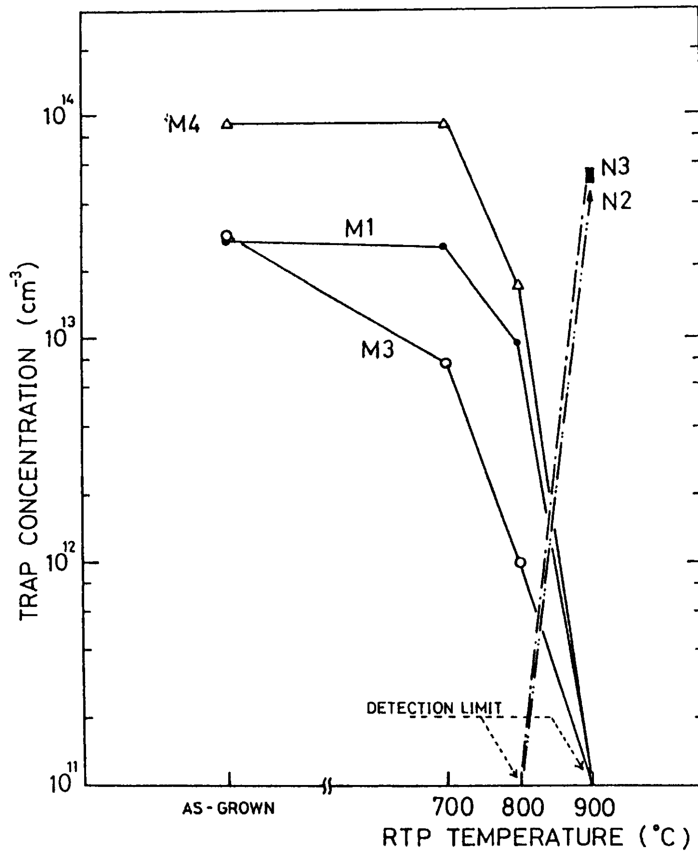


Fig.3-3. RTP temperature dependence of the trap concentration for M1, M3, M4, N2, and N3.

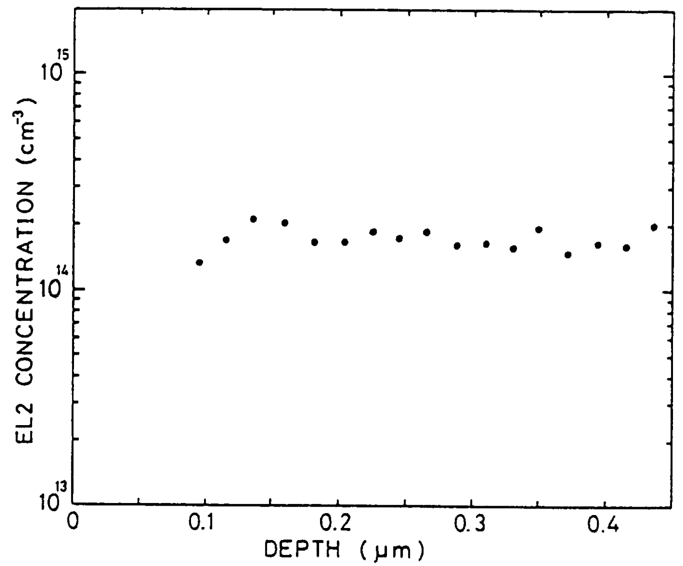


Fig.3-4. Depth profile of the trap EL2 produced by RTP at 800 °C for 6 s.

3.5 Spatial variations of RTP-induced trap EL2 and N1 concentration

The depth profile of the trap EL2 in the CL-800 is shown in Fig. 3-4. The EL2 trap profile is flat in the measured depth range. The similar depth profiles of the trap EL2 are observed in the other RTP layers. This suggests that the production of EL2 in the MBE layer is not due to the in-diffusion of defects from the surface and the out-diffusion of defects from the substrate. It is difficult to obtain the profiles of the trap N1

because of the bias-controlled metastability.

The spatial variations of M1, M3, M4, N2, and N3 traps across the GaAs layers are not pronounced. On the other hand, the variations of the EL2 and N1 traps across the RTP layers are notable. Figure 3-5 represents the spatial variation of the EL2 trap across the OP-800 layer along the <100> and <110> directions. These trap concentrations are calculated from DLTS signals at the depth of $\sim$0.2 μm below the surface. This peculiar shape of the EL2 trap is generally found in the RTP layers with the edge around it open. Schottky-barrier height from the forward I-V characteristics is high (>0.8 eV) across the OP-800H sample. In the FP-800 layers the EL2 concentration is lower compared to that for the RTP layers and is approximately uniform over the surface.[4] In the conventional furnace, the radiation rate balances between the furnace and sample over all radiating surfaces of the sample, that is to say, if the flux of heat transfer from GaAs to surrounding ambient is negligible, the system is in thermal equilibrium. On the other hand, the RTP system is in nonequilibrium and has a temperature distribution. The higher temperature gradient occurs across the films by heat radiation from the edge during RTP, but the temperature gradient decreases near the center of the sample.[20] The larger concentration of the trap EL2 is observed near the edge of the sample and the minimum lies between the center and the edge of the sample, in a ward, a W-shaped distribution. Therefore, it is found that this peculiar spatial distribution of EL2 in "OP layers" is not consistent with that of the temperature across the

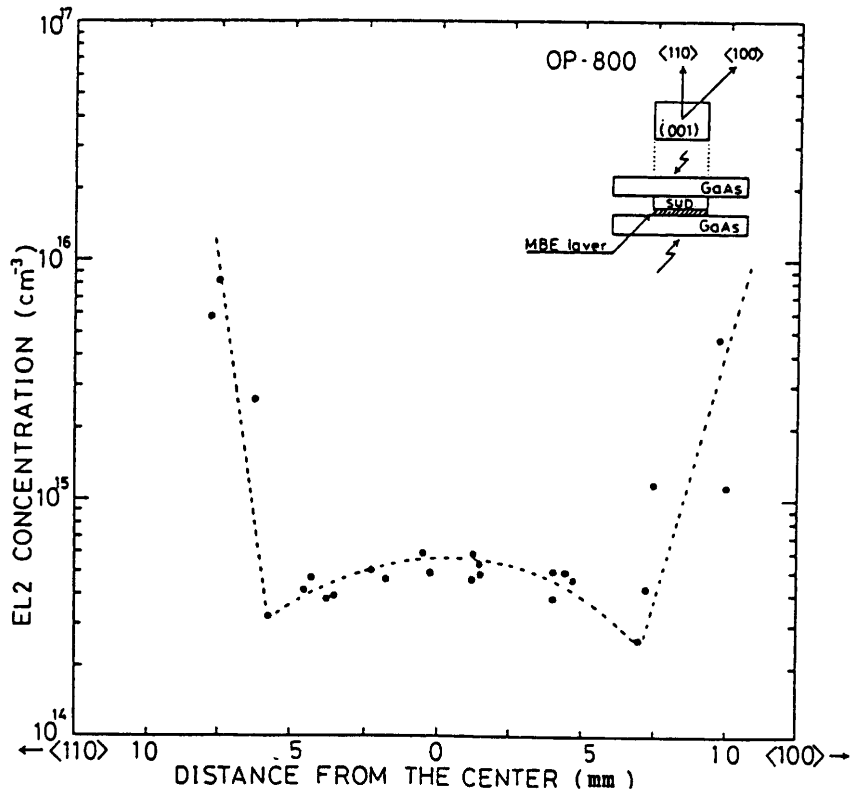


Fig.3-5. Spatial distribution of the trap EL2 in the layer OP-800.

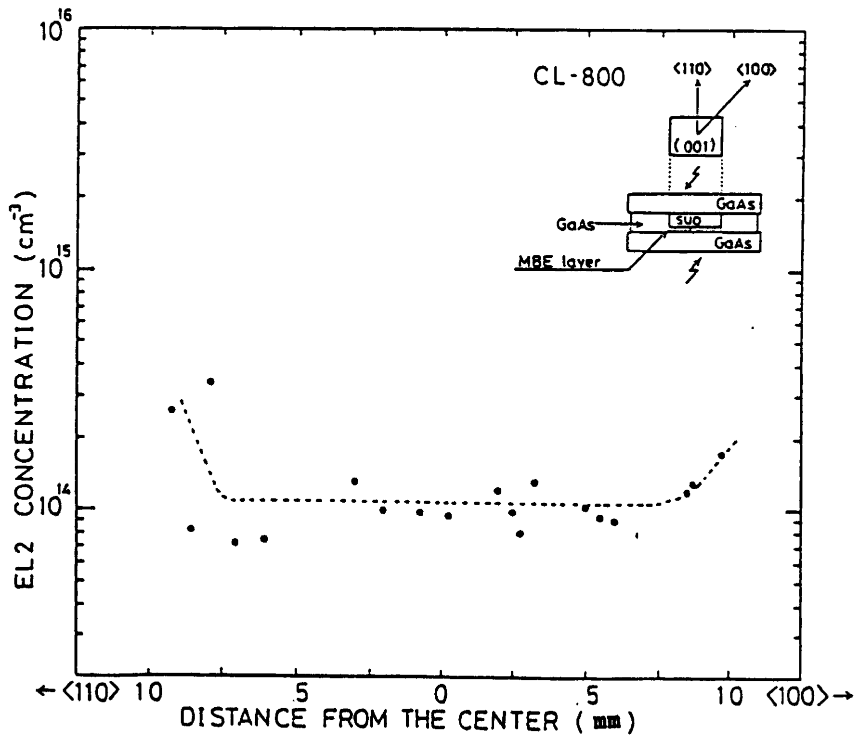


Fig.3-6. Spatial distribution of the trap EL2 in the layer CL-800.

layer, since the temperature distribution is not a W-shaped distribution.

We observed the W-shaped distribution of EL2 across the RTP layer through the careful experiment for the large number of diodes per area. It was suggested that the spatial variations of EL2 concentration in the RTP layer were consistent with those of the thermal stress.[4] The thermal stress is induced by the temperature gradient across the sample and was larger, especially near the edge.[20] On the other hand, the temperature gradient is small through the sample thickness, since the sample is thin. As a result, the thermal stress is uniform through the thickness. Therefore, the depth profiles of the trap EL2 are also consistent with those of the thermal stress.

RTP of GaAs wafers results in crystallographic slip networks. The use of guard rings has been found to be very effective in reducing slip line.[21] The slip generation is caused by the stress developed as a result of temperature nonuniformity across the wafer.[20] Therefore, it is expected that the use of guard rings is effective in reducing thermal stress. We used the guard ring for RTP as seen from the inset (cross section) in Fig. 3-6 in order to improve the temperature nonuniformity across the layer during RTP. For the layer CL-800, the EL2 concentration is smaller and its nonuniformity is improved in comparison with that for the OP layers. It is considered that the uniformity of the EL2 concentration is due to the absence of thermal stress. However, the trap EL2 remains in the CL-800 layer at the concentration of 10^{14} cm^{-3}, which is of the same order as those in GaAs grown by MOCVD[22] or vapor-phase

epitaxy.[23] Therefore, it is concluded that the thermal stress enhances the production of the trap EL2, but the origin of the production is not only thermal stress. Various possible mechanisms are considered as follows to account for the stress enhanced production of EL2. (1) The formation of a large number of As interstitials (As_i) by stress furthers the production of EL2 [$(As_i)_x$-As_{Ga} model[24,25]]. (2) Stress causes Ga vacancies (V_{Ga}), and V_{Ga} interacts with the arsenic to create the antisite defect (V_{As}-As_{Ga},[26] divacancy-As_{Ga} model[27]). (3) Stress causes nonuniform electric fields and the arsenic preferentially migrates to locations of highest field.[28] (4) The elastic field of a dislocation that exists in the MBE GaAs layer[29] is deformed by extrinsic thermal stress, and the thermal stress-assisted precipitation of arsenic on dislocation.[30] This excess arsenic on the dislocations is related to the formation of EL2.

A plastic flow will occur in those regions of the sample where the thermal stress is larger than the yield stress.[31] Hence, the distribution of a crystallographic slip is not expected to be a W-shaped pattern. The spatial variation of the EL2 concentration in MBE GaAs after RTP is not due to the effect of plastic deformation.

Figure 3-7 shows the EL2 trap concentrations as a function of heating rate. These EL2 concentrations were measured in the layers OP-800L, M, N, and H in Table 3-I. In OP-layers, since the EL2 concentration distributes across the layer, the minimum concentration, which corresponds to the bottom of the W-shaped pattern, and the concentration at the center of these layers are

both presented in Fig. 3-7. The minimum value of the W-shaped pattern is the EL2 concentration which is expected not to be affected by a thermal stress, and the concentration at the center of the layer is affected by a thermal stress. For the layers OP-800-20 (RTP 800 °C, 20 s, 50 °C/s) and FP-800, the EL2 concentration is also shown in this figure for reference. The minimum EL2 concentration in OP-800-20 is larger than that in OP-800N (RTP 800 °C, 6 s, 50 °C/s) by about three times. Therefore, it is expected that the time to reach the dynamical equilibrium in the formation reaction for EL2 is longer than 6 s. It is noted that the extent of this time is approximately consistent with the time to reach the equilibrium in a formation reaction of EL2 proposed by Wada and Inoue.[24]

The heating rate dependence of the EL2 concentration is similar to that of the electron trap EN1 reported by Kuzuhara and Nozaki[6] suggesting that the trap EL2 may be produced by the same origin for the trap EN1. However, the DLTS signals for EN1 and ED1 produced in bulk GaAs by RTP[5,6] is absent from any DLTS spectrum in rapid-thermal-processed MBE GaAs layers. This result indicates that En1 and ED1 relate to native defects or impurities in bulk GaAs. The remarkable difference between MBE and bulk grown GaAs before RTP is whether the EL2 trap is present or not. Katayama and co-workers[5] have suggested that the trap ED1 seems to correspond to defects related to As_i. If the formation of EL2 is also related to the existence of As_i, the formation of EL2 and ED1 have a close connection with each other, and probably ED1 is more readily produced in LEC GaAs than MBE GaAs. Because in LEC GaAs the EL2 and excessive As_i concentrations are already large

before RTP. On the other hand, according to the model of Kuzuhara and Nozaki,[6] EN1 is created at the expense of EL2, and it is hardly formed in MBE GaAs which is free from EL2 before RTP. Therefore, it seems that our present results (the absence of EN1 and ED1 from RTP MBE GaAs) are not inconsistent with previous results given in Refs. 5 and 6.

Figure 3-8 shows the spatial variation of the N1 concentration across the OP-800 layer along the <100> and <110> directions. In case of the low concentrations of an N1 trap, the DLTS signal for N1 is convoluted by the signal for EL2, and the

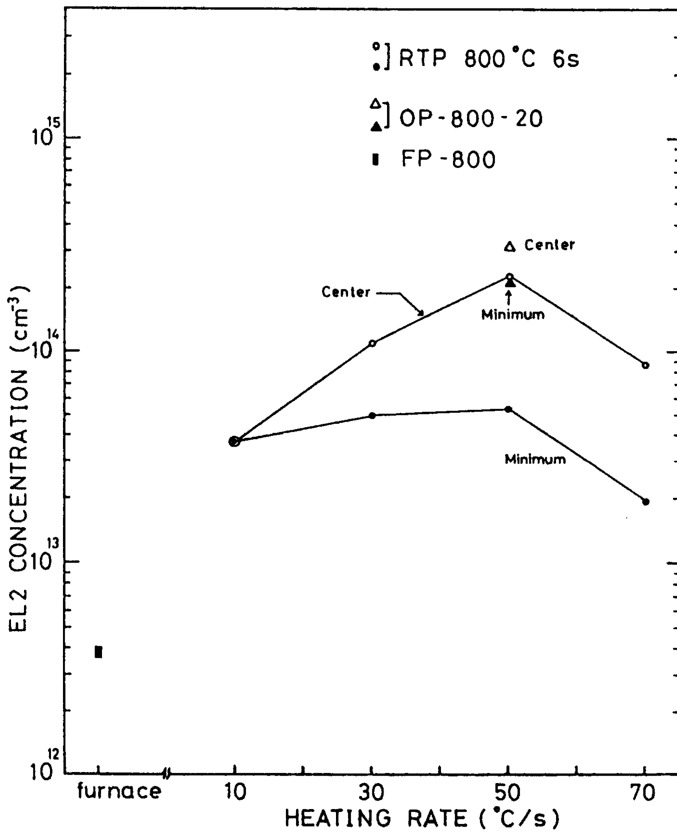


Fig.3-7. EL2 concentrations as a function of heating rate.

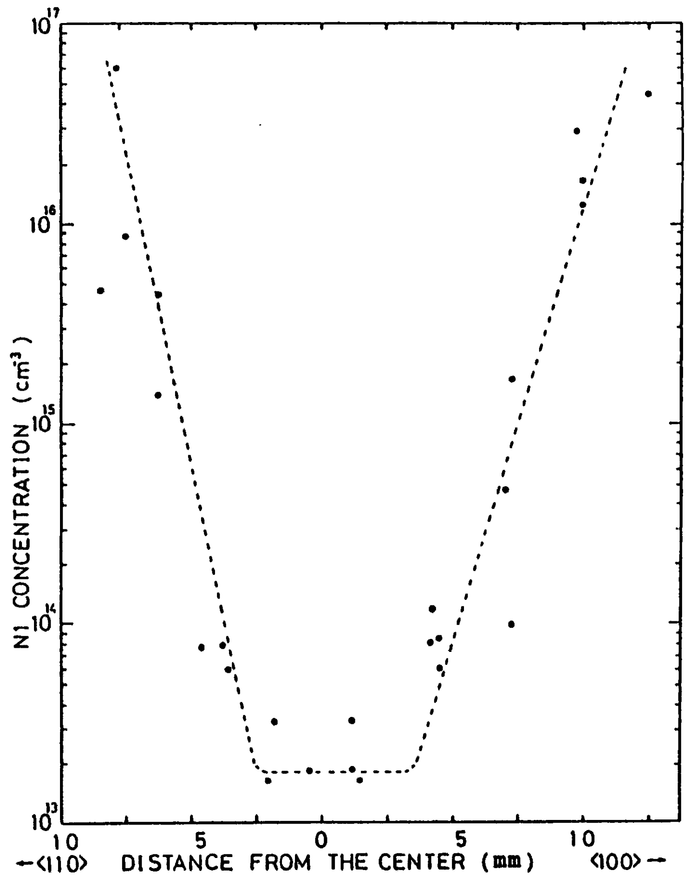


Fig.3-8. Spatial distribution of the trap N1 in the sample-OP-800.

uncertainty in the DLTS signal intensity yields an experimental error for the N1 concentration. For that reason the distribution of N1 is uncertain near the center of the sample, but it seems that the distribution of N1 is similar to that of EL2. The N1 trap is absent from the CL-800 and FP-800 layers. It is considered that N1 is hardly produced by a stress-free condition in constant with EL2.

3.6 Analysis of the thermal stress in the GaAs wafers during RTP

A. Temperature distribution

To verify the correlation of the EL2 distribution with a thermal stress distribution, the temperature and thermoelastic stress components during RTP are calculated. In RTP, the cooling of the sample occurs essentially by radiation. As a consequence, differences in heat radiation by different regions of the sample can give rise to thermal gradients, thus, for instance, the edge of the wafer becomes cooler than the central region because of the comparatively higher radiation. In spite of the good uniformity of the energy supply over the sample surface and the small temperature gradient through the sample thickness, thermal stress can be produced by the radial, or in-plane temperature gradient.

The trap EL2 is almost produced by RTP during hold time at maximum temperature. Therefore, the steady-state temperature distribution is calculated at the maximum temperature attained during RTP. we suppose that the wafer is free and heat is

supplied at a rate Q per unit time per unit area by a light to both surfaces of the wafer. The wafer loses heat by radiation toward the ambient. The thermal conduction is approximately isotropic. In this case the condition $h \ll a$ (h: thickness, a: wafer radius) allows a further simplification, i.e. the thin plate approximation. In this scheme, the heat flow problem is discussed in two dimensions only. The schematic diagram of the uniform irradiation of a free wafer and x-y coordinates are given in Fig. 3-9. The temperature distribution T(x,y) satisfies the equations (3-3a) and (3-3b).

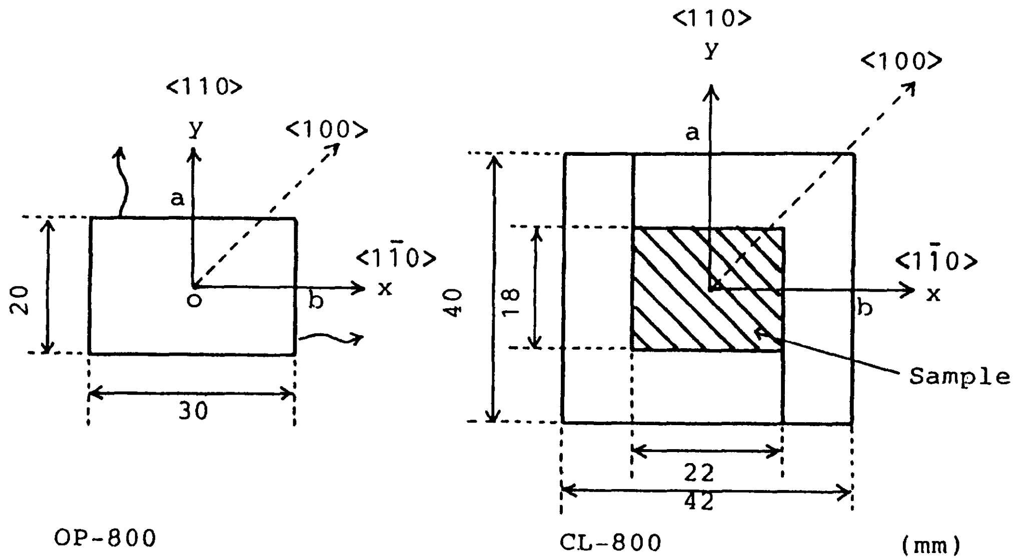


Fig.3-9. The schematic diagrams of the irradiated free wafer and x-y coordinates for the thermal stress analysis.

$$\frac{\partial T}{\partial t} = k\ \Delta T + \frac{W}{c \cdot \rho} \qquad (3\text{-}3a)$$

$$W = (\ Q - 2E\ )/h \qquad (3\text{-}3b)$$

where k is the thermal diffusivity, c is the specific heat, ρ is

the density of GaAs, E is the radiation rate per unit area, and h is the sample thickness. The factor 2 in the radiation term of Eq. (3-3b) takes into account that both surface of the sample radiate.

$$E = \varepsilon\sigma T^4 + H_c(T - T_g) \quad (3\text{-}4a)$$

where ε is the GaAs emissivity, σ is the Stefan-Boltzmann constant (5.67032×10^{-5} erg/cm^2/s/K^4), H_c is the heat transfer coefficient, and T_g is the temperature of the ambient gas. The heat transfer from semiconductor to ambient gas is negligible at the high temperature. Thus the Eq. (3-4a) can be written as

$$E \doteqdot \varepsilon\, \sigma T^4(x,y) \quad (3\text{-}4b)$$

The steady-state temperature distribution T(x,y) satisfies the Eq. (3-5).

$$K\left(\frac{\partial^2 T(x,y)}{\partial x^2} + \frac{\partial^2 T(x,y)}{\partial y^2} \right) = -(Q - 2\,\varepsilon\sigma\, T^4)/h \quad (3\text{-}5)$$

where K is the thermal conductivity. Approximate boundary conditions will be used in order to obtain an manageable problem, by assuming that the radiation rate is uniform over all radiating surfaces of the sample and equal to

$$E \doteqdot \varepsilon\sigma T_o{}^4 \quad (3\text{-}6)$$

where T_o is the steady-state temperature of infinite plane. This approximation appears reasonable, since temperature differences $v(x,y) \ll T_o$ are expected over the sample surface. Thus the boundary conditions can be written as

$$K\frac{\partial T(\pm a,y)}{\partial x} = \mp\ \varepsilon\, \sigma T^4(a,y) \doteqdot \mp\, \varepsilon\, \sigma T_o{}^4 = \mp H_o \quad (3\text{-}7a)$$

$$K\frac{\partial T(x,\pm b)}{\partial y} = \mp \; \varepsilon\sigma T^4(x,b) \doteqdot \mp \; \varepsilon\sigma T_o{}^4 = \mp H_o \qquad (3\text{-}7b)$$

since we choose T_o so that $2\cdot\varepsilon\sigma T_o{}^4 = Q$ (3-8)

The differential equation for this problem is

$$hK\left(\frac{\partial^2 T(x,y)}{\partial x^2} + \frac{\partial^2 T(x,y)}{\partial y^2} \right) = 2\cdot\varepsilon\sigma\left(T^4 - T_o{}^4 \right) \qquad (3\text{-}9)$$

Assuming that T(x,y) is written as $T_o + v(x,y)$, we can obtain

$$T^4(x,y) \doteqdot T_o{}^4 + 4T_o{}^3 v(x,y) \qquad (3\text{-}10)$$

From Eqs. (3-10), (3-9), (3-7a) and (3-7b) can be simplified to

$$\frac{\partial^2 v(x,y)}{\partial x^2} + \frac{\partial^2 v(x,y)}{\partial y^2} - \frac{1}{\lambda^2} v(x,y) = 0 \qquad (3\text{-}11a)$$

$$\lambda = \sqrt{\frac{Kh}{8 \; \varepsilon\sigma T_o{}^3}} \qquad (3\text{-}11b)$$

$$K\frac{\partial v(\pm a,y)}{\partial x} = \mp \; H_o \qquad (3\text{-}11c)$$

$$K\frac{\partial v(x,\pm b)}{\partial y} = \mp \; H_o \qquad (3\text{-}11d)$$

we obtain the two boundary conditions from the symmetry of the sample.

$$K\frac{\partial v(0,y)}{\partial x} = 0 \qquad (3\text{-}11e)$$

$$K\frac{\partial v(x,0)}{\partial y} = 0 \qquad (3\text{-}11f)$$

The numerical solution of Eqs. (3-11a) - (3-11f) is shown in Figs. 3-10 and 3-11. The variables x, y, and v have been replaced by x/λ , y/λ , and v/λ^2 , respectively, (and Eqs. (3-

11a) - (3-11f) are dispersed, and solved by complete pivoting Gauss-Jordan method).

Table 3-III. Constants for the calculation.[32)]

Thermal conductivity	K (erg/s/cm/K)	1.8×10^6
Sample thickness	h (cm)	0.05
Emissivity		0.7

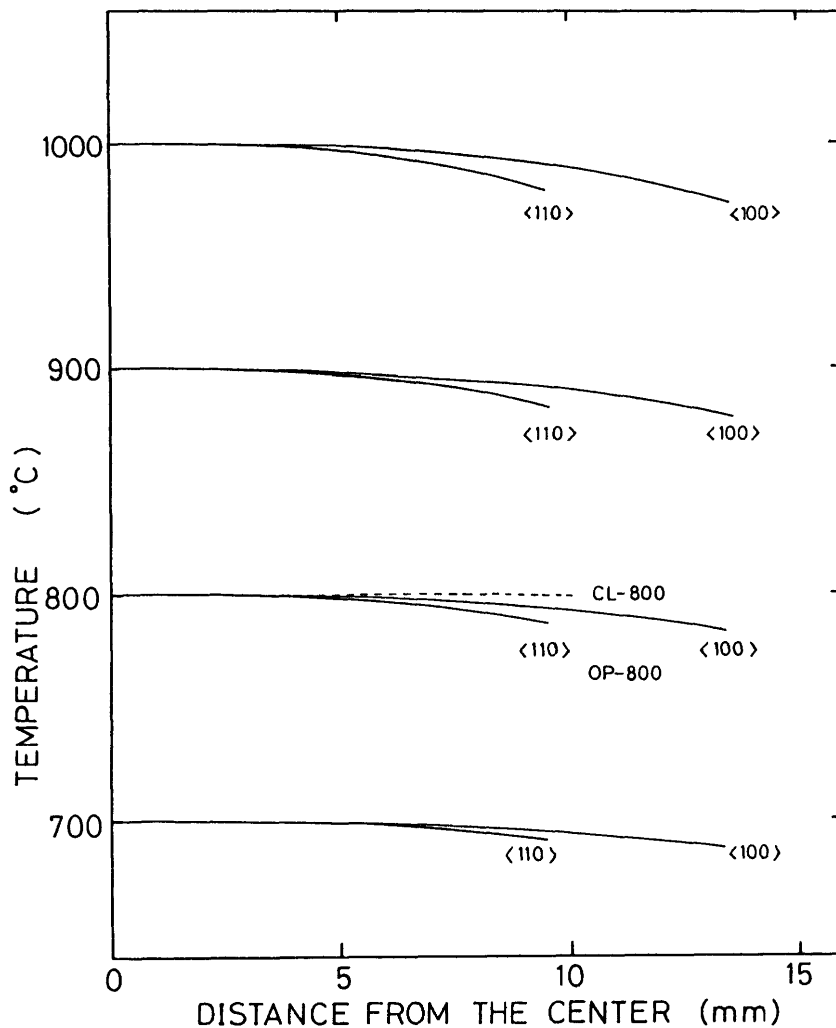


Fig.3-10. Computed temperature profiles along <110> and <100> directions.

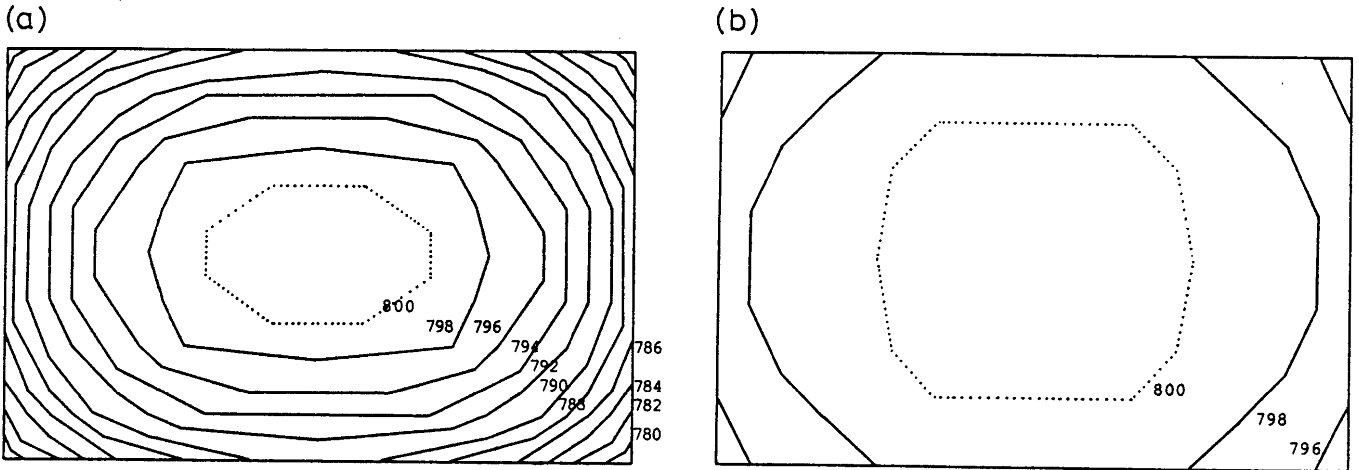


Fig.3-11. Calculated temperature distributions on RTP-GaAs wafer samples: (a) OP-800, (b) CL-800.

B. Thermal stress

When the temperature distribution in the wafer is known, in principle it is possible to evaluate the corresponding distribution of the thermoelastic stress. The following simplifying hypotheses will be introduced. The approximations of the "quasi-isotropic body" and "plane stress state" can be applied to GaAs crystal.

Equilibrium equations are :

$$\frac{\partial \sigma_x}{\partial x} + \frac{\partial \tau_{xy}}{\partial y} = 0 \qquad (3\text{-}12)$$

$$\frac{\partial \tau_{xy}}{\partial x} + \frac{\partial \sigma_y}{\partial y} = 0 \qquad (3\text{-}13)$$

where σ_x, σ_y, and τ_{xy} are stress components. Condition of

compatibility (including strain-displacement relation):

$$\frac{\partial^2 \varepsilon_x}{\partial y^2} + \frac{\partial^2 \varepsilon_y}{\partial x^2} = \frac{\partial^2 \gamma_{xy}}{\partial x \, \partial y} \qquad (3\text{-}14)$$

where ε_x, ε_y, and γ_{xy} are strain components.

Stress-strain relation:

$$\varepsilon_x = (\sigma_x - \nu\sigma_y)/E + \alpha\Delta T \qquad (3\text{-}15)$$

$$\varepsilon_y = (\sigma_y - \nu\sigma_x)/E + \alpha\Delta T \qquad (3\text{-}16)$$

$$\gamma_{xy} = \tau_{xy}/G \qquad (3\text{-}17)$$

where E is Young's modulus, ν is Poisson's ratio, α is the coefficient of linear expansion, G is the shear modulus, and T is the temperature fluctuation. If any thermal stress function χ exists, χ satisfies the equations (3-18a) - (3-18c).

$$\sigma_x = \frac{\partial^2 \chi}{\partial y^2} \qquad (3\text{-}18a)$$

$$\sigma_y = \frac{\partial^2 \chi}{\partial x^2} \qquad (3\text{-}18b)$$

$$\tau_{xy} = - \frac{\partial^2 \chi}{\partial x \, \partial y} \qquad (3\text{-}18c)$$

Substituting Eqs. (3-18a) - (3-18c) into Eqs. (3-14) - (3-17),

$$\Delta\Delta\chi = - \alpha E \, \Delta T \qquad (3\text{-}19)$$

$$\Delta\Delta\chi = \frac{\partial^4 \chi}{\partial x^4} + \frac{\partial^4 \chi}{\partial y^4} + 2\frac{\partial^4 \chi}{\partial x^2 \partial y^2}$$

Because the wafer edge is free, the boundary conditions can be written as

$$\chi(P) = \frac{\partial \chi(P)}{\partial n} = 0 \qquad (3\text{-}20)$$

where P is the edge of the wafer, n is perpendicular to periphery of the wafer. Figure 3-12 is show the calculated stress distribution from Eqs. (18) - (20).

Table 3-IV. Thermoelastic properties of GaAs.[32]

Thermal expansion coefficient	(1/K)	7.3×10^{-6}
Young's modulus	E (dyn/cm2)	8.51×10^{11}

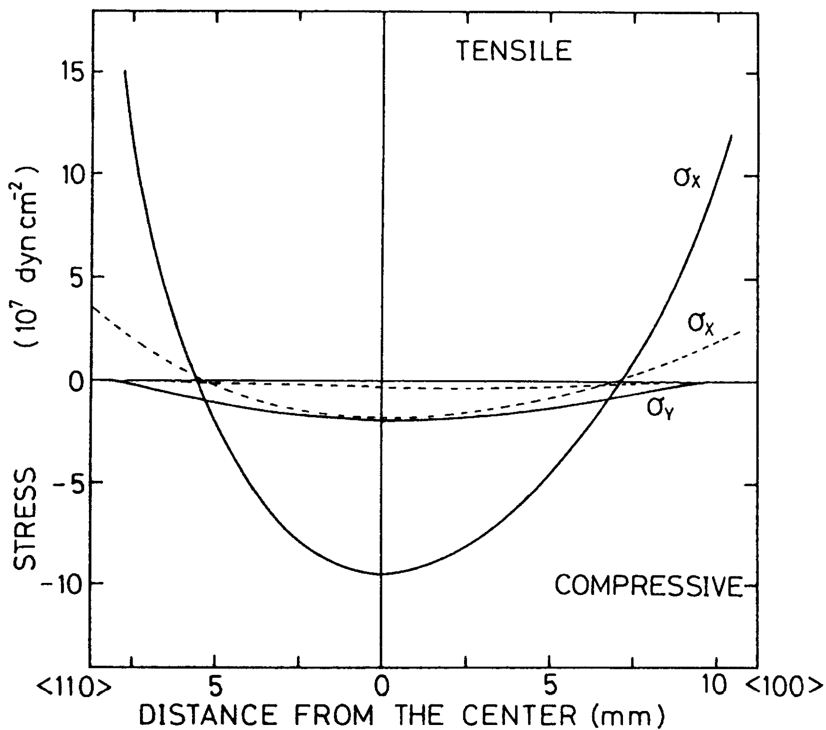


Fig.3-12. Computed profiles of σ_x and σ_y stress components in OP-800 and CL-800 (broken lines).

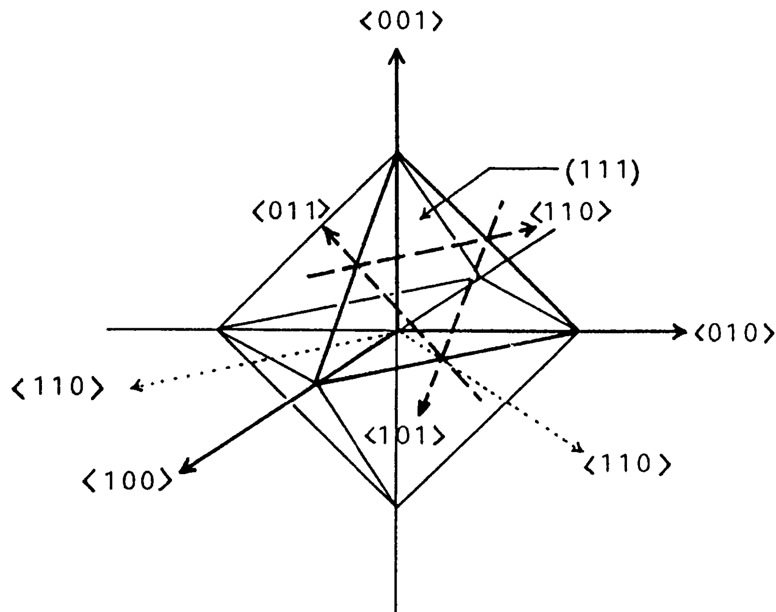


Fig.3-13. Elemental octahedron showing slip planes and slip directions (broken lines).

C. Shear stress

To evaluate the conditions of introduction of thermoplastic damage, it is consider that shear movements occur only along well-defined crystallographic directions, therefore the calculated stress must be resolved on the slip planes in the slip directions. The slip planes are {111} and the slip directions are <110>. The relevant planes, directions, and the shape of the samples are illustrated in Fig. 3-13. The resolved shear stresses and their total values are obtained from Table 3-V. The distribution of σ_{tot} is shown in Fig. 3-14.

Table V. The resolved shear stresses.

Resolved stress	slip direction	a number of equivalent directions
$\sigma_1 = \sqrt{2/3}\ \lvert \tau_{xy} \rvert$	$\langle \bar{1}00 \rangle$	4
$\sigma_2 = \sqrt{1/6}\ \lvert \sigma_x + \tau_{xy} \rvert$	$\langle 0\bar{1}1 \rangle$	2
$\sigma_3 = \sqrt{1/6}\ \lvert \sigma_x - \tau_{xy} \rvert$	$\langle 10\bar{1} \rangle$	2
$\sigma_4 = \sqrt{1/6}\ \lvert \sigma_y + \tau_{xy} \rvert$	$\langle \bar{1}0\bar{1} \rangle$	2
$\sigma_5 = \sqrt{1/6}\ \lvert \sigma_y - \tau_{xy} \rvert$	$\langle 0\bar{1}1 \rangle$	2
$tot = 4 \cdot \sigma_1 + 2(\sigma_2 + \sigma_3 + \sigma_4 + \sigma_5)$		-

D. Thermal stress for CL-800

For the "CL-800" sample, RTP was performed at 800 °C for 6 s with the cleaved edge around the sample kept in contact with GaAs pieces. The thermal stress in CL-800 sample are calculated assuming that the thermal contact between the sample and guard ring (GaAs pieces) is ideal, and cleaves surfaces of sample are free from the stress. Thus the boundary conditions can be given as

$$K \frac{\partial T(\pm C, Y)}{\partial x} = \mp H_o \qquad (3\text{-}21a)$$

$$K \frac{\partial T(x, \pm d)}{\partial y} = \mp H_o \qquad (3\text{-}21b)$$

$$\chi(\pm a,y) = \frac{\partial\chi(\pm a,y)}{\partial x} = 0 \qquad (3\text{-}21c)$$

$$\chi(x,\pm b) = \frac{\partial\chi(x,\pm b)}{\partial y} = 0 \qquad (3\text{-}21d)$$

In Fig. 3-11b the temperature distribution is shown. In Figs. 3-10, 3-12, and 3-14 the results of the calculation with the boundary conditions (3-21a) - (3-21d) are also shown.

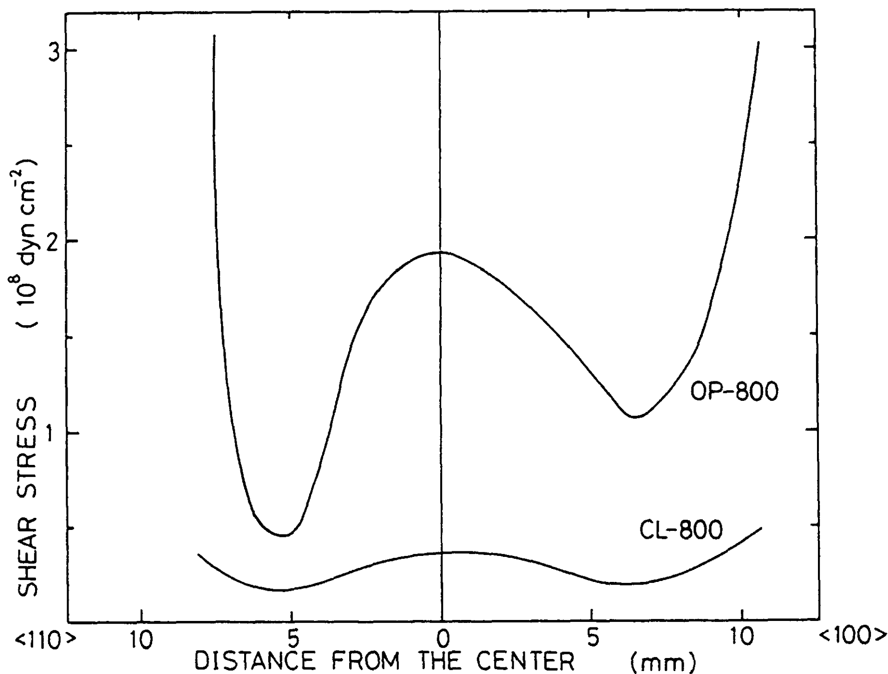


Fig.3-14. The calculated shear stress profiles resolved on {111} slip planes in OP-800 and CL-800 samples.

3.7 Correspondence of the defect distribution with the thermal stress profiles

The key question is if thermal stress is linked to EL2 concentration. Weber et al. reported the creation of EL2 defect during plastic deformation of GaAs.[33] In this section, it is

verify that the EL2 concentration has to do with the RTP-induced thermoelastic stress calculated in section 3.6.

The EL2 distribution shows a W-shaped pattern, so it can be related to the absolute value of the line stress or the resolved shear stress on {111} planes. Previously, the correspondence between the EL2 or dislocation and thermal, resolved shear stress induced in LEC GaAs has been reported.[28,34] As shown in Chap. IV, the EL2 distribution can be related with the resolved shear stress during RTP. Figure 3-15 shows the comparison between the EL2 distribution in "OP-800" and "CL-800" sample, and the resolved shear stress calculated in section 3.6. A stress conversion coefficient C_c was obtained

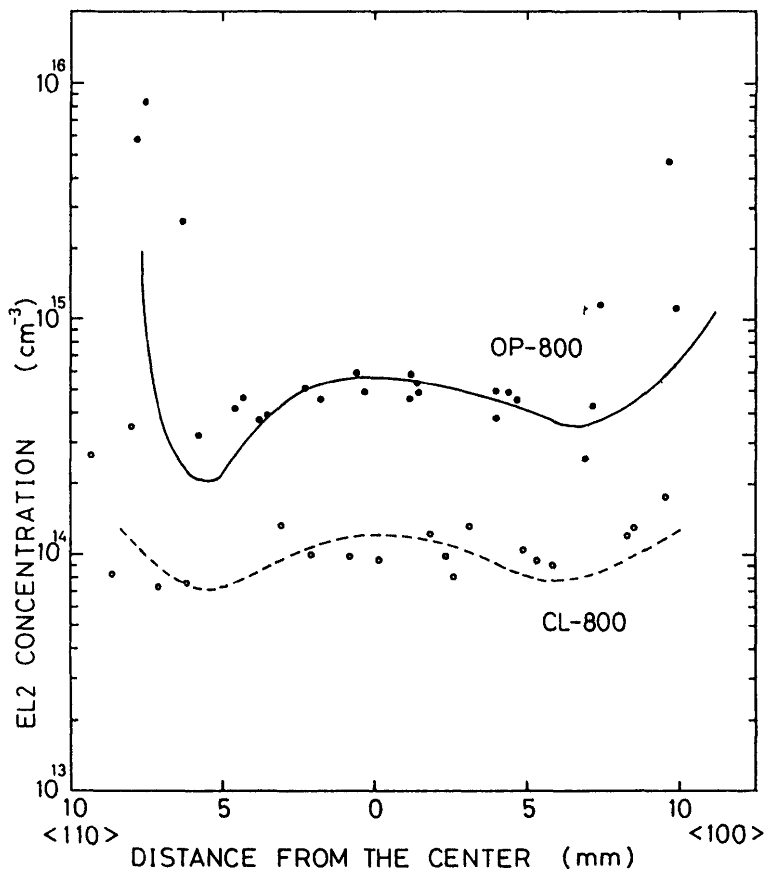


Fig.3-15. Comparison of the calculated EL2 distribution using the Eqs. 3-22 and 3-23 against the experimental result.

from this comparison, that is, multiplying the calculated thermal stress by a stress conversion coefficient yields the EL2 concentration.

$$C_c = 2.36 \times 10^6 \quad (dyn^{-1} cm^{-1})$$
$$C_s = 1.00 \times 10^{14} \quad (cm^{-3}) \quad \text{for OP-800} \qquad (3\text{-}22)$$
$$C_s = 3.03 \times 10^{13} \quad (cm^{-3}) \quad \text{for CL-800}$$
$$[EL2] = C_c \sigma_{tot} + C_s \quad (cm^{-3}) \qquad (3\text{-}23)$$

where C_s is defined as a constant that is probably dependent on the stoichiometry of GaAs crystal.

The calculated distribution are not coincident with the experimental data in peripheral region of wafer sample. In this region the plastic deformation may be occurred by the large thermal stress during RTP, and the EL2 is changeable to other defects.[35] In addition, EL2 concentration depends on the stoichiometry.[36] The stoichiometry in this region may be changed by As evaporation during RTP,[37] because of the insufficiency of proximity capping.

Kuhn et al. reported the stress conversion coefficient for as-grown LEC GaAs wafer.[28] Their value was given as

$$C_c = M_{cc}/S_{cc} = 2.6 \times 10^7 \quad (dyn^{-1} cm^{-1}) \qquad (3\text{-}24)$$

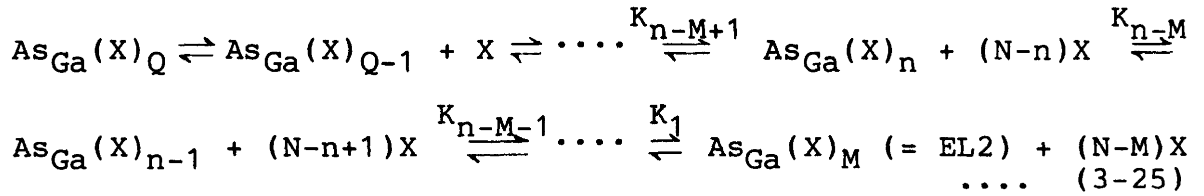
where M_{cc} is the normalized-stress conversion coefficient (cm^{-4}), $S_{cc} = \sigma_{tot}/S_{nor}$, and S_{nor} is the normalized stress which is depend on the boric oxide layer thickness, heat transfer parameter and the pulling rate in LEC growth conditions.[34] This value reported by Kuhn et al. is larger than that for the EL2 production by RTP. This result also suggests the plastic deformation in the LEC growth or the difference of the

stoichiometry and carrier concentration between the LEC substrate and MBE layer.[26,36]

Possibly the plastic deformation enhances the production of EL2 by RTP. Figure 3-16 shows the thermal stress dependence of the EL2 production during RTP. The EL2 concentration increases gradually up to $\sim 2 \times 10^8$ dyn/cm^2, and in the higher stress region over $\sim 2 \times 10^8$ dyn/cm^2 the EL2 concentration rapidly increases. This result indicates that RTP must be performed in the conditions which the thermal stress is below this critical point.

An origin of the EL2 production by thermal stress is cannot be concluded from present results. The antisite defect As_{Ga} are related to the stoichiometry, on the other hand, the concentration of the native defect As_i, V_{As}, or divacancy may be dependent on the thermal stress.[38] It is considered that these defects are related to EL2 defect.[39-44] The RTP-induced trap N1 concentration are also dependent on the distribution of thermal stress, because the N1 trap is not observed in the CL-800 sample. Thus, the N1 might be structural defect which is similar atomic structure to the EL2. It is assumed from this reason that the N1 defect is structural complex defect which can be composed of the same point defects as the components of EL2. Ito et al. suggests that the N1 is the complex defect composed of some As_i and an As_{Ga} defect.[45] The N1 distribution will be explained by this model, assuming that the EL2 structure is As_{Ga}-$(X)_M$, N1 structure is As_{Ga}-$(X)_n$, and X is a point defect which is increased by the tensile stress. M and n are the number of X

involved in EL2 defect and N1 defect. When the maximum number of n is Q, we have the following reaction equations.



$$As_{Ga}(X)_Q \rightleftharpoons As_{Ga}(X)_{Q-1} + X \rightleftharpoons \cdots \overset{K_{n-M+1}}{\rightleftharpoons} As_{Ga}(X)_n + (N-n)X \overset{K_{n-M}}{\rightleftharpoons}$$
$$As_{Ga}(X)_{n-1} + (N-n+1)X \overset{K_{n-M-1}}{\rightleftharpoons} \cdots \overset{K_1}{\rightleftharpoons} As_{Ga}(X)_M \ (= EL2) + (N-M)X \quad \cdots\cdots (3\text{-}25)$$

The mass action relations corresponding to the above reactions are as follows.

$$[As_{Ga}(X)_n] = \frac{1}{K_{n-M}}[X][As_{Ga}(X)_{n-1}] = \frac{1}{K_1 K_2 \cdots K_{n-M}}[X]^{n-M}[EL2] \quad (3\text{-}26)$$

If the N1 size n is mainly N, the dominant N1 concentration is written as follows.

$$[N1] = \frac{1}{K_1 K_2 \cdots K_{N-M}}[X]^{N-M}[EL2] \quad (3\text{-}27)$$

Therefore, the total concentration of N1 (N_{tot}) is

$$N_{tot} = [EL2]\sum_{n=1}^{Q-M} A_n [X]^n \quad (3\text{-}28)$$

$$A_n = 1/K_1 K_2 \cdots K_n$$

The mean of the N1 defect size $\bar{n}$:

$$\bar{n} = \frac{\sum_{n=1}^{Q-M} A_n n [X]^n}{\sum_{n=1}^{Q-M} A_n [X]^n} - M \quad (3\text{-}29)$$

Equation 3-29 suggests that the mean N1 size $\bar{n}$ increases with increasing the concentration of X. Frenkel defect concentration

is proportional to the strain . Assuming that [X] is given approximately by

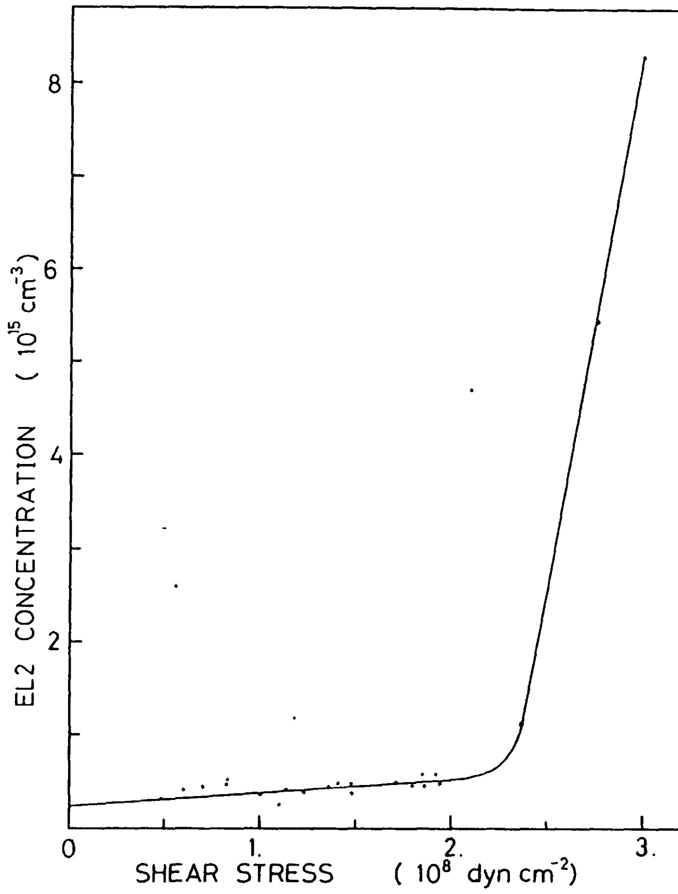
$$[X] = B\,\sigma_t + X_o \qquad (3\text{-}30)$$

where B is the linear conversion coefficient, σ_t is the hydrostatic tensile stress, and X_o is the concentration of X in stress free condition, Substituting Eq. 3-30 into Eq. 3-27.

$$\frac{[EL2]}{[N1]} = \frac{(B\sigma_t + X_o)^{-N+M}}{A_{N-M}} \qquad (3\text{-}31)$$

The [EL2]/[N1]- σ_x plot is given in Fig. 3-17. σ_t is the hydrostatic pressure, while σ_x is uniaxial stress. σ_x was, however, used in place of the σ_t, because the stress σ_y and σ_z is negligible. In this case it is difficult that the curve obtained from Eq. 3-31 is fitted to the [EL2]/[N1]- σ_x plot, because of the variation of the number N-M. Figure 3-17 indicates the positive value of N-M, that is, the defect size for N1 is larger than that of EL2. N-M is estimated to be between 1 and 4. For example, if the origin of EL2 is identified with As_{Ga}-As_i, the N1 level results in $As_{Ga}-(As_i)_2$, $As_{Ga}-(As_i)_3$, $As_{Ga}-(As_i)_4$, or $As_{Ga}-(As_i)_5$.

The change of stoichiometry in GaAs crystal also causes leads to the change of the N1 concentration. It is expected that the formation of N1 is suppressed by the production of some point defects, such as V_{Ga}, which is produced by As evaporation and outdiffusion of Ga into SiO_2 encapsulant. we can selectively induces the defects N1 and EL2 in the surface layer in GaAs by control of the stoichiometry and thermal stress, which can be changed by coating of the wafer with a discontinuous film. This



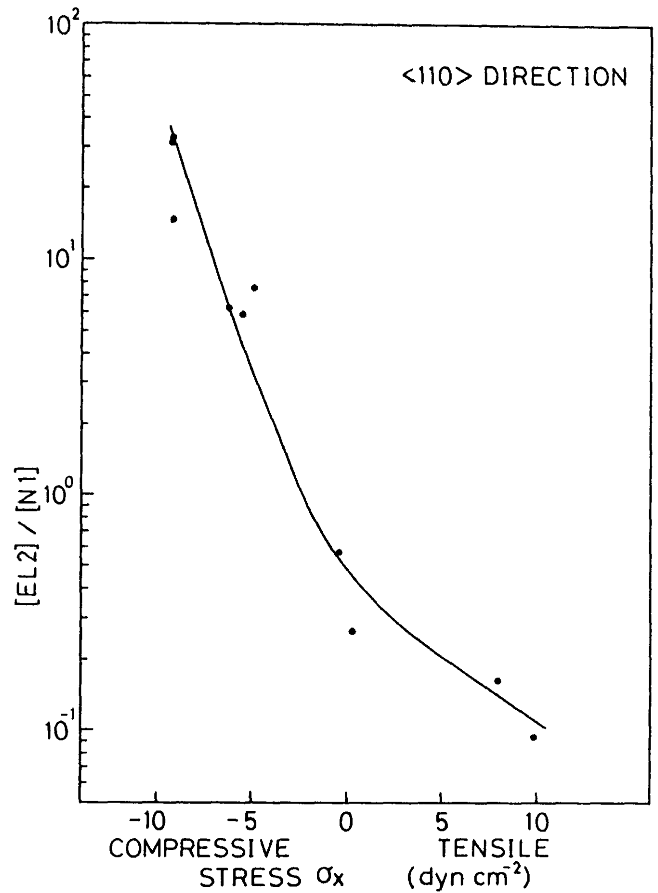


Fig.3-16. EL2 concentration vs. the calculated shear stress σ_{tot} for OP-800 sample.

Fig.3-17. [EL2]/[N1] vs. calculated stress component σ_x for OP-800 sample.

technique is applicable to separation of devices on the conductive epitaxial layer, since the electrical properties of GaAs are controlled this midgap level which makes the material SI. Figure 3-18 and 3-19 show the Fermi-level position in the energy gap calculated using the 3-level model and carrier concentration calculated from the result shown in Fig. 18. In this thesis, this application will not be followed, but be reported elsewhere.

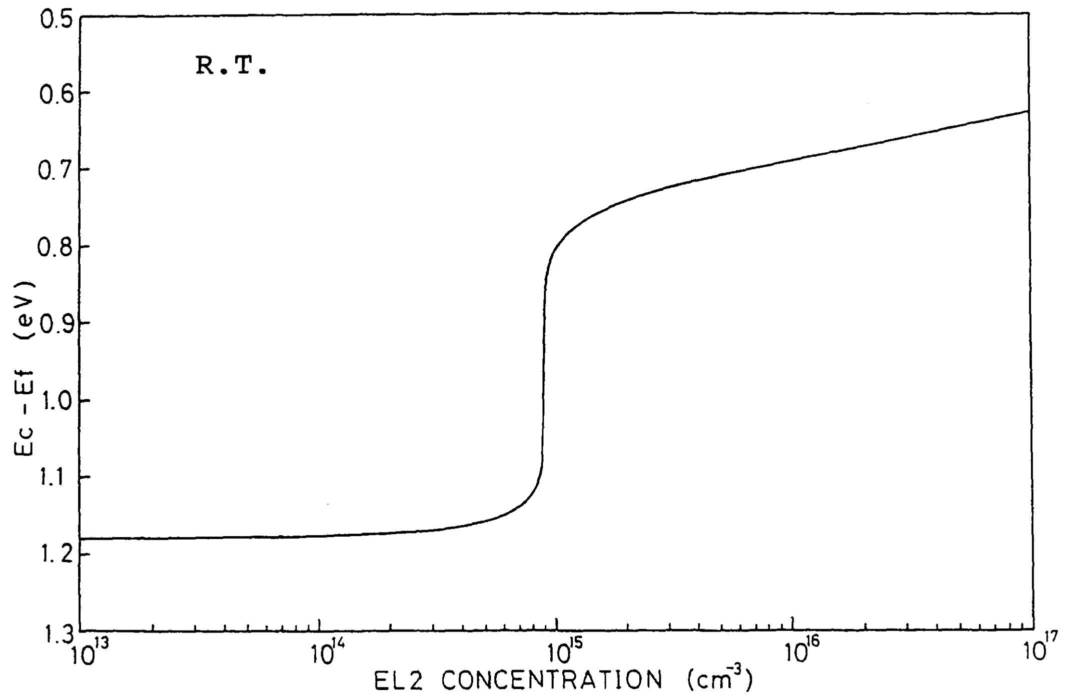


Fig.3-18. Calculated variation of Fermi level in band gap with the EL2 concentration. Acceptor level Ea(Be) = 0.028 (eV). Donor level Ed(Si) = 0.006 (eV). EL2 level Et = Ec - 0.75 (eV). Acceptor concentration $Na=10^{15}(cm^{-3})$. Donor concentration $Nd=10^{14}(cm^{-3})$.

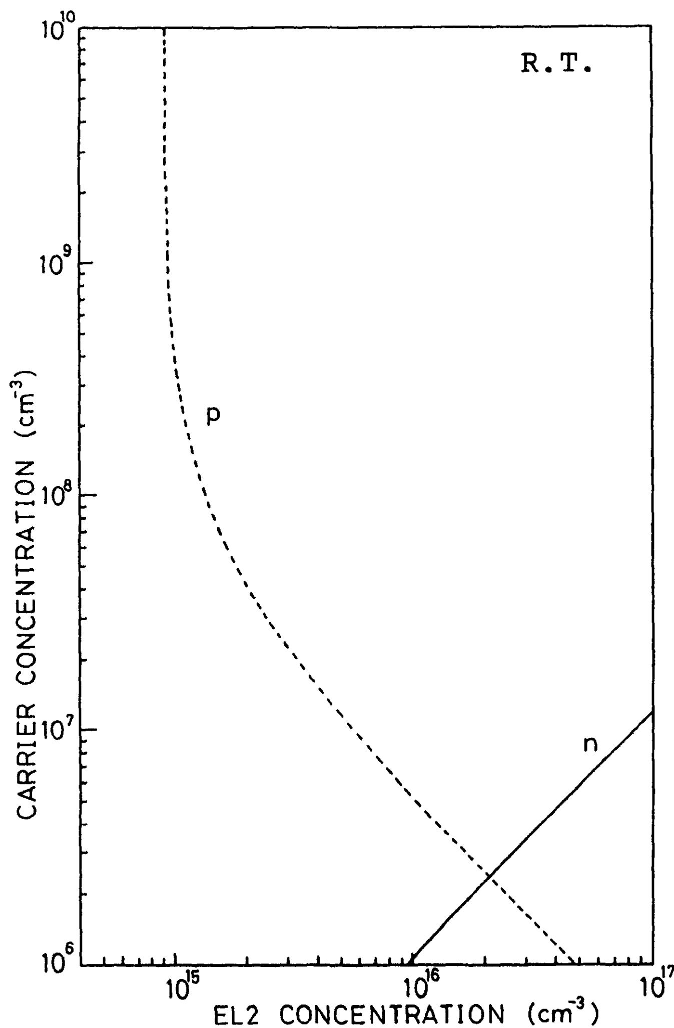


Fig.3-19. EL2 concentration dependence of carrier concentrations p and n calculated from the result shown in Fig.3-18.

3.8 Summary

Variations of deep levels in the MBE n-type GaAs layers by RTP (700 - 900 °C) have been studied by DLTS using Au Schottky-barrier diodes. RTP has been conducted by placing the sample between a bottom and a top GaAs wafer without any encapsulant. In as-grown MBE GaAs layers, there are three electron traps: M1, M3, and M4. These electron traps are annealed out by RTP at 900 °C. On the other hand, two electron traps N1 (E_c - 0.5-0.7 eV) and EL2 (E_c - 0.82 eV) are produced by RTP.

The spatial distribution of N1 and EL2 are observed. The EL2 distribution is especially a W-shaped pattern, and the N1 distribution is similar to EL2 distribution. It is supposed that this peculiar shape of the spatial variation for EL2 and N1 concentration is consistent with that of the thermal stress induced by RTP. When RTP is performed with the guard ring composed of GaAs pieces, in order to improve the temperature nonuniformity and to prevent to generate the thermal stress, the nonuniformity of EL2 production is improved and EL2 remains at a uniform concentration of 10^{14} cm^{-3} across the layer. On the other hand, N1 is absent from the same layer. The thermal stress enhances the production of the trap EL2, but the origin of the production is not only thermal stress.

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IV. DISTRIBUTION OF DEEP LEVELS AND IMAGE PROCESSING FOR SEMI-INSULATING GaAs WAFERS

4.1 Introduction

The nonuniform distributions of the deep donor EL2 and dislocations are usually observed in the liquid-encapsulated Czochralski (LEC) and horizontal Bridgman (HB) GaAs wafers.[1-5] An understanding of how these defects are distributed throughout crystals of GaAs is important, since the nonuniformity of this deep level or the dislocations in GaAs wafers is possible candidate for the fluctuations of the characteristics in GaAs-based devices.[6,7]

RTP has been proposed for the annealing of ion implanted GaAs,[8] and has attractive features, for example, minimum redistribution and high activation of the implanted ions. The RTP, however, produces some deep levels[9,10] andthe slip lines[11], that are distributed across the GaAs wafers.[12] The inhomogeneities caused by the distributions of these defects in RTP GaAs must be evaluated and the distributions of these defects in RTP GaAs must be evaluated and improved.

In this chapter, the redistribution of deep levels in semi-insulating (SI) GaAs wafer by RTP is demonstrated and the distributions of deep levels are compared with dislocation patterns in undoped and In-doped LEC GaAs wafers. The distributions of deep levels are detected by the contactless measurement of the optically injected excess carrier signal height by reflectance microwave probe (RMP) method.[13] This

method is a practical and useful to characterize the distribution of deep levels in SI GaAs substrates at room temperature. The x-ray topography (XRT) is used to determine the relative density distribution of the dislocations or the crystallographic slip caused by RTP.

4.2 Contactless measurement by the reflectance microwave prove method

Figure 4-1 shows a schematic illustration of the apparatus for the contactless measurement of optically injected excess carrier concentration in GaAs wafer by RMP method (DAINIPPON SCREEN MFG. Co. LTD. "WAFER-EL2"). A GaAs wafer was placed on the position-controllable x-y stage against the output aperture of the ridge waveguide. A Gunn diode operating at 10 GHz was used as the detecting probe. The reflected wave due to the photo-induced excess carriers in the sample was isolated by a circulator. The excitation source for excess carriers was semiconductor laser diode with the wavelength of 904 nm. The pulse width of the injection light was 150 ns. We can regard the carrier concentration for the pulse width as the steady-state concentration. Carriers cannot be excited directly between the valence band and the conduction band, in the case of light irradiation by the 904 nm (1.37 eV) laser diode.[13] They are only excited through the intermediate stepping states by the two-photon process, as shown in Fig. 2. Therefore, the signal height by microwave prove increases with the concentration of deep

levels which causes near-infrared optical absorption, and the map of the signal intensity presents the relative concentration profile of EL2.[14,15]

The transitions of electrons through intermediate-level centers taking place under the illumination by the 904 nm laser are illustrated in Fig. 4-2. The rates of six processes are also shown in this figure. If the injected electrons equal the injected holes, the rate equations under steady state ($dn/dt = dp/dt = 0$) yield the electron and hole concentration.

Rate equations:

$$dn/dt = \sigma_n \phi n_t + e_n n_t - c_n n(N_t - n_t) = 0 \quad (4\text{-}1a)$$

$$dp/dt = \sigma_p \phi (N_t - n_t) + e_p(N_t - n_t) - c_p p n_t = 0 \quad (4\text{-}1b)$$

Charge neutrality ($\Delta p = \Delta n$):

$$n_t = p - n + N_t \quad (4\text{-}2)$$

Mass action density:

$$n^* = e'_n/c_n,\ p^* = e'_p/c_p,\ e'_n = \sigma_n \phi + e_n,\ e'_p = \sigma_p \phi + e_p \quad (4\text{-}3)$$

Electron concentration:

$$n^3 + n^* n^2 - (n^* N_t + n^* p^*)n - n^{*2} p^* = 0 \quad (n > 0) \quad (4\text{-}4)$$

To demonstrate the detection of a variation of deep level concentration by the RMP method, the electron concentration is numerically calculated for steady state condition under the illumination by the 904 nm laser and shown in Fig. 4-3(a), assuming that the transitions of electrons are only six as shown in Fig. 4-2 and the intermediate center is the deep donor EL2 in GaAs. We took no account of the band-to-band recombination. The photoionization cross sections of EL2 for electrons (σ_n) and holes (σ_p) are 1.5×10^{-16} cm^2 and 0.5×10^{-16} cm^2,

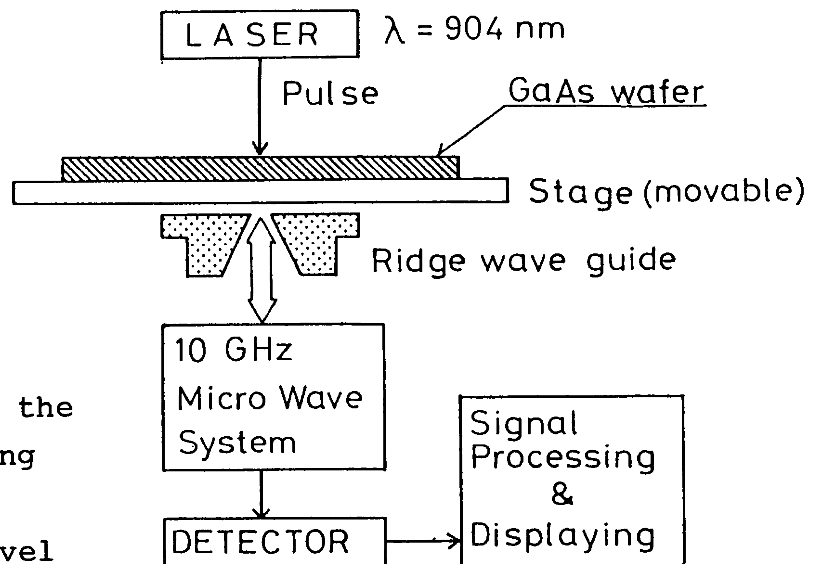
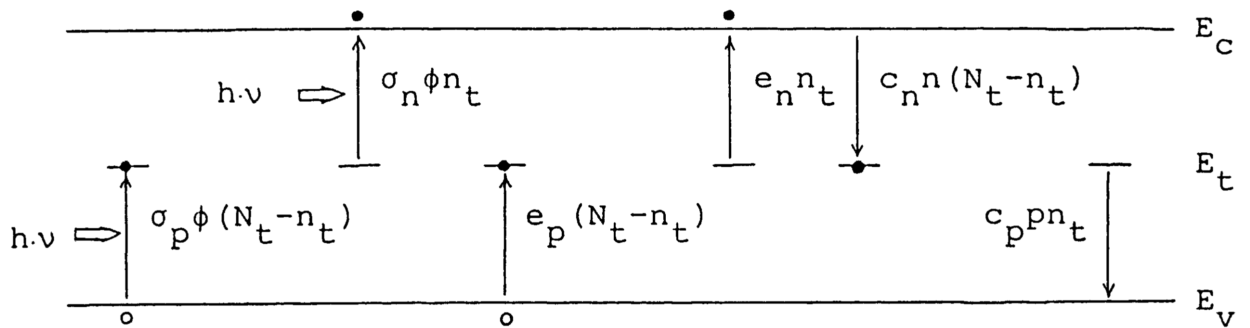


Fig.4-1. Block diagram of the point-by-point wafer mapping system for the contactless measurement of the deep level distribution.



n_t : neutral EL2 concentration

N_t : total EL2 concentration

e_n : thermal electron emission rate

e_p : thermal hole emission rate

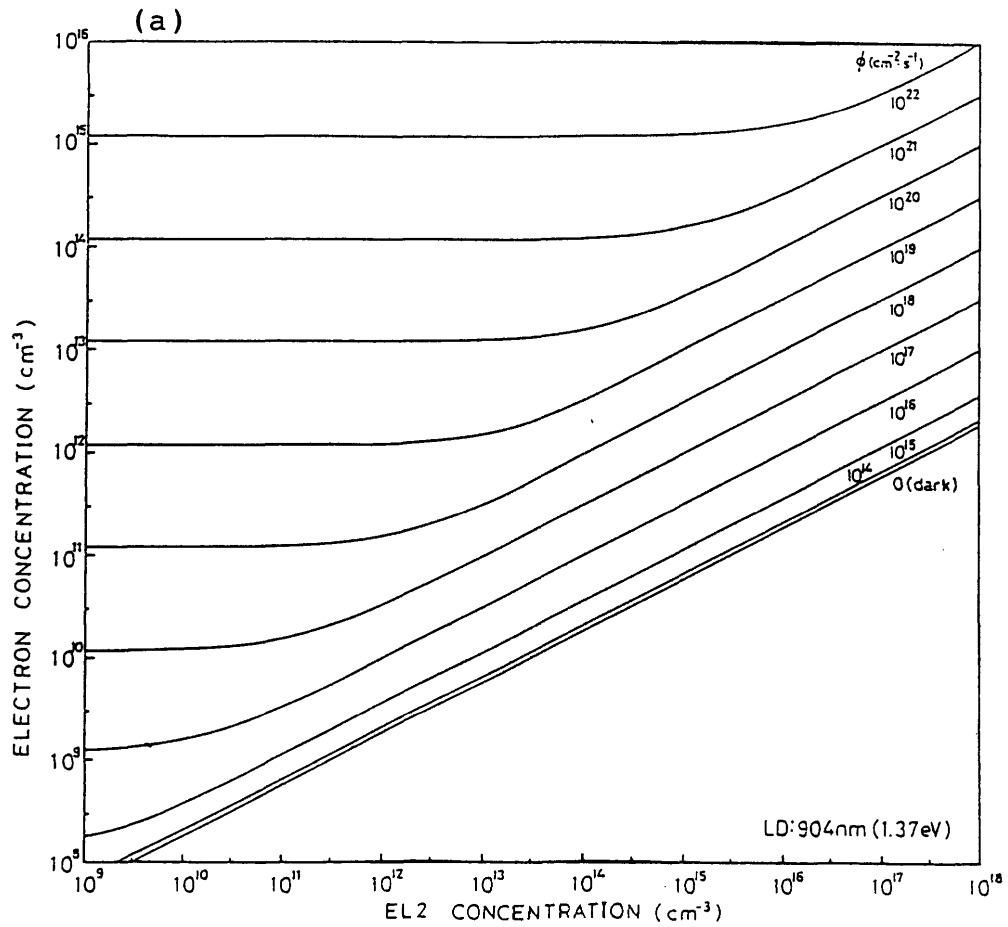
c_n : electron capture coefficient

c_p : hole capture coefficient

ϕ : photon flux

σ_n, σ_p : photoionization cross sections

Fig.4-2. The transitions of electrons through intermediate-level centers under the illumination.



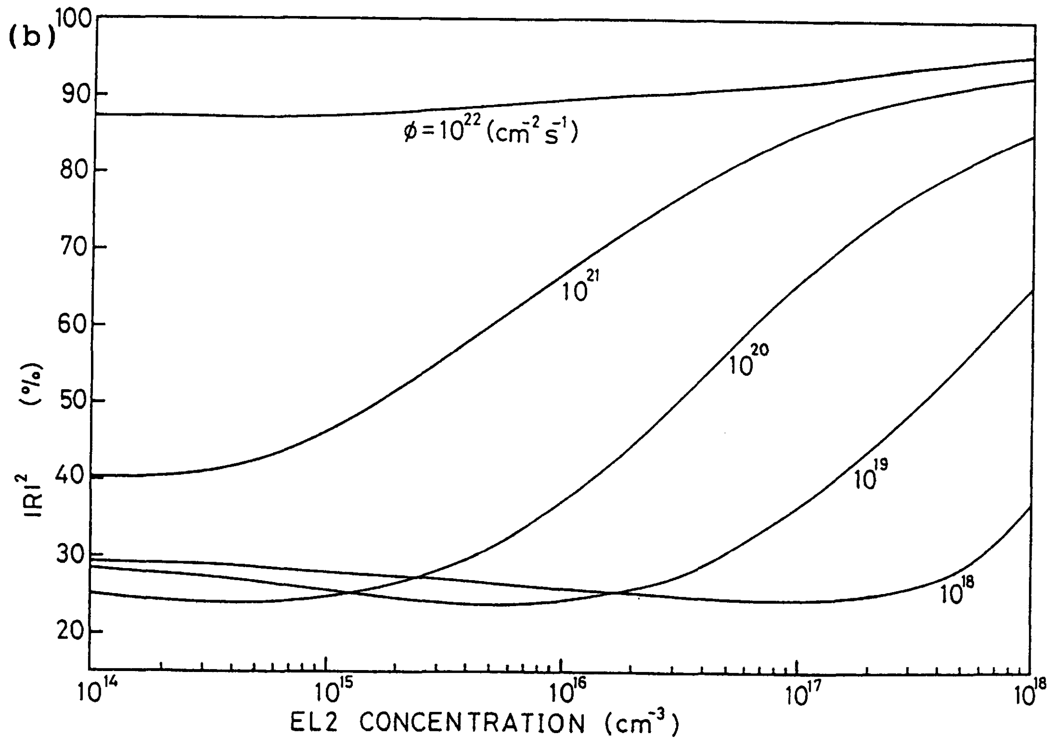


Fig.4-3. (a) The EL2 concentration dependences of the electron concentration under 904 nm laser illumination. ϕ is the photon flux. (b) Calculated variations with the EL2 concentration of the reflected power of 10 GHz- microwave.

respectively.[16] The thermal electron and hole emission rates (e_n, e_p) are (5.3×10^{-2}, 6.5×10^{-5}) (1/s), and the electron and hole capture coefficients (c_n, c_p) are (2.0×10^{-3}, 3.3×10^{-11}) (cm^3/s) at 300 K.[17]

Figure 4-3(b) shows the theoretical reflected power of 10 GHz-microwave by a wafer of 500 μm thickness, obtained from the carrier concentration in Fig. 4-3(a), under the illumination with varying photon flux (ϕ). It is found that this system is made with enough sensitivity to permit analysis of GaAs wafer of the ordinary thickness. The optimum photon flux for the high sensitivity depends on a range of the EL2 concentration measured by the RMP method. The optimum photon flux of $\sim 10^{21}$ ($cm^{-2}s^{-1}$) is known by this figure, because the EL2 concentration is commonly within 10^{15} - 10^{16} cm^{-3} in LEC crystals. It is necessary that the laser power is 400 mW on the average, for sensitive detection of EL2 with RMP method. The laser power in this experimental system is, however, 10 W (r.m.s.). This result suggests that the effective recombination center such as EL6 in addition to EL2 center exists in these materials.

4.3 Redistribution of defects by RTP

The wafers used in this study were Cr-doped, In-doped and undoped, (100) oriented SI GaAs grown by the LEC method. RTP was carried out for the Cr-doped LEC 2 in.-diam wafer at 800 °C for 6 s in flowing N_2 with another GaAs wafer placed over it (proximity capping method). The heating rate was 50 °C/s, and the wafer was cooled without any control. It took about 9 s to reach 600 °C.

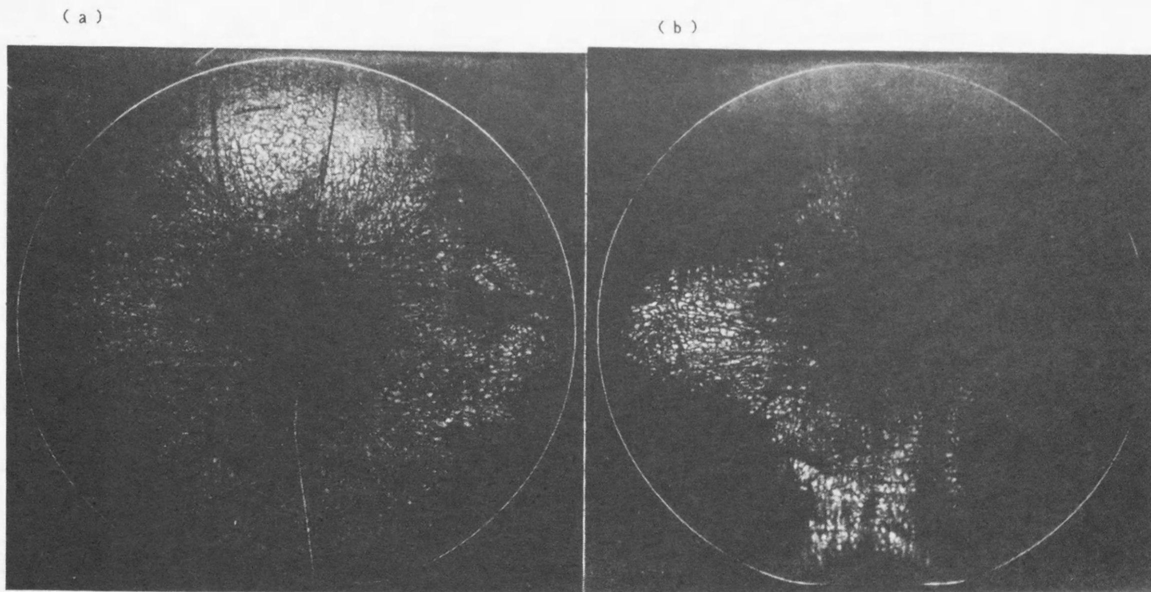


Fig.4-4. The transmission x-ray topographs for the wafers (a) before RTP and (b) after RTP.

Figures 4-4(a) and 4-4(b) show the transmission XRT using Mo K_{1} radiation for the wafer before and after RTP, respectively. RTP results in the generation of slip networks from the periphery to the center of the wafer. The XRT of the wafer after RTP shows a four-fold symmetrical pattern. The likely cause of the slip generation is relief of thermal stress developed as a result of small temperature nonuniformity across the wafer.[11,18] To verify the correlation between a thermal stress distribution with this experimental result, we calculate the sum of the shear stress resolved on {111} planes in the slip direction in the case of the thin plate approximation, assuming that the heat radiation rate is uniform over all radiating surface of the wafer and equal to $\varepsilon\sigma T^4$, where σ is the Stefan-Boltzmann constant, the GaAs emissivity ε is 0.7 and the RTP temperature T is 1073 K (800 °C).[11] The equations for the calculation are given, as follows.

Diffusion equations for RTP:[18)]

$$Kh/r\frac{d}{dr}\left(r \frac{dT(r)}{dr} \right) = -2Q + 2\cdot\varepsilon\sigma T(r)^4 \qquad (4\text{-}5)$$

$$K\frac{dT(a)}{dr} = -\varepsilon\sigma T(a)^4 \qquad (4\text{-}6)$$

where $Q = \varepsilon\sigma T_o$, K is the thermal conductivity, h is the sample thickness, and T(r) is the temperature on the wafer.

Thermal stress by RTP:

$$\sigma_{rr} = -\frac{\alpha E H_o \lambda^2}{K}\left(1/a - I_1(r/\lambda)/I_1(a/\lambda)/r \right) \qquad (4\text{-}7)$$

$$\sigma_{\theta\theta} = -\frac{\alpha E H_o \lambda^2}{K}\left(1/a + I_1(r/\lambda)/I_1(a/\lambda)/r - I_0(r/\lambda)/I_1(a/\lambda)/\lambda \right) \qquad (4\text{-}8)$$

$$\sigma_{r\theta} = 0$$

where α is the thermal expansion coefficient, E is the Young's modulus, $H_o = \varepsilon\sigma T_0{}^4$, $\lambda = \sqrt{Kh/8\ \varepsilon\sigma T_0{}^3}$, and I_0, I_1 are the modified Bessel functions (order 0 and 1).

The result of this calculation is shown in Fig. 4-5. No slip generation by RTP is observed near the four local minima in the calculated shear stress.

Figure 4-6(a) and 4-6(b) show the contour map of deep level concentration before and after RTP measured by the RMP method, respectively. After RTP the signal intensity by the RMP method increases at the center and periphery of the wafer. Hence, the signal intensity profile shows a W-shaped pattern, especially along the <100> radial direction. The increase of the signal intensity indicates that deep levels are produced by RTP. We

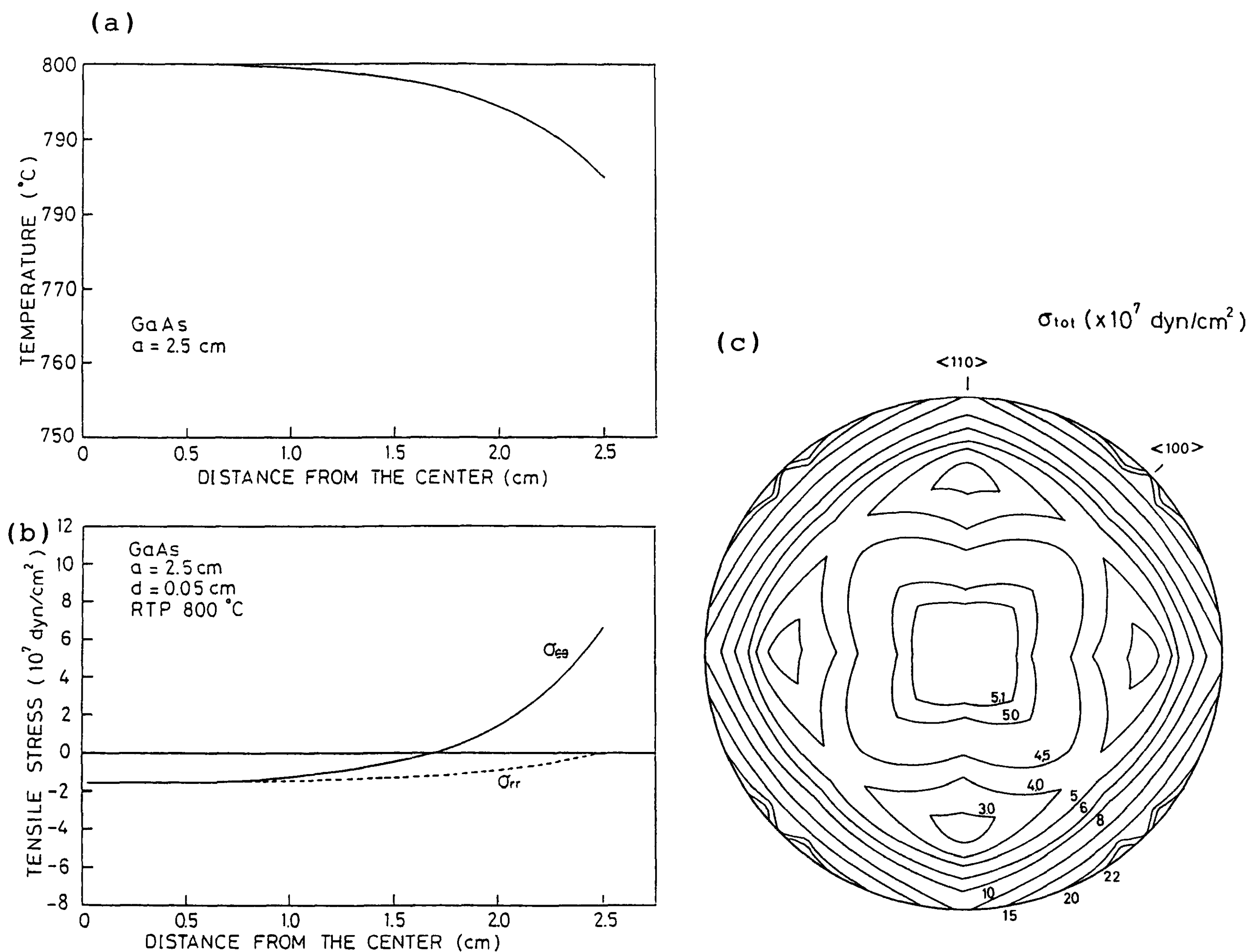


Fig.4-5. (a) Computed temperature profiles along the radial direction for RTP at 800 °C and (b) thermal stress components. (c) The contour map of the calculated shear stress resolved on {111} planes.

have reported that the trap EL2 is produced by RTP in molecular-beam-epitaxial (MBE) GaAs and the spatial distribution of EL2 concentration shows the W-shaped pattern across the MBE wafer.[12) It seems that the present result in the LEC wafer measured by RMP method is due to the same origin as the production of EL2 in the MBE layer.[14) According to the correlation between the pattern

of the redistributed EL2 concentration by RTP and that of the slip generation or the thermal stress, it is suggested that the EL2 is produced by the large thermal stress during RTP. To prevent the nonuniformity of EL2 and the slip caused by the thermal stress during RTP, it is necessary to use the guard rings for RTP or to employ thermal processing with milder heating and cooling rate.[11)]

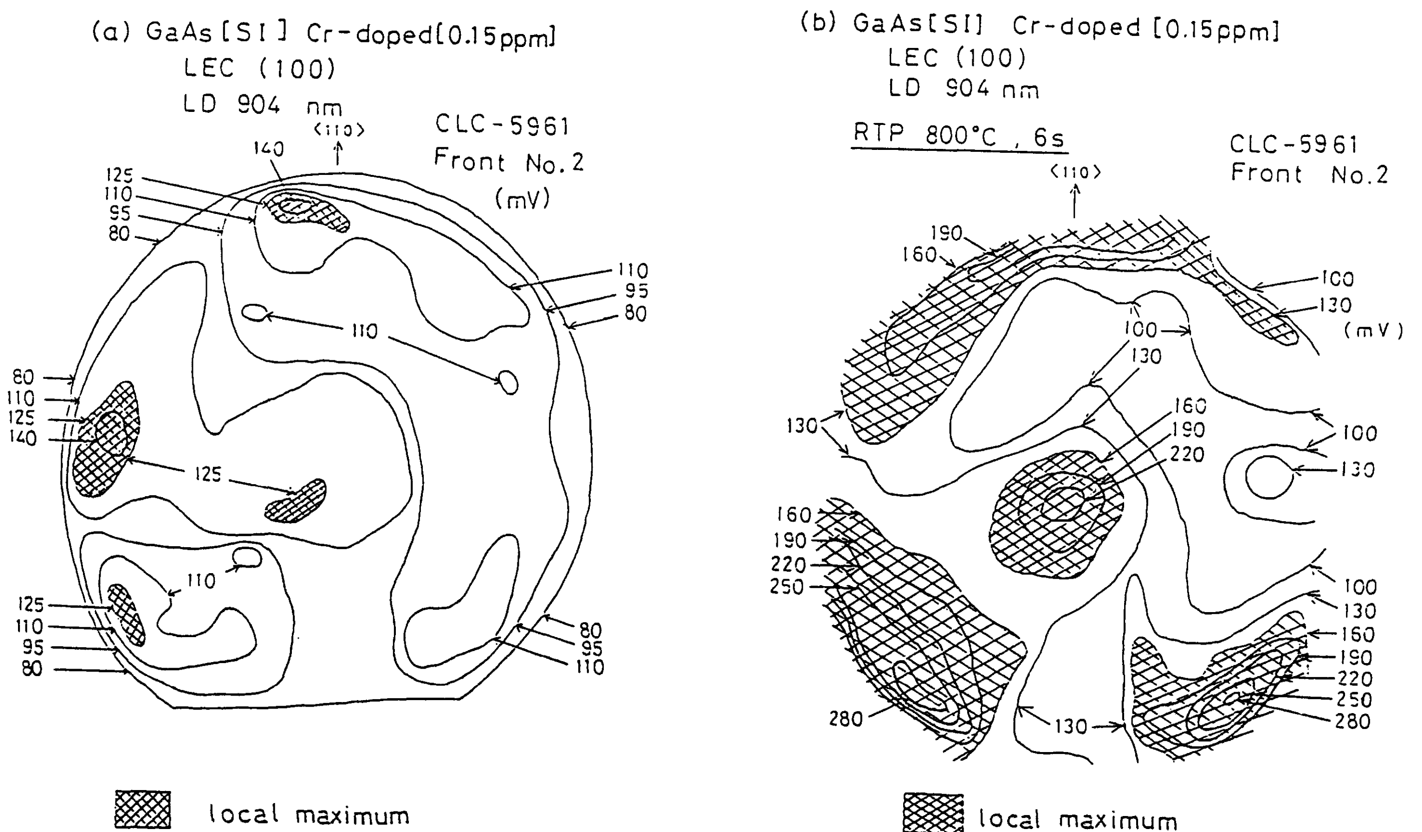


Fig.4-6. Contour maps of deep level concentration relative value in the SI GaAs (a) before RTP and (b) after RTP.

4.4 Distributions of dislocation and EL2 in LEC GaAs substrates

Figures 4-7(a) and 4-7(b) show the XRT and the deep level map measured by the "WAFER-EL2" system for the 2 in.-diam (100) undoped SI GaAs wafer grown by LEC method. The thickness of this wafer is 450 μm. The four-fold symmetry in the RMP signal pattern of Fig. 4-7(b) is consistent with the dislocation distribution in part (a) of these figures.

Figures 4-8(a) and 4-8(b) show the XRT and the deep level map for the 2 in.-diam (100) In-doped SI LEC GaAs wafer. The thickness of the wafer is 400 μm. The RMP signal distribution in the In-doped wafer is also dependent of dislocation patterns. In the LEC and boat-grown GaAs, since the EL2 center is predominantly observed[1,2] and the neutral EL2 causes the dominant sub-bandgap near-infrared optical absorption,[15] we can consider that the RMP signal distribution presents the distribution of the relative EL2 concentration. Therefore, in these undoped and In-doped wafers, these correlations of dislocation and RMP signal patterns support the EL2 is a direct consequence either of the stress (lattice strain) or of the dislocation.

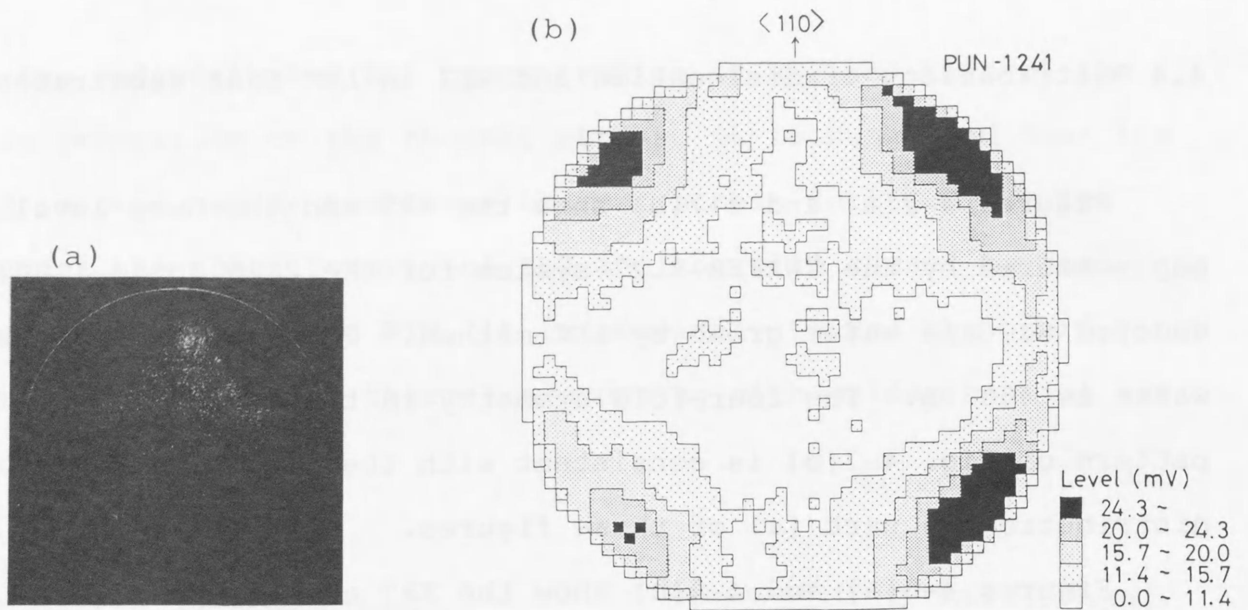


Fig.4-7. (a) The x-ray topography and (b) the deep level map for the undoped LEC GaAs wafer.

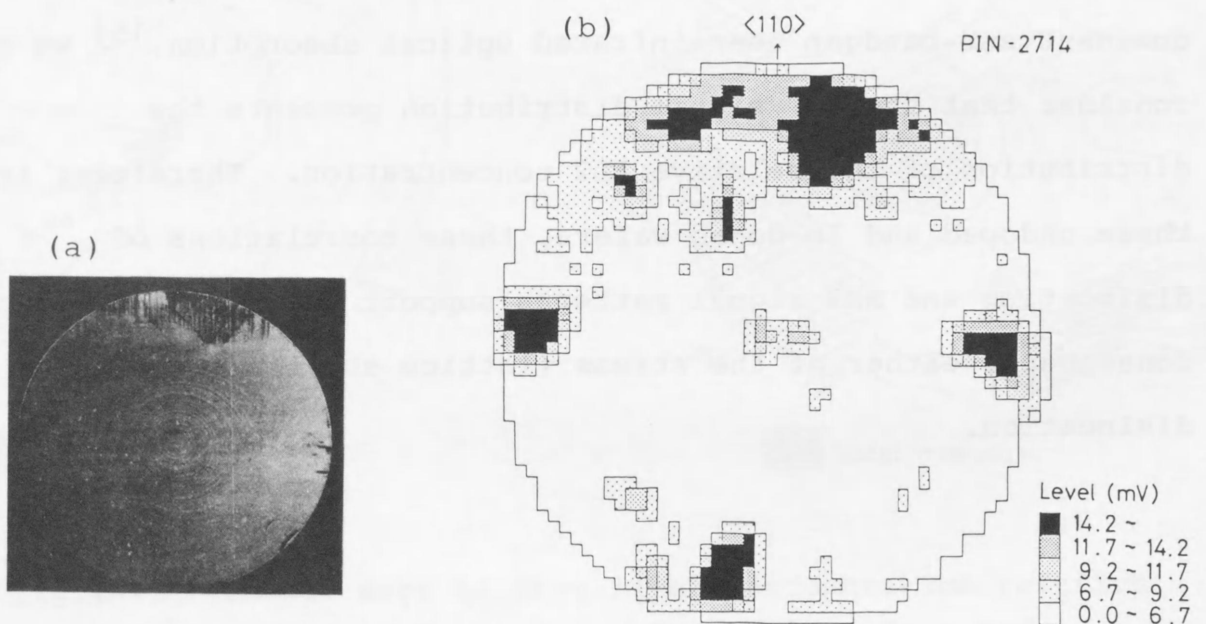


Fig.4-8. (a) The x-ray topography and (b) the deep level map for the In-doped LEC GaAs wafer.

4.5 Summary

The detection of a variation of EL2 concentration in GaAs wafer by the RMP method has been demonstrated by the numerical calculation. The contactless measurement by the RMP method has been adopted for the observation of the redistribution of the EL2 center in LEC SI GaAs by RTP. The four-fold symmetrical distribution of EL2 and he crystallographic slip is observed in the 2 in.-diam (100) GaAs wafer after RTP. The redistribution of the EL2 center in the GaAs wafer is due to the production of it by the large thermal stress during RTP.

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V. SPECTRAL RESPONSES OF GaAs PHOTODIODES FABRICATED BY RAPID THERMAL DIFFUSION

5.1 Introduction

GaAs photodiodes have a broad range of applications to sensors and detectors for optical communications. In particular, there is a interest in the application to monolithic optoelectronic integrated circuits (OEIC) including AlGaAs laser diodes. Zn diffusion into GaAs is an important technique for the fabrication of optoelectronic devices and its integrated circuits.[1,2] The furnace process requires high temperature and long diffusion times. Consequently it is difficult to prevent the surface degradation and to form the shallow heavily doped p-type lȧyers by the conventional open furnace processing.

RTP with tungsten-halogen lamps has an inherent advantage of short time processing[3-5] and is appropriate for the GaAs device processing, for instance, because it is expected that a redistribution of prior doped impurity and surface decomposition is suppressed[6-9] in the modulation-doped structure. Rapid thermal diffusion (RTD) has been applied for the fabrication of shallow p^+n junction in GaAsP, and this shallow junction is suitable for the construction of light emitting diodes and photodiodes.[10] Furthermore, the RTD of Zn into GaAs from a doped SiO_2 film has potential applications in the Zn-diffused junction stripe and the current blocking layer for laser diodes, and shallow p^+n junctions of the photodiodes on OEIC.

In this chapter, we present the results of RTD from Zn-doped

oxide films to n-type GaAs substrates, and the characteristics of the p^+ photodiodes fabricated by RTD of Zn, which is studied with spectral response and deep level transient spectroscopy. I propose the RTD with the junction depth controlled by a heating rate, and discuss the relation between depth profiles of Zn concentration and spectral response of photodiodes.

5.2 Device processing for GaAs photodiodes

The wafers used in this study were (100) Si-doped LEC n-type GaAs ($n \sim 3 \times 10^{17}$ cm^{-3}). Zn-doped oxide films with the thickness of 200 nm was formed on the wafer surfaces by spinning a solution consisting of alcohol, tetrahydroxysilane and carboxyester. Then these were placed face up on a Si wafer susceptor in flowing N_2 gas in a quartz tube and irradiated by a cylindrical array of tungsten halogen lamps. RTD of Zn was carried out at temperatures from 800 to 1000 °C for hold times of 0 and 6 s at diffusion temperatures with the heating rates of 10, 50 and 70 °C/s, and the sample was cooled without any control. The initial rate of cooling was about -30 °C/s. For comparison, Zn diffusion using the conventional furnace was also performed at 850 °C for 20 min. After Zn diffusion samples were etched in HF to remove the oxide films. To investigate the diffusion of Zn into GaAs by RTD the carrier profiles were estimated by an electrochemical C-V method. For the fabrication of photodiodes by RTD was performed at 850 °C for 0 and 6 s with the heating rates of 10, 30, 50 and 70 °C/s. Al and Au-Ge were alloyed onto

the p^+ layers and substrates, respectively, for ohmic contacts. The junction area of p^+n photodiodes is 1.67 mm^2.

5.3 Experimental diffusion profiles

The p^+n junction depth from the GaAs surface is shown in Fig. 5-1 as a function of the diffusion temperature, where the hold time at the diffusion temperature was 6 s. The junction depth is determined by a crosspoint of the bulk carrier concentration and the hole concentration of Zn-diffused layer, which are measured by the electrochemical C-V method. Zn diffusions to deeper position as the diffusion temperature increases, and the Zn concentration at the surface of the RTD

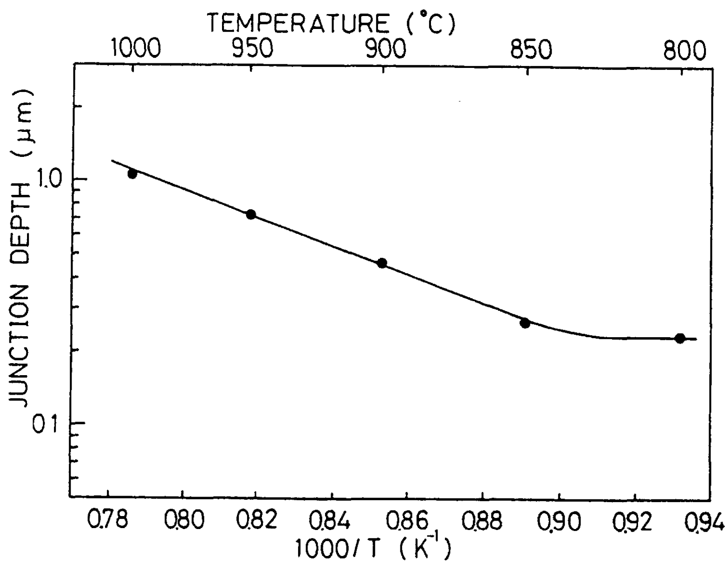

Fig.5-1. The temperature dependence of the junction depth in RTD-GaAs for 6 s with the heating rate of 50 °C/s.

sample at 800 °C (∿2 x 10^{18} cm^{-3}) is lower than other samples (∿ 2 x 10^{19} cm^{-3}). The diffusion temperature of 850 °C is appropriate to the fabrication of photodiodes by RTD, since the surface concentration is not quite fluctuating in the

temperatures over 850 °C, on the other hand the higher temperature above 900 °C are rather undesirable to prevent a surface degradation of GaAs crystals.

Almost all Zn atoms occupy the substitutional site in GaAs.[11] Hence the acceptor concentration profiles indicate the Zn concentration profiles. Figure 5-2 shows the Zn profiles obtained after RTD at 850 °C for 0 and 6 s, and the ordinary furnace diffusion at 850 °C for 20 min. It seems that the diffusion is forwarded in the heating or cooling stage of RTD, since the Zn profile after RTD is nearly independent on the hold time. Furthermore, the diffusion by the RTD is enhanced in comparison with the furnace diffusion. This result is consistent with that for GaAsP.[10] This anomalously rapid diffusion suggests that significant differences in the diffusion mechanism exist between RTD in heating or cooling period and conventional furnace diffusion. The anomalous Zn diffusion profiles in GaAs or the dependence of the effective diffusion coefficient on the impurity concentration by the furnace process have been explained assuming that the interstitial Zn is the dominant diffusing species and its concentration is controlled by the interstitial-substitutional equilibrium.[12,13] In rapid thermal processing (RTP) it has been reported that the diffusion coefficient of Ga in SiO_2 is found to be about two orders of magnitude larger than that for conventional furnace processing, and slight loss of As is observed.[14,15] It has been concluded that the RTP-induced thermal stress at the SiO_2/GaAs interface in the heating stage is responsible for this results. The RTP-induced stress are

estimated at 1.2×10^6 dyn/cm^2,[16] assuming that a temperature difference of 100 °C exists between GaAs and SiO_2 in the heating stage. This thermal stress is below the dislocation yield of GaAs. However, the RTP-induced stress may result in some defect production, such as divacancies,[17] or the rapid diffusion of Ga to SiO_2 film may produce the Ga vacancy in GaAs surface layer. Therefore, it is also expected that the diffusion coefficient of the substitutional species is not negligible. In addition, the radiation by halogen lamps changes the hole distribution in GaAs surface layer in the heating stage. It is speculated that the effective diffusion coefficient of Zn is increased by an increase of the hole activity coefficient.[12] Because each of the radiation power and the thermal stress in the heating stage of RTD is time-dependent, it is difficult to estimate the effective diffusion coefficient of Zn by RTD.

If the Zn diffusion is enhanced in the heating stage of RTD, the effective diffusion coefficient of Zn must increases with the heating rate. Figure 5-3 shows the profiles of Zn concentration obtained after RTD at 850 °C for 6 s with the heating rates of 10, 50 and 70 °C/s. Zn diffuses from the surface to a deeper position as the heating rate increases in spite of the shorter processing time.[18] This characteristics of Zn-RTD is important for device fabrication, since the p^+n junction depth is controlled without extending the short diffusion time of RTD and without elevating the diffusion temperature. Figure 5-4 shows the heating rate dependence of the junction depth of p^+n junction by RTD and conventional furnace diffusion. The p^+n junction depth increases as the heating rate increases.

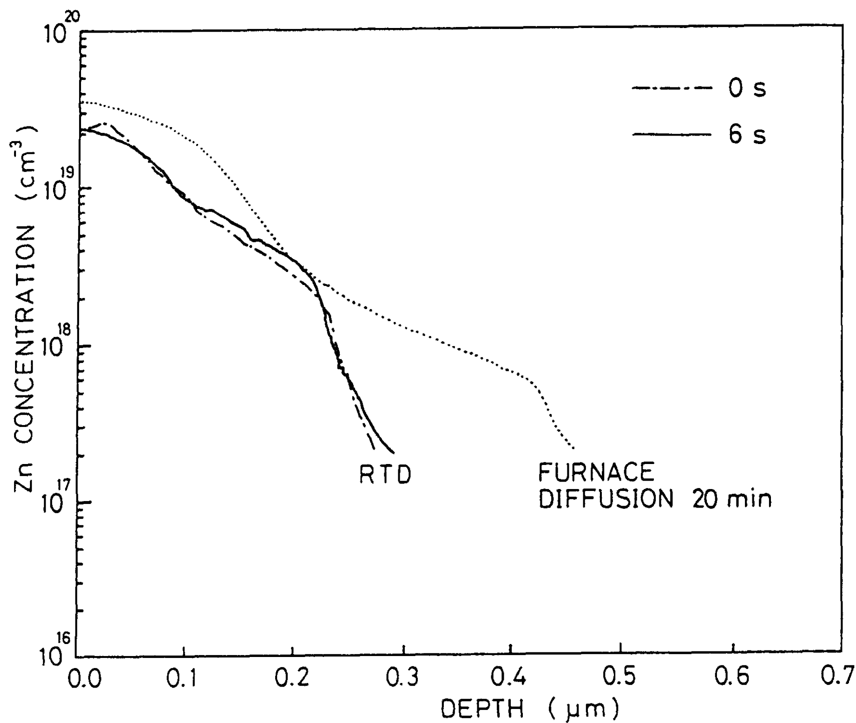

Fig.5-2. Zn concentration profiles of RTD samples at 850 °C with the heating rate of 50 °C/s and the furnace-diffused sample at 850 °C for 20 min.

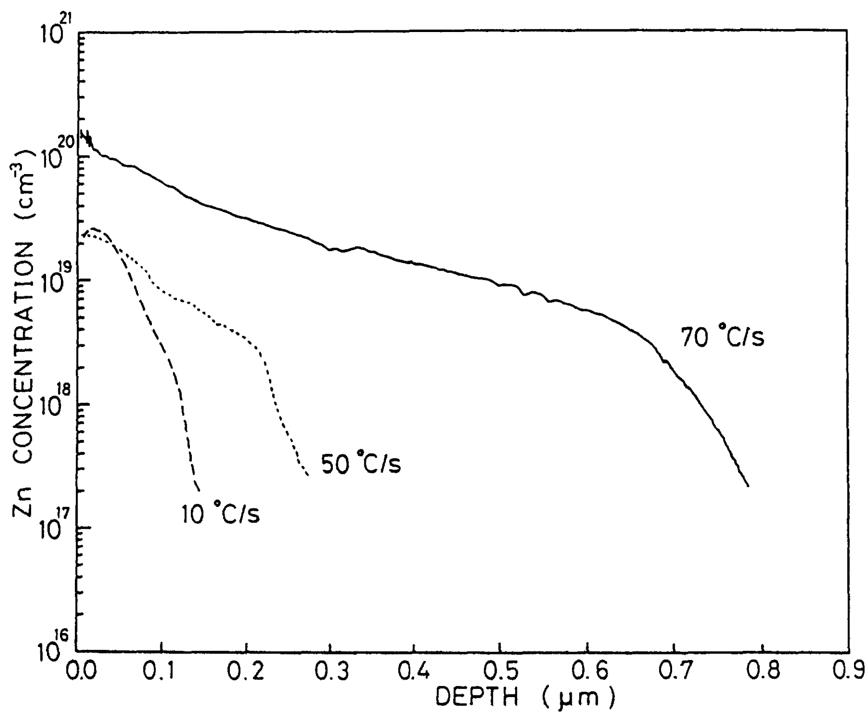

Fig.5-3. Zn concentration profiles for RTD at varying heating rates, 10, 50 and 70 °C/s. The diffusion temperature and hold time at diffusion temperature is 850 °C and 6 s.

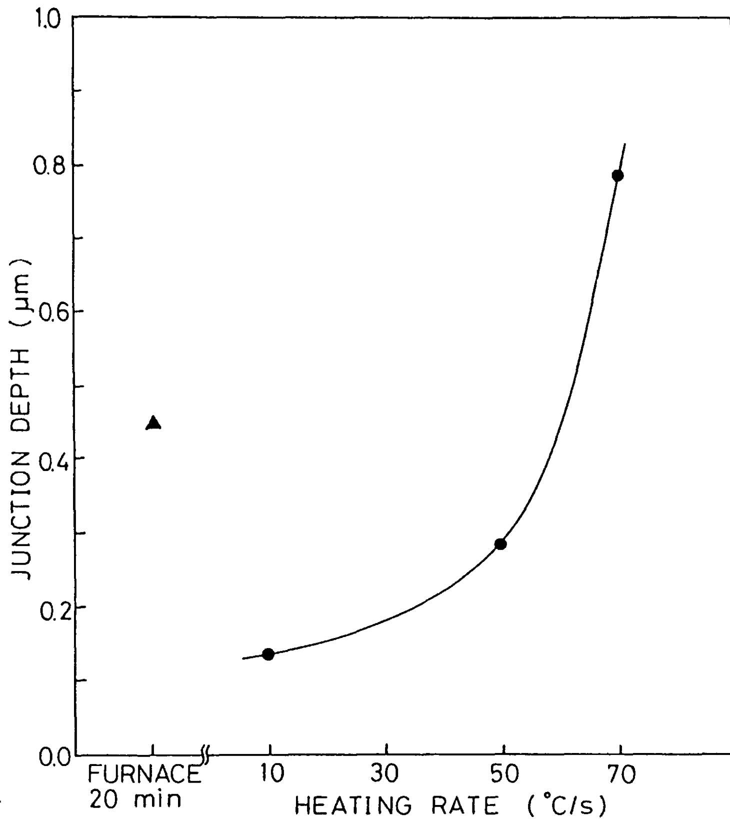

Fig.5-4. The heating rate dependence of the junction depth. RTD temperature and hold time are 850 °C and 6 s. The junction depth of the furnace-diffused sample at 850 °C for 20 min is also shown.

5.4 Characteristics of photodiodes fabricated by RTD

Figures 5-5(a) and 5-5(b) show the spectral responses as a function of heating rate of RTD at a diffusion temperature of 850 °C for the hold time of 0 s and 6 s, respectively. The spectral response slightly increases over the wavelength of 800 - 1000 nm as the heating rate increases. On the other hand, the large improvement in shorter wave length response is observed as the heating rate decrease. For comparison, the spectral response of photodiode formed by furnace diffusion is also shown in Fig. 5-6. The short and long wavelength response for the shallow junction are to be attributed mainly to an contribution from the p-type surface side and n-type bulk side, respectively. Therefore if the junction depth from the surface is decreased equally to a

reciprocal absorption coefficient at short wavelength, the short wavelength response for the shallow junction diode is improved by an increased contribution from the n-side. In addition, diffusion lengths L_n, L_p, minority carrier lifetimes τ_n, τ_p in both surface diffusion layer and bulk region, and surface

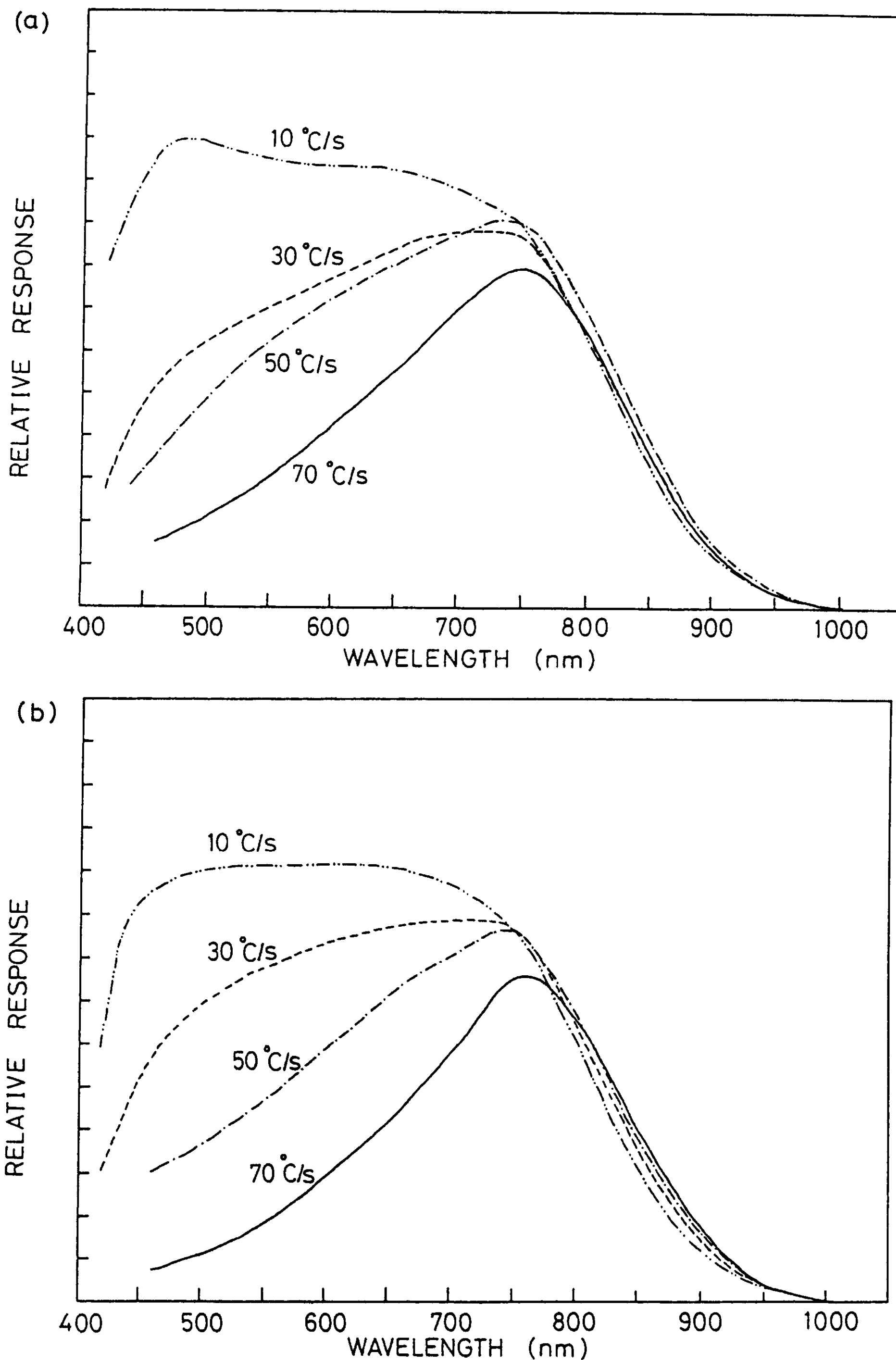

Fig. 5-5. Spectral responses of RTD photodiodes. RTD temperature and hold time are 850 °C and (a) 0 s, (b) 6 s, respectively.

recombination velocity S are important parameters to determine the spectral response curve. To investigate which of variables (L_n, L_p, τ_n, S) and junction depth X_j, attributes to significant effects in a spectral response of RTD photodiodes, an analysis by a numerical calculation has been made of the spectral response of GaAs photodiodes, in which the effect of the electric field present in the Zn diffused surface layer has been considered. We have used equations (5-1) - (5-5) reported by Dale and Smith[19] to obtain the theoretical response curves.

Bulk response :

$$I_b \fallingdotseq \frac{\exp(- \alpha X_j)}{1 + 1/(\alpha L_p)} \tag{5-1}$$

Surface response :

$$I_s = \frac{\dfrac{2 \exp(-X_j (M-m))}{1 + (m + S/Dn)/M} - \dfrac{\exp(- \alpha X_j)(\alpha + m + M)}{\alpha + 2m + S/Dn}}{\dfrac{\alpha + 2m}{\alpha + 2m + S/Dn} - \dfrac{1}{L_n^2 (\alpha + 2m + S/Dn)}} \tag{5-2}$$

$$M = \sqrt{m^2 + 1/L_n^2} \tag{5-3}$$

$$m = qE/(2kT) \tag{5-4}$$

$$SR = G (I_b + I_s) \tag{5-5}$$

,where E is the electric field in Zn-diffused layer, α is a absorption coefficient as a function of wavelength for GaAs, Dn is a diffusivity of electron in p-type surface layer, SR is a total response and G is a arbitrary gain. The field E is due to a very large impurity gradient in diffusion layers and aids the flow of minority carriers from the surface towards the junction.

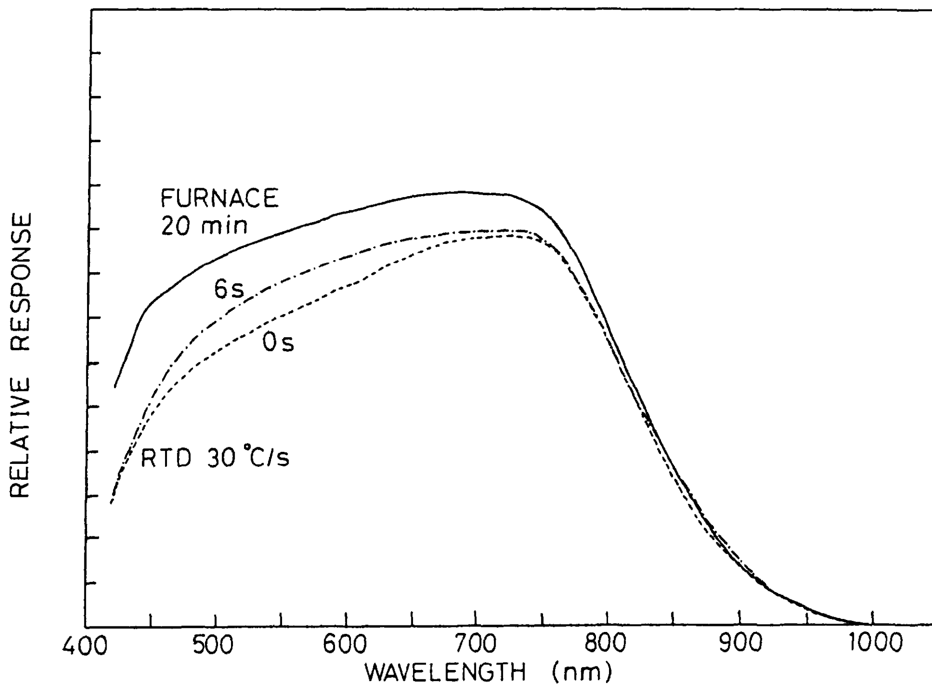

Fig.5-6. Spectral responses of photodiodes by the furnace diffusion at 850 °C for 20 min, and RTD for 0 and 6 s with the heating rate of 50 °C/s.

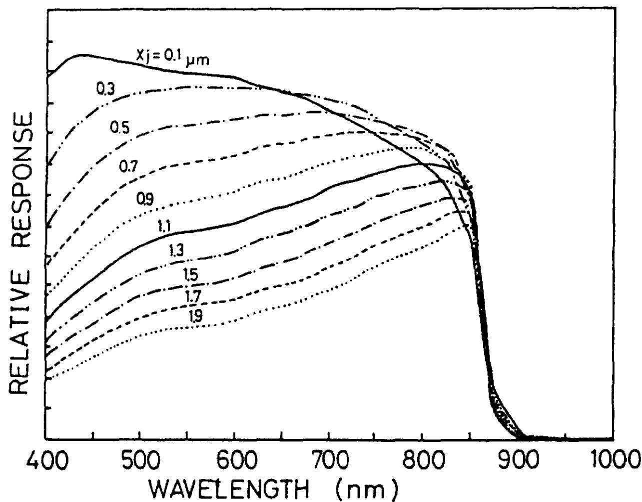

Fig.5-7. Calculated response curves. The surface concentration of acceptor C_s and the bulk concentration of donor C_b are 2×10^{19} and 3×10^{17} cm^{-3}, respectively. $L_p = L_n = 1$ μm. Dn = 100 cm^2/s. S = 1×10^7 cm/s.

This would give a increase of surface response in the shorter wavelength region. In Eqs. (5-1) - (5-5), it has been assumed that E has been constant across the diffusion layer, that is, the impurity concentration is an exponential function of X_j. E is approximately estimated by the junction depth X_j. Figure 5-7 shows the shift in calculated spectral response which would result from the photodiodes with different junction depths. The

shift of practical response curve given in Figs. 5-5(a) and (b) may be explained by the change of the junction depths.

Figure 5-8 is an example of the agreement obtained between theoretical and practical responses for the photodiode fabricated by RTD for 6 s with the heating rate of 10 °C/s. The surface and bulk region responses are also shown in this figure. The curve calculated for any value of parameters has not agreed with the practical curves in the wavelength of 800 - 1000 nm. Perhaps this difference between the practical and theoretical curves are due to the difference between absorption coefficient of the present samples and the data reported in Ref. 20, which are used for the calculation of the theoretical spectra, or a dependence of the lifetime on excessive carrier concentration. The best fit over the wavelength range of 400 - 800 nm has been obtained with the parameters : L_n, L_p, S listed in Table 5-I. The junction depths which are used in fitting are measured by the electrochemical C-V method. The value of L_p for the RTD diode

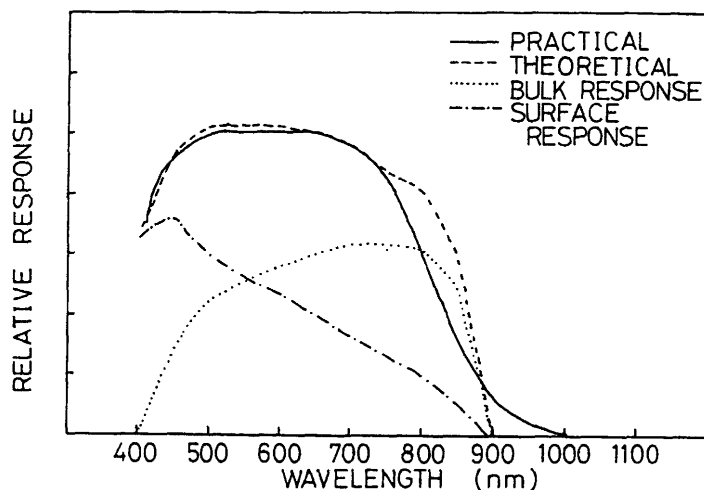

Fig.5-8. An example of the theoretical response curve fitted into the practical response for the photodiode by RTD for 6 s with the heating rate of 10 °C/s.

prepared by the heating rate of 70 °C/s is much smaller than that of the furnace-diffused one. It seems that the bulk region lifetime of the RTD diodes is decreased by the very high heating rate above 70 °C/s.

Table 5-I. Analysis of spectral responses by the curve fitting. Parameters : diffusion length of hole in the bulk region L_p, diffusion length of electron L_n and surface recombination velocity S in the surface region are obtained with the best fit of the theoretical curve in the wavelength of 400 - 800 nm.

Hold time (s)	Heating rate (°C/s)	L_p (μm)	L_n (μm)	S (cm/s)	X_j (μm)
6	10	7.2×10^{-1}	7.2×10^{-2}	1×10^{7}	0.14
6	50	7.2×10^{-1}	5.1×10^{-2}	1×10^{7}	0.29
6	70	1.1×10^{-2}	8.8×10^{-2}	1×10^{7}	0.79
0	50	3.6×10^{-1}	1.6×10^{-1}	1×10^{7}	0.27
20 min	(furnace)	5.1×10^{-1}	2.3×10^{-1}	1×10^{7}	0.45

Figure 5-9 shows typical DLTS spectra for electron traps in the heating rate of 70 °C/s. Four traps are observed, and three traps among them are identified with the trap EL6, EL5 and EL2.[21)] The thermal activation energy to the conduction band and capture cross section of the trap EZ are 0.57 eV and 5.9×10^{-12} cm^{-2}, respectively. The traps labeled EZ and trap EL2 are generated by RTD.[22-24)] These RTD-induced deep levels are possibly effective recombination centers in the photodiodes fabricated by the high heating rate of RTD, and reduce the bulk region lifetime.[25)] The electron traps induced by RTP are strongly dependent on the film thickness of SiO_2 encapsulant.[26)]

The generation of the deep levels by RTD may decreased by using the optimum thickness of Zn-doped SiO_2 film. It is suggested from the results shown in Table 5-I and the DLTS spectrum that the spectral response curve of RTD-photodiode prepared by the heating rate of 70 °C/s is under the influence of the degradation of the minority carrier lifetime in the bulk region. On the other hand, the shift in the spectral response of the RTD-photodiodes with increase of the heating rate to 70 °C/s is caused by the heating rate dependence of the junction depth.

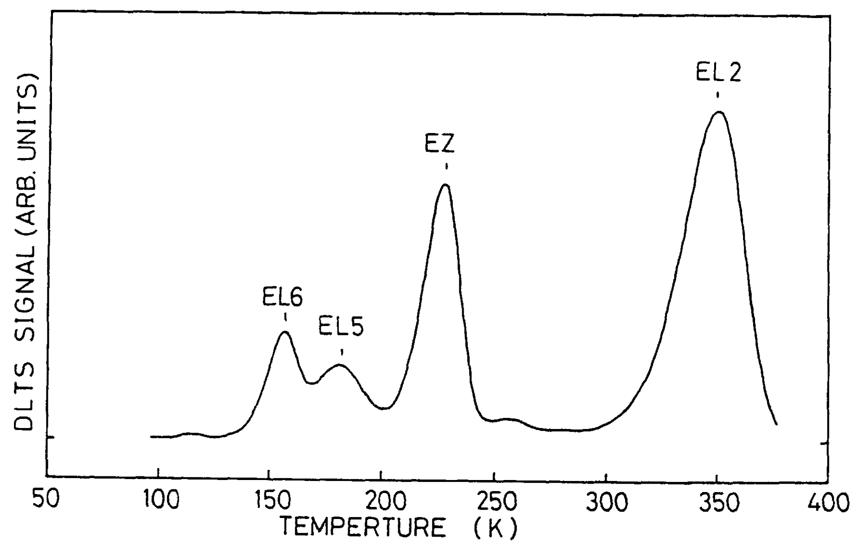

Fig.5-9. DLTS spectrum for electron traps in the bulk region of photodiodes by RTD for 6 s with the heating rate of 70 °C/s.

5.5 Numerical analysis of spectral response

The photodiode characteristics are considered to be sensitive to the parameters S, τ_n, L_p and diffusion profile.

To give the dependences of the spectral response of GaAs photodiodes on S, L_p, τ_n, surface Zn concentration C_s and bulk donor concentration C_b, spectral responses are calculated using the parameters around the values obtained from the experimental response curves and listed in Table 5-I. Figures 5-10, 5-11, and 5-12 show the calculated response curves for five different L_p, τ_n and six S values, respectively. The diffusion length L_p in Table 5-I were considered to be reasonably accurate since the response curves are quite sensitive to L_p, as shown in Fig. 5-10. The responses are, however, insensitive to S and τ_n, consequently S is subject to considerable error. No great significance is therefore to be attached to the large value of S in RTD-photodiodes.

The field E in the diffusion layer is dependent on the diffusion profiles of Zn. We have examined the effect of the electric field on the spectral response by using equations (5-1)-(5-5). Figures 5-13(a) and (b) show the surface and bulk concentration dependence of the spectral response. The sensitive GaAs photodiodes which have the very heavy surface concentration of Zn and low bulk concentration is expected to be formed by RTD.

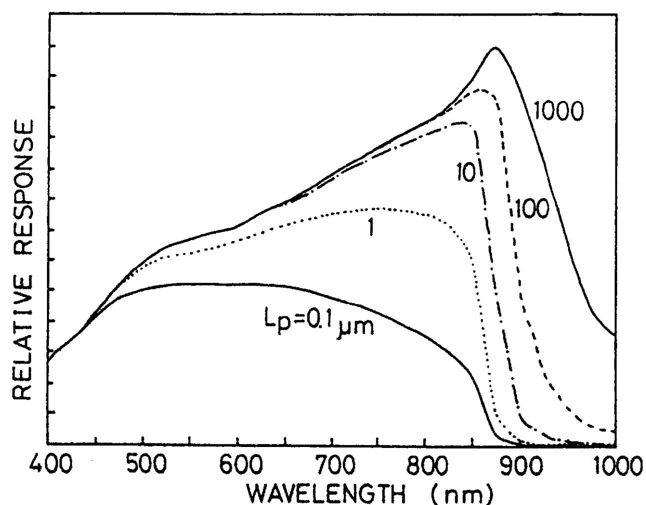

Fig.5-10. The L_p dependence of the spectral response calculated for X_j = 0.3 μm, L_n = 0.1 μm, D_n = 100 cm^2/s, S = $1x10^7$ cm/s, C_s = $2x10^{19}$ cm^{-3}, and C_b = $3x10^{17}$ cm^{-3}.

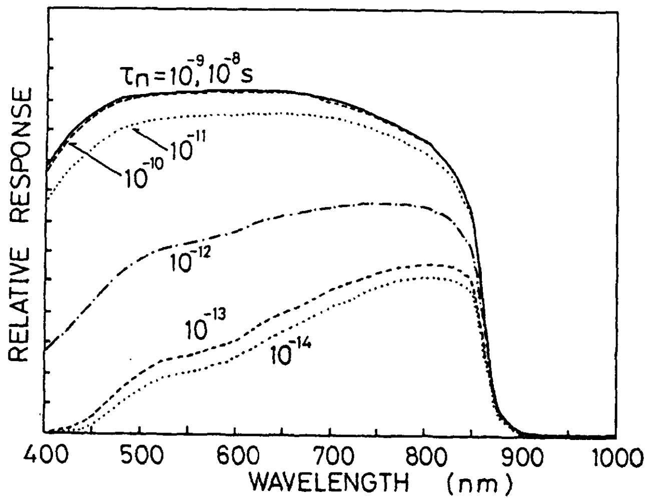

Fig.5-11. The τ_n dependence of the spectral response calculated for X_j = 0.3 μm, L_n = 0.1 μm, S = $1x10^7$ cm/s, C_s = $2x10^{19}$ cm^{-3}, and C_b = $3x10^{17}$ cm^{-3}.

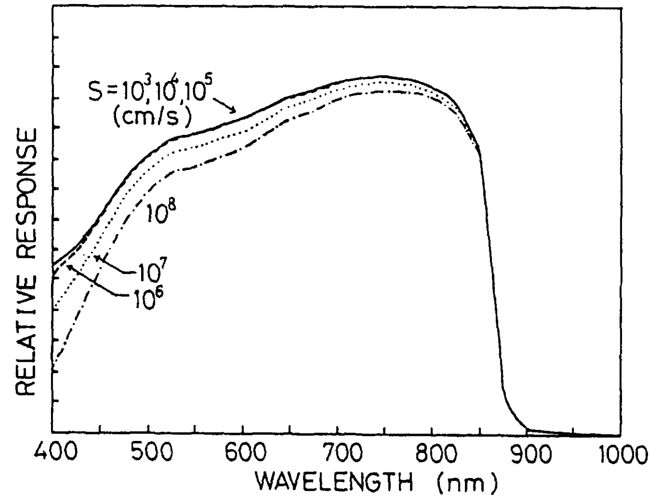

Fig.5-12. The effect of S on the spectral response calculated for the parameters : the junction depth X_j = 0.3 μm, L_p = 1 μm, L_n = 0.1 μm, Dn = 100 cm^2/s, C_s = $2x10^{19}$, and C_b = $3x10^{17}$ cm^{-3}.

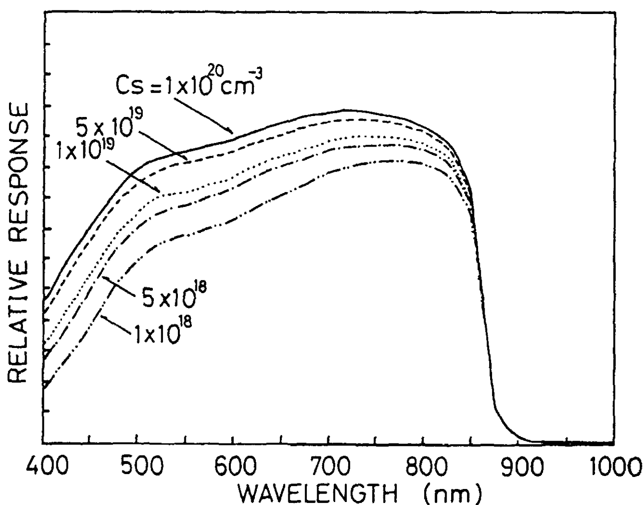

Fig.5-13(a). The surface concentration dependence of the spectral response calculated with the parameters : x_j = 0.3 μm, L_p = 1 μm, L_n = 0.1 μm, Dn = 50 cm^2/s, S = $1x10^7$ cm/s, and C_b = $1x10^{17}$ cm^{-3}.

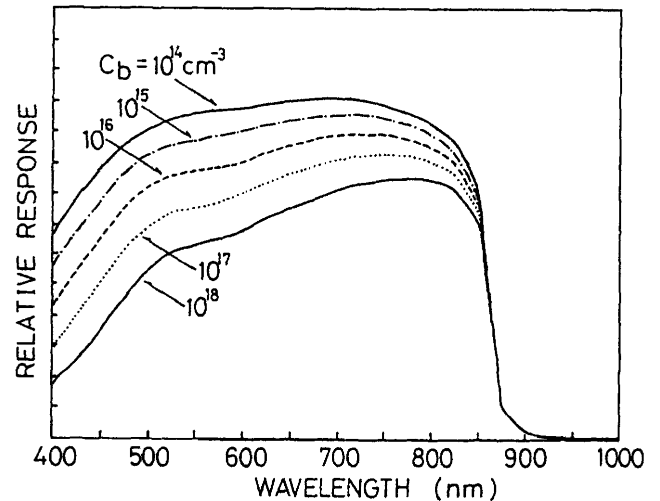

Fig.5-13(b). The bulk concentration dependence of the spectral response calculated for the parameters : x_j = 0.3 μm, L_p = 1 μm, L_n = 0.1 μm, Dn = 50 cm^2/s, S = $1x10^7$ cm/s, and C_s = $1x10^{19}$ cm^{-3}.

5.6 Summary

The properties of GaAs p^+n diodes fabricated by RTD of Zn into Si-doped GaAs from Zn-doped SiO_2 films were presented. The spectral responses of these photodiodes are dependent on the heating rate of RTD. In particular, the large improvement in the short wavelength response between 400 and 800 nm is observed as the heating rate decreases. Theoretical response curves are given for both p and n region, with diffusion length, lifetime of minority carriers, and surface recombination velocity as parameters. By curve fitting, it is concluded that the shift in the spectral response of the RTD-photodiode by increase of the heating rate so far as 70 °C/s is due to the heating rate dependence of the junction depth. In RTD with the rapid heating rate above 70 °C/s, the diffusion length in the bulk region is reduced by the generation of some deep levels. It is rather necessary to employ RTD with milder heating rate for the fabrication of GaAs photodiodes.

The sensitive GaAs photodiodes will be fabricated by the heavy surface concentration of Zn and low n-type bulk concentration, that is, the steep diffusion profile easily obtained by RTD is appropriate for the photodiodes.

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VI. CONCLUSIONS

In this study, the nature and distribution of the electrically active defects in rapidly thermal-annealed GaAs have been investigated. Deep levels arising from these defects or impurities are characterized by DLTS, and its spatial variations on wafer samples and depth profiles are obtained by the contactless measurement of optically injected excess carrier concentration by RMP method for SI GaAs substrates and the DLTS measurement for the large number of Schottky diodes per area on the electrically active layers.

In Chap II, the electrical characteristics and distribution of deep levels in Si-implanted (250 keV, 2 x 10^{13} cm^{-2} dose) n^+-type layers on SI substrates, activated by RTP are investigated. It is found that the trap NI2 (Ec - 0.55 eV) or EL2 (Ec - 0.78 eV) is most dominant electron trap in RTA samples over 800 °C, but in FA samples at 800 °C for 20 min, the EL2 concentration decreases and the trap NI2 is dominant. The notable spatial variation of NI2 concentration is observed across the wafer. It is proposed that the trap NI2 is created by the association of defects in the original substrate and implantation induced damage during high temperature ($\sim$800 °C) annealing. It is possible that the non-uniformity of NI2 concentration is settled by improvement in a perfection and purity of a LEC substrates. On the other hand, the peculiar spatial distribution of the EL2 concentration is not observed across the RTA sample. It seems that the fluctuation of EL2 concentration depends on the LEC growth condition and EL2 concentration is, however, screened by

the uniform EL2 production caused by Si implantation.

In Chap. III, variations of deep levels in MBE n-type GaAs layers by RTP have been studied with DLTS. Two electron traps N1 (Ec - 0.5 ∿ 0.7 eV) and EL2 are produced by RTP over 700 °C in MBE layer. The electron traps N2 (Ec - 0.36 eV) and N3 (Ec - 0.49 eV) are produced by RTP at 900 °C. The peculiar spatial distributions of N1 and EL2 are observed across the RTP layers. In particular, the EL2 distribution is found to be a W-shaped pattern. It is supposed that this shape of the spatial variation is consistent with that of the thermal stress induced by RTP. The thermal stress distribution has been computed by the thermoelastic model. The resolved shear stress on the (111) plane has been compared by the EL2 concentration, and the stress conversion coefficient has been determined as 2.36×10^6 ($dyn^{-1}cm^{-1}$). The plastic deformation and the change of stoichiometry also affect the EL2 concentration. The plastic deformation enhances the production of EL2 during RTP. The thermal stress should be suppressed below the yield of thermo-plastic deformation. The spatial variations of EL2 are suppressed by use of the guard ring composed of GaAs pieces, since it is effective to prevent the thermal stress during RTP, but EL2 remains at an uniform concentration of 10^{14} cm^{-3} across the RTP-layer. On the other hand, another dominant deep level N1 disappears by the use of the guard ring.

The evaluation of the defect distribution in the conductive and SI wafers is important for the integration of GaAs devices. In Chap. IV, in order to determine the spatial distributions of

the midgap defect concentration in LEC SI GaAs wafers, the reflectance-microwave-probe method using optically injected carrier is employed. The four-fold symmetrical distribution of EL2 in the (100) plane is observed after RTP. This distribution corresponds to the crystallographic slip generation pattern obtained from X-ray topography. The correlation between the pattern of the redistributing EL2 concentration and the slip generation in the RTP wafer also indicates that the EL2 is produced by the large thermal stress generated in RTP. The similar distribution of dominant generation-recombination centers and dislocations are observed in undoped LEC wafer before RTP, but are not observed in In-doped wafer.

In Chap. V, to dope Zn acceptor from Zn-doped oxide film to n-type GaAs substrates, RTP is applied. In order to investigate the diffusion of Zn into GaAs by RTP the carrier concentration profiles were estimated by an electrochemical C-V method. The the depth of p^+n junction is controlled by the heating rate of RTP without extending the diffusion time. Furthermore, the p^+n photodiodes fabricated by RTD of Zn were characterized with the analysis of spectral response curves and DLTS. The spectral response of photodiodes formed by RTD is strongly dependent on the heating rate. The improvement of the spectral response in the wavelength of 400 - 800 nm with decreasing the heating rate is mainly caused by the dependence of Zn diffusivity upon the heating rate. It is found from the analysis of the spectral response that the diffusion length of minority carrier in the bulk region is degraded by the generation of some defects in the photodiode fabricated by the RTD with the rapid heating rate over

70 °C/s.

Consequently, in order to prevent the RTP-induced thermal stress, the temperature gradient must be suppressed by the use of the guard ring on the wafer edge or forming an oxide ring on the wafer surface in the periphery to reduce the light reflectance from this region. RTP with the milder heating and cooling rates is a simple and effective method to suppress the large thermal stress. RTP at 800 °C or so, with regard for these conditions, is appropriate for the GaAs device processing, such as the activation of ion implants, defect annealing, and impurity diffusion to form shallow p^+n junctions.

Although this study would give a knowledge of electrically active defect production, elimination and defect distribution on the GaAs wafer during RTP, further investigations are needed for understanding the production mechanisms and the origin of defects. It is possibly expected that the electrical properties of the epitaxial wafers are controlled by the intentional and selective introduction of midgap center. In addition, it is important to study the effects of RTP on the insulator/GaAs- and hetero- interfaces.

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ADDENDUM

(i) PUBLICATIONS

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