Heteroepitaxial Growth of GaAs on Si by MOCVD

and

Its Application to Optoelectronic Devices

MOCVD法を用いた

Si上へのGaAsヘテロエピタキシャル成長

および

光電子デバイスへの応用

1991

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Chapter 1. Introduction

1.1 Background

In the past few years there has been growing interest in the heteroepitaxial growth of GaAs on Si (GaAs/Si)[1,2] using metalorganic chemical vapor deposition (MOCVD) or molecular beam epitaxy (MBE). The most important results of GaAs/Si study are the knowledge gained in heteroepitaxial growth that is applicable to other mismatched semiconductor materials (GaAs/InP, InP/GaAs, InP/Si, etc.)[3-6] and the numerous potential applications of the monolithic integration of GaAs and Si circuits[7-9]. More substantial benefits of monolithic GaAs/Si technology would be realized by monolithic integration of GaAs optoelectronic circuits and high-speed electronic circuits with Si very-large-scale integrated (VLSI) circuits. One potential application of monolithic GaAs/Si integration is in the fabrication of optical interconnections between Si VLSI chips, where signals are passed from chip to chip through optical interconnections rather than electrical wires. Another potential application is the integration of high-speed digital and microwave GaAs circuits with Si VLSI circuits to achieve greatly enhanced system performance.

The properties of Si and GaAs at 300 K are tabulated in Table I. The major advantages for the replacement of GaAs substrates by Si substrates are as follows:

Table I. Properties of Si and GaAs at 300 K.

	Si	GaAs
Mobility (cm^2/V-s)	1500	8500
Electron arrival velocity (cm/s)	1×10^7	3×10^7
Band gap energy (eV)	1.12	1.424
Thermal conductivity (W/K-cm)	1.5	0.46
Thermal expansion coefficient (°C^{-1})	2.6×10^{-6}	6.86×10^{-6}
Density (g/cm^3)	2.328	5.32
Lattice constant (nm)	0.5431	0.5653
Intrinsic resistivity (Ω-cm)	2.3×10^5	10^8
Dislocation density (cm^{-2})	0	$<10^5$
Band structure	Indirect	Direct
Crystal structure	Diamond	Zincblend
Mechanical strength	Strong	Fragile
Heterojunction	Difficult	Easy (AlGaAs)
Wafer size (inches)	≤8	≤4
Price	Cheap	Expensive

(1)Optical devices such as lasers and light emitting diodes (LED's) can be grown on GaAs because the band structure of GaAs is direct.

(2)High-speed digital and microwave circuits can be fabricated because the electron drift velocity of GaAs is about 5 times larger than that of Si.

(3)The low cost, large diameter and mechanical strength of Si make the GaAs processing compatible with developed Si technology.

(4)The higher thermal conductivity of Si is useful to dissipate heat from high power density devices such as power field effect transistors (FET's) and lasers.

(5)The lower density of Si is useful to solar cells, particularly those intended for space-based applications. The mass of the solar cell can be reduced.

However, there are some formidable obstacles that must be overcome in the materials in order to realize the above applications. The first is anti-phase domain generation due to the polar on nonpolar system[10-13]. The second is a high density of dislocations due to a 4.1 % difference in the lattice constants and a large difference in the thermal expansion coefficients between Si and GaAs[14,15]. The third is residual stress arising from the difference in the thermal expansion coefficients between Si and GaAs[16,17]. The fourth is the relatively low resistivity of undoped layers caused by unintentional Si autodoping[18-21]. The last is the roughness of the surface morphology[22-26].

1.2 Heteroepitaxial Growth of GaAs Layers on Si

Many threading dislocations originate at the GaAs/Si interface due to the difference in the lattice constants and the thermal expansion coefficients between Si and GaAs[14,15]. In the case of minority carrier devices such as lasers, solar cells and LED's, the threading dislocations form non-radiative recombination centers and dark-line defects that cause rapid degradation in the AlGaAs/GaAs optical devices[27,28]. Numerous dislocation reduction techniques have been attempted, including the use of a strained layer superlattice[29-33], in-situ and ex-situ thermal cycle annealing[34-36], and a combination of these techniques[37,38]. However, none of these techniques has successfully reduced the dislocation density to below 1×10^4 cm^{-2}, where the material becomes really useful for practical applications.

The thermal expansion mismatch between Si and GaAs introduces biaxial tensile stress manifested by wafer bowing during post-growth cooling. The tensile stress in the GaAs/Si can be on the order of 10^8-10^9 dyn/cm^2, depending on the growth temperature. MBE-grown GaAs/Si tends to have lower stress than MOCVD-grown GaAs/Si because of the lower growth temperatures. It is known that the stress applied to the active layer in the laser structure reduces the lifetime[27]. The large degree of bowing in the GaAs/Si is undesirable for the photolithography and processing of the

GaAs/Si LSI. To minimize the stress and bowing, selective area growth[39-44] and GaAs on a SOS (Si on sapphire) substrate[45,46] have been proposed. There have been reports that both stress and dislocation density are reduced within approximately 10 μm of the edge of selectively grown GaAs/Si[42]. It should also be noted that microcracking in the GaAs/Si due to stress can be suppressed by a selective area growth, which allows growth of a thicker layer. This results in the improved quality of the GaAs/Si. The growth of GaAs on SOS substrate is also effective in reducing the stress because of better matching of the thermal expansion coefficients. Recently, Sakai et al.[47] have proposed that more than one order of magnitude in the stress can be reduced by partially separating the GaAs layer from Si.

It is difficult to grow high resistivity undoped layers on Si using the MOCVD technique[18-21]. The carrier concentrations in the undoped GaAs layers on GaAs is near the 10^{14} cm^{-3} range. In contrast, MOCVD-grown undoped GaAs layers on Si have n-type conductivity, with carrier concentrations typically in the 10^{16}-10^{17} cm^{-3} range. The unintentional Si autodoping affects pinch-off characteristics of metal-semiconductor field-effect transistors (MESFET's) and high electron mobility transistors (HEMT's) on Si, which depend on the background doping of the undoped GaAs layers beneath the channel layers[48]. Freundlish et al.[19] have proposed "pipe" diffusion along the high density of threading dislocations.

They have shown that Si diffusion in the GaAs/Si is concentrated in channels with Si cores that correlate with the dislocation density. In addition to the pipe diffusion model, Azoulay et al.[20] and Nozaki et al.[21] have proposed gas phase transport of Si atoms to the growing layers. In order to obtain high resistivity undoped GaAs layers on Si, Kawarada et al.[49] have shown that the acceptor vanadium seems to be a suitable candidate as a deep level. George et al.[50] have also shown that the use of passivating layers such as SiO_2 and Si_3N_4 are useful to obtain the high resistivity undoped layers on Si. Egawa et al.[48] have recently fabricated an MOCVD-grown GaAs MESFET with a good pinch-off characteristic on SiO_2 back-coated Si.

1.3 Device Applications

One of the most cited applications of GaAs/Si is the optical input/output for Si ICs where signals are passed from chip to chip through optical signals rather than electrical wires. For this application, reliable GaAs optical components on a Si substrate must be developed[51-68]. Sakai et al.[51,52] have reported for the first time that an MOCVD-grown double heterostructure (DH) laser on Si has a pulsed threshold current density of 27 kA/cm^2 at room temperature. Room-temperature continuous-wave (cw) operation of an AlGaAs/GaAs quantum well heterostructure laser on Si has been reported by Deppe et al.[57,58], who

grew the buffer layer using the MBE technique and the laser structure using the MOCVD technique. They have obtained a cw threshold current density of 1.8 kA/cm^2 at room temperature. Chen et al.[60, 61], who used the MBE technique for the growth of the buffer layer and the laser structure, have also reported room-temperature cw operation. Very recently, by using thermal cycle annealing to reduce the threading dislocations, Choi et al.[64] and Egawa et al.[66-68] have reported room-temperature cw operation of all-MOCVD-grown AlGaAs/GaAs lasers on Si. Growth which uses MOCVD entirely is an advantage for large-scale production. In spite of recent progress, however, there is a serious problem in device lifetime. Even for the most reliable AlGaAs/GaAs lasers on Si so far reported[63], the cw threshold current increased by a factor of 3 in 10 h. This rapid degradation is caused by the formation and propagation of dark-line defects, which take place at high rates because the active layer on Si is not only subject to high tensile stress but also contains a high density of threading dislocations. Yamaguchi et al.[28] have fabricated high-efficiency solar cells on the GaAs/Si with total area efficiencies of 18.3 % (AM0) and 20 % (AM1.5).

Besides optical devices, the integration of GaAs and Si digital circuits can take advantage of the two IC technologies, i.e. the high speed of GaAs and the integrated Si process. The successful fabrication of MESFET's[48,69-79] and HEMT's[80-82] on Si makes sense as a first step in

applying this technology to manufacturing. Choi et al.[69] have reported that a 2.1-μm-gate-length GaAs MESFET on a Ge coated Si with a maximum transconductance of 105 mS/mm was fabricated using the MBE technique. Nonaka et al.[70] have reported 17 stage MESFET ring oscillators using the MOCVD technique. In order to grow high resistivity undoped GaAs layer, they used vanadium and a minimum propagation delay time of 51 ps/gate has been obtained at a power dissipation of 1.1 mW/gate. Fischer et al.[80] have grown an AlGaAs/GaAs HEMT on Si using the MBE technique. A transconductance of 170 mS/mm at 300 K, a maximum frequency of 24.5 GHz and a current gain cutoff frequency of 15 GHz have been obtained for a 1-μm-gate-length HEMT on Si. The most impressive result using GaAs/Si as yet is the fabrication of a 1-kbit SRAM consisting of enhancement/depletion (E/D) MESFET's at the LSI level[76]. An access time of 6-14 ns has been obtained for the GaAs/Si, which is a little inferior to that for the semi-insulating bulk substrate (4-12 ns). Choi et al.[8] have monolithically integrated a Si driver with 10 MOSFET's and an AlGaAs/GaAs LED. Shichijo et al.[9] have also demonstrated the integration of GaAs MESFET and Si CMOS circuits in a planal structure compatible with IC processing.

Thus, majority carrier devices provide some fruitful results and advantages over minority carrier devices. However, as will be mentioned in chapters 2 and 5, unintentional Si autodoping is a serious problem in

obtaining a good pinch-off characteristic for MOCVD-grown GaAs MESFET on Si. There has been little data concerning the effects of dislocations on the sidegating effect and uniformity of the electrical property, which are important for the GaAs LSI on Si.

1.4 Purpose and Organization of Dissertation

Although the GaAs/Si has numerous potential applications, there still remain some formidable obstacles that must be overcome in the materials and the device characteristics of the GaAs/Si. In order to realize the above applications, study of the effect of crystallinity on optical and electronic devices is necessary and important. The successful fabrication of lasers and MESFET's on the GaAs/Si grown entirely using the MOCVD technique makes sense as a first step in transforming the GaAs/Si into useful technology.

The dissertation is divided into six chapters, each of which is summarized below.

In chapter 2, heteroepitaxial growth and the characterization of GaAs layers on Si are described. It is shown that the crystallinity of the GaAs/Si is improved by using the $Al_{0.5}Ga_{0.5}As/Al_xGa_{1-x}P$ intermediate layers, and affected by the composition of x in the $Al_xGa_{1-x}P$ intermediate layer. The $Al_xGa_{1-x}P$ layer grows two-dimensionally on Si when the composition of x is greater

than or equal to 0.45. The $Al_{0.5}Ga_{0.5}As$ layer also grows two-dimensionally on the $Al_{0.55}Ga_{0.45}P/Si$. In this way, the best crystallinity of the GaAs layer has been obtained for the $GaAs/Al_{0.5}Ga_{0.5}As/Al_{0.55}Ga_{0.45}P/Si$ structure.

The main causes of fluctuation in the quantum well thickness are three-dimensional growth at the initial stage and threading dislocations. A combination of thermal cycle annealing and the $Al_{0.5}Ga_{0.5}As/Al_{0.55}Ga_{0.45}P$ intermediate layers is effective in obtaining smoother heterointerfaces on the GaAs/Si.

The effects of selective area growth on the reduction in the etch pit density (EPD) of the GaAs layers selectively grown on Si are discussed. The EPD decreases with the narrowing of the selective area. By using a combination of strained layer superlattice and thermal cycle annealing, a minimum EPD of 1.4×10^6 cm^{-2} can be obtained.

The unintentional Si autodoping can be reduced by using SiO_2 back coating. An additional mechanism involves gas phase reaction ($Si+H_2 \rightarrow SiH_4$) and transport of Si atoms to the heteroepitaxial layers during growth.

In chapter 3, laser diodes grown on Si are described. The topic is room-temperature cw operation of lasers on Si grown entirely using the MOCVD technique. Data are presented showing that the laser characteristics have been improved by use of the $Al_{0.5}Ga_{0.5}As/Al_{0.55}Ga_{0.45}P$ intermediate layers, compared with those grown by the two-step growth technique.

In chapter 4, Schottky diodes grown on Si are presented. The relationship between crystallinity and characteristics of Schottky diodes fabricated on the GaAs/Si with various intermediate layers has been studied. The best performances have been obtained for the GaAs/Si grown with the $Al_{0.55}Ga_{0.45}P$ intermediate layer. However, leakage current is observed under both reverse and small forward bias, which is caused by recombination and generation centers associated with a high density of threading dislocations in the GaAs/Si.

In chapter 5, GaAs MESFET's grown on Si are described. A combination of SiO_2 back-coated Si and higher growth temperature techniques has contributed to the successful fabrication of GaAs MESFET's on Si by the MOCVD technique. By using these techniques, a GaAs MESFET on Si has a good pinch-off characteristic, suppressed sidegating effect and microscopically uniform property.

In chapter 6, the summary of this research is described. The scope for future work is also presented.

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Chapter 2. Heteroepitaxial Growth of GaAs Layers on Si

2.1 Introduction

Heteroepitaxial growth of GaAs layers on Si has been attracting considerable attention because this technology has the numerous potential applications described in chapter 1. Gale et al.[1] first reported the GaAs layer on a Ge coated Si substrate because the lattice constant and the thermal expansion coefficient of Ge are almost the same as those of GaAs. Akiyama et al.[2] reported direct growth of the GaAs layer on Si, which is the most popular technique and is the so-called two-step growth technique. However, the GaAs/Si still has problems such as a high density of misfit and threading dislocations[3], roughness of surface morphology[4,5] and unintentional Si autodoping[6-8]. The threading dislocations, which are caused by the difference in the lattice constants and the thermal expansion coefficients between GaAs and Si, can act as non-radiative recombination centers in optical devices. The roughness of surface morphology of the GaAs/Si, especially those grown by the two-step growth technique, causes fluctuation in the thickness and roughness of the heterointerfaces. The fluctuation and roughness lead to degradation of the optical and transport properties of heterostructure devices[9,10]. The unintentional Si autodoping into the growing GaAs layers affects the carrier concentration level and the pinch-off

characteristic of GaAs metal-semiconductor field-effect transistors (MESFET's)[11]. In order to reduce the threading dislocations in the GaAs/Si, strained layer superlattice[12-14], in-situ and ex-situ annealing[15-17], selective area growth[18-20] and a combination of these techniques[21] have been proposed. It has also been reported that the surface morphology can be improved by using the $Al_{0.55}Ga_{0.45}P$ or $Al_{0.5}Ga_{0.5}As/Al_{0.55}Ga_{0.45}P$ intermediate layers[4,5] and that SiO_2 back coating is effective in suppressing unintentional Si autodoping[11,22].

In this chapter, the growth and characterization of GaAs layers on Si are described. This chapter is organized as follows: In section 2.2, the growth of GaAs layers on Si is described. The growth of AlGaAs/GaAs quantum wells on Si is presented in section 2.3. Selective area growth of GaAs layers on Si is described in section 2.4. In section 2.5, unintentional Si autodoping is presented. This chapter is concluded in section 2.6.

2.2 Heteroepitaxial Growth of GaAs Layers on Si

GaAs layers have been grown on Si by the two-step growth technique and by using some kinds of strained layer superlattices. However, the GaAs/Si reported previously have shown scalelike morphology. When heterostructure devices are grown on the GaAs/Si with rough surface morphology, the devices are degraded. As will be described

in chapter 3, single quantum well lasers on the GaAs/Si grown by the two-step growth technique have lower differential quantum efficiencies due to the roughness at the heterointerfaces. Noto et al.[4] have reported that the GaAs/Si with a specular surface morphology can be grown using the $Al_{0.5}Ga_{0.5}As/Al_{0.55}Ga_{0.45}P$ intermediate layers.

In this section, the heteroepitaxial growth and characterization of the GaAs/Si grown by the two-step growth technique and by using the $Al_xGa_{1-x}P$ and the $Al_{0.5}Ga_{0.5}As/Al_xGa_{1-x}P$ intermediate layers are discussed. The effects of the intermediate layers on crystallinity of the GaAs/Si are also discussed.

2.2.1 Experimental Procedure

All samples were grown on n-type Si substrates oriented 2° off (100) toward [011] in an RF-heated horizontal MOCVD reactor at atmospheric pressure. Trimethylgallium (TMG), trimethylaluminum (TMA), pure arsine (AsH_3) and phosphine (PH_3) were used as the Ga, Al, As and P sources, respectively. The substrates were degreased in organic solvents and then cleaned in $4H_2SO_4+H_2O_2$ and $HF+4H_2O$ solutions. Prior to the growth, the substrates were heated in H_2 atmosphere at 1000 ^oC for 10 min to remove native oxide from the substrate surface. The following describes the growth details of the samples used in this study. In the two-step growth technique, a GaAs layer with a thickness of 12.5 nm was first deposited at 400 ^oC with a V/III ratio

of 80. For the $Al_xGa_{1-x}P$ growth, the total molar fraction of group III element sources ([TMG]+[TMA]) was maintained at $1.4x10^{-4}$ and the ternary alloys of $Al_xGa_{1-x}P$ were grown with various values of x from 0 to 1 by changing their molar ratio ([TMA]/[TMA]+[TMG]). For the $Al_{0.5}Ga_{0.5}As$ growth, a 200-nm-thick $Al_{0.5}Ga_{0.5}As$ layer was grown at 700 ^oC with a V/III ratio of 70. The thickness of the GaAs top layers were kept 3 μm for all samples. The growth rate of the GaAs layer was 50 nm/min.

The surface morphology and crystallinity of the GaAs/Si were characterized by a Nomarski microscope, cross-sectional transmission electron microscopy (TEM), double crystal X-ray diffraction, photoluminescence at 4.2 K and etch pit density (EPD) revealed by molten KOH. The electrical property was obtained from Hall measurement using the van der Pauw method.

2.2.2 Characterization of GaAs/Si

First, the uniformity of the GaAs layer thickness on Si was studied. Figure 2.1 shows the uniformity of the GaAs layer thickness on Si grown at 750 ^oC using the two-step growth technique. The variation of the thickness was less than ± 5 %. To evaluate the electrical properties of the epitaxial layer, the Hall measurements at 77 K were performed for the GaAs/GaAs. The Hall mobility at 77 K has been obtained as 64300 and 38700 $cm^2/V\cdot s$ for the electron concentrations of $9.8x10^{14}$ and $2.4x10^{15}$ cm^{-3}, respectively.

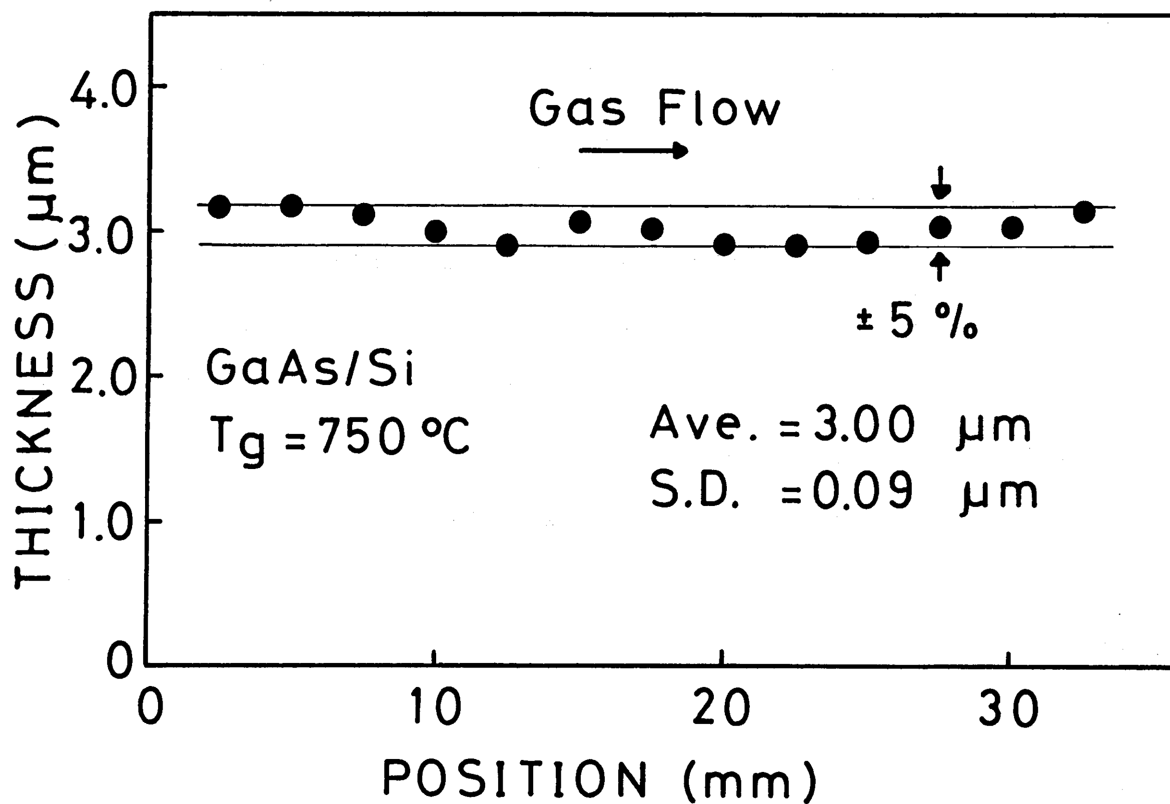
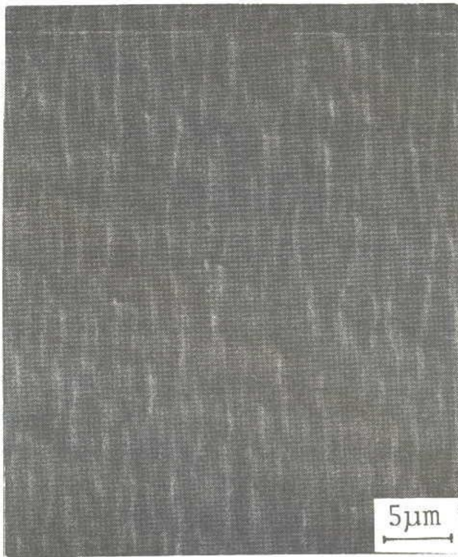


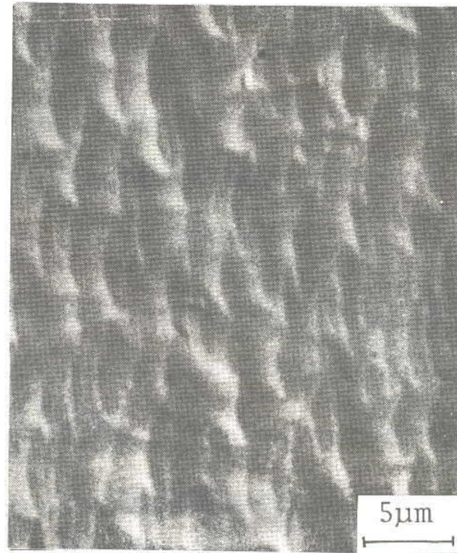
Fig. 2.1. Distribution of the GaAs layer thickness on Si grown at 750 °C by the two-step growth technique.

$GaAs/Al_XGa_{1-X}P/Si$ structures with various compositions (X) were studied. The lattice mismatch between GaP and Si is about 0.4 % and that between AlP and Si is about 0.6 %. The thicknesses of the GaAs and $Al_XGa_{1-X}P$ layers were 3 μm and 50 nm, respectively. In this structure, the growth of $Al_XGa_{1-X}P$ on Si is subjected to a small lattice mismatch, while growth of GaAs on $Al_XGa_{1-X}P$ is subjected to a large lattice mismatch. Figures 2.2 (a), (b), (c) and (d) show the surface morphology of the GaAs/Si grown by the two-step growth technique and using GaP, $Al_{0.45}Ga_{0.55}P$ and AlP intermediate layers. A surface of the GaAs/Si grown by the two-step growth technique and using the GaP intermediate layer shows scaly morphology with "treads and risers". When X is greater than or equal to 0.45, surface morphology becomes very smooth.

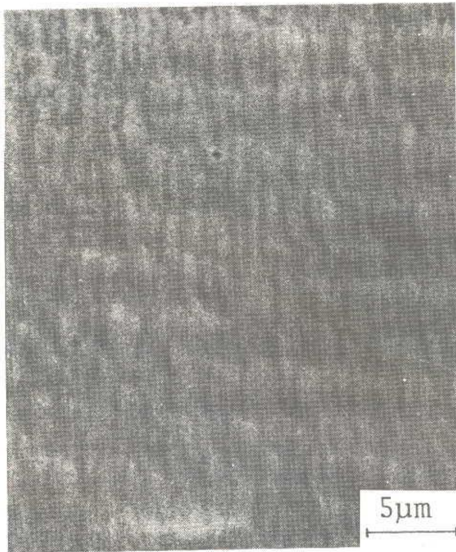
To interpret the results better, the samples were studied by cross-sectional TEM. The TEM micrographs in Figs. 2.3 (a), (b) and (c) represent the GaAs/Si grown by the two-step growth technique and with the GaP and the $Al_{0.55}Ga_{0.45}P$ intermediate layers, respectively. In the GaAs/Si grown by the two-step growth technique, threading dislocations originating at the GaAs/Si interface decrease as the surface is approached. At the initial stage of the GaAs growth, the GaAs grows three-dimensionally, and GaAs islands are formed. In the GaAs/Si grown with the GaP intermediate layer, dislocations originate at the GaAs/Si and GaAs/GaP interface and decrease as the surface is



(a) Two-step growth



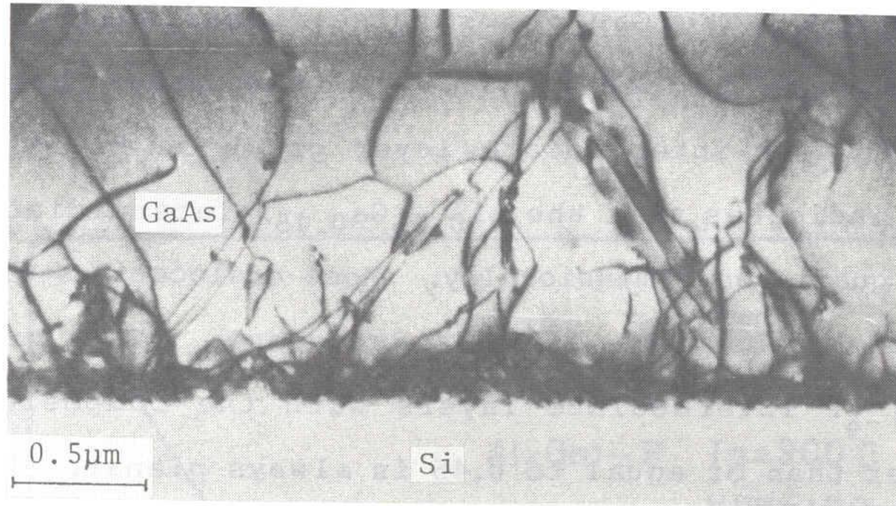
(b) GaP



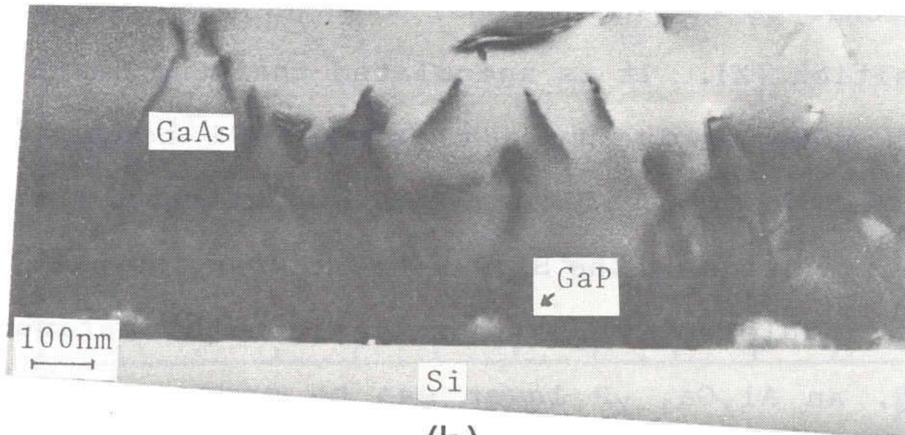
(c) $Al_{0.45}Ga_{0.55}P$

(d) AlP

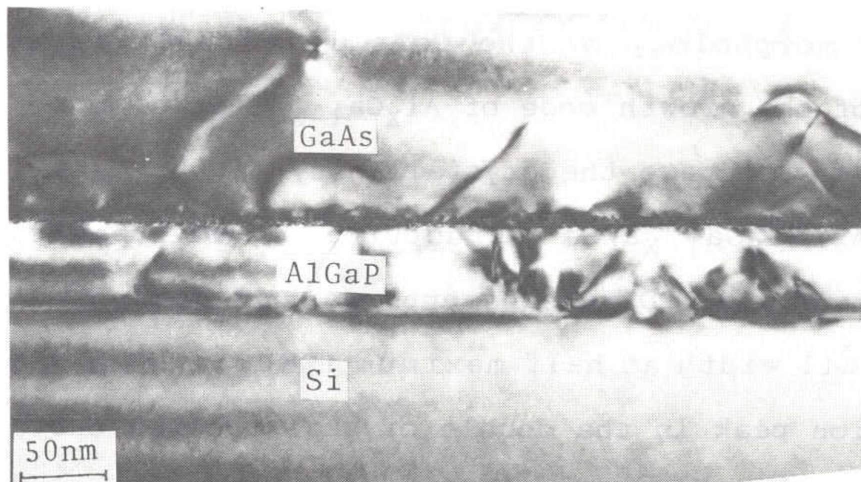
Fig. 2.2. Nomarski micrographs of the surface morphology of the GaAs/Si grown by (a) the two-step growth technique and using (b) GaP, (c) $Al_{0.45}Ga_{0.55}P$ and (d) AlP intermediate layers.



(a)



(b)



(c)

Fig. 2.3. Cross-sectional TEM micrographs of the GaAs/Si grown by (a) the two-step growth technique and using (b) GaP and (c) $Al_{0.55}Ga_{0.45}P$ intermediate layers.

approached. The GaP grows three-dimensionally and GaP islands are formed on Si. On the other hand, the $Al_{0.55}Ga_{0.45}P$ intermediate layer grown on Si is planar, which indicates that the $Al_{0.55}Ga_{0.45}P$ intermediate layer grows quasi-two-dimensionally. Most dislocations originate at the $GaAs/Al_{0.55}Ga_{0.45}P$ interface. The growth of $Al_XGa_{1-X}P$ intermediate layers with the composition (X) greater than or equal to 0.45 is always planar. It shows that the growth mode of $Al_XGa_{1-X}P$ changes from three-dimensional to two-dimensional with an increase in the AlP composition (X). It is speculated that the change of the growth mode is due to a strong Al-Si bond. Another possibility is that aluminum strongly attracts oxygen from the native oxide of the Si substrate when the native oxide is not completely removed by pre-growth heating. As a result, an $Al_XGa_{1-X}P$ layer can be grown on a fresh Si surface and nucleation can occur easily. The change of the surface morphology of the GaAs layer well reflects the change of the growth mode of $Al_XGa_{1-X}P$ layers on Si.

To investigate the crystallinity of the GaAs layers in the $GaAs/Al_XGa_{1-X}P/Si$ structure, double crystal X-ray diffraction and EPD measurements were performed. Figure 2.4 shows full width at half maximum (FWHM) of the X-ray (400) reflection peak in the double crystal rocking curve for the $GaAs/Al_XGa_{1-X}P/Si$ as a function of the AlP composition (X) in the $Al_XGa_{1-X}P$ intermediate layers. The FWHM is greatly affected by the AlP composition (X). With an increase in

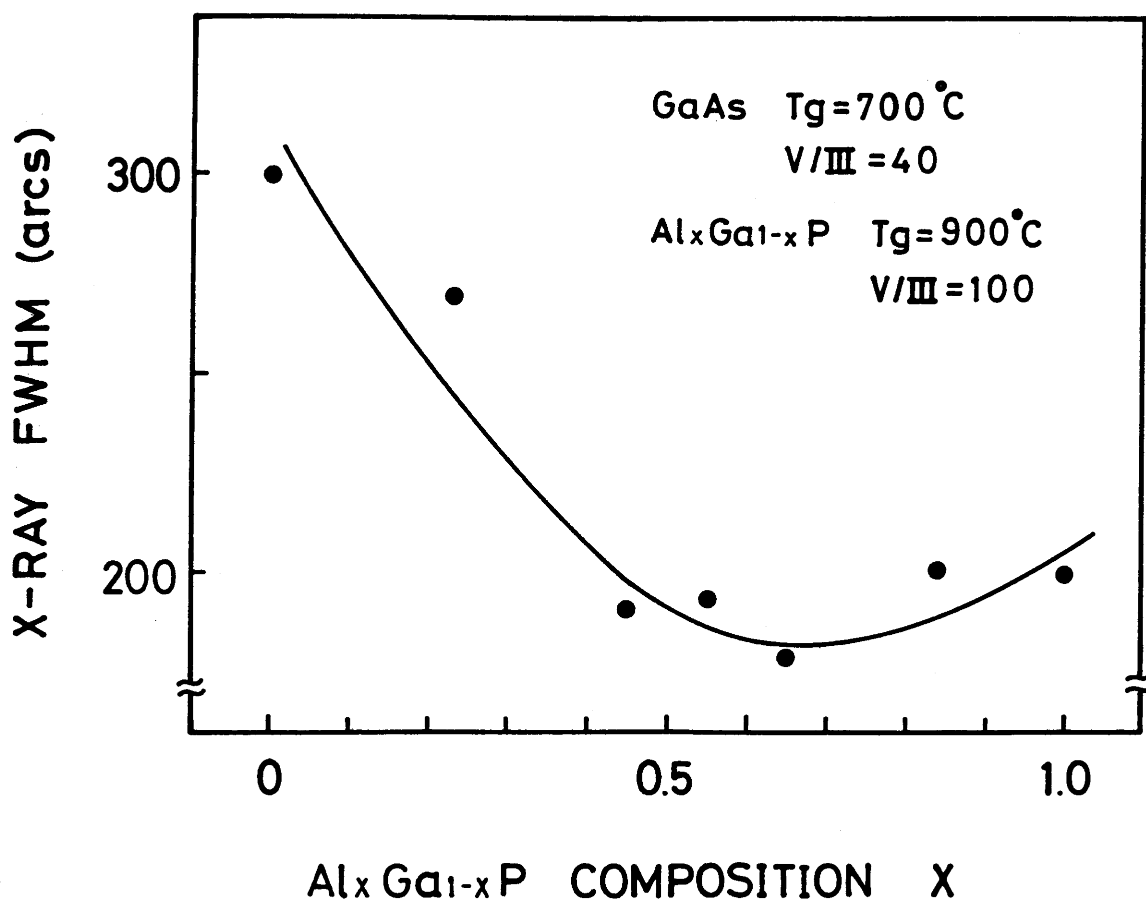


Fig. 2.4. X-ray FWHM of the GaAs/$Al_xGa_{1-x}P$/Si as a function of AlP composition (x) in the $Al_xGa_{1-x}P$ intermediate layer.

the AlP composition (X), the FWHM decreases drastically and it has a minimum value of 180 arcs when X is near 0.55. Once again this well reflects the transition of the growth mode of the $Al_XGa_{1-X}P$ layers on Si. For a higher AlP composition (X), the FWHM increases gradually. Figure 2.5 shows the EPD of the GaAs layer revealed by molten KOH etching as a function of the AlP composition (X). In the GaAs/GaP/Si structure, the EPD is about 7×10^7 cm^{-2}. It is almost the same EPD obtained by the conventional two-step growth technique. The EPD has a dependence on the AlP composition (X) similar to that seen in Fig. 2.4, and the EPD of 2.5×10^7 cm^{-2} is obtained when X is 0.55. It seems that more crystal defects are generated at the island boundaries at coalescence. At the transition of the growth mode from three-dimensional to two-dimensional, crystallinity of the GaAs layer is improved drastically. Above the AlP composition of 0.55, crystallinity of GaAs starts degrading with increases in the AlP composition. One possible explanation is that aluminum is very active with residual H_2O in source and/or carrier gases. Moreover, aluminum strongly attracts oxygen from SiO_2 since our MOCVD system consists of a quartz reactor and quartz wafer tray. It is considered that the oxidation of $Al_XGa_{1-X}P$ degrades crystallinity of the $Al_XGa_{1-X}P$ layer with a high AlP composition (X).

The optical properties of the GaAs/Si grown with the $Al_xGa_{1-x}P$ intermediate layer were studied by PL measurement

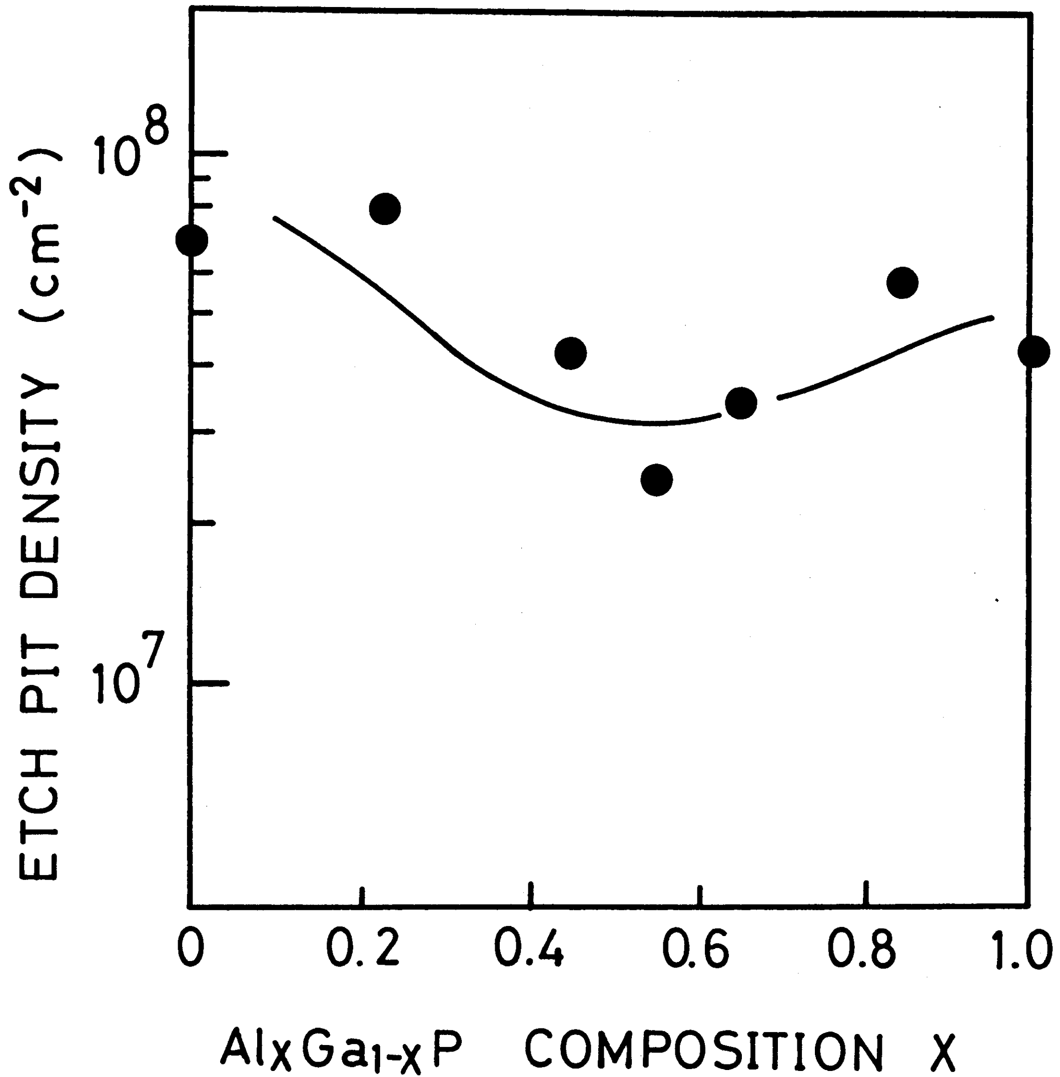


Fig. 2.5. EPD of the GaAs/$Al_xGa_{1-x}P$/Si as a function of the AlP composition (x) in the $Al_xGa_{1-x}P$ intermediate layer.

at 4.2 K. Figure 2.6 shows the FWHM of the exciton-related peak. The data obtained from the PL measurement support the findings that the crystallinity improves when x approaches 0.5.

From the above results, it is clear that crystallinity of the GaAs layer is strongly affected by the composition (X) in the $Al_XGa_{1-X}P$ intermediate layers. The best crystallinity of the GaAs layer was obtained when X is near 0.55 in the $GaAs/Al_XGa_{1-X}P/Si$ structure.

A 10-nm-thick GaAs was grown on the $Al_{0.55}Ga_{0.45}P/Si$ and the initial stage of the GaAs growth was studied by cross-sectional TEM. Figure 2.7 shows a cross-sectional TEM micrograph of the $GaAs/Al_{0.55}Ga_{0.45}P/Si$ structure. It shows that GaAs grows three-dimensionally on the planar $Al_{0.55}Ga_{0.45}P$ layer. The height of a GaAs island is about 50 nm. It seems that three-dimensional island growth degrades crystallinity of the GaAs layer. To avoid the three-dimensional growth of the GaAs, an $Al_{0.5}Ga_{0.5}As$ layer was grown as an additional intermediate layer between GaAs and $Al_{0.55}Ga_{0.45}P/Si$. This $Al_{0.5}Ga_{0.5}As$ layer on $Al_{0.55}Ga_{0.45}P/Si$ was characterized by cross-sectional TEM observation. Figure 2.8 shows a cross-sectional TEM micrograph of the $Al_{0.5}Ga_{0.5}As/Al_{0.55}Ga_{0.45}P/Si$ structure. The thicknesses of the AlGaAs and AlGaP layers were 10 nm and 50 nm, respectively. In spite of a large lattice mismatch (3.5 %) between $Al_{0.5}Ga_{0.5}As$ and $Al_{0.55}Ga_{0.45}P$, the $Al_{0.5}Ga_{0.5}As$ is found to grow on $Al_{0.55}Ga_{0.45}P/Si$ two-

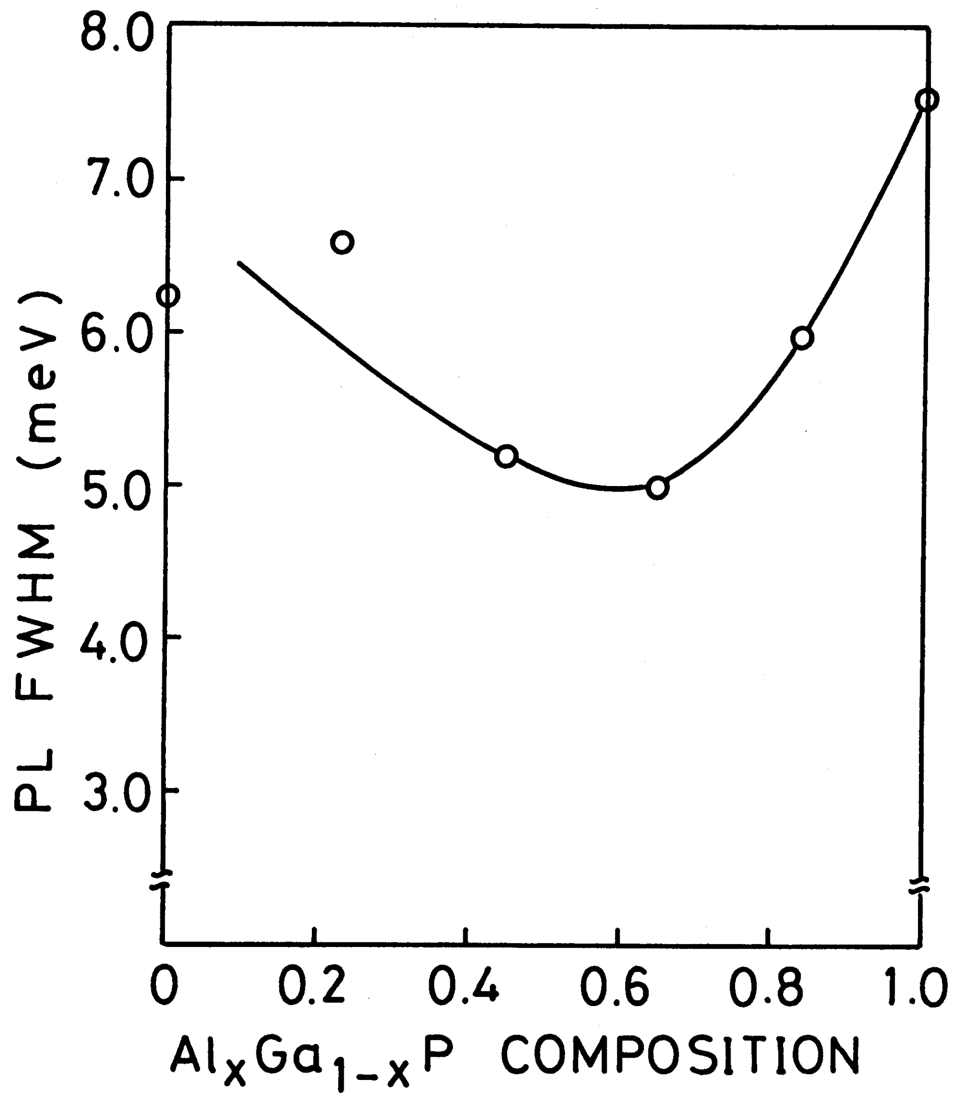


Fig. 2.6. FWHM obtained from PL spectra at 4.2 K for the $GaAs/Al_xGa_{1-x}P/Si$ as a function of the AlP composition (x) in the $Al_xGa_{1-x}P$ intermediate layer.

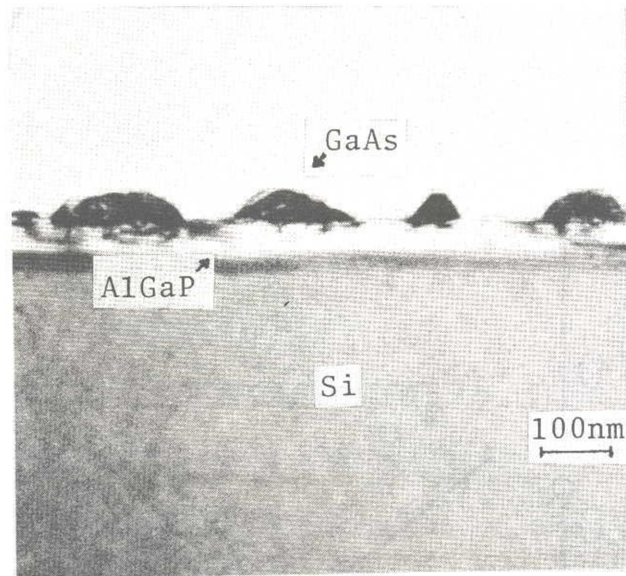


Fig. 2.7. Cross-sectional TEM micrograph of the $GaAs/Al_{0.55}Ga_{0.45}P/Si$.

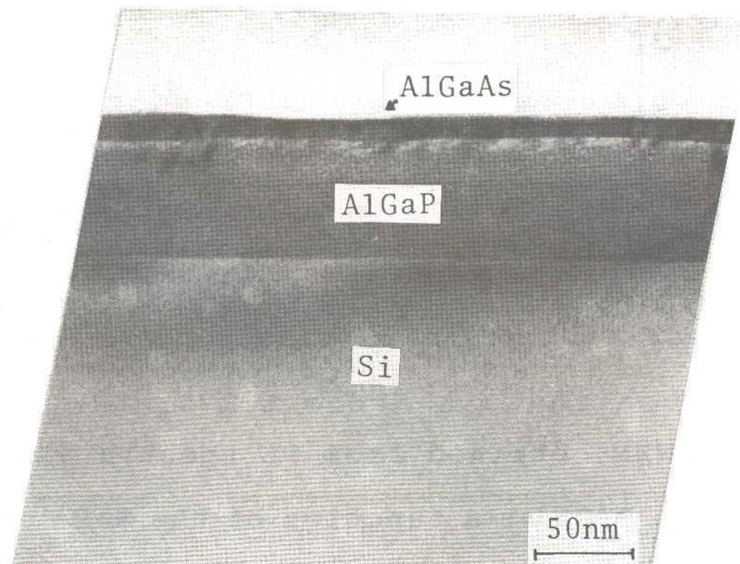


Fig. 2.8. Cross-sectional TEM micrograph of the $Al_{0.5}Ga_{0.5}As/Al_{0.55}Ga_{0.45}P/Si$.

dimensionally from the TEM observation. Since the GaAs layer is expected to grow two-dimensionally on the AlGaAs layer, every epitaxial layer is found to be grown two-dimensionally in the GaAs/$Al_{0.5}Ga_{0.5}As$/$Al_{0.55}Ga_{0.45}P$/Si structure.

A 200-nm-thick $Al_{0.5}Ga_{0.5}As$ layer was grown between GaAs and $Al_{0.55}Ga_{0.45}P$/Si. Figure 2.9 shows the surface morphology of the GaAs layer in the GaAs/$Al_{0.5}Ga_{0.5}As$/$Al_{0.55}Ga_{0.45}P$/Si structure. The surface morphology is smoother than that of the GaAs layer directly grown on $Al_{0.55}Ga_{0.45}P$/Si. In order to further improve crystallinity of the GaAs layer, thermal cycle annealing was performed. When a 1.0-μm-thick GaAs layer was grown on $Al_{0.55}Ga_{0.45}P$/Si, the substrate was cooled down to 300°C and then heated up to 800°C. The thermal cycle annealing was repeated three times in AsH_3/H_2 atmosphere. After the thermal cycle annealing, another 2.0-μm-thick GaAs layer was grown. Table I shows the FWHMs of the X-ray (400) reflection peak in the double crystal rocking curve for GaAs/AlGaP/Si and GaAs/AlGaAs/AlGaP/Si structures. The FWHM was reduced from 191 arcs to 161 arcs by introducing an $Al_{0.5}Ga_{0.5}As$ intermediate layer and it was further reduced to 126 arcs by the thermal cycle annealing. Figures 2.10 (a) and (b) show cross-sectional TEM micrographs of the GaAs/$Al_{0.5}Ga_{0.5}As$/$Al_{0.55}Ga_{0.45}P$/Si structure without and with the thermal cycle annealing, respectively. In Fig. 2.10 (a), many dislocations are observed in the AlGaAs

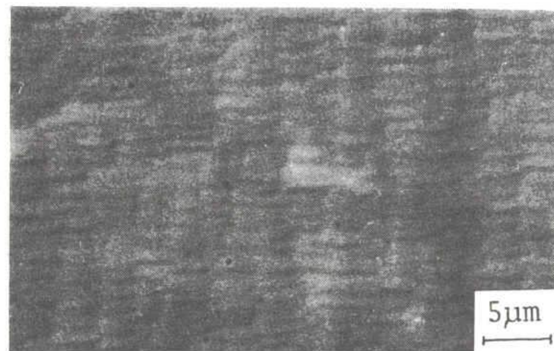
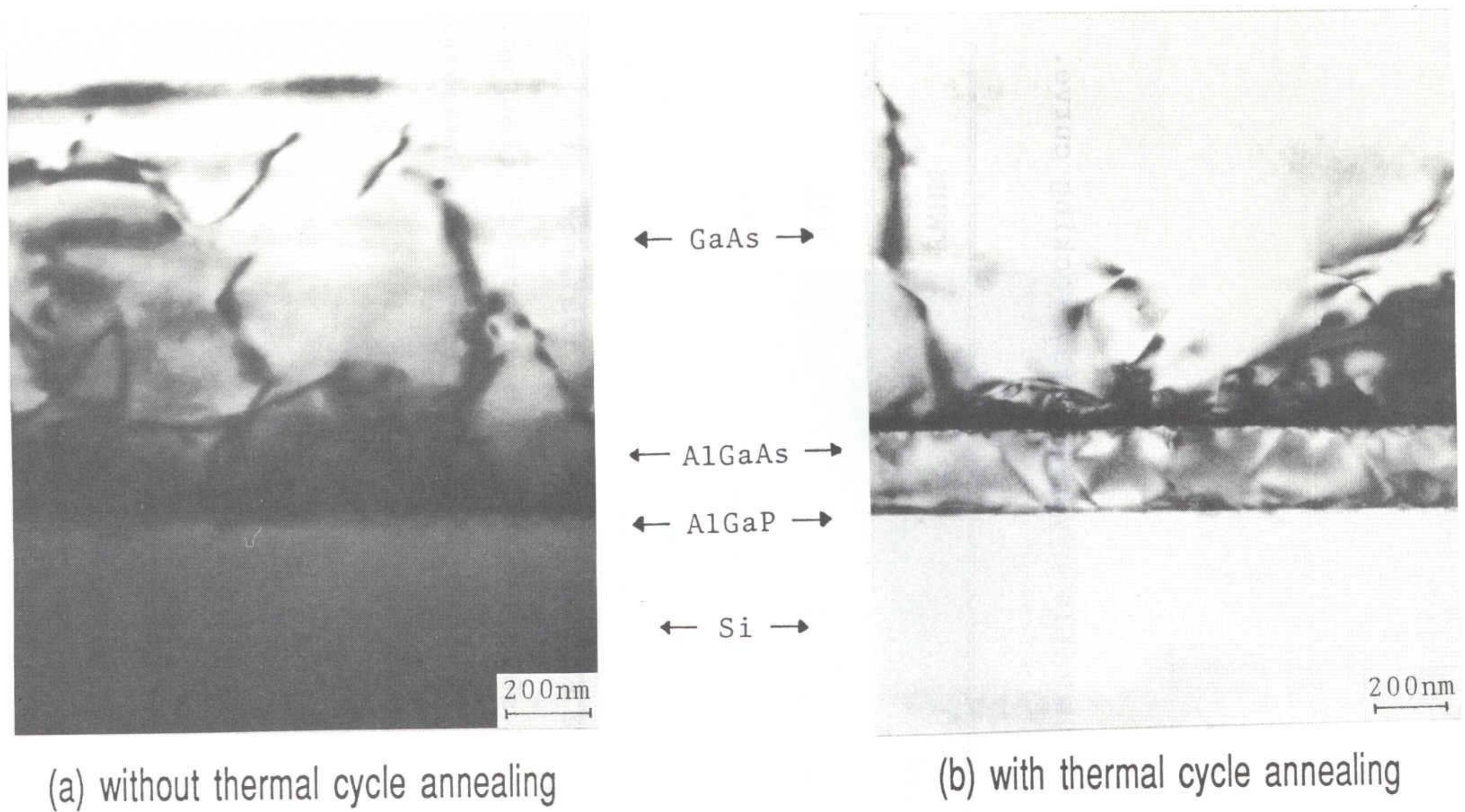


Fig. 2.9. Nomarski micrographs of the surface morphology of the GaAs/Si grown with the $Al_{0.5}Ga_{0.5}As/Al_{0.55}Ga_{0.45}P$ intermediate layers.

Table I. FWHMs of double crystal X-ray rocking curve.

structure	FWHM (arcs)
$GaAs/Al_{0.55}Ga_{0.45}P/Si$	191
$GaAs/Al_{0.5}Ga_{0.5}As/Al_{0.55}Ga_{0.45}P/Si$	161
$GaAs/Al_{0.5}Ga_{0.5}As/Al_{0.55}Ga_{0.45}P/Si$ with thermal cycle annealing	126



(a) without thermal cycle annealing

(b) with thermal cycle annealing

Fig. 2.10. Cross-sectional TEM micrographs of the $GaAs/Al_{0.5}Ga_{0.5}As/Al_{0.55}Ga_{0.45}P/Si$ (a) without and (b) with

layer, and some intrude into the GaAs layer. It is clear that the number of dislocations in the GaAs layer was reduced by the thermal cycle annealing, as seen in Fig. 2.10(b).

2.3 Growth of AlGaAs/GaAs Quantum Wells on Si

Heterostructure devices such as quantum well lasers and high electron mobility transistors (HEMT's) have been fabricated on Si using MOCVD and MBE techniques. It is known that variation of band gap with distance through the interface, fluctuation in the thickness and roughness of the heterointerface affect the optical and transport properties of heterostructure devices. The GaAs/Si, especially if it is grown by the two-step growth technique, shows roughness in the surface morphology. As a result, the heterostructures on Si show fluctuation in thickness and roughness of the heterointerfaces. The fluctuation and roughness lead to degradation of laser performances[9,10], namely, higher threshold current, lower differential quantum efficiency and shorter device lifetime. In the HEMT's on Si, they cause electron scattering and result in decreasing mobility of two-dimensional electron at the heterointerface.

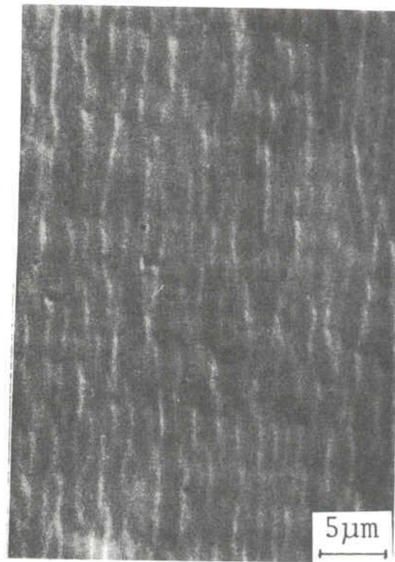
In this section, AlGaAs/GaAs single quantum wells (SQW's) on Si grown by the two-step growth technique and using the $Al_{0.5}Ga_{0.5}As/Al_{0.55}Ga_{0.45}P$ intermediate layers are investigated.

2.3.1 Experimental Procedure

The $Al_{0.3}Ga_{0.7}As/GaAs$ SQW's were grown on Si in an atmospheric pressure MOCVD reactor using the two-step growth technique and the $Al_{0.5}Ga_{0.5}As/Al_{0.55}Ga_{0.45}P$ intermediate layers. In the two-step growth technique, a 12.5-nm-thick GaAs layer was deposited on Si at 400 ^{o}C with a V/III ratio of 80. For the AlGaAs/AlGaP intermediate layers, a 50-nm-thick $Al_{0.55}Ga_{0.45}P$ layer was grown on Si at 900 ^{o}C with a V/III ratio of 100, and a 200-nm-thick $Al_{0.5}Ga_{0.5}As$ layer was grown at 750 ^{o}C with a V/III ratio of 70. The $Al_{0.3}Ga_{0.7}As/GaAs$ SQW's were grown at 750 ^{o}C. The SQW's consisted of GaAs layers with well thicknesses from 2.5 to 25 nm separated by 50-nm-thick $Al_{0.3}Ga_{0.7}As$ barriers. The SQW's were located 2 μm away from the substrate surface. For comparison, SQW's with the same structure were grown on GaAs. The SQW's were studied using photoluminescence at 4.2 K and cross-sectional TEM. The 514.5 nm line of an argon laser whose beam intensity was about 8 mW was focused onto the sample surface. The excitation density was about 255 mW/cm^2.

2.3.2 Characterization of Quantum Wells

Nomarski micrographs of the surface morphology of the SQW's on Si, grown by the two-step growth technique and with AlGaAs/AlGaP intermediate layers are shown in Figs. 2.11 (a) and (b), respectively. The surface morphology of the SQW's on Si grown by the two-step growth technique is scaly with a



(a) Two-step growth

(b) AlGaAs / AlGaP

Fig. 2.11. Nomarski micrographs of the surface morphology of the SQW's on Si grown by (a) the two-step growth technique and with (b) the $Al_{0.5}Ga_{0.5}As/Al_{0.55}Ga_{0.45}P$ intermediate layers.

periodic "tread and riser". In contrast, the SQW's on Si grown with the AlGaAs/AlGaP intermediate layers show smoother surface morphology. Scalelike steps in the surface are decreased using the AlGaAs/AlGaP intermediate layers. In the two-step growth technique, as described in section 2.2, the GaAs grows three-dimensionally and GaAs islands are formed on Si, which result in scalelike morphology. In the AlGaAs/AlGaP intermediate layers, on the other hand, the $Al_{0.55}Ga_{0.45}P$ layer grows two-dimensionally on Si. The two-dimensional growth of the $Al_{0.45}Ga_{0.55}P$ layer on Si results in specular surface morphology of the SQW's on Si grown with the intermediate layers.

Figure 2.12 shows the PL spectra at 4.2 K of the SQW's with three single quantum wells on Si grown with the AlGaAs/AlGaP intermediate layers. Figure 2.13 shows the full width at half maximum (FWHM) obtained from the PL spectra at 4.2 K as a function of the quantum well thickness for the SQW's on GaAs and Si substrates grown by the two-step growth technique and with the AlGaAs/AlGaP intermediate layers. The FWHM values of the SQW's on GaAs are 11.9, 7.1 and 3.7 meV for the well thickness of 2.5, 5.0 and 10 nm, respectively. In the case of the SQW's on Si without thermal cycle annealing, the FWHM values are 45.7, 35.3 and 21.7 meV for the two-step growth technique and 38.0, 28.2 and 14.7 meV for the AlGaAs/AlGaP intermediate layers, respectively. This result indicates that the heterointerfaces on Si grown with the AlGaAs/AlGaP

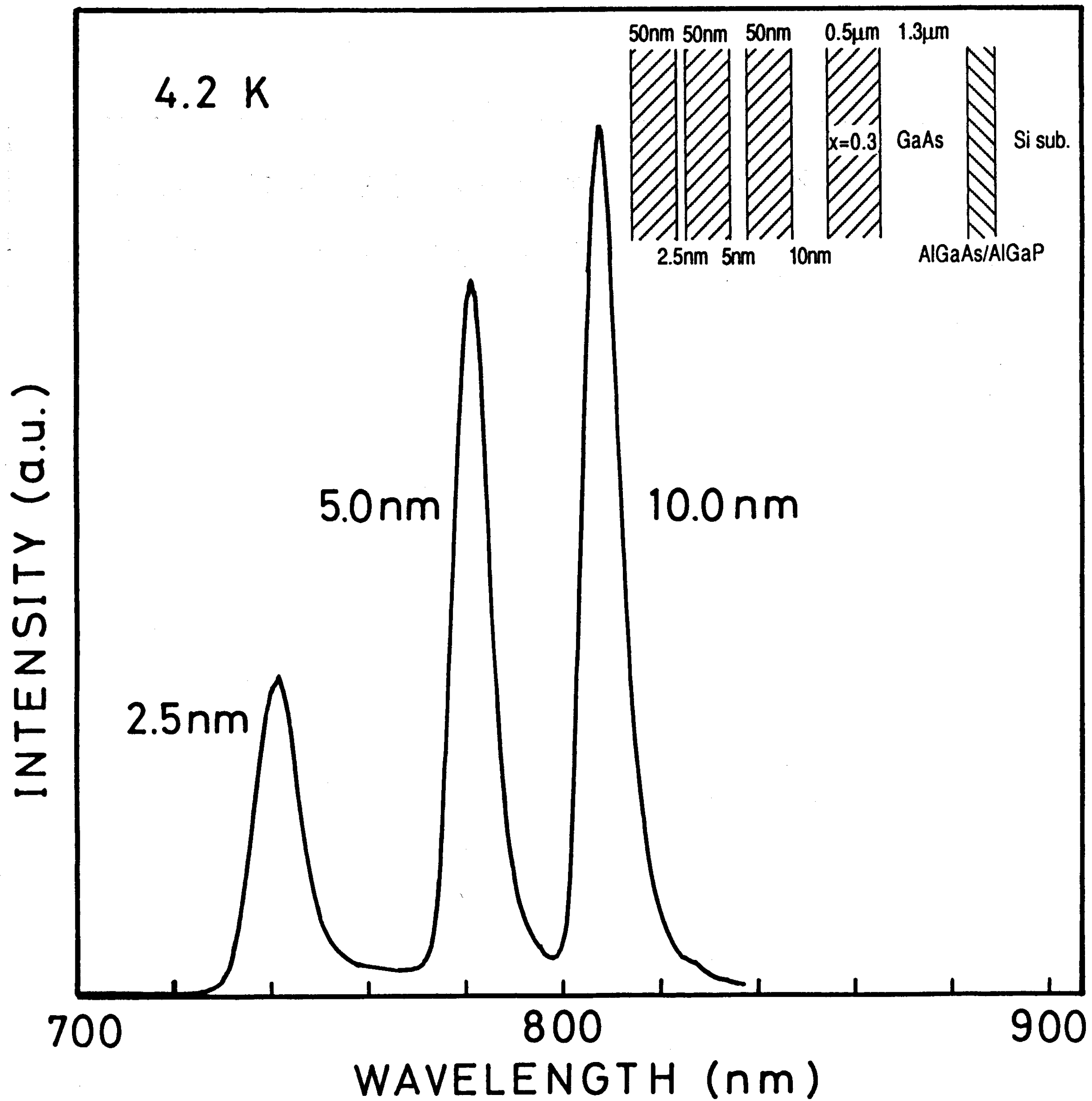


Fig. 2.12. Photoluminescence spectra at 4.2 K of the SQW's on Si grown with the $Al_{0.5}Ga_{0.5}As/Al_{0.55}Ga_{0.45}P$ intermediate layers. The SQW's consist of three single quantum wells with the thickness of 10.0, 5.0 and 2.5 nm, in order from the Si substrate. The $Al_{0.3}Ga_{0.7}As$ barriers are 50 nm thick, as is shown in the inset.

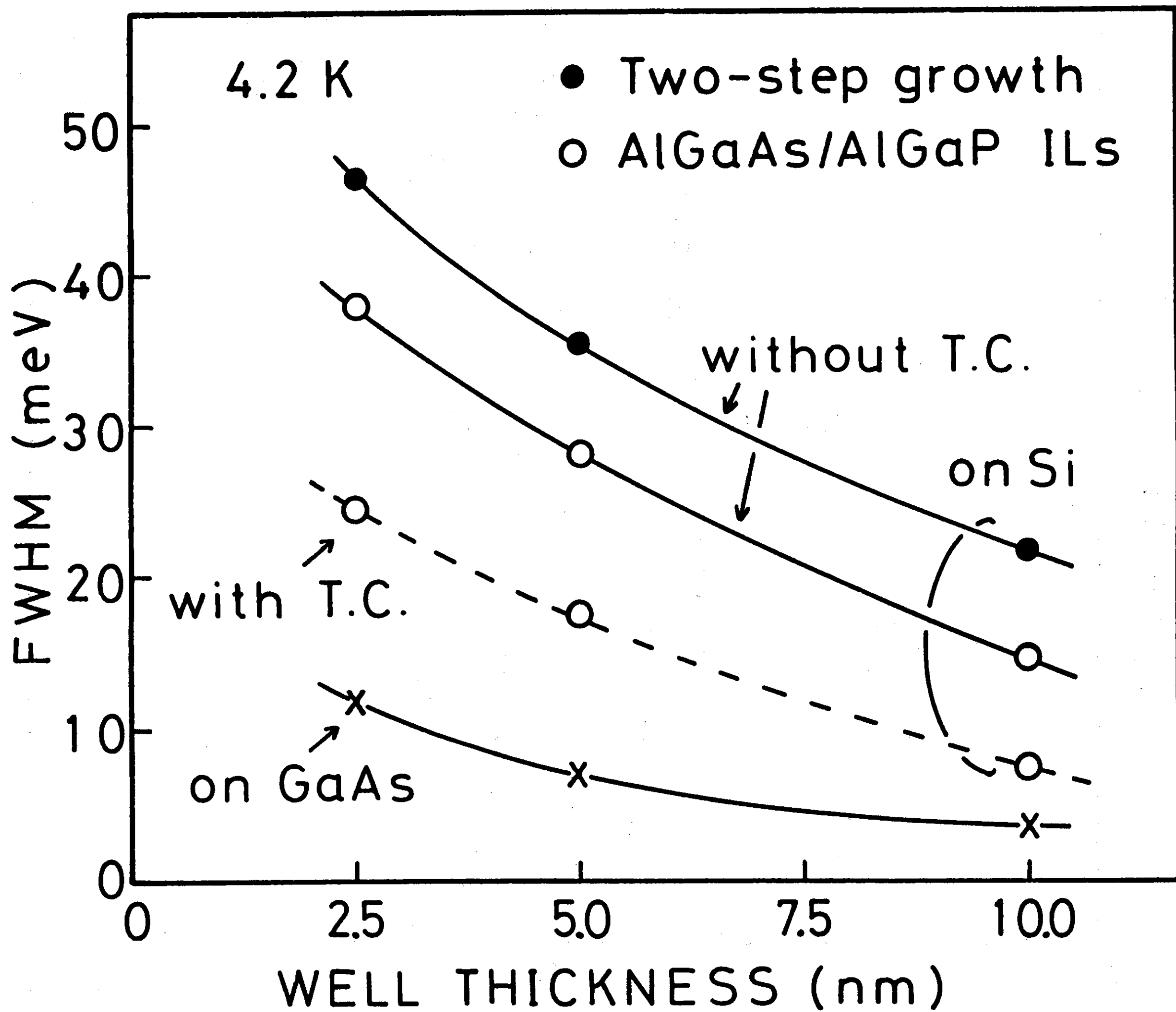


Fig. 2.13. FWHM obtained from the photoluminescence spectra at 4.2 K for the SQW's on GaAs and Si grown by the two-step growth technique and the $Al_{0.5}Ga_{0.5}As/Al_{0.55}Ga_{0.45}P$ intermediate layers.

intermediate layers are smoother than those grown by the two-step growth technique, which are caused by the two-dimensional growth of the AlGaAs and AlGaP layers. Another important result is that the values of FWHM are decreased by performing thermal cycle annealing. The FWHM values of the SQW's on the AlGaAs/AlGaP/Si with thermal cycle annealing are 24.7, 17.8 and 7.5 meV for the same structure. In order to study the effect of thermal cycle annealing on the heterointerfaces, cross-sectional TEM was performed. Figure 2.14 shows the cross-sectional TEM micrograph of the SQW's on Si without thermal cycle annealing. Many dislocations propagate into the quantum wells and cause the fluctuation of the quantum well thickness. The causes of the fluctuation in the quantum well thickness of the GaAs/Si are three-dimensional growth at initial stage and propagation of dislocations. Compared with the SQW's grown on GaAs, however, the SQW's on Si grown with the AlGaAs/AlGaP intermediate layers have broader PL spectra, which are caused by poor crystallinity of the GaAs/Si.

2.4 Selective Area Growth of GaAs Layers on Si

One of the major remaining problems of GaAs/Si is a high density of dislocations resulting from the large lattice mismatch and thermal expansion coefficient difference between GaAs and Si. In order to realize high quality devices such as lasers, it is necessary to reduce

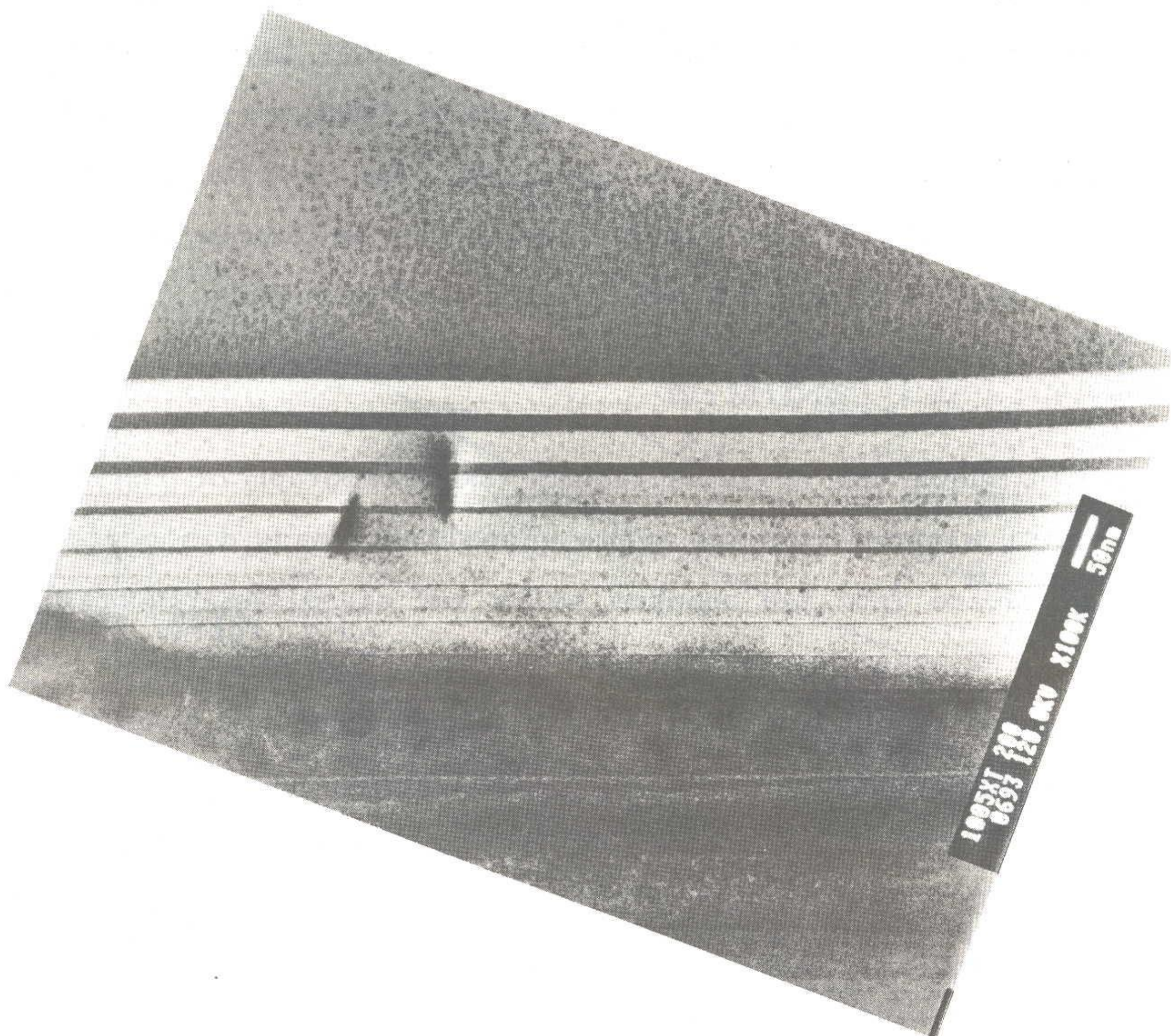


Fig. 2.14. Cross-sectional TEM micrograph of the SQW's on Si grown by the two-step growth technique without thermal cycle annealing.

the density of dislocations, which act as non-radiative recombination centers and reduce minority carrier lifetime. Several dislocation reduction techniques, such as thermal cycle annealing and inserting a strained layer superlattice as a buffer layer have been proposed for the GaAs/Si. Recently, selective area growth has been found to reduce dislocation density in the GaAs/Si. In this section, it has been demonstrated that the dislocations can be reduced by a combination of selective area growth, thermal cycle annealing and strained layer superlattice.

All samples were grown on Si substrates oriented 2° and 4° off (100) toward [011] in an RF-heated horizontal MOCVD reactor at atmospheric pressure. Trimethylgallium(TMG), pure arsine (AsH_3) and phosphine (PH_3) were used as the Ga, As and P sources, respectively. Prior to the growth, the substrates were degreased in organic solvents and then cleaned in $4H_2SO_4+H_2O_2$ and $HF+4H_2O$ solutions. After 300-nm-thick sputtered SiO_2 films were deposited on the cleaned Si substrates, 50-2000-μm-wide stripes were defined photolithographically, and the stripes were etched to the Si substrate by a buffered HF solution. The following is a description of the growth sequence. The substrates were heated in H_2 atmosphere at 1000 ^oC for 10 min to remove native oxide from the substrate surface. GaAs layers were grown on selectively patterned Si substrates by the two-step growth technique and using the GaAs/GaAsP strained layer superlattice (SLSs) as intermediate layers. In the two-step

growth technique, a 12.5-nm-thick GaAs layer was deposited at 400 °C with a V/III ratio of 80. The GaAs/GaAsP SLSs consisted of five periods of 20-nm-thick $Ga_{0.5}As_{0.5}P$/20-nm-thick GaAs grown at 750 °C. Thermal cycle annealing was performed for some samples. Thermal cycle annealing was performed in an AsH_3 ambient by varying substrate temperature from 300 to 850 °C and from 850 to 300 °C. 3-μm-thick GaAs layers were grown at 750 °C.

Figure 2.15 shows the effect of selective area growth on the reduction in the EPD of the GaAs layers selectively grown on Si oriented 2° off toward [011]. For all samples, the EPD decreases with the narrowing of the patterned width. A lower EPD has been achieved for the GaAs/Si grown with the SLSs intermediate layers and thermal cycle annealing. A minimum EPD of 2.8×10^6 cm^{-2} was obtained for the selectively grown GaAs/Si with a 60-μm-width. Figure 2.16 shows the effect of selective area growth on the reduction in the EPD of the GaAs layers selectively grown on Si oriented 4° off toward [011]. The minimum EPD of 1.4×10^6 cm^{-2} has been obtained. The reason for the EPD reduction in the GaAs layers selectively grown on Si is considered to be caused by stress relief due to the selective area growth.

2.5 Unintentional Si Autodoping

It is difficult to grow high resistivity undoped GaAs layers on Si using the MOCVD technique. The carrier

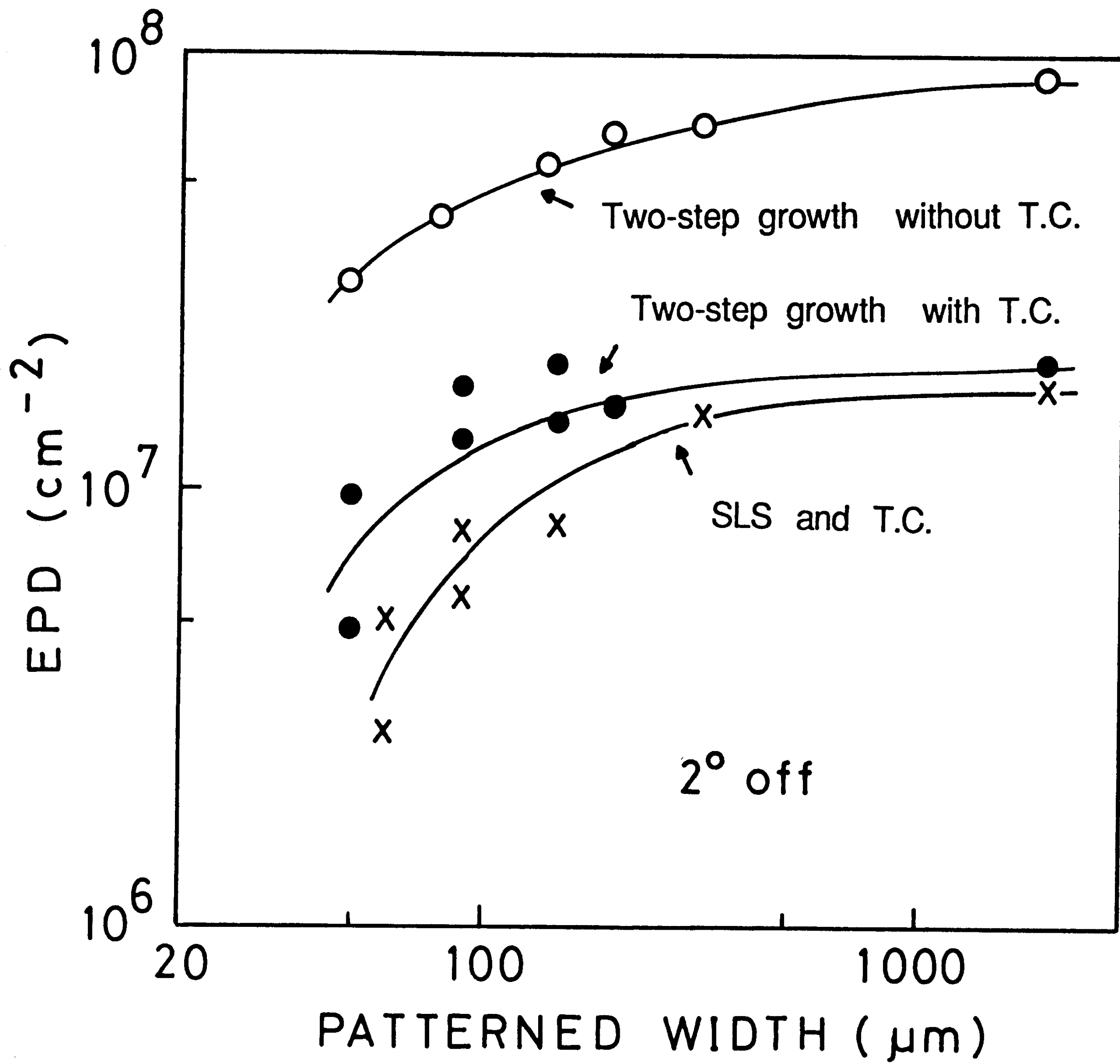


Fig. 2.15. Effect of selective area growth on reduction in the EPD of the GaAs layers selectively grown on Si oriented 2° off toward [011].

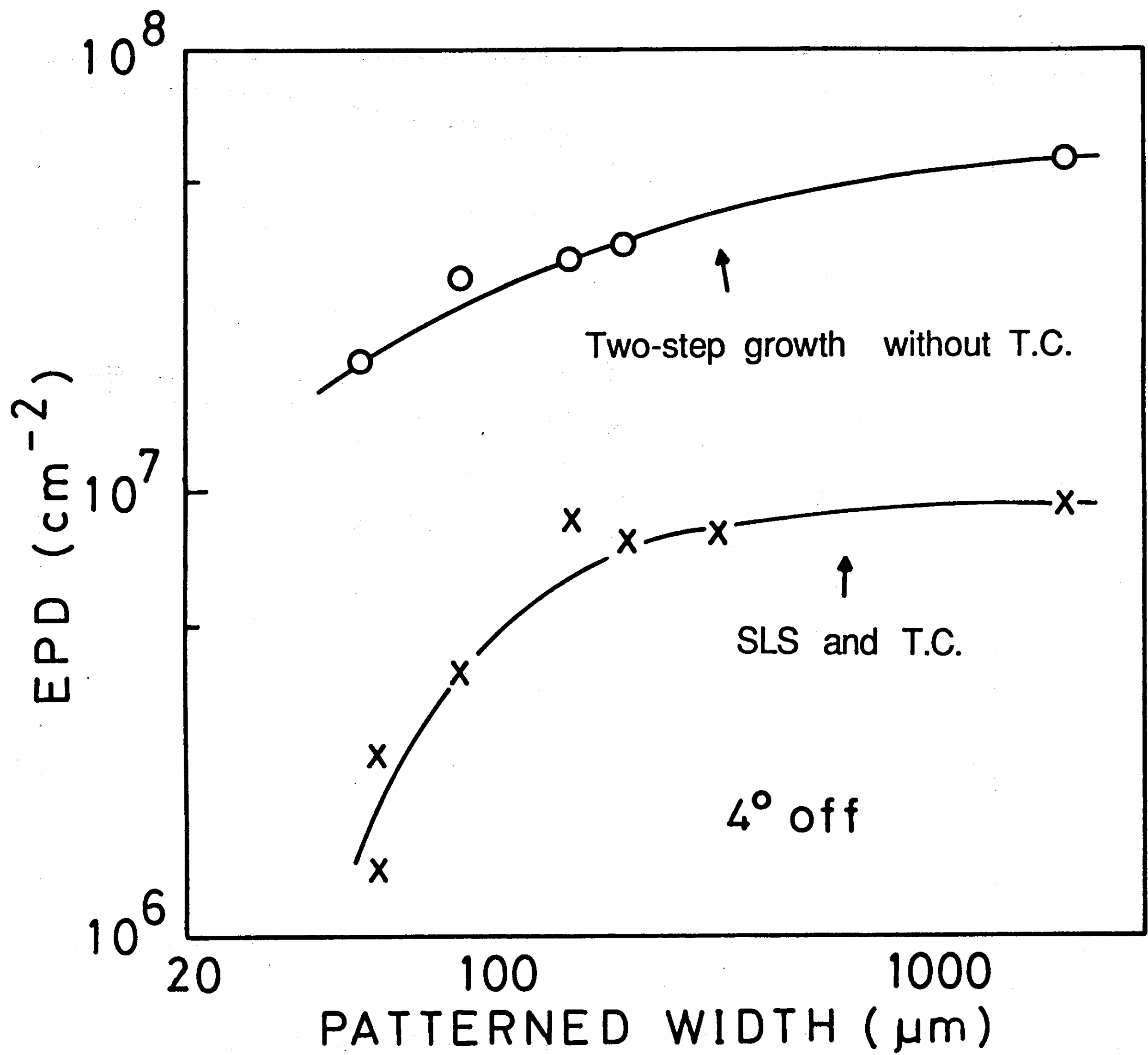


Fig. 2.16. Effect of selective area growth on reduction in the EPD of the GaAs layers selectively grown on Si oriented 4° off toward [011].

concentrations in the undoped GaAs layers on GaAs is near the 10^{14} cm^{-3} range. In contrast, MOCVD-grown undoped GaAs layers on Si have n-type conductivity, with carrier concentrations in the 10^{16}-10^{17} cm^{-3} range. This unintentional or background doping is caused by a high concentration of Si in the GaAs layers[6-8]. As will be described in chapters 3 and 5, the unintentional Si autodoping becomes a crucial problem in the fabrication of many devices such as laser diodes, MESFET's and HEMT's. The unintentional Si autodoping affects carrier concentration levels and pinch-off characteristics, which depend on the background doping of the undoped GaAs layers beneath the channel layers[11].

In this section, it has been shown that SiO_2 back coating is useful in growing high resistivity undoped GaAs layers on Si using the MOCVD technique even at a higher growth temperature. A new mechanism is proposed for Si incorporation in GaAs layers on Si.

All samples were grown in an atmospheric pressure MOCVD reactor using the two-step growth technique. 12.5-nm-thick initial buffer GaAs layers were grown at 400 °C on n-type Si substrates with various thickness of sputtered SiO_2 back coating, prior to the growth of 4-μm-thick undoped GaAs layers at growth temperatures from 650 to 750 °C. Carrier concentration profiles were obtained for all samples by electrochemical capacitance-voltage (C-V) measurements using a Polaron model PN 4200 system. The atomic Si

concentrations were obtained by secondary-ion mass spectroscopy (SIMS) measurements using a Riber-M1Q156 SIMS system with Cs^+ primary-ion bombardment. The $AsSi^-$ ion signal was used to determine the Si content having a threshold detection limit of $5x10^{15}$ cm^{-3}. Concentration and depth accuracies in both systems are of the order of 30 %.

Figure 2.17 shows the electron concentration profiles of the 4-μm-thick undoped GaAs layers grown at 750 ^{o}C on Si with and without SiO_2 back coating. For all samples, the electron concentrations are as high as $1.5x10^{18}$ cm^{-3} at the interfaces between Si and GaAs. This result is caused by the Si autodiffusion near the heterointerface because the heterointerface has a very high density of dislocations and is strained. The electron concentration of $1x10^{17}$ cm^{-3} is obtained for the GaAs/Si without SiO_2 back coating, but the electron concentration decreases with increases in the SiO_2 thickness. The electron concentration in the GaAs/Si with SiO_2 back coatings thicker than 480 nm is as low as $1x10^{15}$ cm^{-3}.

Figure 2.18 shows the growth temperature dependence of the electron concentration in the 4-μm-thick undoped GaAs layers on Si without and with 720-nm-thick SiO_2 back coating. The electron concentrations in the GaAs/Si without SiO_2 back coating increase in the range of 10^{15}-10^{17} cm^{-3} at a higher growth temperature. For the GaAs/Si with back coating, however, the electron concentration is as low as $1x10^{15}$ cm^{-3} between 650 and 750 ^{o}C. This result indicates

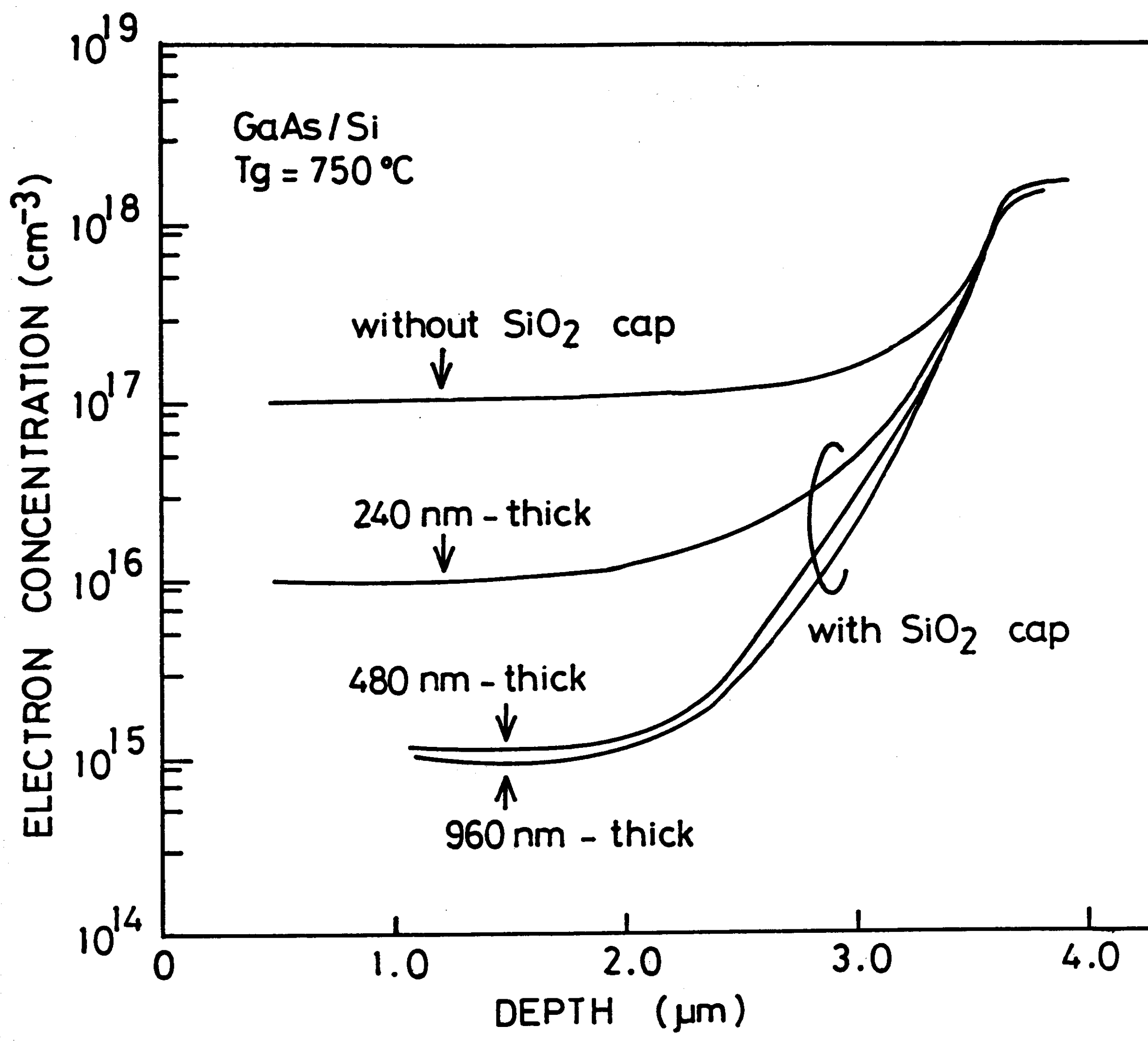


Fig. 2.17. Electron concentration profiles of the 4-μm-thick undoped GaAs layers grown at 750 °C on Si with and without SiO_2 back coating.

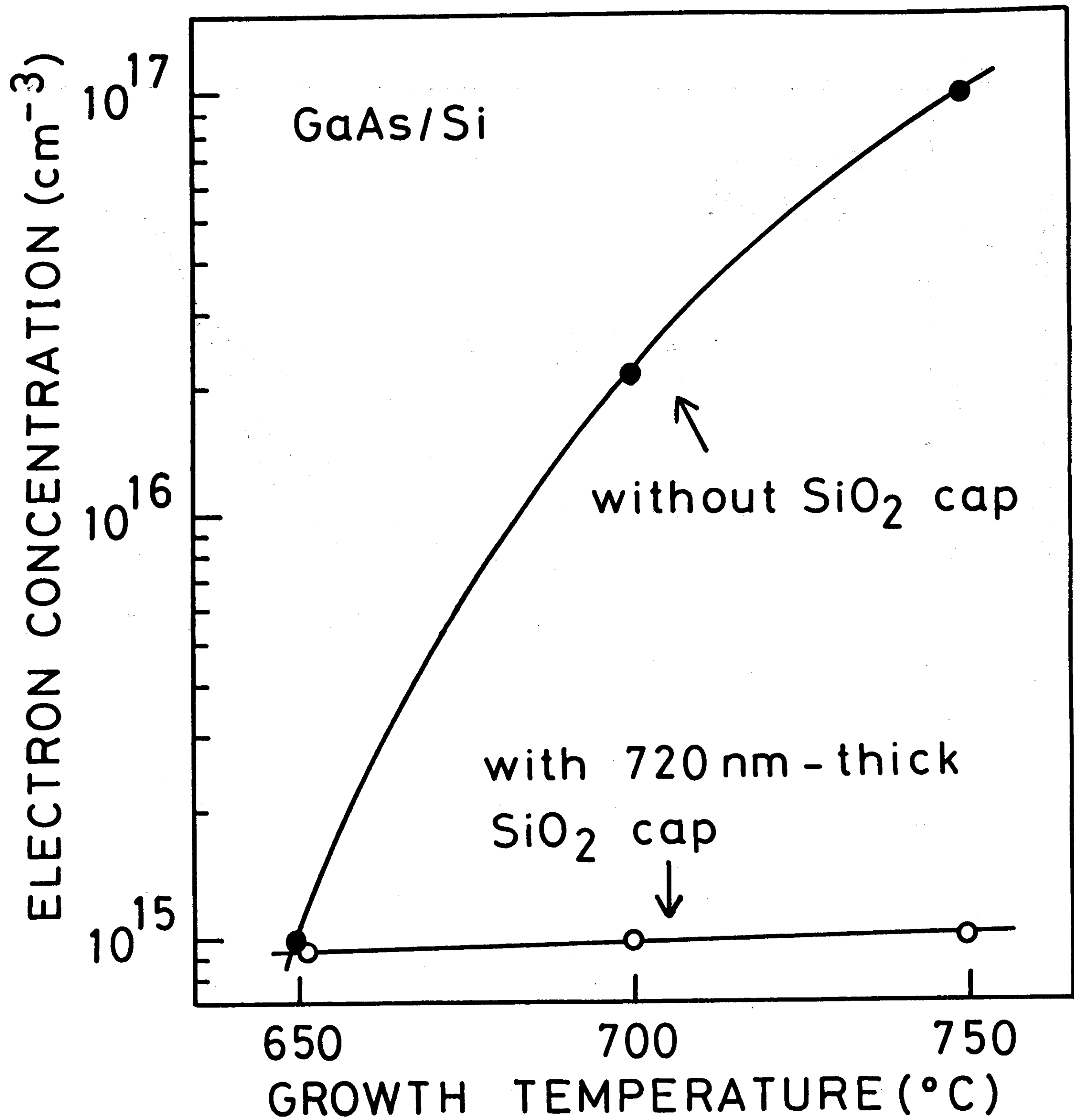


Fig. 2.18. Growth temperature dependence of the electron concentration in the undoped GaAs layers on Si with and without 720-nm-thick SiO_2 back coating.

that SiO_2 back coating is useful to grow high resistivity undoped GaAs layers on Si even at higher growth temperature.

Figure 2.19 shows the Si profiles obtained by SIMS analysis for the GaAs/Si with various thickness of SiO_2 back coating. When the profiles of the electron concentration (Fig. 2.17) are compared to those of the Si atoms (Fig. 2.19), there is qualitatively good agreement between the two profiles. However, there is almost one order of magnitude difference between the Si concentration obtained by SIMS and the electron concentration by C-V measurements. The reason for this lack of electrical activity may be related to the diffusion mechanism of Si. Greiver et al.[23)] have proposed that the Si in the GaAs diffuses as a pair (Si_{As}-Si_{Ga}), resulting in a high degree of self-compensation for large atomic concentrations. The results obtained from C-V and SIMS measurements indicate that SiO_2 back coating prevents the Si atoms from transporting into the growing GaAs layers on Si. However, these results cannot be explained only by the previously proposed models, which involve pipe diffusion along the threading dislocations and point defect mechanisms. One of the probable mechanisms is the gas phase reaction ($Si+H_2 \rightarrow SiH_4$) and transport of Si to the growing GaAs layers on Si.

It is clear that the use of SiO_2 back-coated Si substrate is effective in obtaining a low background electron concentration in an undoped GaAs layer grown on Si, particularly at high temperature, using the MOCVD technique.

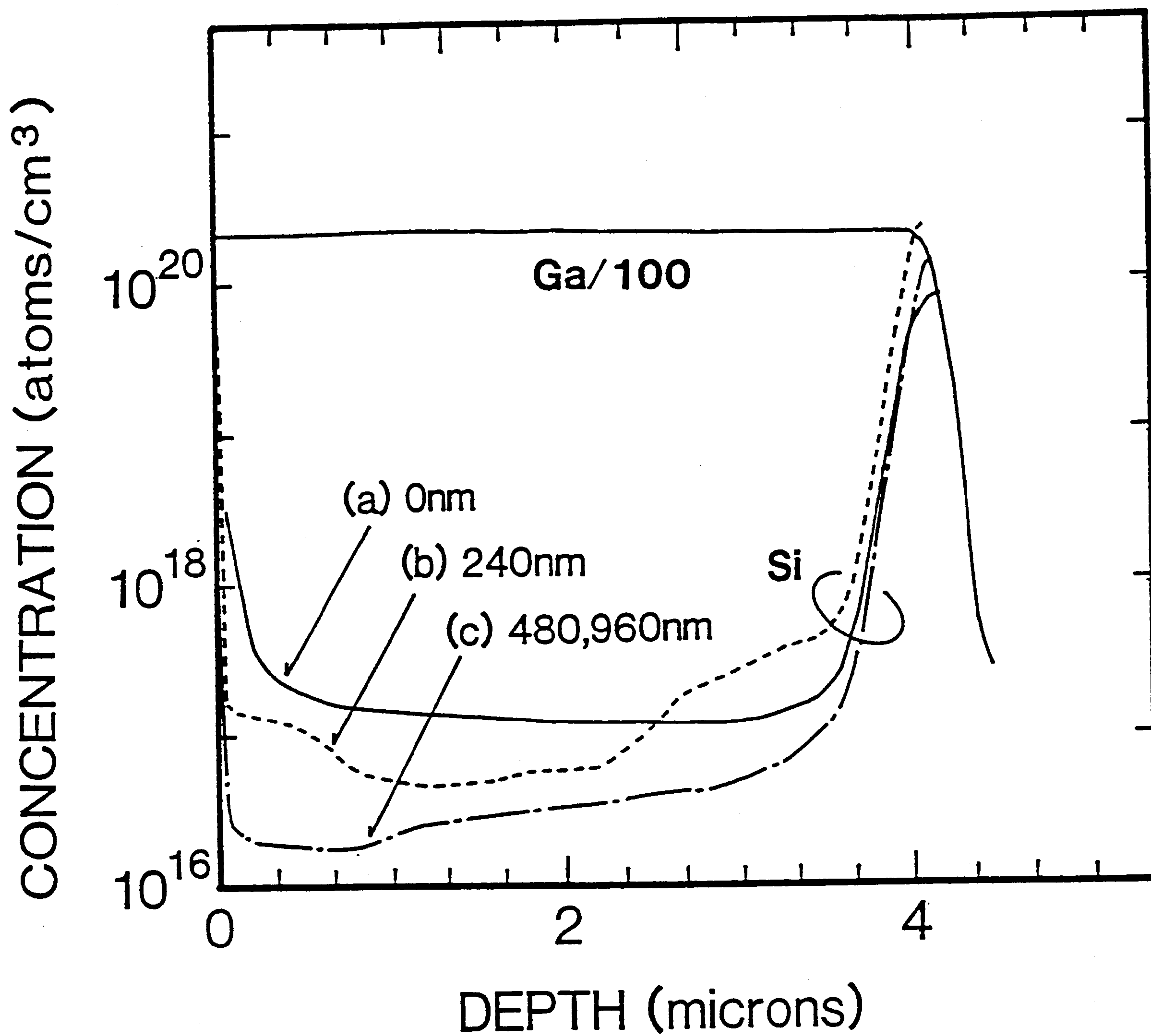


Fig. 2.19. Si profiles obtained by SIMS analysis for the GaAs/Si with various thickness of SiO_2 back coating.

The back coating suppresses the gas phase transport of Si from the substrate and reduces Si incorporation into the undoped GaAs layer during the MOCVD growth, even at high temperature.

2.6 Conclusions

The crystallinity of the GaAs/Si is improved by using the $Al_{0.5}Ga_{0.5}As/Al_xGa_{1-x}P$ intermediate layers and affected by the composition of x in the $Al_xGa_{1-x}P$ intermediate layer. The $Al_xGa_{1-x}P$ layer grows two-dimensionally on Si when the composition (x) is greater than or equal to 0.45. In spite of a large lattice mismatch (3.5 %) between $Al_{0.5}Ga_{0.5}As$ and $Al_{0.55}Ga_{0.45}P$, the $Al_{0.5}Ga_{0.5}As$ layer grows two-dimensionally on the $Al_{0.55}Ga_{0.45}P/Si$. The best crystallinity has been obtained for the $GaAs/Al_{0.5}Ga_{0.5}As/Al_{0.55}Ga_{0.45}P/Si$ structure, which has a specular surface morphology and the FWHM of X-ray of 126 arcs with thermal cycle annealing.

The quantum wells on Si grown with the $Al_{0.5}Ga_{0.5}As/Al_{0.55}Ga_{0.45}P$ intermediate layers show smoother heterointerfaces than those grown by the two-step growth technique. The causes of the fluctuation in the quantum well thickness of the GaAs/Si are three-dimensional growth at the initial stage and propagation of dislocations.

The EPD in the GaAs/Si can be reduced by selective area growth. By using a combination of strained layer

superlattice and thermal cycle annealing, a minimum EPD of 1.4×10^6 cm^{-2} was obtained.

The use of SiO_2 back-coated Si substrate is effective in obtaining a low background electron concentration in an undoped GaAs layer grown on Si, particularly at high temperature using the MOCVD technique. By using SiO_2 back-coated Si substrate, the undoped GaAs layer with an electron concentration as low as 1×10^{15} cm^{-3} has been grown at 750 ^oC. The back coating suppresses the gas phase transport of Si from the substrate and reduces Si incorporation into an undoped GaAs layer during the MOCVD growth even at high temperature.

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Chapter 3. Laser Diodes Grown on Si

3.1 Introduction

Heteroepitaxial growth of GaAs layers on Si offers important advantages for such applications as monolithic integration of optoelectronic and microelectronic devices, and optical interconnections between very-large-scale integrated circuits. Room-temperature continuous-wave (cw) operation with a sufficiently low threshold current of AlGaAs/GaAs laser on Si will become a key technology to realize the above applications. Room-temperature cw operations of AlGaAs/GaAs lasers on Si have been reported by Deppe et al.[1,2], who grew the buffer layer using the molecular beam epitaxy (MBE) technique and the laser structure using the metalorganic chemical vapor deposition (MOCVD) technique. Room-temperature cw operation has also been reported by Chen et al.[3], who grew both the buffer layer and the laser structure with the MBE technique. Recently, Choi et al.[4] and Egawa et al.[5-7] have reported room-temperature cw operation of an all-MOCVD-grown AlGaAs/GaAs laser on a Si substrate. The growth, entirely using the MOCVD technique is an advantage for high-volume production.

However, the GaAs/Si still has problems such as a high density of misfit and threading dislocations[8], unintentional Si autodoping[9-11] and roughness of surface

morphology[12]. The threading dislocations, which is caused by the difference in the lattice constants and the thermal expansion coefficients between GaAs and Si, can act as non-radiative recombination centers in optical devices[13-17]. The unintentional Si autodoping into the growing GaAs layer affects the carrier concentration level and the conversion of the p-type cladding layer to n-type[18]. The roughness of surface morphology of the GaAs/Si, especially grown by the two-step growth technique[19], causes nonuniformity and undulation of the quantum well thickness. These problems lead to degradation of laser performances, namely, higher threshold current, lower differential quantum efficiency[6,7] and shorter device lifetime. In order to overcome the above problems, many efforts have been made. It has been reported that the high density of threading dislocations can be reduced by using thermal cycle annealing[20,21] and strained layer superlattice[22]. It has been also reported that SiO_2 back coating is effective in suppressing the unintentional Si autodoping[23,24] and the surface morphology can be improved using $Al_{0.55}Ga_{0.45}P$[12,25] or $Al_{0.5}Ga_{0.5}As/Al_{0.55}Ga_{0.45}P$ intermediate layers[6,7,26].

In this chapter, room-temperature cw operation has been demonstrated for lasers on Si grown entirely by the MOCVD technique. The laser characteristics on Si grown by the two-step growth technique and using the $Al_{0.5}Ga_{0.5}As/Al_{0.55}Ga_{0.45}P$ intermediate layers are discussed in detail. This chapter is organized as follows: The

AlGaAs/GaAs double heterostructure (DH) lasers on Si are described in section 3.2. In section 3.3, AlGaAs/GaAs single quantum well (SQW) lasers on Si are presented. This chapter is concluded in section 3.4.

3.2 AlGaAs/GaAs Double Heterostructure Lasers

3.2.1 Epitaxial Growth and Fabrication Process

DH lasers were grown on n-type (Sb-doped, 0.02 Ω-cm) Si substrates oriented 2° off (100) toward [011] in an RF-heated horizontal MOCVD reactor at atmospheric pressure using intermediate layers consisting of $GaP/GaAs_{0.5}P_{0.5}$ and $GaAs_{0.5}P_{0.5}/GaAs$ strained layer superlattices on GaP (SLSs/GaP). Trimethylgallium (TMG), trimethylaluminum (TMA), pure arsine (AsH_3) and phosphine (PH_3) were used as the Ga, Al, As and P sources, respectively. The substrates were degreased in organic solvents and then cleaned in $4H_2SO_4+H_2O_2$ and $HF+4H_2O$ solutions. Prior to the growth, the substrates were heated in a H_2 atmosphere at 1000 ^{o}C for 10 min to remove native oxide from the substrate surface. In the structure with the SLSs/GaP intermediate layers, a 0.1-μm-thick GaP layer was grown on Si at 900 ^{o}C with a V/III ratio of 100, followed by five periods of 20-nm-thick GaP/20-nm-thick $GaAs_{0.5}P_{0.5}$ SLS and five periods of 20-nm-thick $GaAs_{0.5}P_{0.5}$/20-nm-thick GaAs SLS at 750 ^{o}C. After that, the DH laser structure was grown at 750 ^{o}C. The laser structure consisted of a 1.5-μm-thick Se-doped

($1.3x10^{18}$ cm^{-3}) GaAs layer, a 1.4-μm-thick Se-doped ($4x10^{17}$ cm^{-3}) $Al_xGa_{1-x}As$ cladding layer, a 0.08-μm-thick undoped GaAs active layer, a 1.4-μm-thick Zn-doped ($4x10^{17}$ cm^{-3}) $Al_xGa_{1-x}As$ cladding layer, and a 0.65-μm-thick Zn-doped ($1.3x10^{18}$ cm^{-3}) GaAs cap layer.

After the growth, 0.4-μm-thick SiO_2 films were sputtered and 10-μm-wide striped windows were opened by chemical etching. After the substrates were lapped off down to about 100-μm-thick, Au-Zn/Au and Au-Sb/Au ohmic electrodes were formed by vacuum deposition on the p-GaAs cap layer and the n-Si substrate, respectively. The deposited ohmic electrodes were annealed at 420 ^{o}C for 2 min in N_2 ambient. The samples were cleaved into chips about 100 μm x 300 μm. Figure 3.1 shows the schematic structure of the DH laser on Si grown with the SLSs/GaP intermediate layers. Each chip was mounted on a Cu heat sink with a p-side-up configuration. Injection current-light output power (I-L) characteristics were measured under pulsed and cw conditions at various temperatures. The pulsed width and repetition rate were 100 nsec and 1 kHz, respectively.

3.2.2 Laser Characteristics

Figure 3.2 shows the I-L characteristics of the $Al_{0.3}Ga_{0.7}As/GaAs$ DH lasers grown on GaAs and Si substrates under the pulsed condition at 300 K. The laser on GaAs has the pulsed threshold current (I_{th}) of 96 mA, corresponding

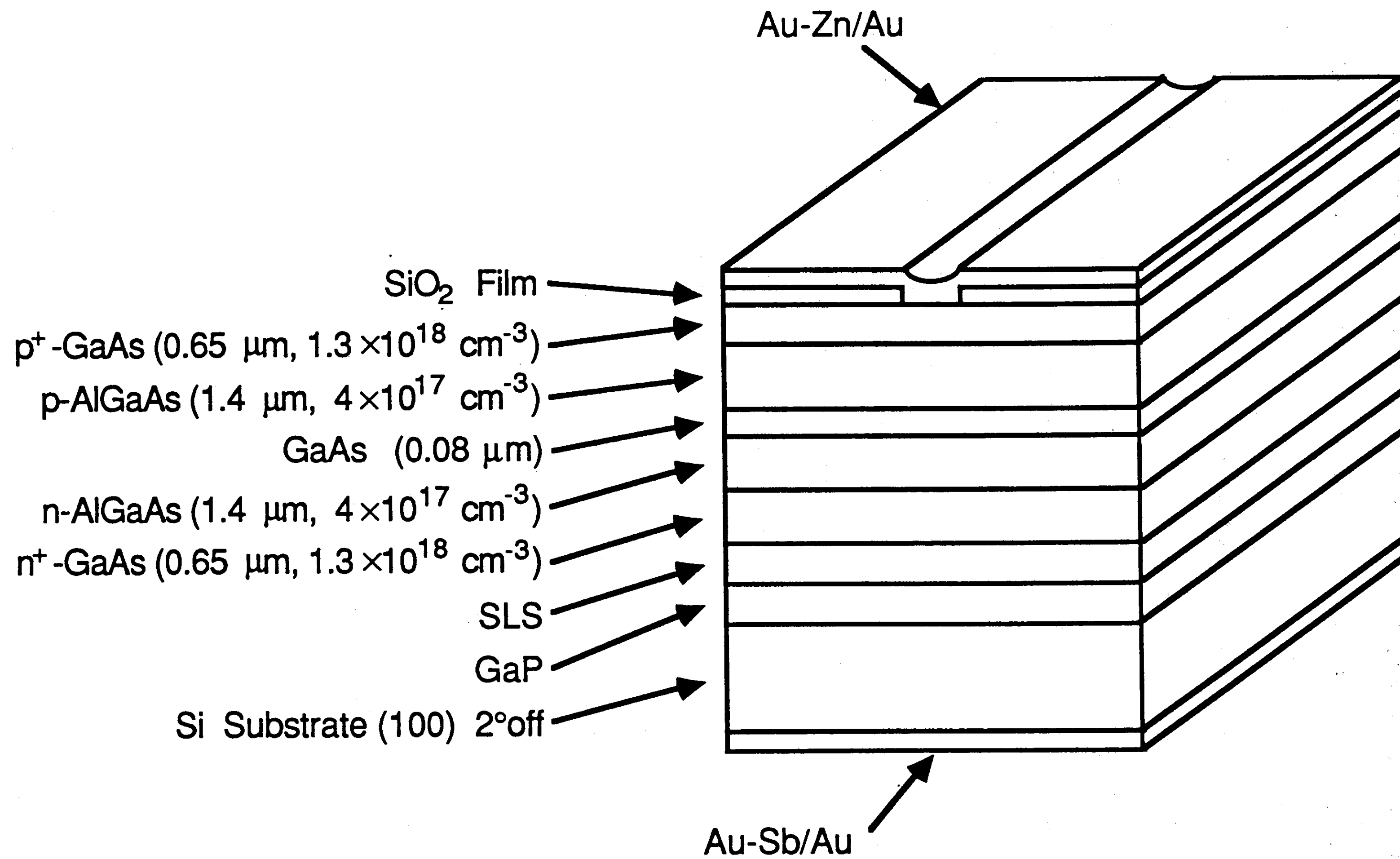


Fig. 3.1. Schematic structure of the DH laser on Si grown with the SLSs/GaP intermediate layers.

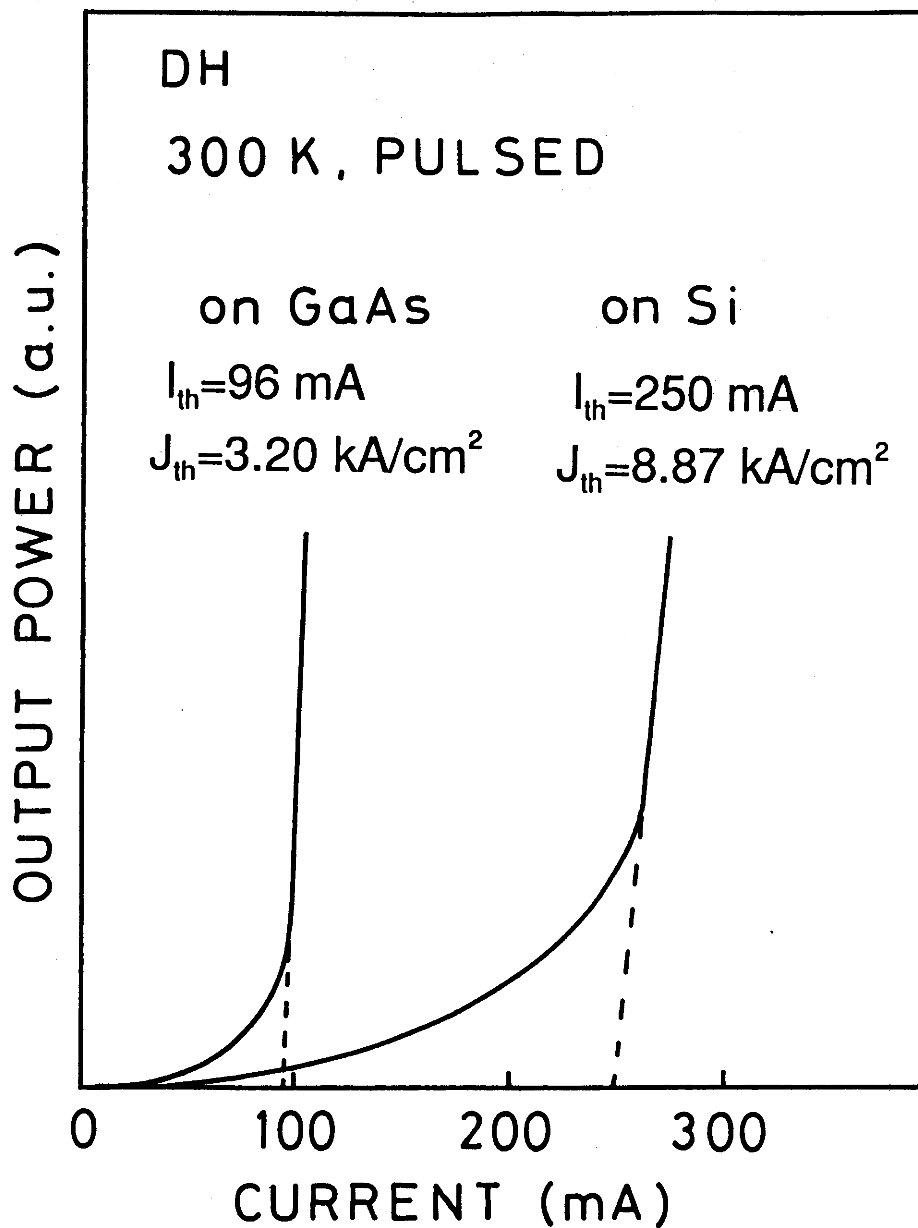
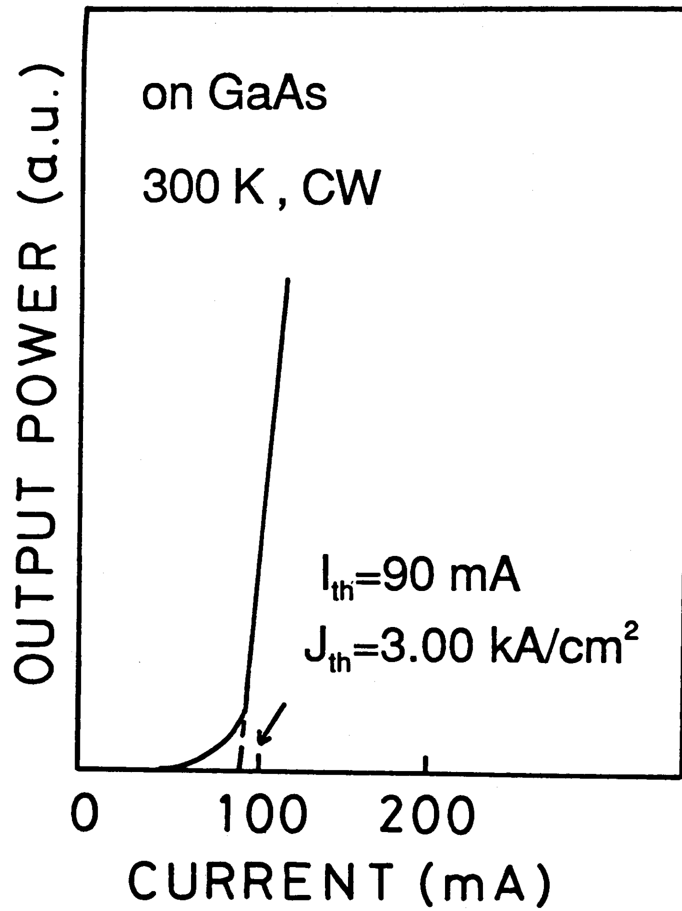


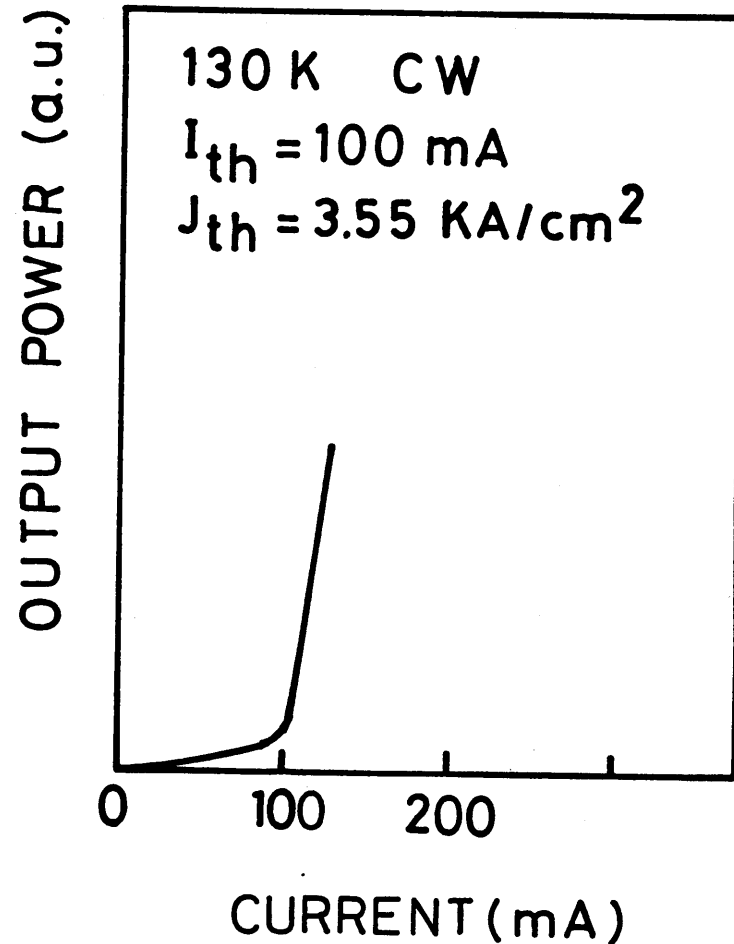
Fig. 3.2. I-L characteristics of the DH lasers grown on GaAs and Si substrates under the pulsed condition at 300 K.

to the pulsed threshold current density (J_{th}) of 3.20 kA/cm^2. The laser on Si has the pulsed I_{th} of 250 mA (J_{th}=8.87 kA/cm^2). The I-L characteristics under the cw condition for the DH lasers on GaAs at 300 K and on Si at 130 K are shown in Figs. 3.3 (a) and (b), respectively. The laser on GaAs has the cw I_{th} of 90 mA (J_{th}=3.00kA/cm^2) at 300 K. However, the laser on Si, which cannot be operated under the cw condition at 300 K, has the cw I_{th} of 100 mA (J_{th}=3.55 kA/cm^2) at 130 K.

The polarizations of the $Al_{0.3}Ga_{0.7}As$/GaAs DH lasers on GaAs and Si substrates are shown in Figs. 3.4 (a) and (b), respectively, under the pulsed condition at 300 K. As shown in Fig. 3.4, the laser on GaAs emits in the transverse electric (TE) mode. In contrast, the laser on Si emits in the transverse and magnetic (TE+TM) modes or the TM mode. The difference in the polarization selection between these two lasers is thought to be related to the tensile stress applied to the active layer. In order to study the effect of the stress on the polarization selection, the polarizations of the emissions were measured at low temperatures for the laser on Si. Figures 3.5 (a), (b) and (c) show the polarizations of the DH lasers on Si under pulsed condition at 200, 100 and 30 K, respectively. Decreasing the temperature, the TE component disappears and the laser emits only in the TM mode. The higher tensile stress, which is due to the difference in the thermal expansion coefficients between Si and GaAs, is applied to

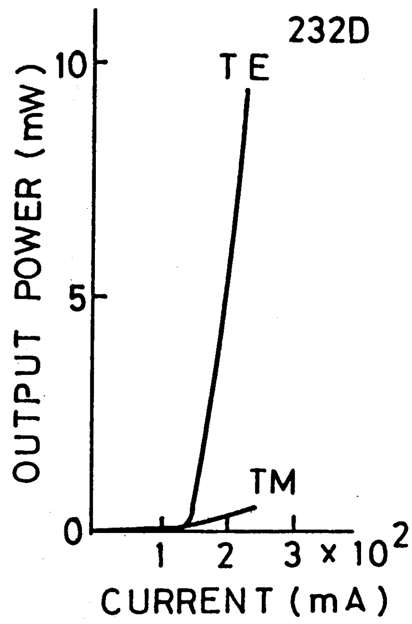


(a) on GaAs

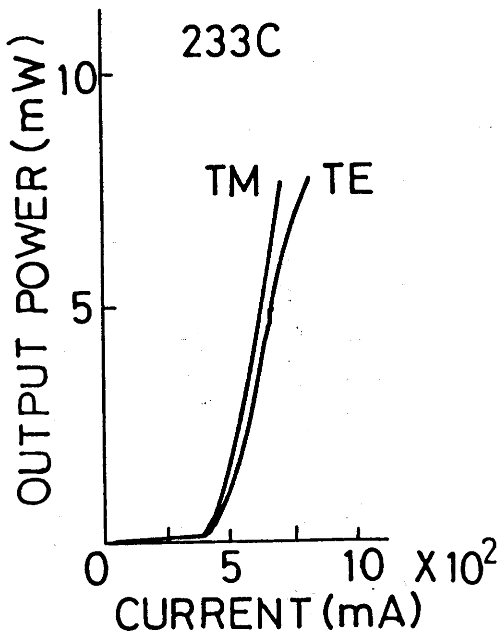


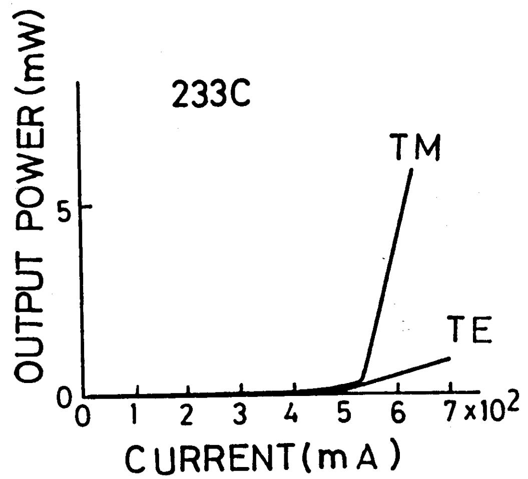
(b) on Si

Fig. 3.3. I-L characteristics of the DH lasers grown on (a) GaAs at 300 K and (b) Si at 130 K under the cw condition.



(a) on GaAs





(b) on Si

Fig. 3.4. Polarizations of the DH lasers on (a) GaAs and (b) Si under the pulsed condition at 300 K.

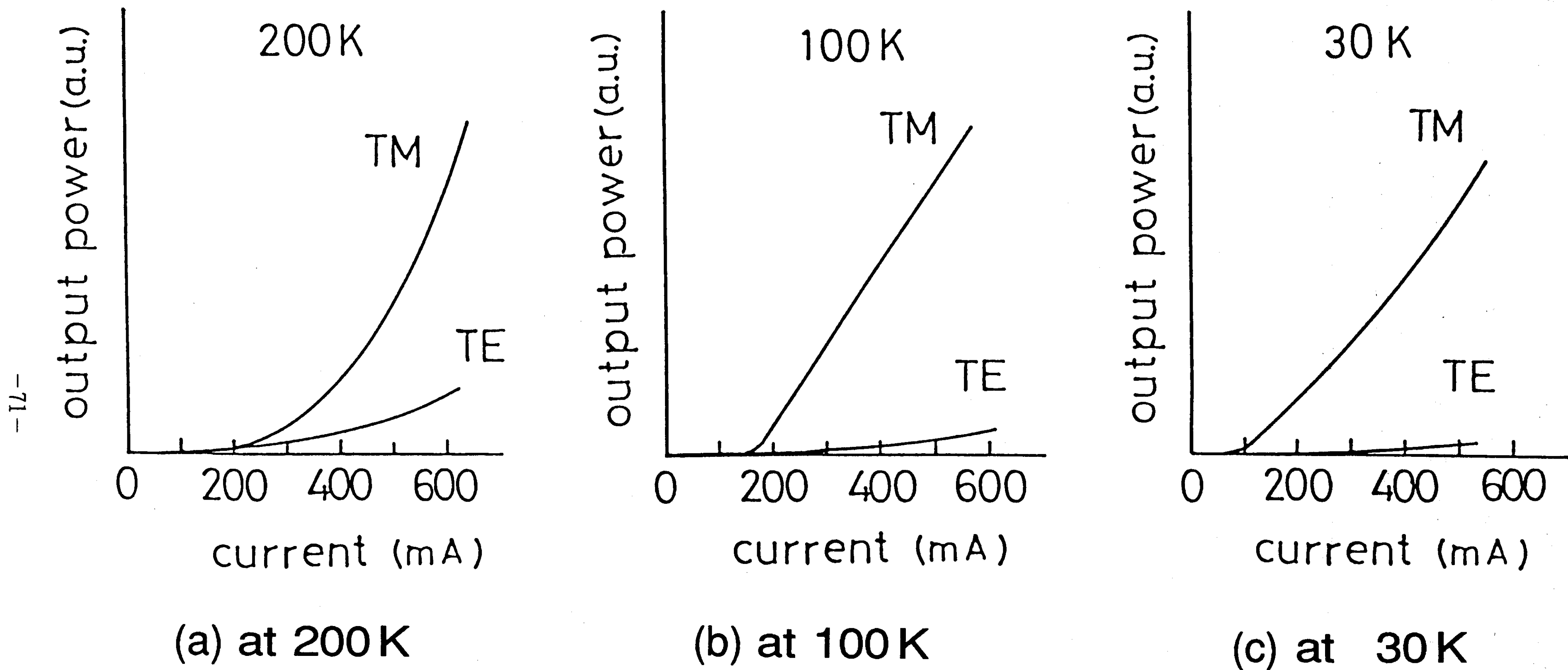


Fig. 3.5. Polarizations of the DH lasers on Si under the pulsed condition at (a) 200 K, (b) 100 K and (c) 30 K.

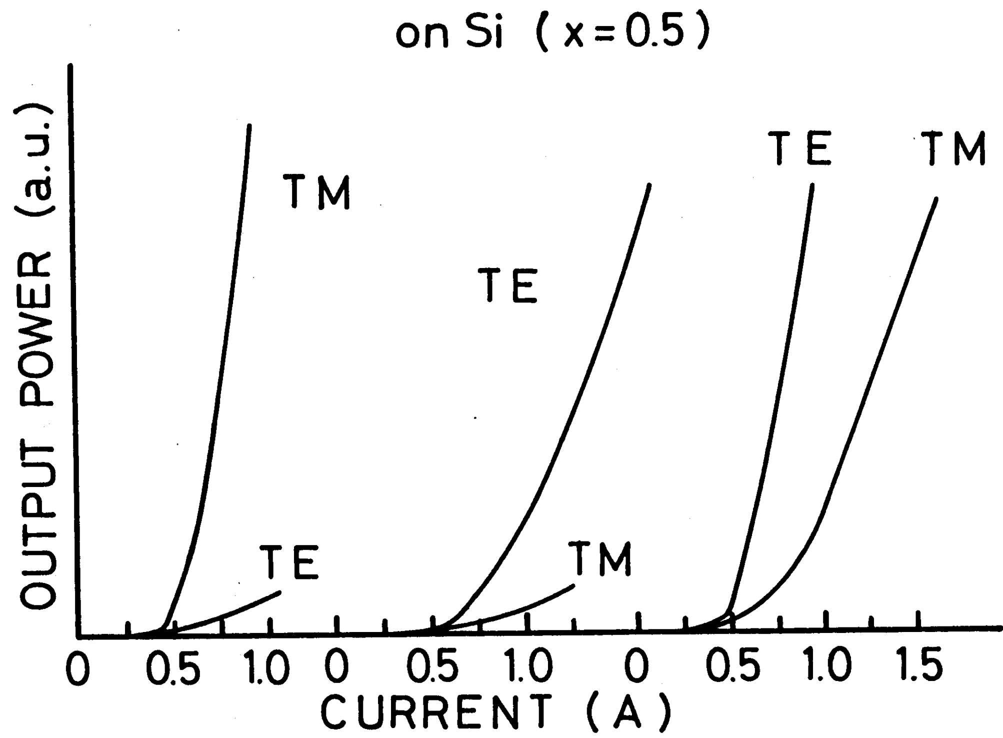
the active layer on Si at a lower temperature. The change in the polarization is caused by the higher tensile stress applied to the active layer. The reason for the TM polarized mode in the DH laser on Si is that the gain is higher for the TM mode than that for the TE mode at the stress of $1.9x10^9$ dyn/cm^2.

The polarization selection of the DH laser on Si is found to depend on the Al composition of x in the $Al_xGa_{1-x}As$ cladding layer. Figures 3.6 (a) and (b) show the polarization of the emission for the DH lasers on Si with x=0.5 and 0.7, respectively. As shown in Fig. 3.4 (b), the laser with x=0.3 emits in the TE+TM modes or the TM mode. In the case of x=0.5, the laser emits in the TE, TM or TE+TM modes. In the case of x=0.7, the laser emits only in the TE mode. These results indicate that the lasers on Si have a tendency to emit in the TE mode as the Al composition of x increases.

The refractive index n_1 of the $Al_xGa_{1-x}As$ cladding layer is given by[27)]

$$n_1=3.590-0.710x+0.091x^2$$

where x is the composition of Al. The refractive index n_2 of the GaAs active layer is 3.590. As the composition of Al increases, the difference of the refractive index Δn ($\Delta n=n_2-n_1$) increases. As a result, the facet reflectivity for the TE mode increases and that for the TM mode



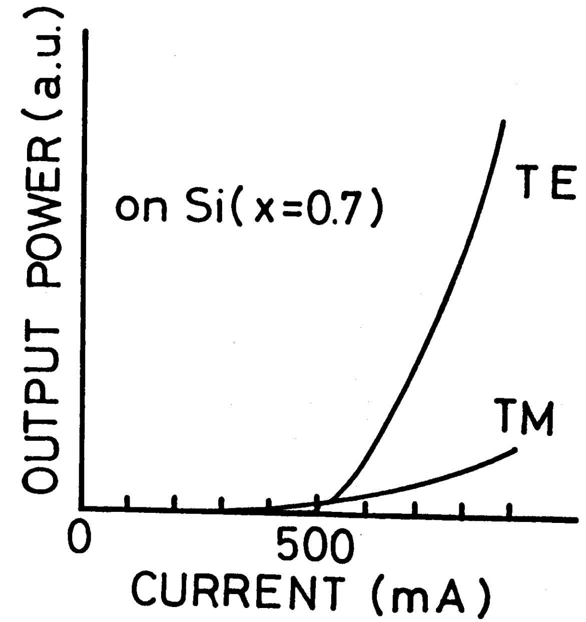


Fig. 3.6. Polarizations of the DH lasers on Si with (a) x=0.5 and (b) x=0.7.

decreases. Therefore, the increase of the composition of Al results in the TE mode.

3.3 AlGaAs/GaAs Single Quantum Well Lasers

3.3.1 Epitaxial Growth and Fabrication Process

In order to suppress unintentional Si autodoping in the epitaxial layer, some 720-nm-thick sputtered SiO_2 back-coated n-type (Sb-doped, 0.02 Ω-cm) Si substrates were used for the epitaxial growth. All samples were grown on Si substrates oriented 2° off (100) toward [011] in an RF-heated horizontal MOCVD reactor at atmospheric pressure.

In the AlGaAs/AlGaP intermediate layers, a 50-nm-thick $Al_{0.55}Ga_{0.45}P$ layer was grown on Si at 900 ^oC with a V/III ratio of 100, and a 200-nm-thick $Al_{0.5}Ga_{0.5}As$ layer was grown at 750 ^oC with a V/III ratio of 70. The $Al_{0.3}Ga_{0.7}As$/GaAs SQW laser was grown on Si at 750 ^oC. The laser consisted of a 2.0-μm-thick Se-doped ($2x10^{18}$ cm^{-3}) GaAs layer, a 1.0-μm-thick Se-doped ($1x10^{18}$ cm^{-3}) $Al_{0.7}Ga_{0.3}As$ cladding layer, a 70-nm-thick undoped $Al_{0.3}Ga_{0.7}As$ barrier layer, a 9-nm-thick undoped quantum well active layer, a 70-nm-thick undoped $Al_{0.3}Ga_{0.7}As$ barrier layer, a 1.0-μm-thick Zn-doped ($1x10^{18}$ cm^{-3}) $Al_{0.7}Ga_{0.3}As$ cladding layer, and an 80-nm-thick Zn-doped ($1x10^{19}$ cm^{-3}) GaAs cap layer. Thermal cycle annealing was performed twice in AsH_3 ambient by varying substrate temperature from 300 to 850 ^oC and from 850 to 300 ^oC after

the growth of the 1-μm-thick Se-doped GaAs layer. It was performed three times after growth of the 2-μm-thick Se-doped GaAs layer. For comparison, similar structures of SQW lasers were grown on GaAs and Si substrates by the two-step growth technique. In the two-step growth technique, a 12.5-nm-thick GaAs layer was deposited at 400 ^{o}C with a V/III ratio of 80.

After the growth, 0.1-μm-thick SiO_2 films were sputtered and 10-μm-wide striped windows were opened by chemical etching. After the substrates were lapped off down to about 100-μm-thick, Au-Zn/Au and Au-Sb/Au ohmic electrodes were formed by vacuum evaporation on the p-GaAs cap layer and the n-Si substrate, respectively. The evaporated ohmic electrodes were annealed at 420 ^{o}C for 2 min in N_2 ambient. The samples were cleaved into 300-μm-wide chips. Figure 3.7 shows the schematic structure of the SQW laser on Si grown with the $Al_{0.5}Ga_{0.5}As/Al_{0.55}Ga_{0.45}P$ intermediate layers. Each chip was mounted on a Cu heat sink with a p-side-up configuration. The laser characteristics were measured under pulsed and cw conditions at room temperature.

The surface morphology and crystallinity of the lasers were characterized by a Nomarski microscope, cross-sectional transmission electron microscopy (TEM) and etch pit density (EPD) revealed by molten KOH.

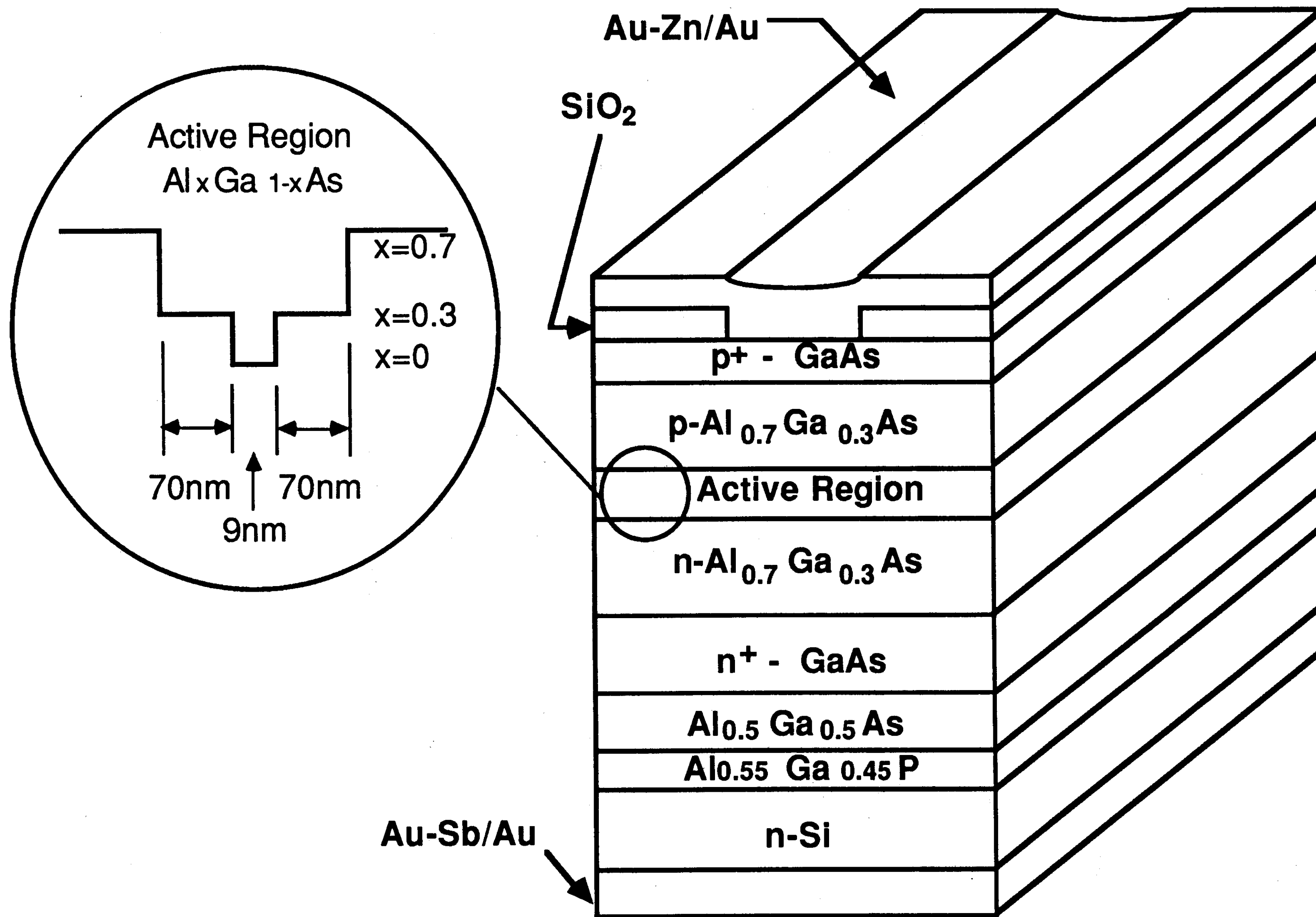


Fig. 3.7. Schematic structure of the SQW laser on Si grown with the $Al_{0.5}Ga_{0.5}As/Al_{0.55}Ga_{0.45}P$ intermediate layers.

3.3.2 Laser Characteristics[5-7]

Figures 3.8, 3.9 and 3.10 show the I-L characteristics under cw condition at room temperature for the SQW lasers on the GaAs and SiO_2 back-coated Si grown by the two-step growth technique and with the AlGaAs/AlGaP intermediate layers, respectively. The spectra are also shown in the insets of Fig. 3.8 and 3.10. The laser on GaAs has the I_{th} of 32 mA, corresponding to the J_{th} of 1.64 kA/cm^2 under the cw condition at room temperature. The values of I_{th} and J_{th} of the lasers on Si are 75 mA and 1.77 kA/cm^2 for the two-step growth technique, and 60 mA and 1.72 kA/cm^2 for the AlGaAs/AlGaP intermediate layers, respectively, under the cw condition at room temperature. The etch pit density (EPD) by molten KOH of the lasers on Si is 1.5x10^7 cm^{-2}, which contributes to the cw operation at room temperature. In the laser on Si, single-mode operation is observed with a peak wavelength of 860.5 nm. Radiation is found to be dominated by the TE mode, since the net gain is higher for the TE mode than for the TM mode. The difference in the peak wavelength of lasers between GaAs and Si results from the high tensile stress experienced by the active layer on Si.

The effects of the thermal cycle annealing and SiO_2 back coating on the SQW laser characteristics on Si were investigated. The dependence of the EPD in the GaAs/Si on the number of thermal cycle annealing is shown in Fig. 3.11. The EPD in the GaAs/Si without thermal cycle annealing is about 9.5x10^7 cm^{-2}, while that for the sample with more than

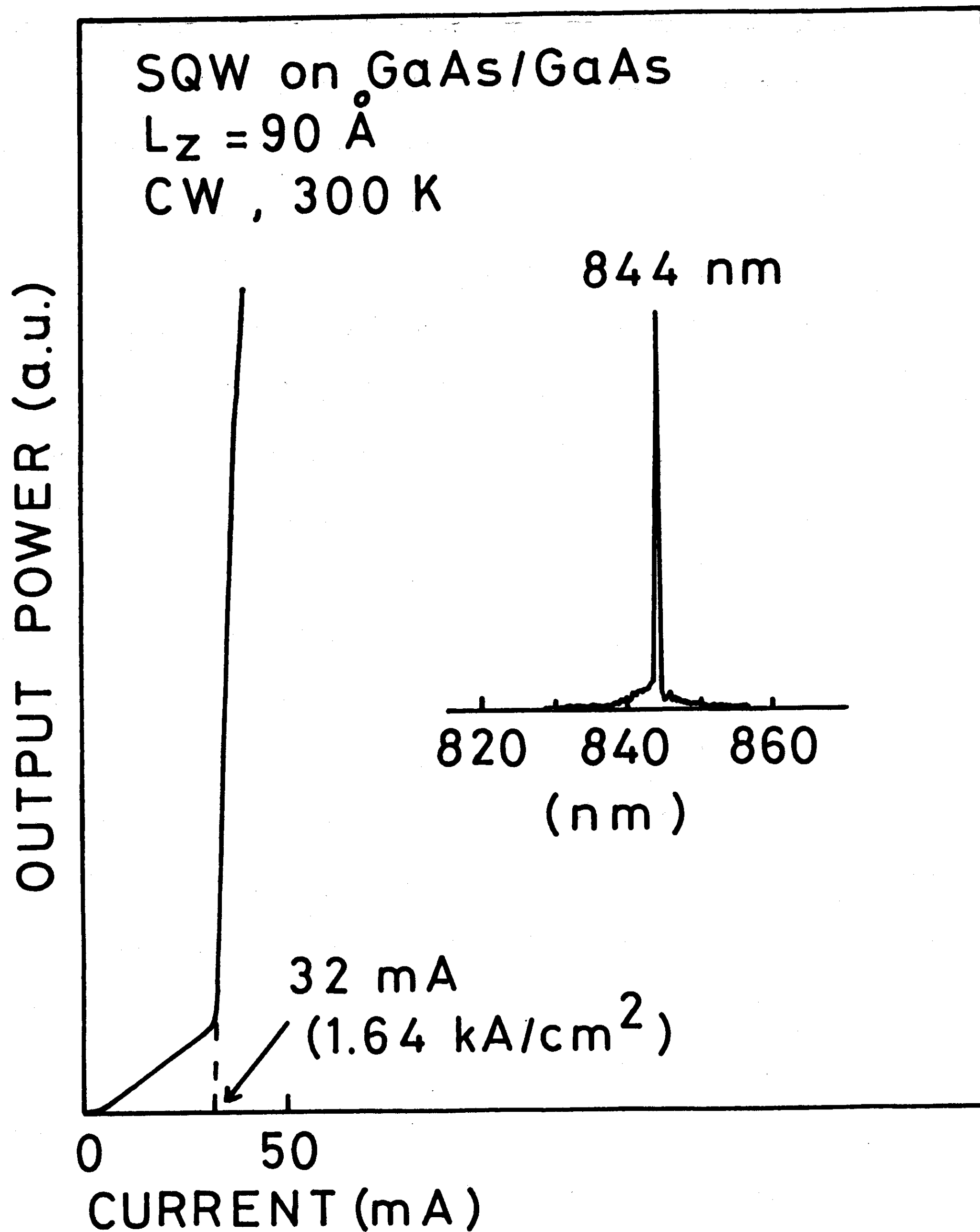


Fig. 3.8. Room-temperature cw I-L characteristic of the SQW laser on GaAs. The single-mode spectrum is also shown in the figure.

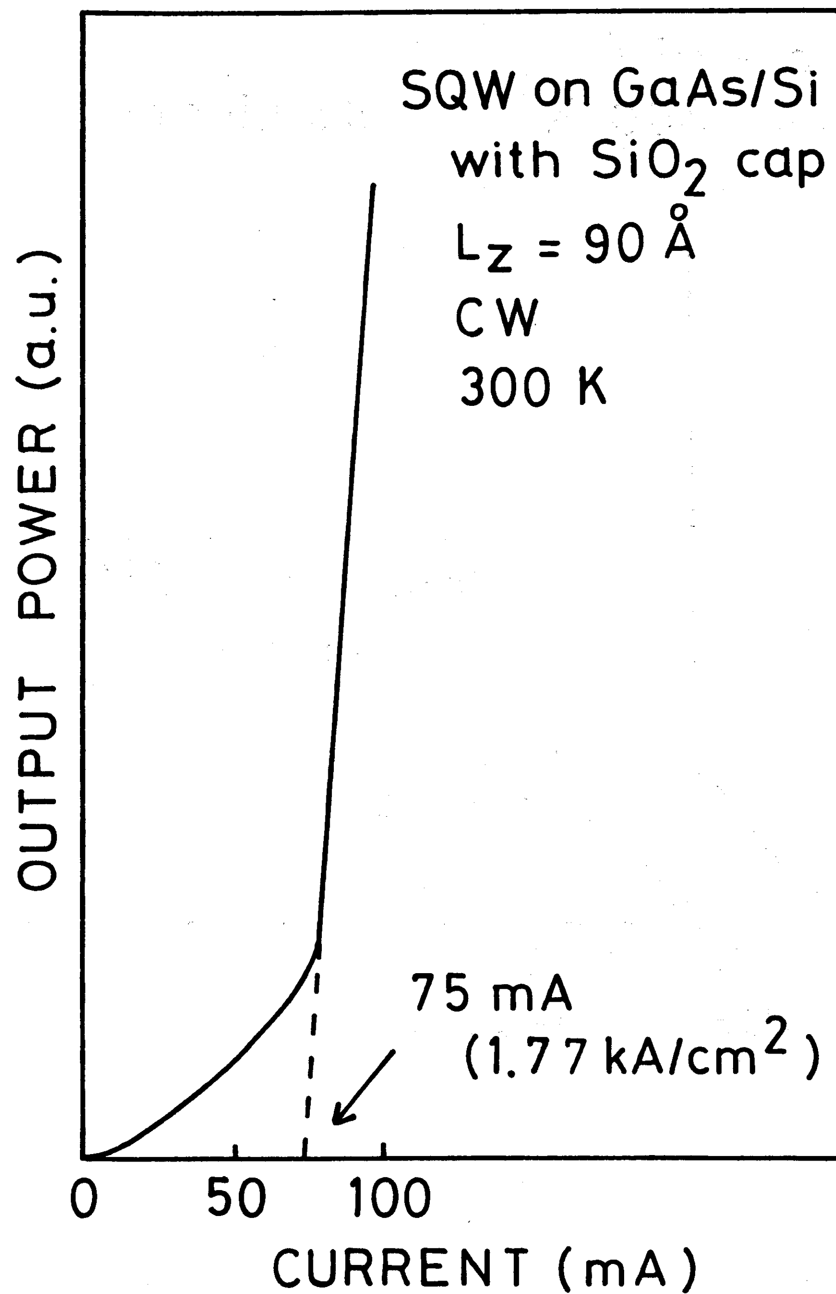


Fig. 3.9. Room-temperature cw I-L characteristic of the SQW laser on Si grown by the two-step growth technique.

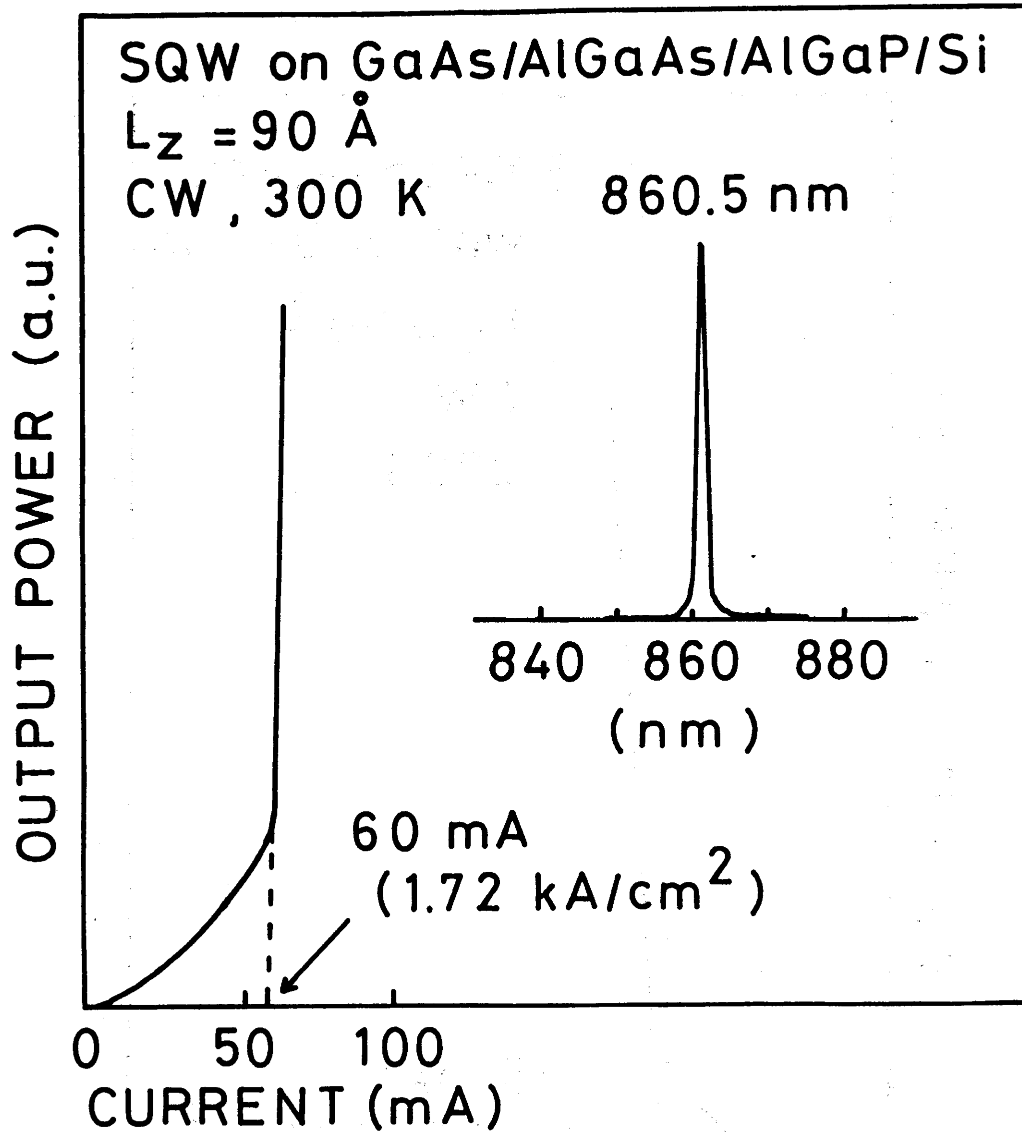


Fig. 3.10. Room-temperature cw I-L characteristic of the SQW laser on Si grown with the $Al_{0.5}Ga_{0.5}As/Al_{0.55}Ga_{0.45}P$ intermediate layers. The single-mode spectrum is also shown in the figure.

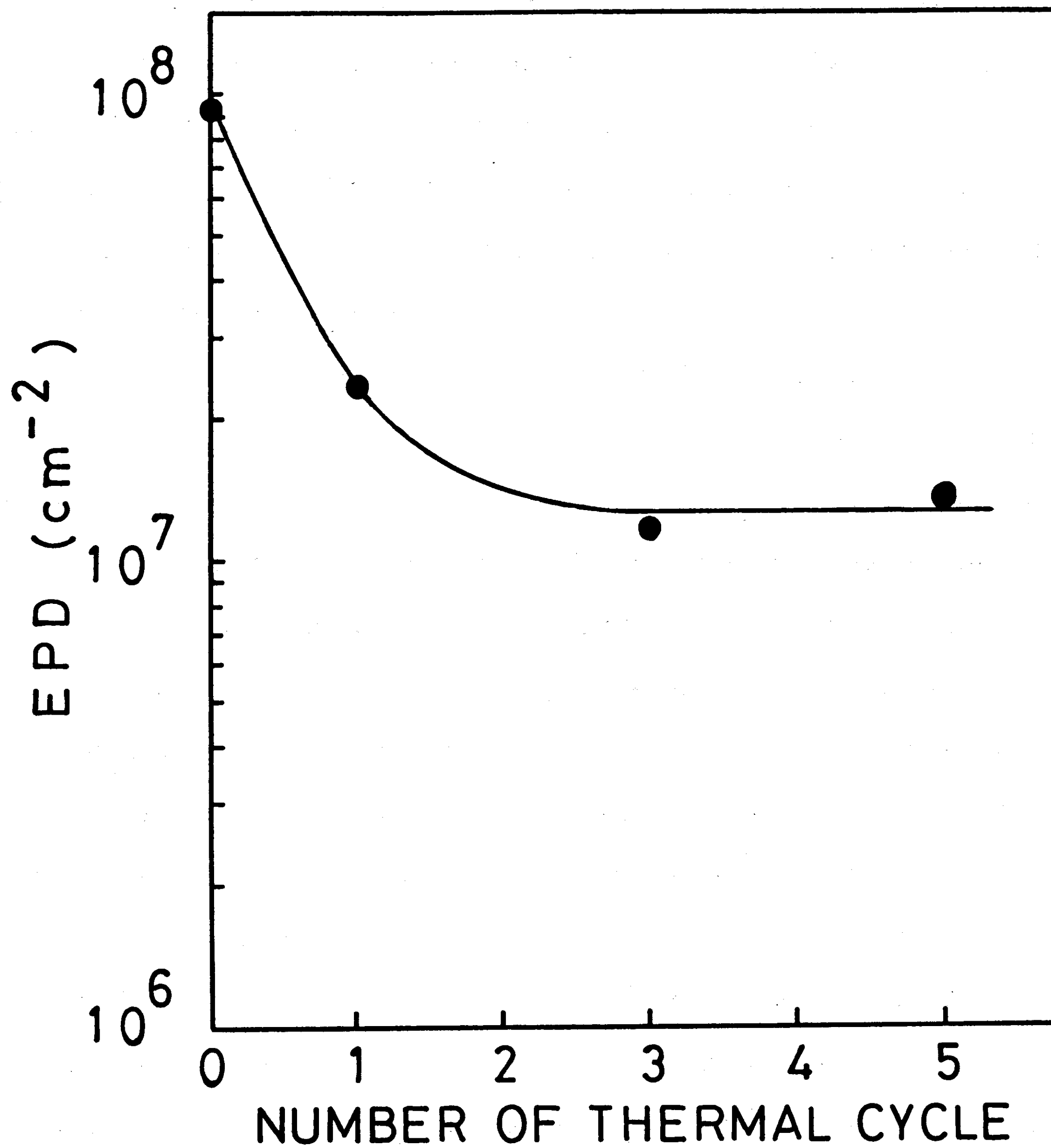


Fig. 3.11. Dependence of the EPD in the GaAs/Si on the number of thermal cycle annealing.

three times of thermal cycle annealing is reduced to 1.5×10^7 cm^{-2}. Figure 3.12 shows the I-L characteristic of the SQW laser, which has an EPD of 9.5×10^7 cm^{-3}, on SiO_2 back-coated Si without thermal cycle annealing. The pulsed I_{th} of 210 mA (J_{th}=5.83 kA/cm^2) has been obtained at room temperature. This laser could not operate under the cw condition because of a high density of threading dislocations. In order to study the propagation of dislocations, cross-sectional TEM was performed for the lasers grown on Si with and without thermal cycle annealing. Figures 3.13 (a) and (b) show cross-sectional TEM micrographs of the lasers grown on Si with and without thermal cycle annealing, respectively. Note that most dislocations in the sample with thermal cycle annealing confine into the Se-doped GaAs layer and not intrude the active layer. This result indicates that confinement of dislocations into the Se-doped GaAs layer is useful to obtain the cw operation. Figure 3.14 shows the I-L characteristic of the laser with thermal cycle annealing on Si without SiO_2 back coating. The laser has the cw I_{th} of 95 mA (J_{th}=2.4 kA/cm^2) at room temperature, which is higher than that of the laser with thermal cycle annealing on a SiO_2 back-coated Si substrate. Another important effect of SiO_2 back coating has been observed in the current-voltage (I-V) characteristic of the laser on Si. The I-V characteristics of the lasers on Si with and without SiO_2 back coating are shown in Fig. 3.15. The lasers on SiO_2 back-coated Si show a sharp turn-on, while the lasers

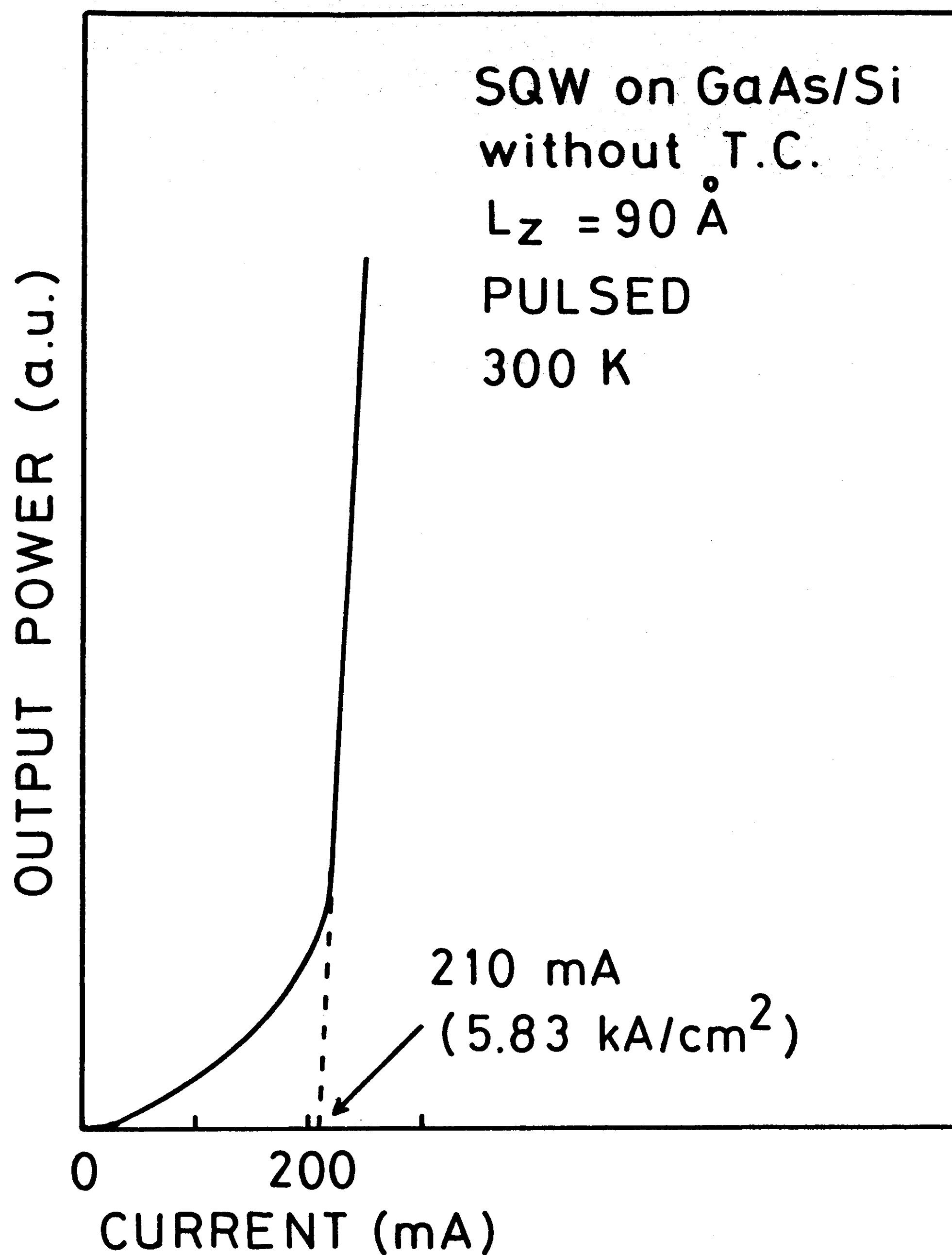
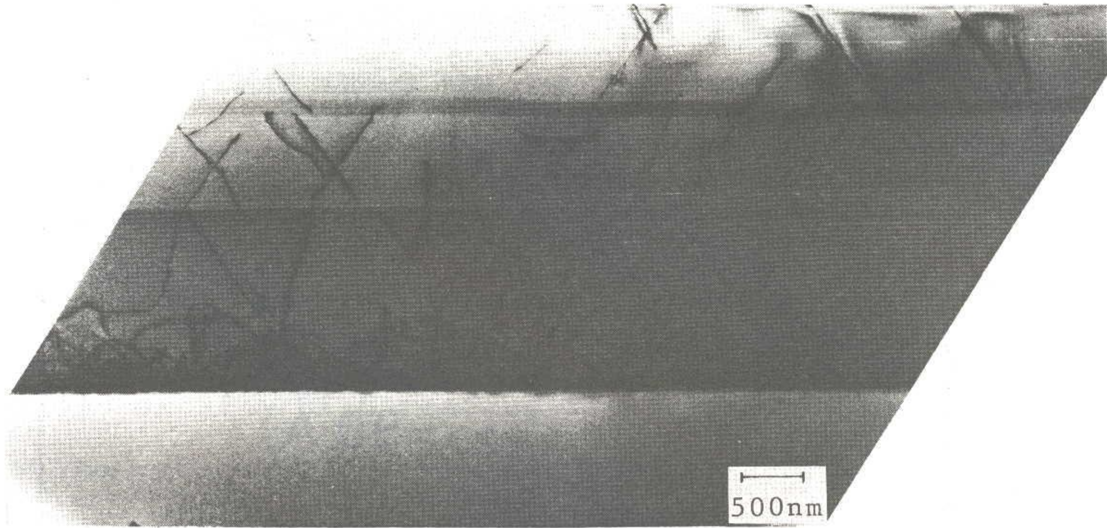
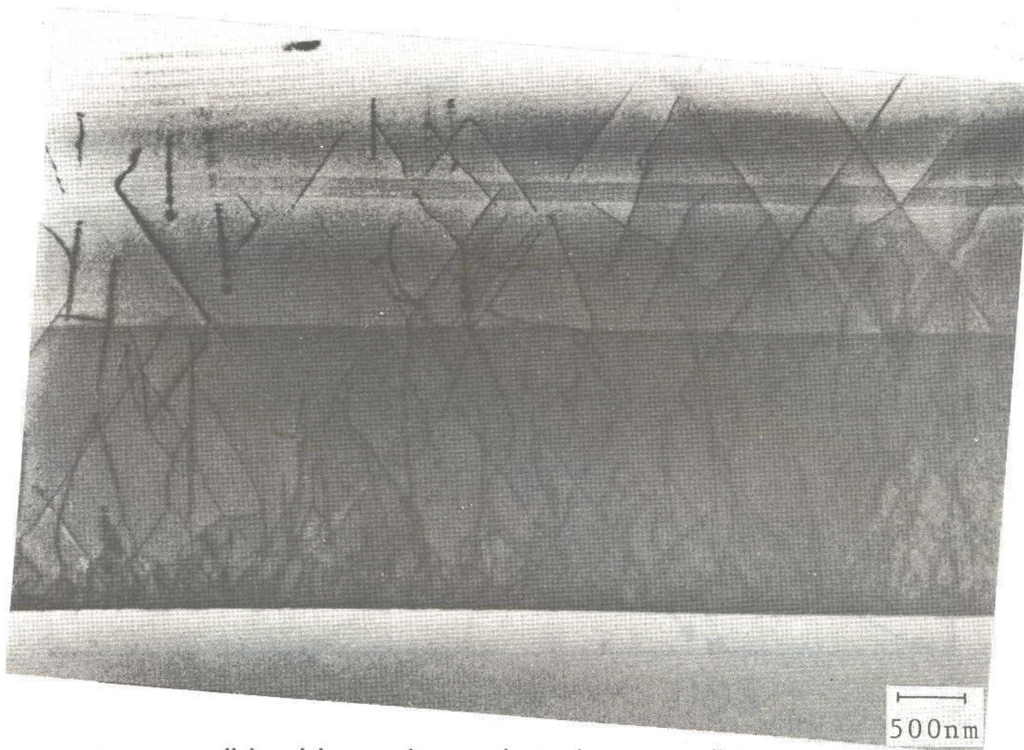


Fig. 3.12. Room-temperature pulsed I-L characteristic of the SQW laser on SiO_2 back-coated Si without thermal cycle annealing.



(a) with thermal cycle annealing



(b) without thermal cycle annealing

Fig. 3.13. Cross-sectional TEM micrographs of the SQW lasers grown on Si (a) with and (b) without thermal cycle annealing.

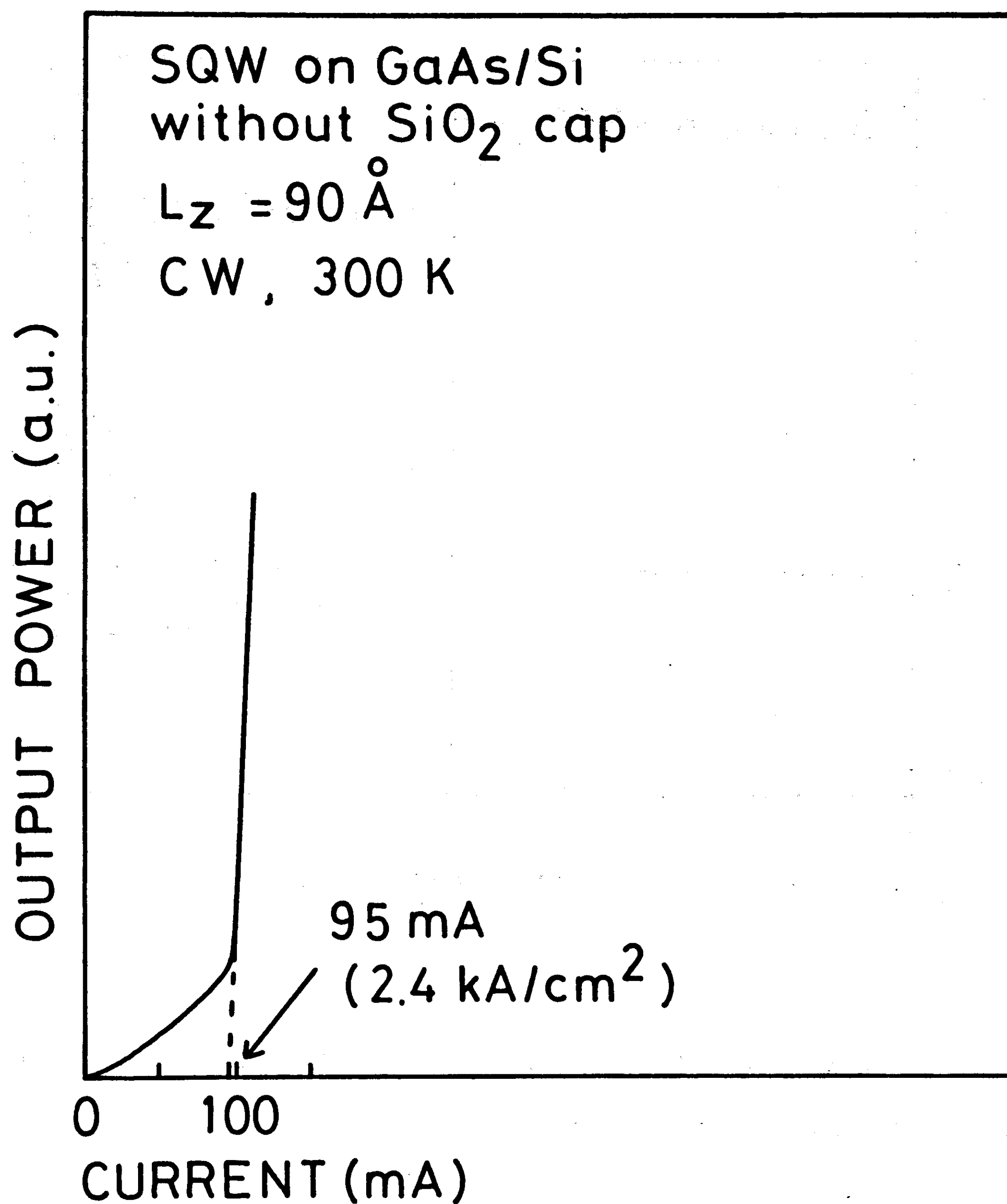


Fig. 3.14. Room-temperature cw I-L characteristic of the SQW laser with thermal cycle annealing on Si without SiO_2 back coating.

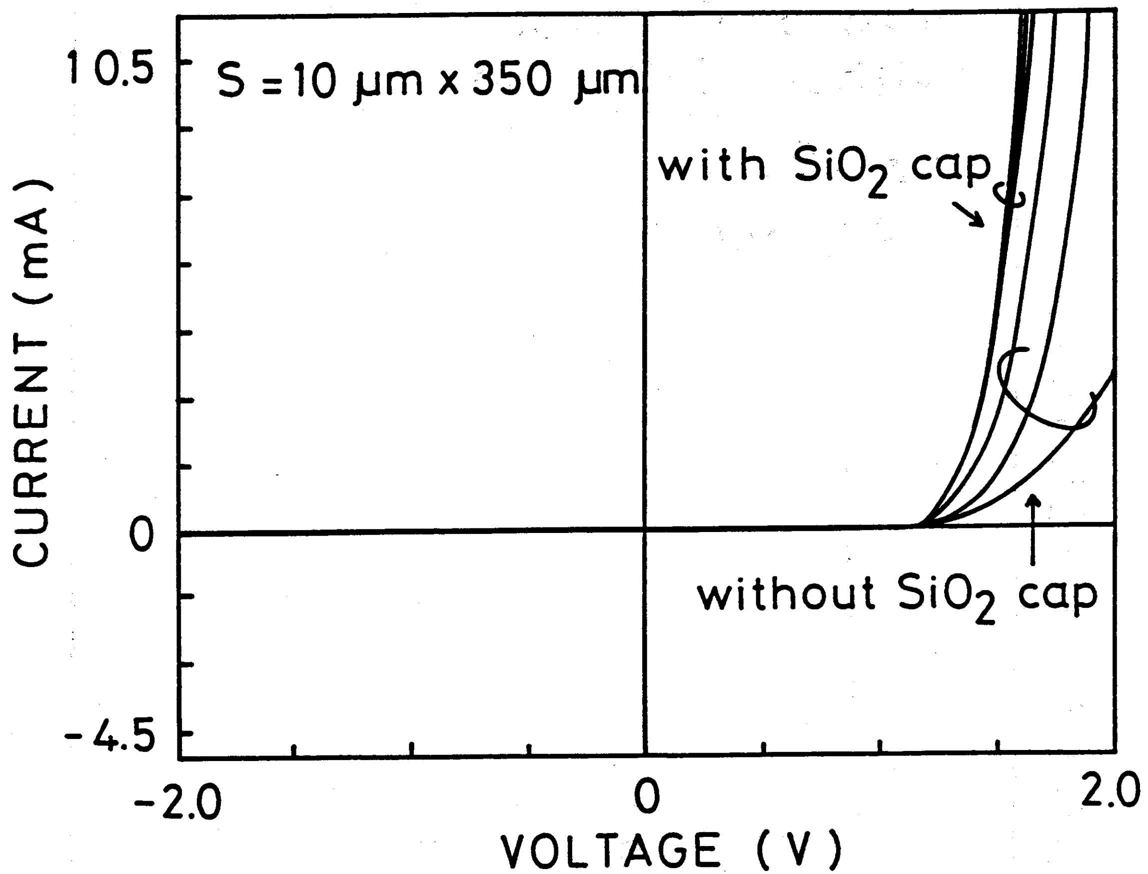


Fig. 3.15. I-V characteristics of the SQW lasers on Si with and without SiO_2 back coating.

on Si without SiO_2 back coating show a gradual turn-on. This result is thought to be due to the conversion of p-type cladding layer to n-type [18]. The above results indicate that SiO_2 back coating is effective in obtaining an excellent I-V characteristic and a lower threshold of the laser on Si.

The average values of J_{th} ($\overline{J_{th}}$), the standard deviation of J_{th} (σJ_{th}), the $\overline{\eta_d}$ and the $\sigma\eta_d$ of the lasers on GaAs and Si grown by the two-step growth technique and with the AlGaAs/AlGaP intermediate layers are summarized in Table I. Figures 3. 16 (a) and (b) show the distribution of the threshold current density and the differential quantum efficiency of the SQW lasers, respectively. For the laser on GaAs, the values of $\overline{J_{th}}$, σJ_{th}, $\overline{\eta_d}$ and $\sigma\eta_d$ are 1.48 kA/cm^2, 0.29 kA/cm^2, 59.6 % and 9.8 %, respectively. For the laser on Si grown by the two-step growth technique, the values of $\overline{J_{th}}$, σJ_{th}, $\overline{\eta_d}$ and $\sigma\eta_d$ are 2.41 kA/cm^2, 0.53 kA/cm^2, 29.2 % and 14.4 %, respectively. For the laser on Si grown with AlGaAs/AlGaP intermediate layers, on the other hand, the values of $\overline{J_{th}}$, the σJ_{th}, the $\overline{\eta_d}$ and the $\sigma\eta_d$ are 2.23 kA/cm^2, 0.33 kA/cm^2, 50.3 % and 11.6 %, respectively, which are superior to those of the laser grown by the two-step growth technique. Note that significant improvement with the use of the AlGaAs/AlGaP intermediate layers is observed in the value of η_d. As discussed in section 2.3, the heterointerfaces of the SQW's on Si grown with the AlGaAs/AlGaP intermediate layers are smoother than those

Table I. Summary of laser characteristics.

SQW laser	$\overline{J_{th}}$ [kA/cm^2]	σJ_{th} [kA/cm^2]	$\overline{\eta_d}$ [%]	$\sigma\eta_d$ [%]
SQW/GaAs	1.48	0.29	59.6	9.8
SQW/Si				
Two-step growth	2.41	0.53	29.2	14.4
AlGaAs/AlGaP ILs	2.23	0.33	50.3	11.6

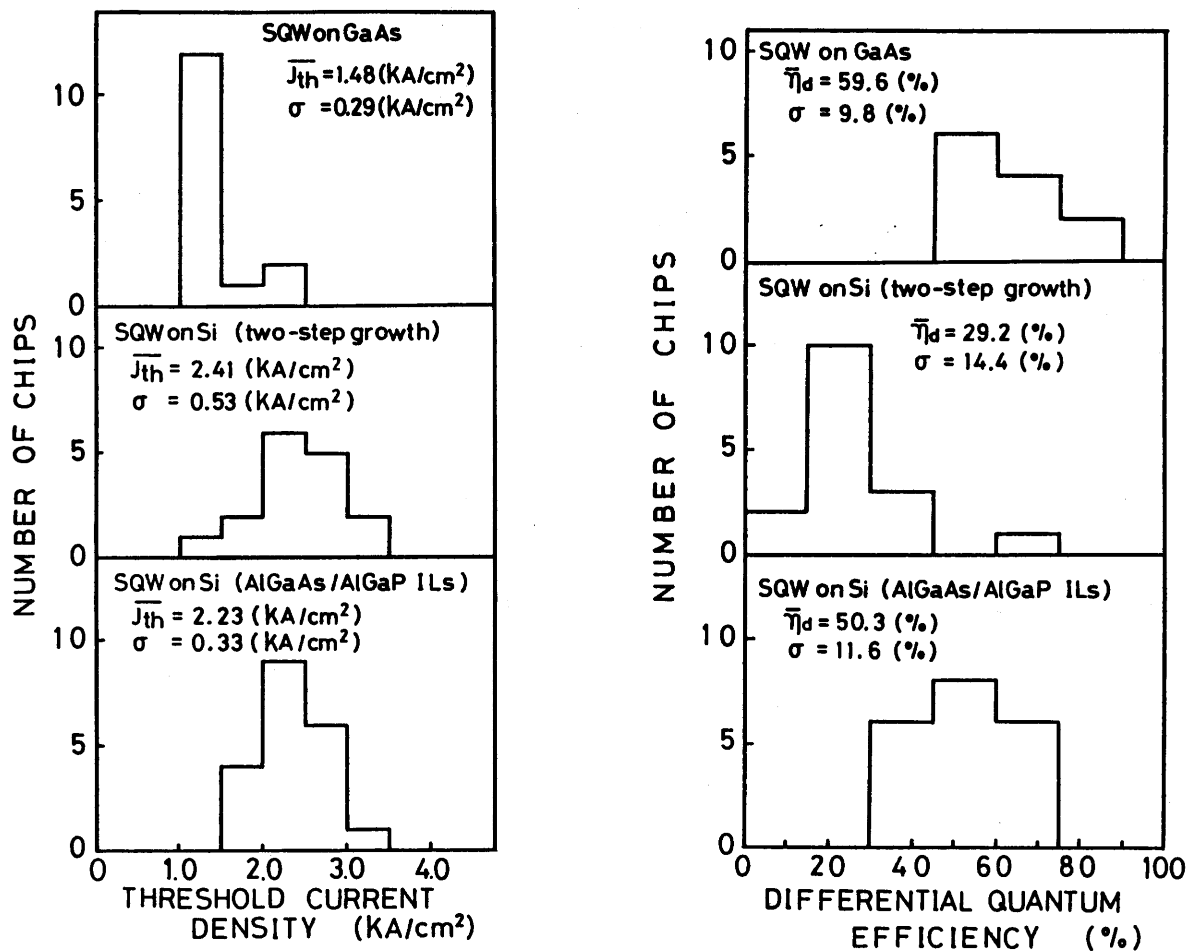
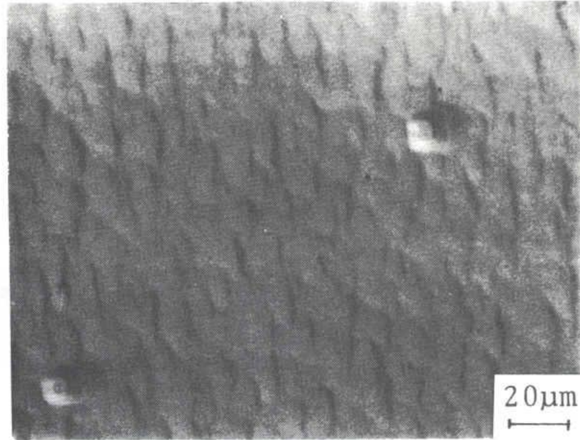


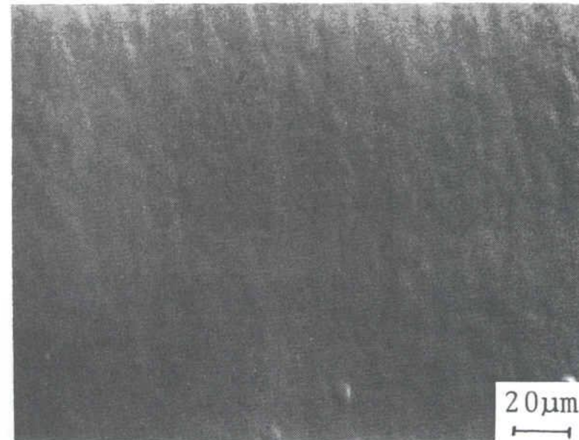
Fig. 3.16. Distribution of (a) the threshold current density and (b) the differential quantum efficiency for the SQW lasers on GaAs and Si grown by the two-step growth technique and with the $Al_{0.5}Ga_{0.5}As/Al_{0.55}Ga_{0.45}P$ intermediate layers.

grown by the two-step growth technique. Figures 3. 17 (a) and (b) show Nomarski micrographs of the surface morphology of the SQW lasers on Si grown by the two-step growth technique and with the AlGaAs/AlGaP intermediate layers, respectively. The surface morphology of the laser grown with the AlGaAs/AlGaP intermediate layers is smoother than that grown by the two-step growth technique. Figures 3.18 (a) and (b) show cross-sectional SEM micrographs of the SQW lasers on Si grown by the two-step growth technique and with the AlGaAs/AlGaP intermediate layers, respectively. Compared with the two-step growth technique, as shown in Fig. 3.18, the waveguide layer in the lasers grown with the AlGaAs/AlGaP intermediate layers are flatter, which results in the decrease of internal loss of the lasers. The improvement of η_d of the lasers on Si grown with the AlGaAs/AlGaP intermediate layers is thought to be due to the decrease of internal loss. The threshold current density J_{th} is shown as a function of the cavity length L in Fig. 3.19 for the 300-μm-wide SQW lasers. In all cases, the values of J_{th} decreases monotonically as the cavity length is increased. The values of J_{th} for the lasers on Si grown with the AlGaAs/AlGaP intermediate layers are lower than those of the lasers on Si grown by the two-step growth technique.

In order to study the effect of the AlGaAs/AlGaP intermediate layers on the laser characteristics in detail, the differential quantum efficiency η_d was measured as a

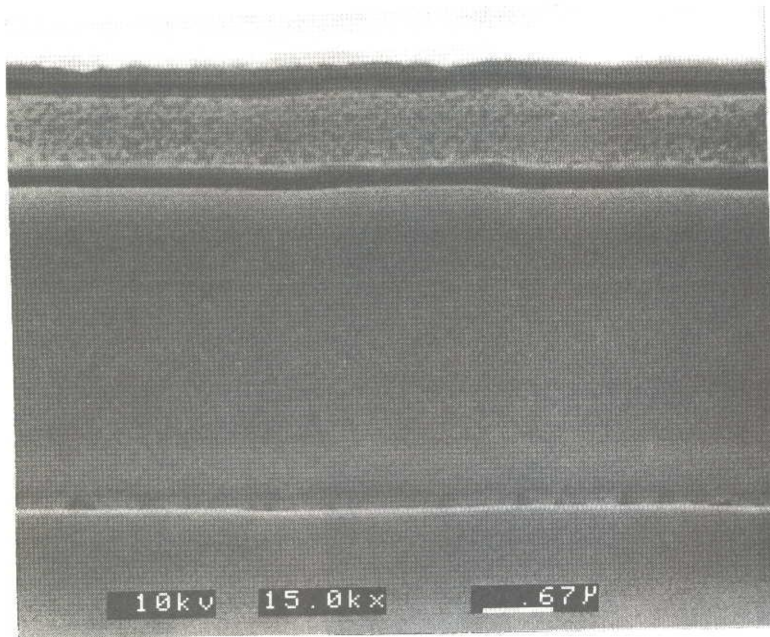


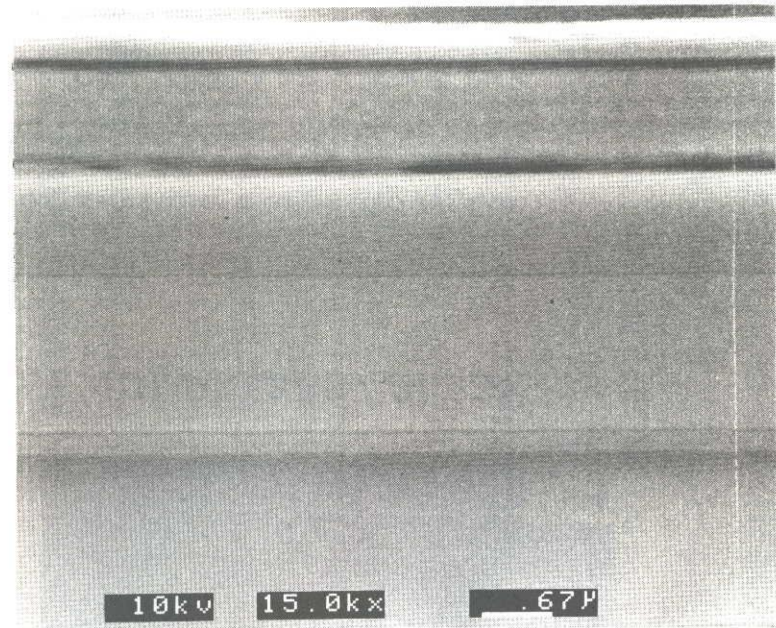
(a) Two-step growth



(b) AlGaAs / AlGaP

Fig. 3.17. Nomarski micrographs of surface morphology for the SQW lasers on Si grown by (a) the two-step growth technique and with (b) the $Al_{0.5}Ga_{0.5}As/Al_{0.55}Ga_{0.45}P$ intermediate layers.





(a) Two-step growth

(b) AlGaAs / AlGaP

Fig. 3.18. Cross-sectional SEM micrographs of the SQW lasers on Si grown by (a) the two-step growth technique and with (b) the $Al_{0.5}Ga_{0.5}As/Al_{0.55}Ga_{0.45}P$ intermediate layers.

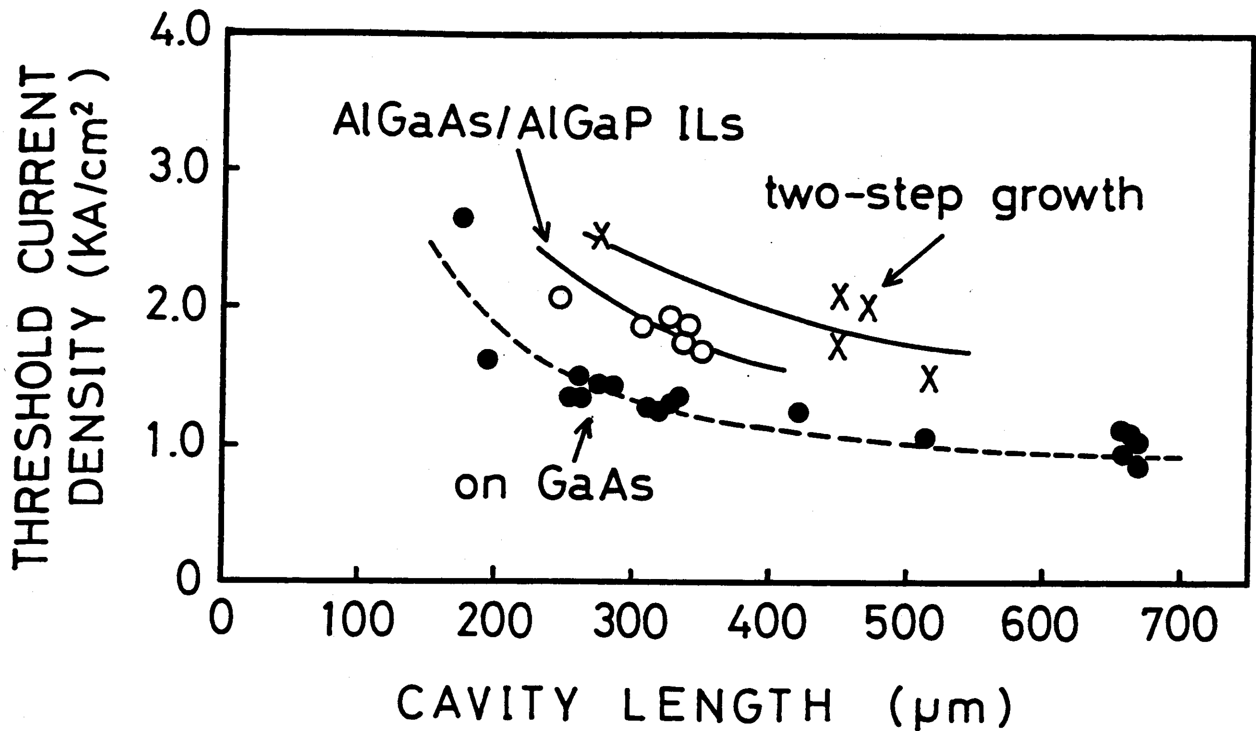


Fig. 3.19. Threshold current density as a function of cavity length for the SQW lasers on GaAs and Si grown by the two-step growth technique and with the $Al_{0.5}Ga_{0.5}As/Al_{0.55}Ga_{0.45}P$ intermediate layers.

function of the cavity length L and the internal quantum efficiency η_i and the intrinsic mode loss coefficient α_i were determined. Under conditions in which η_i and α_i do not vary with cavity length, η_d is given by [28]

$$1/\eta_d=(1/\eta_i)[1+\alpha_i L/\ln(1/R)]$$

where $R=(R_1R_2)^{1/2}$ is the geometric mean of the two facet reflectivities R_1 and R_2 and is taken to be equal to 0.32 for uncoated facets. The reciprocal of η_d is plotted against the cavity length in Fig. 3.20 for the lasers grown on GaAs and Si substrates. The straight line drawn through the points yields the η_i of 87 % and the α_i calculated from the slope of this line is 21 cm^{-1} for the laser on GaAs. For the laser on Si grown by the two-step growth technique, η_i is 73 % and α_i is 31 cm^{-1}. For the laser on Si grown with the AlGaAs/AlGaP intermediate layers, η_i and α_i are 84 % and 22 cm^{-1}, respectively, which are superior to those figures for the laser on Si grown by the two-step growth technique. Analyzed by fitting the $1/\eta_d$ vs. L, the data show the characteristics of a laser grown on Si with the AlGaAs/AlGaP intermediate layers are comparable to those on GaAs.

Figure 3.21 shows the threshold current density J_{th} as a function of the mirror loss $L^{-1}\ln(1/R)$ for the lasers on GaAs and Si substrates. The threshold current density J_{th} is related to differential gain coefficient β and

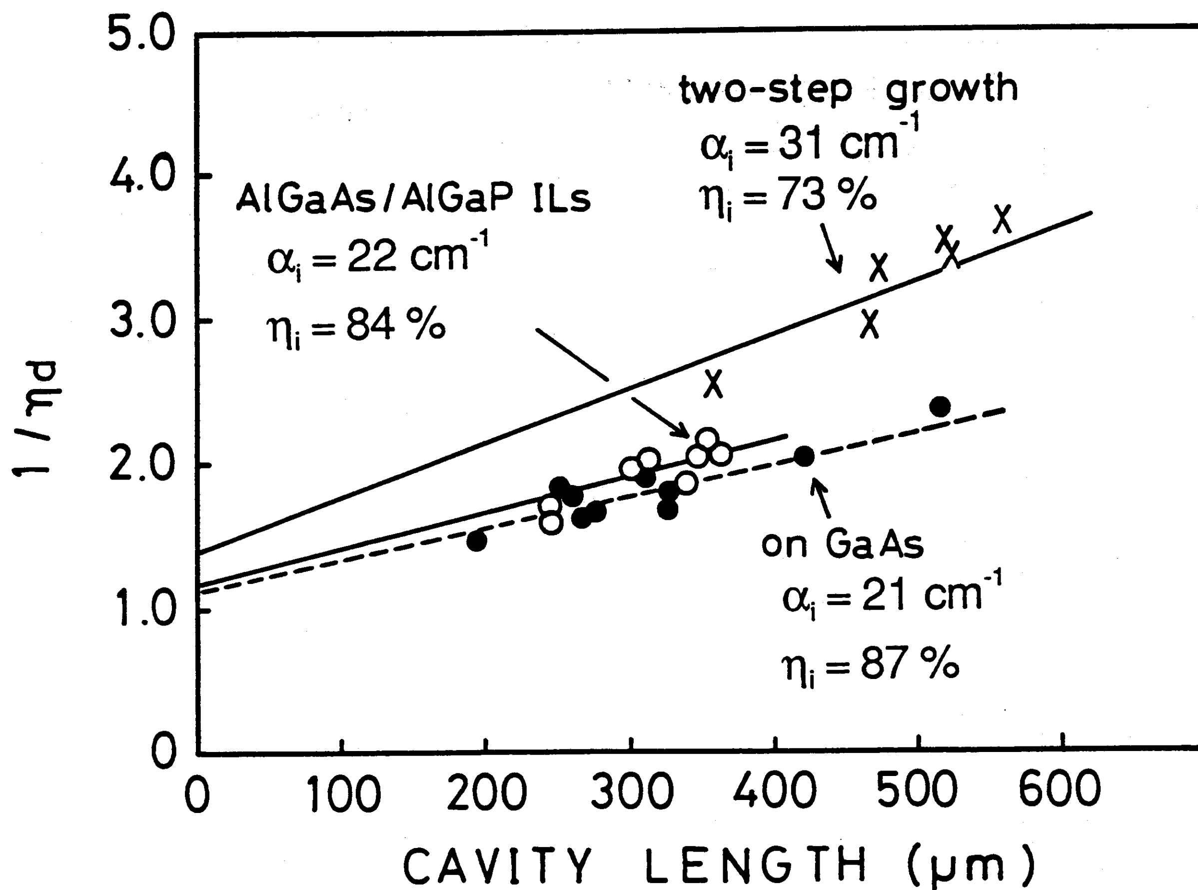


Fig. 3.20. Reciprocal differential quantum efficiency as a function of cavity length for the SQW lasers on GaAs and Si grown by the two-step growth technique and with the $Al_{0.5}Ga_{0.5}As/Al_{0.55}Ga_{0.45}P$ intermediate layers.

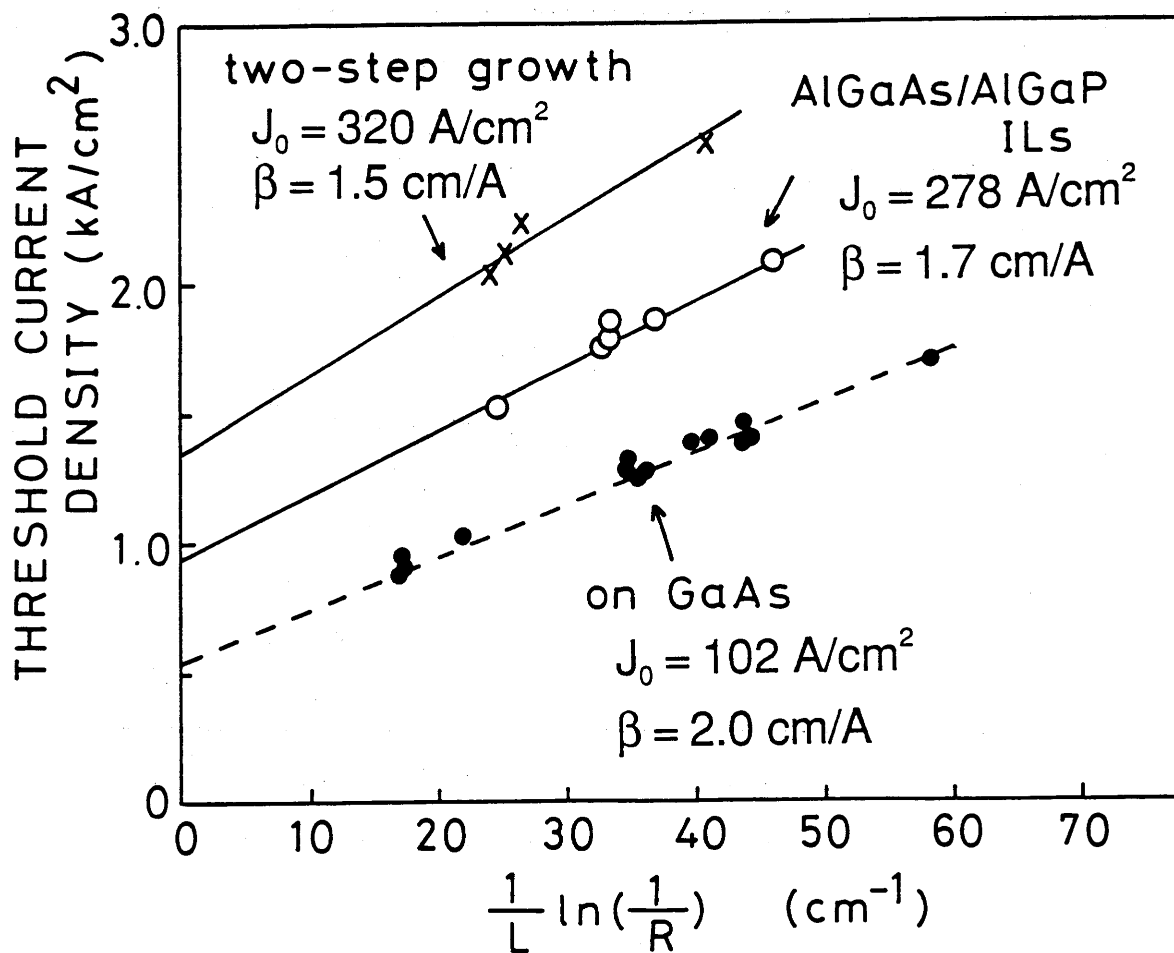


Fig. 3.21. Threshold current density as a function of mirror loss for the SQW lasers on GaAs and Si grown by the two-step growth technique and with the $Al_{0.5}Ga_{0.5}As/Al_{0.55}Ga_{0.45}P$ intermediate layers.

transparency current J_0 as given in the following equation 29):

$$J_{th}=J_0/\eta_i+(\eta_i\beta\Gamma)^{-1}[\alpha_i+L^{-1}\ln(1/R)]$$

where Γ is the optical confinement factor. Assuming that Γ is 0.03 and using the values of η_i and α_i obtained from the relationship of $1/\eta_d$ vs. L, the values of J_0 and β can be estimated and the laser on GaAs are 102 A/cm^2 and 2.0 cm/A, respectively. The J_0 and β of the lasers on Si substrates are 320 A/cm^2 and 1.5 cm/A for the two-step growth technique, and 278 A/cm^2 and 1.7 cm/A for the AlGaAs/AlGaP intermediate layers, respectively. The values of J_0 and β for the SQW laser on Si grown with the AlGaAs/AlGaP intermediate layers are superior to those of the laser on Si grown by the two-step growth technique.

The reliability of lasers on Si are required for practical applications. The aging test was performed at 50 K for the SQW laser on Si grown by the two-step growth technique because the laser on Si has operated for several minutes under the cw condition at room-temperature. The aging characteristic at 50 K of the SQW laser on Si grown by the two-step growth technique is shown in Fig. 3.22. The ambient atmosphere was air and the device was not facet coated. Compared with the laser on GaAs, as will be described in the following paragraph, the laser on Si degrades rapidly. For even the most reliable AlGaAs/GaAs

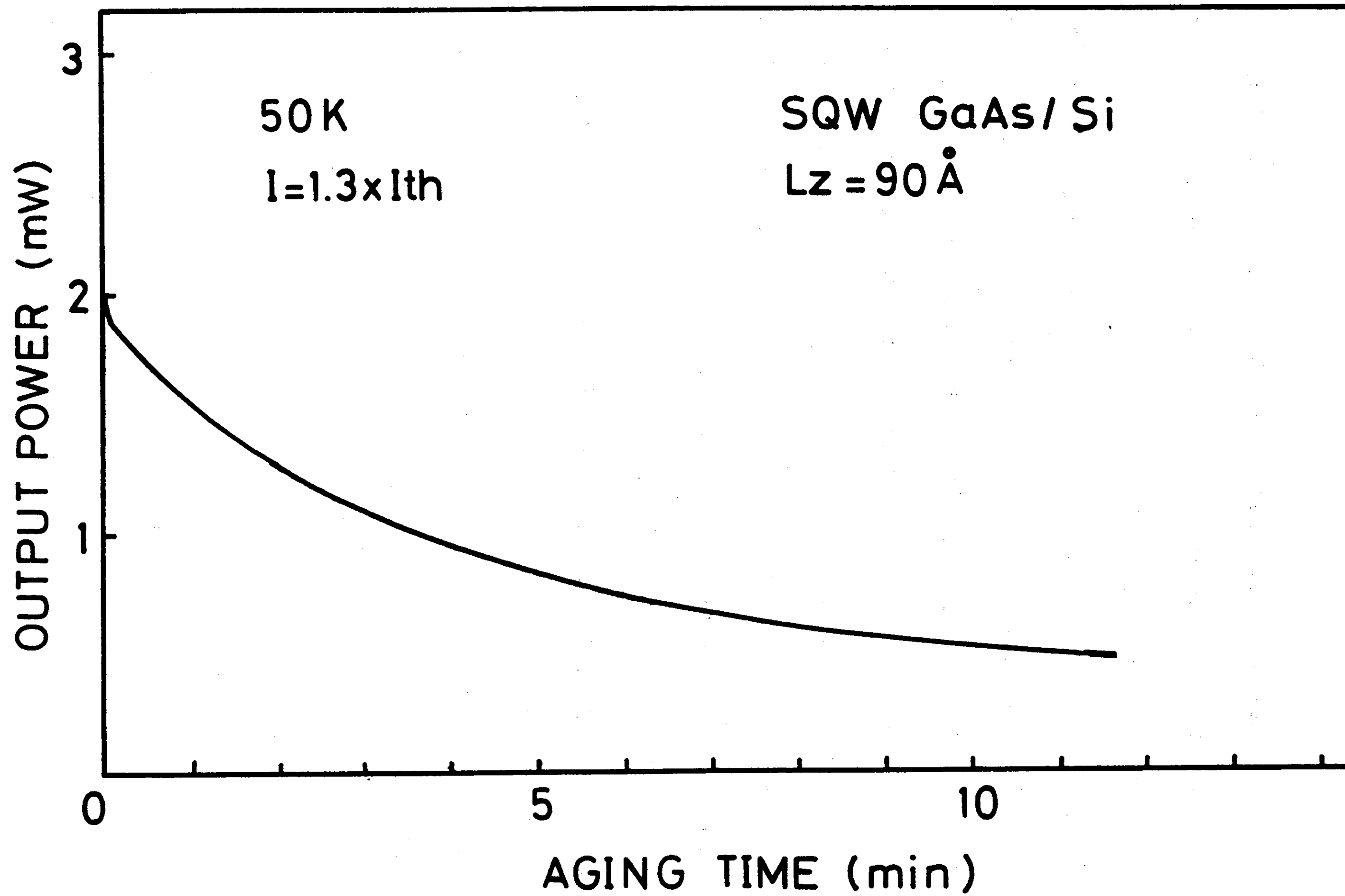


Fig. 3.22. Aging characteristic at 50 K for the SQW laser on Si grown by the two-step growth technique.

laser on Si so far reported, the cw threshold current increased by a factor of 3 in 10 h. This rapid degradation is caused by the formation and propagation of dark-line defects (DLD's), which take place at high rates because the layers on Si substrate are not only subject to high tensile stress but also contain a high density of threading dislocations.

To study the degradation mechanism of the lasers on Si, aging tests at 300 K were performed for the lasers on the GaAs/GaAs and $GaAs_{0.5}P_{0.5}$/GaAs. Figure 3.23 shows the results of the aging tests at 300 K for the lasers on the GaAs/GaAs and the $GaAs_{0.5}P_{0.5}$/GaAs. The laser on GaAs/GaAs, which has an EPD of $5x10^3$ cm^{-2}, operated for over 15 h without significant degradation. In contrast, the laser on $GaAs_{0.5}P_{0.5}$/GaAs, which has an EPD of $1x10^7$ cm^{-2}, degrades rapidly. This rapid degradation in the laser on $GaAs_{0.5}P_{0.5}$/GaAs is thought to be caused by non-radiative recombination centers associated with the dislocations rather than by the stress. Continuous operation, for periods of up to several hours, was obtained by other groups using a laser with low threshold and low dislocations in the active layer. These results suggest that the reduction of threading dislocations in the active layer is necessary to obtain reliable lasers on Si.

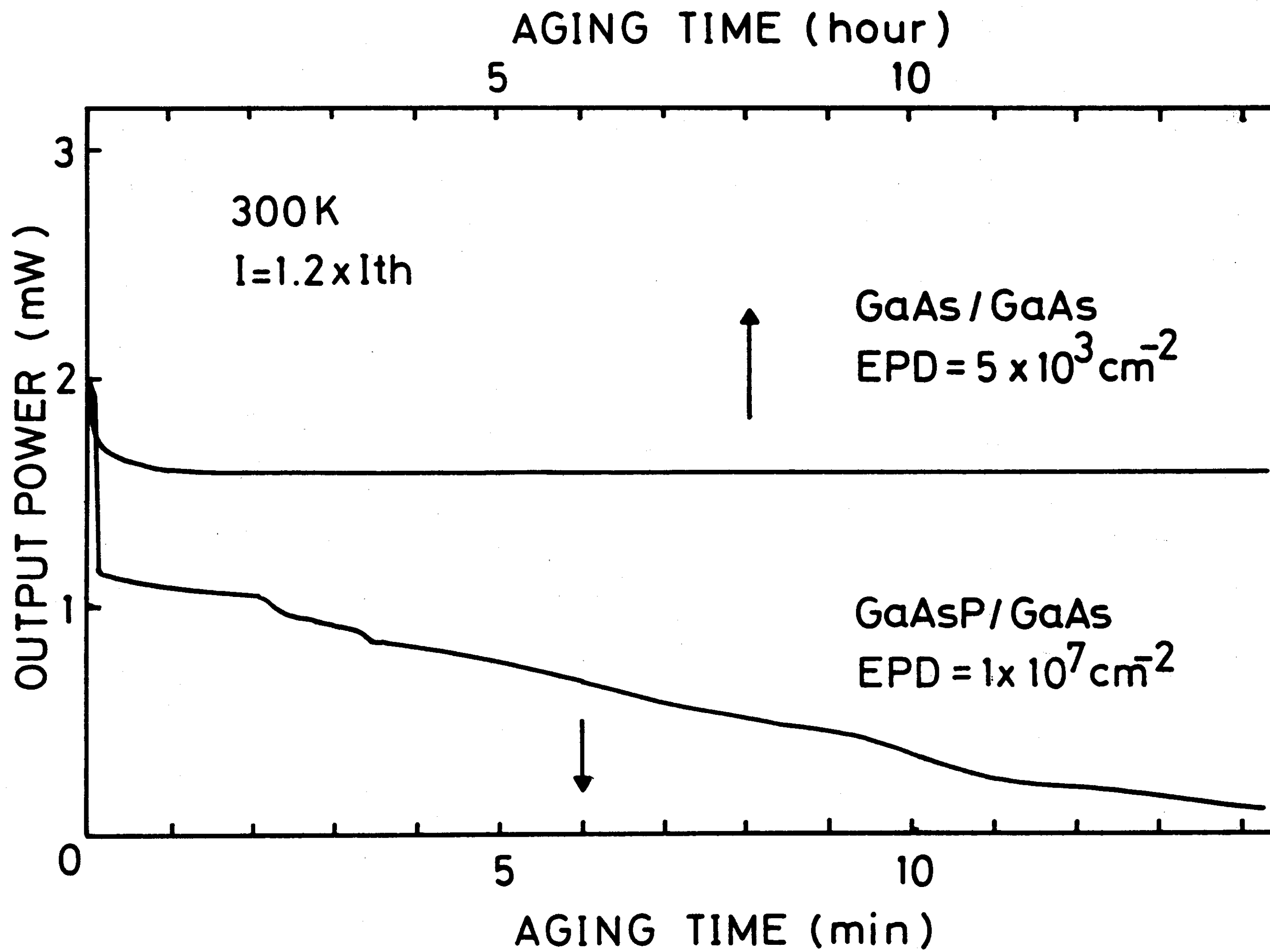


Fig. 3.23. Aging characteristics at 300 K for the SQW lasers on the GaAs/GaAs and GaAsP/GaAs.

3.4 Conclusions

The characteristics of all-MOCVD-grown AlGaAs/GaAs DH and SQW lasers on Si have been studied. The DH laser on Si has been operated under the pulsed condition at room temperature. The cw operation with the I_{th}=100 mA (J_{th}=3.55 kA/cm^2) has been achieved below 130 K. The polarization of the DH lasers can be controlled by the Al composition in the $Al_xGa_{1-x}As$ cladding layer.

By performing thermal cycle annealing, the cw operation at room temperature has been achieved for all-MOCVD-grown SQW lasers on Si by the two-step growth technique and with the AlGaAs/AlGaP intermediate layers. Thermal cycle annealing is effective in reducing the number of threading dislocations in the active layer of the SQW lasers on Si. The values of J_{th}, η_d, η_i, α_i, β and J_0 are 1.72 kA/cm^2, 67 %, 84 %, 22 cm^{-1}, 1.7 cm/A and 278 A/cm^2, respectively, for the SQW lasers on Si grown with the AlGaAs/AlGaP intermediate layers. Compared with the SQW laser on Si grown by the two-step growth technique, the laser characteristics have been improved by use of the AlGaAs/AlGaP intermediate layers, which are caused by the smoother heterointerfaces. It is clear that the AlGaAs/AlGaP intermediate layers have played an important role in achieving the smoother heterointerfaces and the excellent characteristics of the SQW laser on Si. However, the SQW lasers on Si still have a problem with short

lifetime. Major improvements in material quality are necessary in order to increase the reliability of lasers on Si to the level required for practical applications.

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Chapter 4. Schottky Diodes Grown on Si

4.1 Introduction

When GaAs/Si is applied to electronic devices such as metal-semiconductor field-effect transistors (MESFET's)[1-9] and high electron mobility transistors (HEMT's)[10-12], it is necessary to study the electrical characteristics, especially the Schottky diode characteristics, of the GaAs/Si. The Schottky barrier gate[13-16] is one of the two most important elements of GaAs FET's, the other being ohmic metal. However, such a study has been lacking so far because it is well known that dislocations affect minority carrier devices including laser diodes[17-20], solar cells[21,22], light-emitting diodes[23] rather than majority carrier devices including MESFET's and HEMT's. Although many electronic devices have been fabricated on the GaAs/Si[1-12], degradation of electrical characteristics of the devices due to a high density of threading dislocations (10^7-10^8 cm^{-2}) have not been reported in detail.

In this chapter, Schottky diode characteristics on MOCVD-grown GaAs/Si by the two-step growth technique[24] and using intermediate layers consisting of $GaP/GaAs_{0.5}P_{0.5}$ and $GaAs_{0.5}P_{0.5}/GaAs$ strained layer superlattices on GaP (SLSs/GaP)[25], and $Al_xGa_{1-x}P$[15,26-28] are described in detail. The relationship between crystallinity and Schottky diode characteristics on the GaAs/Si are also reported.

This chapter is organized as follows: In section 4.2, epitaxial growth and fabrication process are presented. Crystallinity and Schottky diode characteristics are described in section 4.3, and this chapter is concluded in section 4.4.

4.2 Epitaxial Growth and Fabrication Process

GaAs epitaxial layers were grown on n-type (Sb-doped, 0.02 Ω-cm) Si substrates oriented 2° off (100) towards [011] in an RF-heated horizontal MOCVD reactor at atmospheric pressure by the two-step growth technique and using the $Al_xGa_{1-x}P$ and SLSs/GaP intermediate layers. The source materials were trimethylgallium (TMG), trimethylaluminum (TMA), pure arsine (AsH_3) and phosphine (PH_3). The substrates were degreased in organic solutions and cleaned using H_2O_2+$4H_2SO_4$ and HF+H_2O solutions. Then the substrates were heated at 1000 ^{o}C for 10 min in H_2 ambient in order to remove the oxide. In the two-step growth technique, a GaAs layer with the thickness of 12.5 nm was first deposited at 400 ^{o}C with a V/III ratio of 80, followed by a GaAs epitaxial layer doped with Se. In the structure with the $Al_xGa_{1-x}P$ intermediate layer, a 50-nm-thick $Al_xGa_{1-x}P$ layer was grown on Si at 900 ^{o}C with a V/III ratio of 100, followed by growth of a GaAs epitaxial layer doped with Se. In the structure with the SLSs/GaP intermediate layers, a 0.1-μm-thick GaP film was grown on Si at 900 ^{o}C with a V/III

ratio of 100, followed by five periods of 20-nm-thick GaP/20-nm-thick $GaAs_{0.5}P_{0.5}$ SLS and five periods of 20-nm-thick $GaAs_{0.5}P_{0.5}$/20-nm-thick GaAs SLS at 750 ^{o}C. Then, a GaAs epitaxial layer doped with Se was grown. In all cases, 3-μm-thick GaAs epitaxial layers doped with Se to $5x10^{16}$ cm^{-3} were grown at 650, 700 and 750 ^{o}C with the growth rate of 50 nm/min and a V/III ratio of 40.

Surface morphology was examined under a Nomarski microscope and the crystallinity of the GaAs top layers was characterized by double-crystal X-ray diffraction, the etch pit density (EPD) revealed by molten KOH etch and electron-beam-induced current (EBIC) measurements. The EBIC images were obtained using a scanning electron microscope with an electron beam current of $2.0x10^{-9}$ A and an accelerating voltage of 12 kV. The formation of dislocations and structures of intermediate layers were studied by cross-sectional transmission electron microscopy (TEM). The solid compositions (x) of $Al_xGa_{1-x}P$ ternary alloys were determined by Auger electron microscopy (AES).

AuGe/Ni/Au ohmic electrodes were formed by vacuum evaporation and alloyed at 380 ^{o}C for 1 min in N_2 ambient. After the contacts were etched by chemical solution, Schottky contacts to Se-doped GaAs were then made by the lift-off technique using Au as Schottky contact metal. The area of the Schottky diodes in this study is $7.85x10^{-3}$ cm^2. For comparison, a Schottky diode was fabricated on lightly doped ($7x10^{16}$ cm^{-3}) n-type GaAs substrate. Forward and

reverse current-voltage (I-V) and capacitance-voltage (C-V) characteristics of the Schottky diodes were measured. The ideality factor and the I-V barrier height (ϕ_b^{I-V}) were calculated from the forward I-V at various temperatures from 150 to 313 K. The capacitance was measured at 1 MHz, and the C-V barrier height (ϕ_b^{C-V}) was also calculated.

4.3 Crystallinity and Schottky Diode Characteristics[15)]

Figure 4.1 shows the full width at half maximum (FWHM) of the (400) reflection peak in the x-ray double-crystal rocking curve as a function of growth temperature. For all samples except the GaAs/Si with the $Al_{0.55}Ga_{0.45}P$ intermediate layer, the FWHM decreases with increasing growth temperature of the GaAs top layer, which suggests that the crystallinity of the GaAs/Si improves at higher growth temperatures. Particularly for the two-step-grown GaAs/Si, improvement of the crystallinity by increasing the temperature from 650 to 700 ^{o}C is significant. At 750 ^{o}C, the FWHMs of the GaAs/Si grown by the two-step growth technique and using $Al_{0.55}Ga_{0.45}P$ and SLSs/GaP intermediate layers are 210, 188 and 152 arcsec, respectively.

Figures 4.2 (a), (b) and (c) show Nomarski micrographs of the surface morphology in the GaAs/Si grown at 750 ^{o}C by the two-step growth technique and using the SLSs/GaP and the $Al_{0.55}Ga_{0.45}P$ intermediate layers, respectively. As shown in Fig. 4.2, the surface morphology of the GaAs/Si grown at

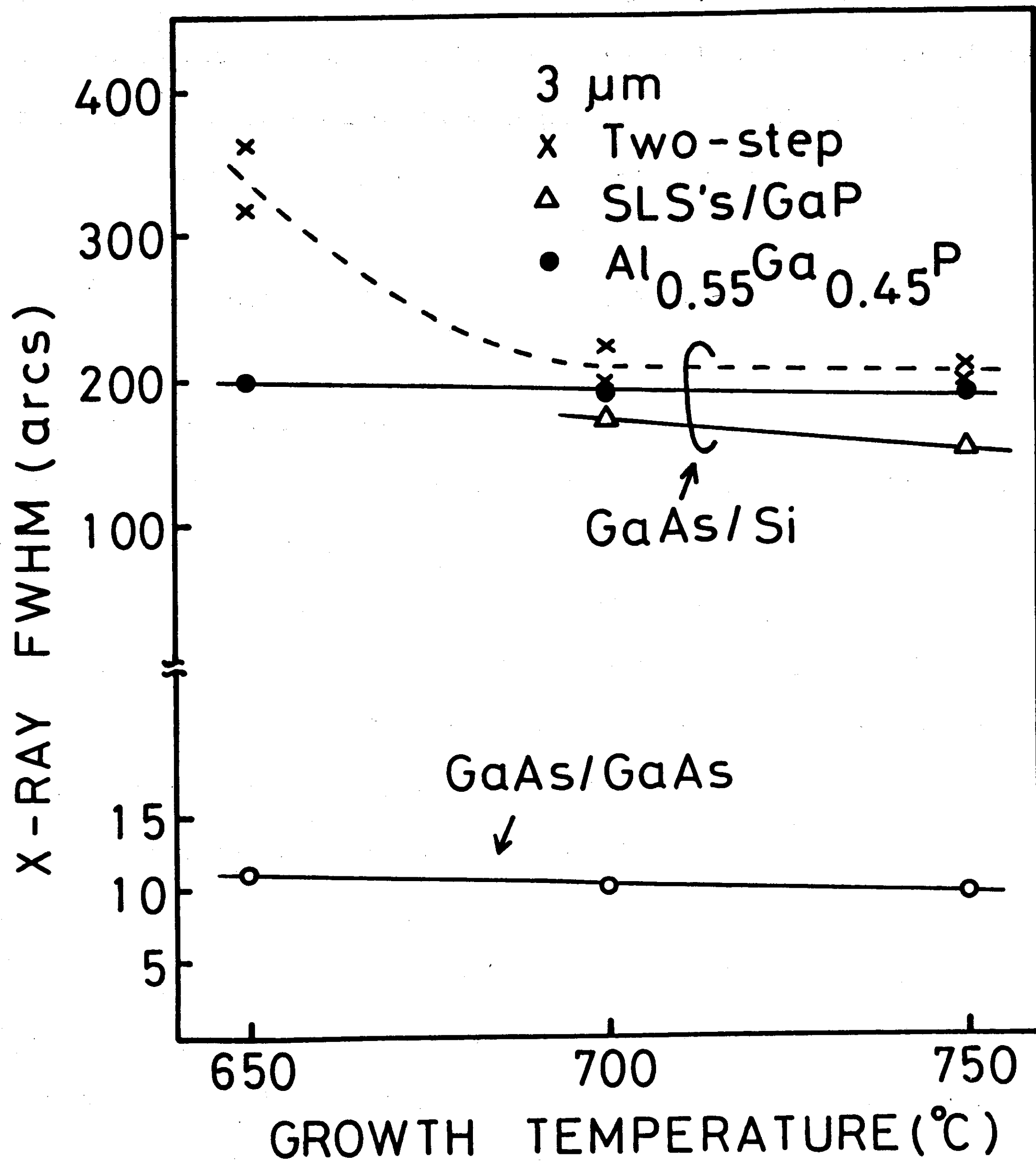


Fig. 4.1. Growth-temperature dependence of X-ray FWHM of GaAs/GaAs and GaAs/Si grown by two-step growth, SLSs/GaP and $Al_{0.55}Ga_{0.45}P$ techniques.

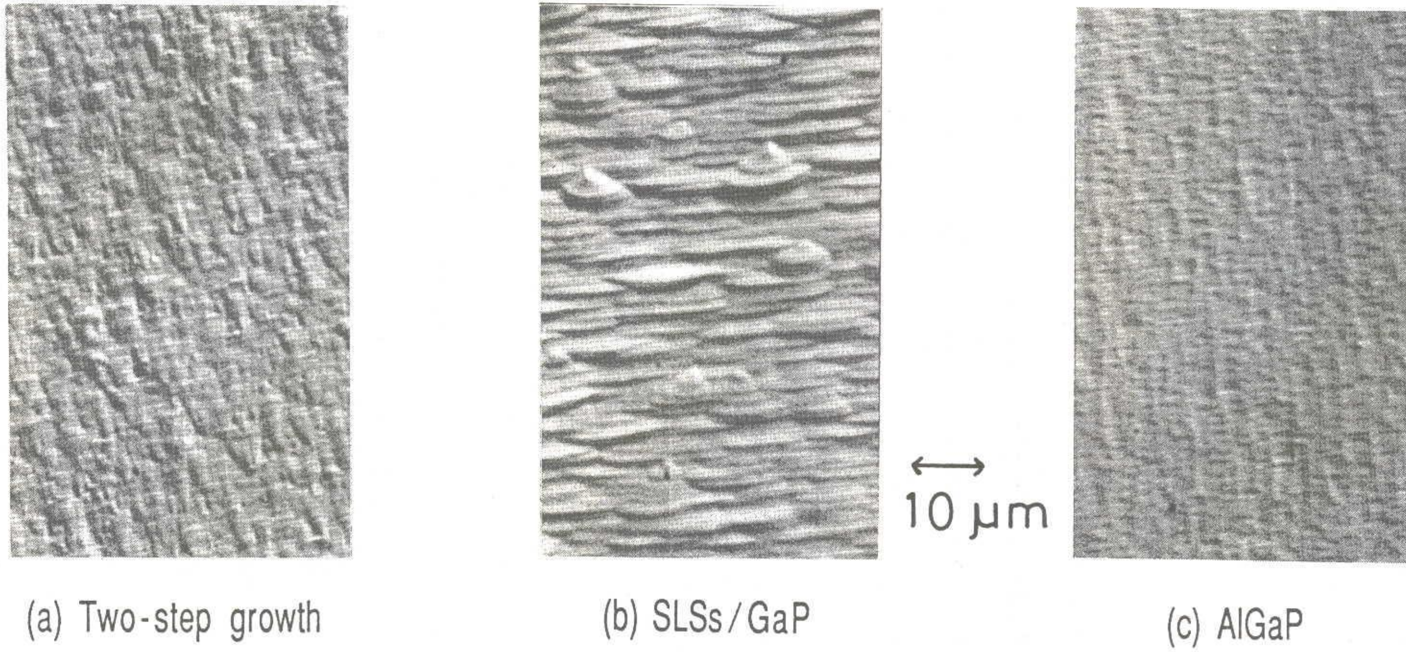
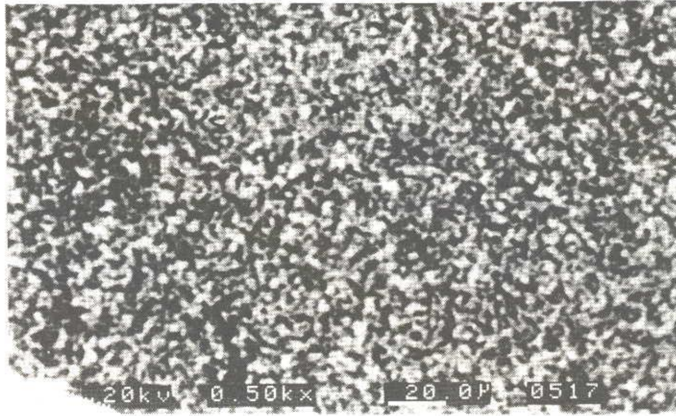


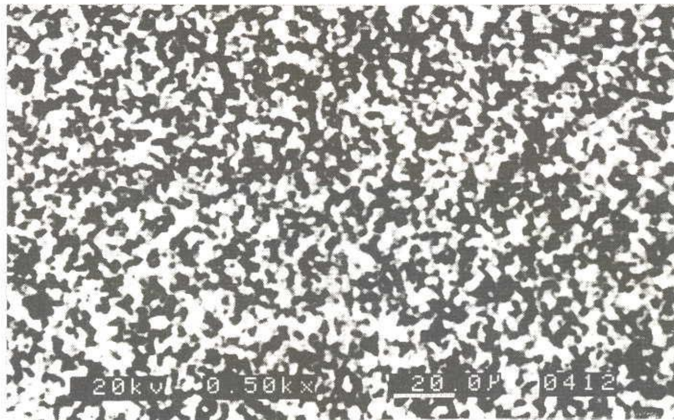
Fig. 4.2. Nomarski micrographs of surface morphology in GaAs/Si grown by (a) two-step growth, (b) SLSs/GaP and (c) $Al_{0.55}Ga_{0.45}P$ techniques.

750 ^{o}C with the $Al_{0.55}Ga_{0.45}P$ intermediate layer is smoother than those of the GaAs/Si grown by the two-step growth technique and using the SLSs/GaP intermediate layers. As shown in section 2.2, in the GaAs/Si grown by the two-step growth technique, threading dislocations originating at the GaAs/Si interface decrease as the surface is approached. The EPD revealed by molten KOH etch is $9.5x10^{7}$ cm^{-2}. At the initial stage of GaAs growth, the GaAs grows three-dimensionally, and GaAs islands are formed. In the GaAs/Si grown with the GaP intermediate layer, the GaP grows three-dimensionally and GaP islands are formed on the Si. Dislocations originate at the GaAs/Si and GaAs/GaP interface and decrease as the surface is approached. On the other hand, the $Al_{0.55}Ga_{0.45}P$ intermediate layer grown on Si is planar, which indicates that the $Al_{0.55}Ga_{0.45}P$ intermediate layer grows quasi-two-dimensionally. Most dislocations originate at the GaAs/$Al_{0.55}Ga_{0.45}P$ interface. However, most of the dislocations are confined near the GaAs/$Al_{0.55}Ga_{0.45}P$ interface and do not reach the surface of the GaAs layer. The EPD of the GaAs/Si grown with the $Al_{0.55}Ga_{0.45}P$ intermediate layer is $2.5x10^{7}$ cm^{-2}. The planar growth of $Al_{0.55}Ga_{0.45}P$ layer on Si is a main factor for improvement of surface morphology and crystallinity in the wide range of growth temperature.

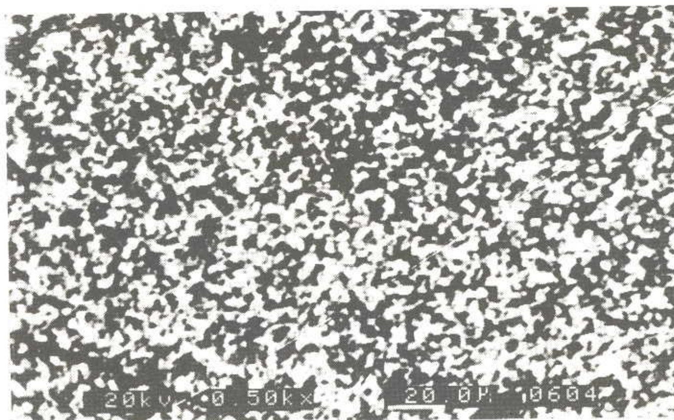
EBIC measurement was performed to study the electrical influence of the dislocations. Figure 4.3 shows the EBIC images of the GaAs/Si grown by the two-step growth technique



(a) Two-step growth



(b) SLSs/GaP



(c) AlGaP

Fig. 4.3. EBIC images of GaAs/Si grown by (a) two-step growth, (b) SLSs/GaP and (c) $Al_{0.55}Ga_{0.45}P$ techniques.

and using the SLSs/GaP and the $Al_{0.55}Ga_{0.45}P$ intermediate layers. The dark spot densities (DSD) of the GaAs/Si grown by the two-step growth technique and using the SLSs/GaP and $Al_{0.55}Ga_{0.45}P$ intermediate layers are 3.6×10^7, 3.4×10^7, and 3.1×10^7 cm^{-2}, respectively. Table I summarizes the results of the x-ray FWHM, EPD, DSD and surface morphology. As will be shown later, Schottky diode characteristics are degraded by a high density of the dark spots in the GaAs/Si.

Figure 4.4 shows the ideality factor calculated from the forward I-V characteristics of Schottky diodes on the GaAs/Si as a function of growth temperature of the GaAs top layer. For comparison, the ideality factor of a Schottky diode fabricated on an n-type GaAs substrate is also shown in the figure. For the $Al_{0.55}Ga_{0.45}P$ intermediate layer, the ideality factor approaches 1 with increasing growth temperature. This result suggests that crystallinity and Schottky diode characteristics of the GaAs/Si improve at higher growth temperature. The ideality factors for the GaAs/Si grown at 750 ^{o}C by the two-step growth technique and by using the SLSs/GaP and $Al_{0.55}Ga_{0.45}P$ intermediate layers are 1.11, 1.09 and 1.06, respectively. The Schottky diode characteristic for the GaAs/Si with the $Al_{0.55}Ga_{0.45}P$ intermediate layer is as good as for the n-type GaAs substrate.

Figure 4.5 shows the dependence of the ideality factor for the GaAs/Si with the $Al_xGa_{1-x}P$ intermediate layer on the Al composition of x. The ideality factors were averaged

TABLE I. Crystallinity of GaAs/Si grown by two-step growth, SLSs/GaP, and $Al_{0.55}Ga_{0.45}P$ techniques.

GaAs/Si	FWHM (arcs)	EPD ($\times10^{7}$ cm^{-2})	DSD ($\times10^{7}$ cm^{-2})	Surface morphology
Two-step growth	210	9.5	3.6	mirrorlike
SLSs/GaP	152	2.0	3.4	mirrorlike
$Al_{0.55}Ga_{0.45}P$	188	2.5	3.1	mirror

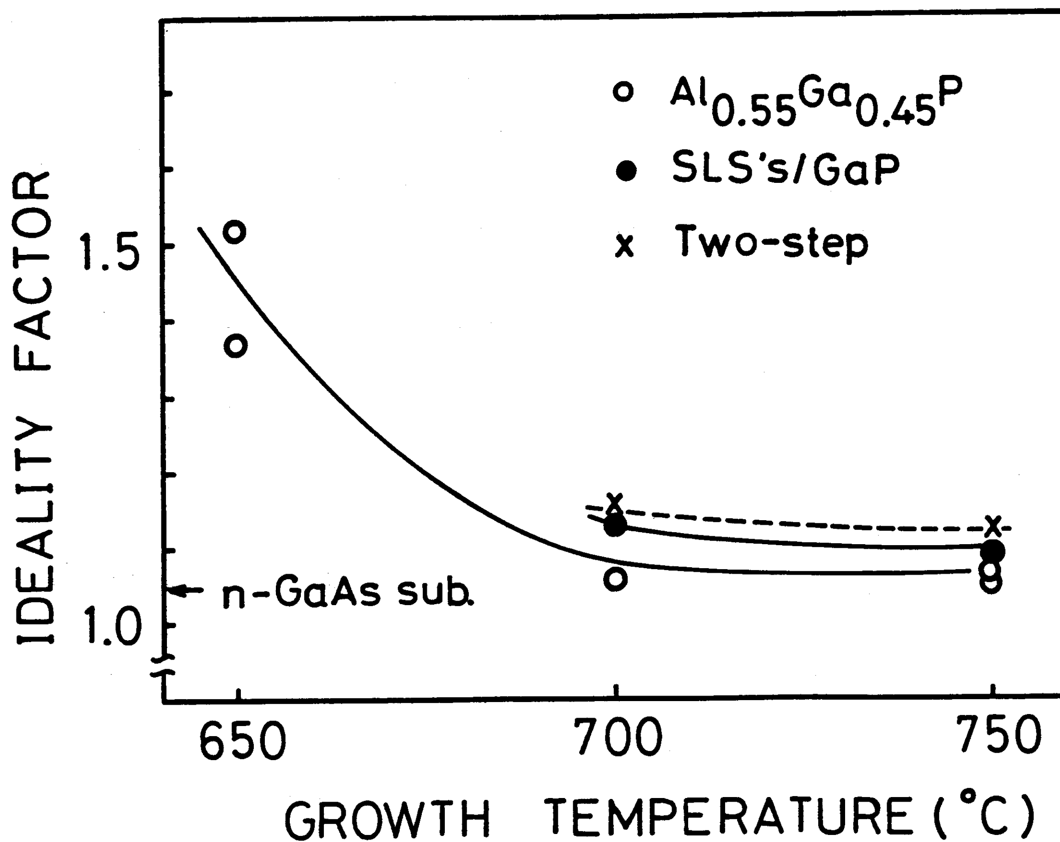


Fig. 4.4. Growth-temperature dependence of ideality factor of Au-GaAs/Si Schottky diodes. The area of the Schottky diode is 7.85×10^{-3} cm^2.

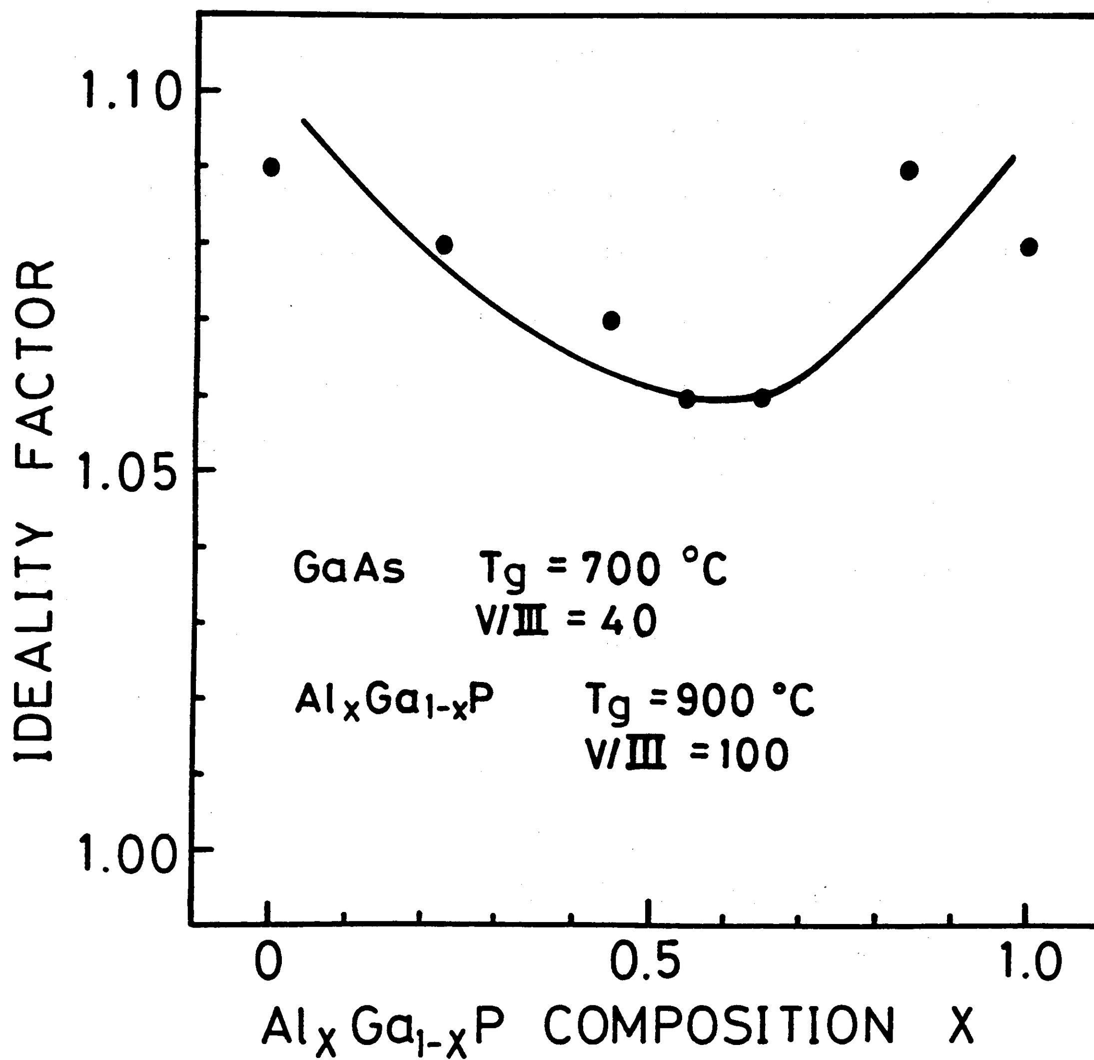


Fig. 4.5. Al composition dependence of ideality factor of Au-GaAs/Si Schottky diodes grown with $Al_xGa_{1-x}P$ intermediate layer. The area of the Schottky diode is 7.85×10^{-3} cm^2.

over 10 samples for each composition. The ideality factor depends on the Al composition of x, and the ideality factor of 1.06 is obtained at the composition of 0.55. This dependence of the ideality factor on the Al composition is similar to those of X-ray FWHMs and the surface morphology discussed in section 2.2.

Assuming the Richardson constant A^{**} is 8.6 $Acm^{-2}K^{-2}$ and that the I-V characteristic follows the thermionic emission model[29], the I-V barrier height (ϕ_b^{I-V}) was calculated from the extrapolated current at 0 V in the forward I-V characteristic, and they are all between 0.86 eV and 0.87 eV.

Figure 4.6 shows plots of C^{-2} vs. V. A linear dependence of C^{-2} on V was found for all samples in the reverse bias voltages from 0 to 4 V. The diffusion potential (V_I) of the Schottky diodes was obtained from the intercept of the horizontal axis in the plots of C^{-2} vs. V. The C-V barrier height (ϕ_b^{C-V}) from the C-V measurement is calculated from[29]

$$\phi_b^{C-V} = V_I + \xi + kT/q$$

where ξ is the energy difference between the Fermi level and the bottom of the conduction band in the bulk semiconductor. The ideality factor, the carrier concentration (N) and the barrier heights, ϕ_b^{I-V} and ϕ_b^{C-V}, are tabulated in Table II. The ideality factor, ϕ_b^{I-V} and ϕ_b^{C-V} of the Schottky diode

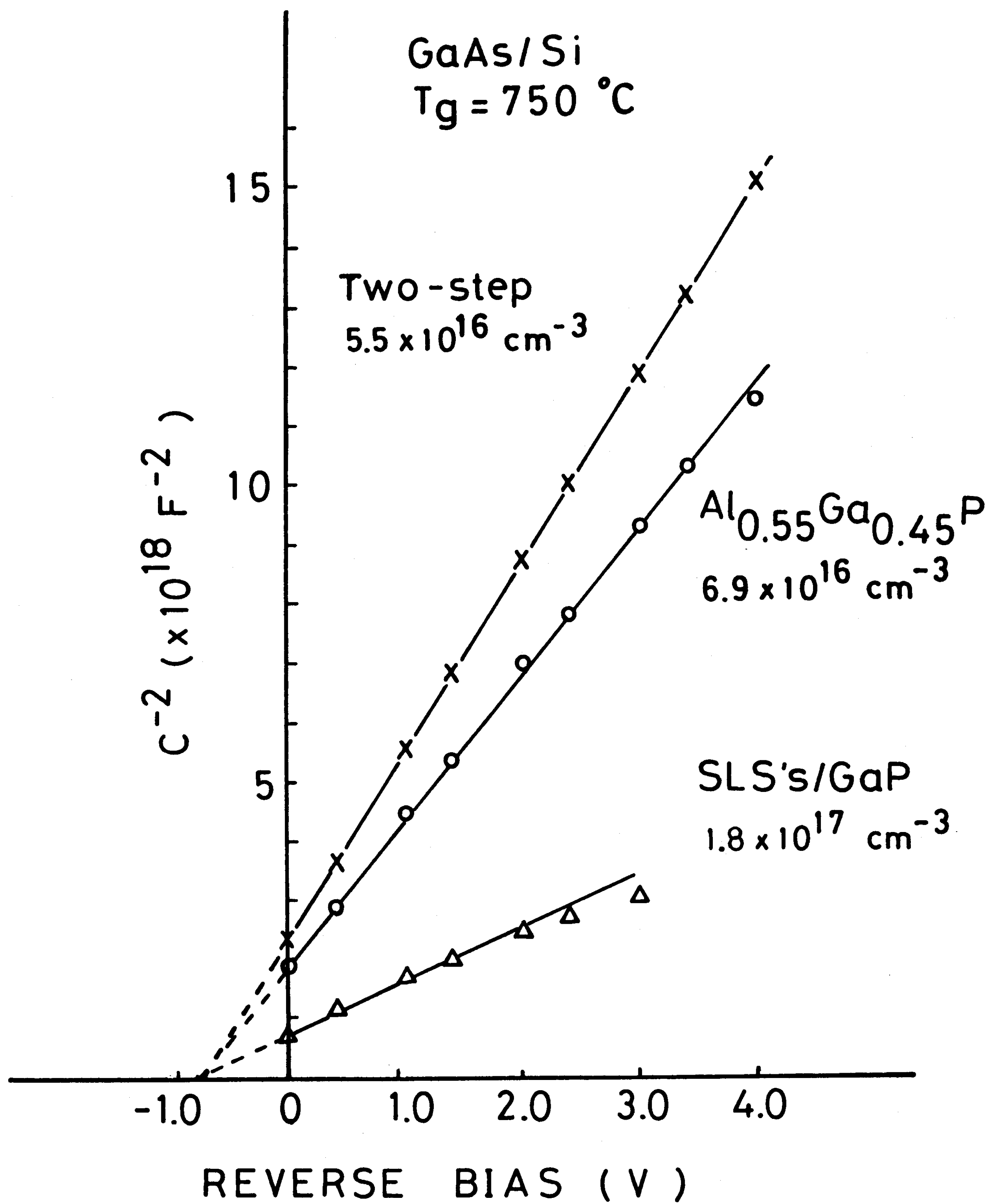


Fig. 4.6. C-V data of Au-GaAs/Si Schottky diodes. The area of the Schottky diode is 7.85×10^{-3} cm^2.

Table II. Ideality factor, carrier concentration, and Schottky barrier heights calculated from forward I-V and C-V characteristics for GaAs/Si grown by two-step growth, SLSs/GaP, and $Al_{0.55}Ga_{0.45}P$ techniques. The area of the Schottky diode is 7.85×10^{-3} cm^2.

GaAs/Si	Ideality factor	Carrier concentration ($\times 10^{16}$ cm^{-3})	ϕ_b^{I-V} (eV)	ϕ_b^{C-V} (eV)
Two-step growth	1.11	5.5	0.87	0.90
SLSs/GaP	1.09	18.0	0.86	0.89
$Al_{0.55}Ga_{0.45}P$	1.06	6.9	0.87	0.92

on the n-type GaAs substrate are 1.05, 0.90 and 0.96 eV, respectively, which indicate that affects of the thin GaAs native oxide or variation of fabrication process on the Schottky diode characteristics are negligible.

Assuming that the I-V characteristic of a Schottky diode is determined by the thermionic emission current (I_{te}) and the recombination current (I_r), the total current is now given by[29,30]

$$I = I_{te} + I_r$$

$$= I_0[\exp(qV/kT)-1] + I_{r0}[\exp(qV/2kT)-1]$$

where $I_0 = AA^{**}T^2\exp(-q\phi_b/kT)$ and $I_{r0} = Aqn_i w/2\tau_r$. Here A is the area of a diode, A^{**} is the Richardson constant, T is the device temperature, V is the applied voltage, k is Boltzmann's constant, ϕ_b is the effective barrier height, n_i is the intrinsic carrier concentration, proportional to $\exp(-qE_g/2kT)$, w is the thickness of the depletion region, E_g is the band gap energy and τ_r is the lifetime within the depletion region. By measuring the forward current as a function of temperature, it is possible to determine which is dominant the thermionic emission or the recombination current. When the thermionic emission current is dominant, a plot of $\ln(I_{te}/T^2)$ as a function of 1/T should yield a straight line with a slope of $-q(\phi_b-V)$, which gives the activation energy. When the recombination current is

dominant, on the other hand, the temperature dependence of the forward current shows two activation energies, and the reverse current (I_{r0}) becomes proportional to the square root of the reverse bias ($V_r^{1/2}$) if the concentration of the recombination centers is uniform across the thickness.

The typical forward I-V characteristics of the Schottky diodes on n-type GaAs and on the GaAs/Si with the $Al_{0.55}Ga_{0.45}P$ intermediate layer as a function of temperature are shown in Fig. 4.7. The nonlinearities in the curves under large forward bias are caused by series resistance. Note that much larger leakage current occurs under a small forward bias for the GaAs/Si. Similar temperature dependence of I-V characteristics are observed in the GaAs/Si grown by the two-step growth technique and using the SLSs/GaP intermediate layer. This leakage current cannot be explained by the thermionic emission current. The ideality factor in this region is about 2, which suggests that this leakage current is due to the recombination current. To further verify that this leakage current is the recombination current, the values of $\ln(I/T^2)$ from the current at the forward voltage of 0.4 V are plotted as a function of 1000/T in Fig. 4.8. The plot for the n-type GaAs substrate shows a single activation energy, while the plots for the GaAs/Si show two activation energies. The activation energy for the GaAs substrate is 0.508 eV, while the activation energy for the GaAs/Si grown with the $Al_{0.55}Ga_{0.45}P$ intermediate layer is 0.407 eV above 180 K and

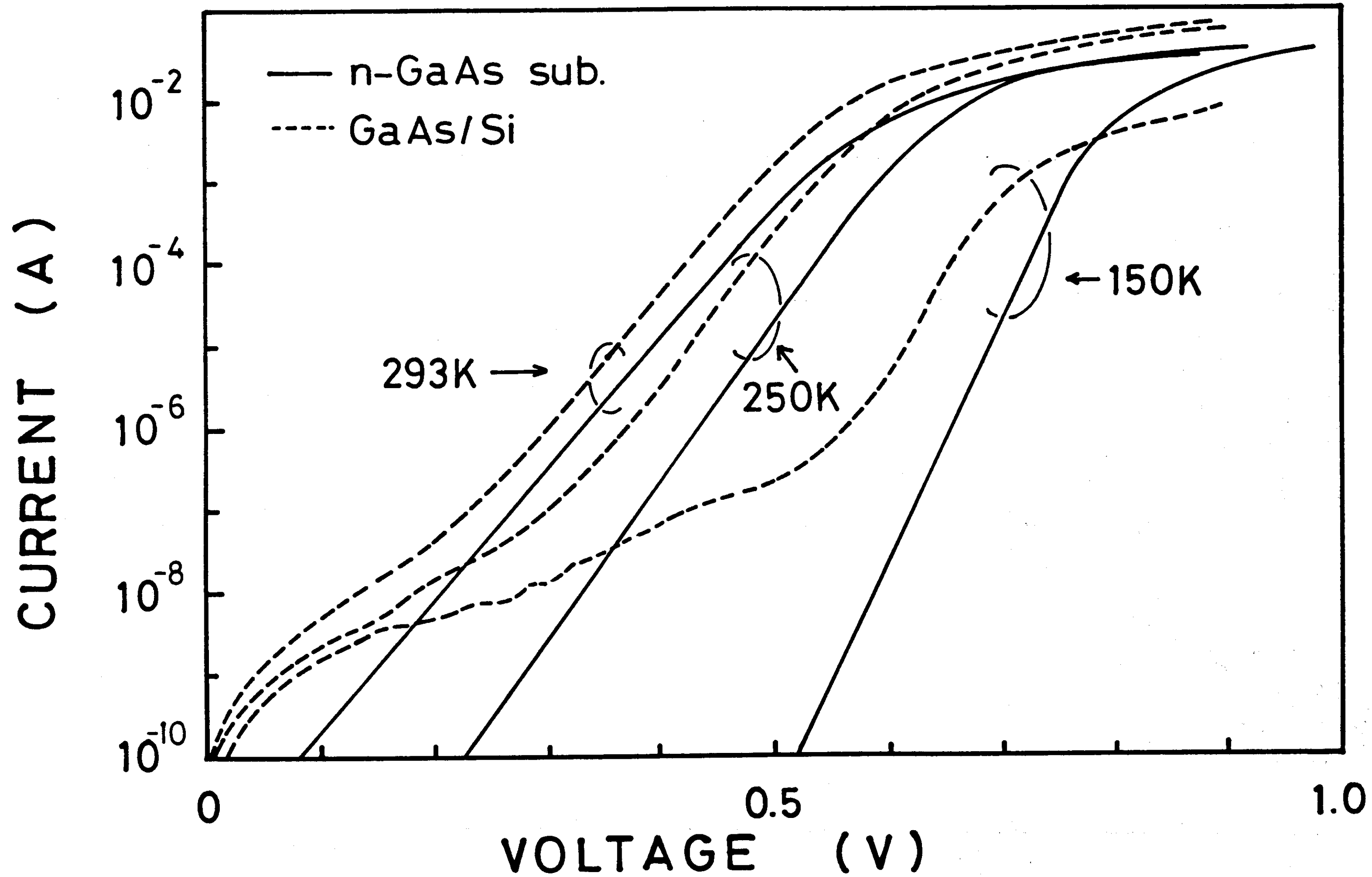


Fig. 4.7. Forward I-V characteristics of Schottky diodes on n-type GaAs substrate and GaAs/Si grown with $Al_{0.55}Ga_{0.45}P$ intermediate layer as a function of temperature. The area of the Schottky diode is 7.85×10^{-3} cm^2.

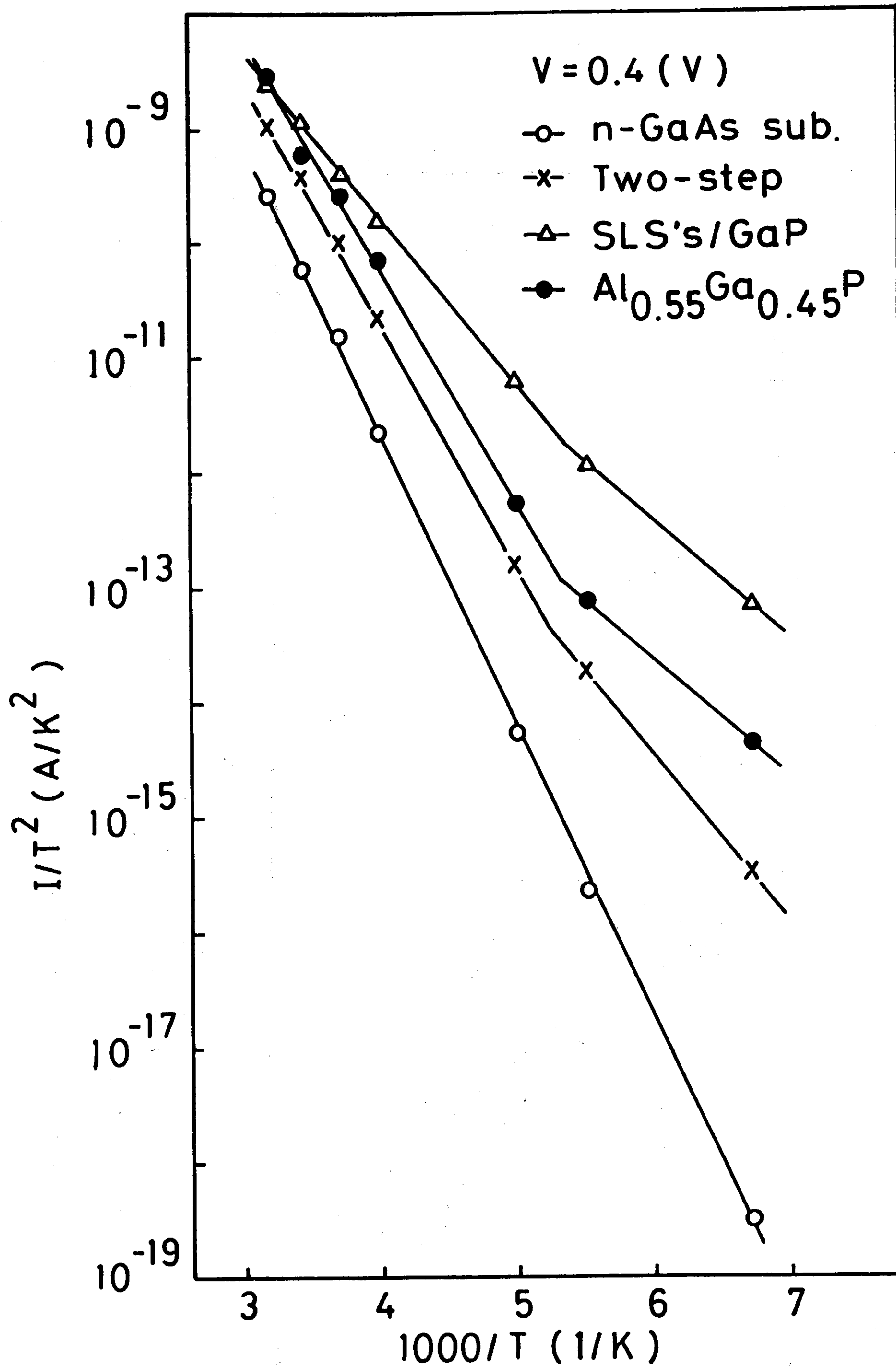


Fig. 4.8. Temperature dependence of I/T^2 obtained from the current at the forward bias of 0.4 V for n-type GaAs substrate and GaAs/Si grown by two-step growth, SLSs/GaP and $Al_{0.55}Ga_{0.45}P$ techniques. The area of the Schottky diode is 7.85×10^{-3} cm^2.

0.221 eV below 180 K. This indicates that the leakage current of the GaAs/Si increases at lower temperatures.

Figure 4.9 shows a plot of $\ln I_{r0}$ vs. $\ln V_r$. In the GaAs/Si, a sharp increase of current at near 4 V is due to avalanche breakdown. The value is rather small compared with that for the GaAs substrate, which may be related to the higher dislocation density in the GaAs/Si. The slope of the plot indicates that the reverse current (I_{r0}) is proportional to $V_r^{1.8}$, which suggests that the reverse current is caused by the generation current due to the recombination centers. The generation current density (J_{gen}) due to the recombination centers in the depletion region is given by

$$J_{gen} = \int_0^W \frac{-q n_i}{\tau_e} dx$$

where $\tau_e \propto 1/N_t$. Here τ_e is the effective lifetime and N_t is the trap density. The depth profile of N_t to satisfy

$$I_{r0} \propto V_r^{1.8},$$

is expected that

$$N_t \propto x^{2.6}.$$

The depth profile of N_t near the surface of the GaAs/Si follows the above relationship.

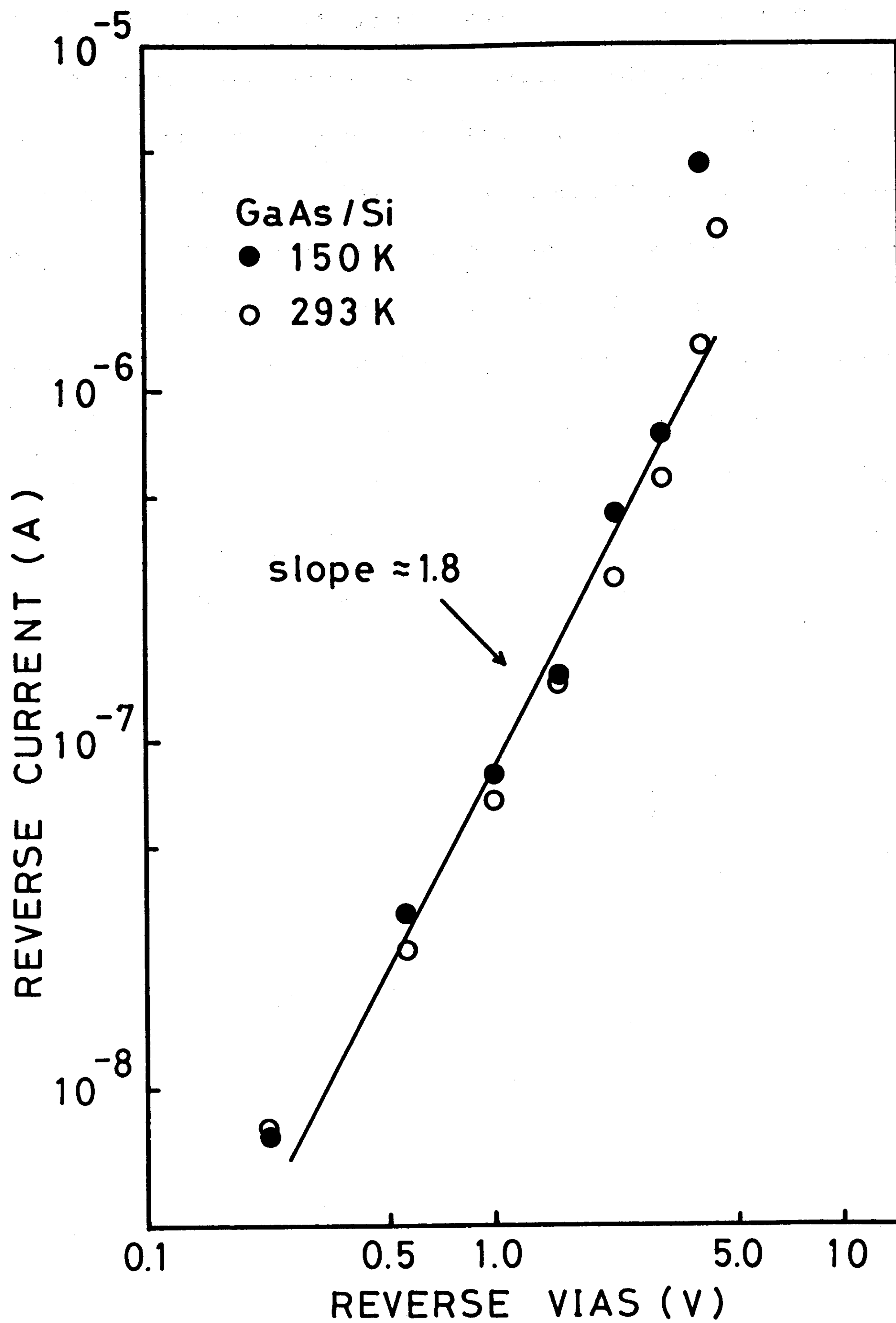


Fig. 4.9. Relationship between reverse current and reverse bias for GaAs/Si grown with $Al_{0.55}Ga_{0.45}P$ intermediate layer at 150 and 293 K. The area of the Schottky diode is 7.85×10^{-3} cm^2.

Figure 4.10 shows the dependence of the ideality factor and the ϕ_b^{I-V} on temperature. The ϕ_b^{I-V} is reportedly a decreasing function of temperature[31]. The ideality factor and ϕ_b^{I-V} for the n-type GaAs substrate are unchanged. For the GaAs/Si, however, the ideality factor and the ϕ_b^{I-V} are decreasing and increasing functions of temperature, respectively. The ideality factor approaches 1 at high temperature where the thermionic emission process becomes dominant compared with the recombination process. The observation that the ϕ_b^{I-V} for the GaAs/Si is an increasing function of temperature may be related to material and electrical properties unique to the GaAs/Si.

4.4 Conclusions

The relationship between crystallinity of MOCVD-grown GaAs/Si and characteristics of Schottky diodes fabricated on the GaAs/Si with various intermediate layers has been studied. Schottky diode characteristics, which depend on the intermediate layers, are superior for the GaAs/Si with the $Al_{0.55}Ga_{0.45}P$ intermediate layer to those for the GaAs/Si by the two-step growth technique and using the SLSs/GaP intermediate layers. Taking account of the results described in chapter 2, it is clear that the intermediate layer plays an important role in improving crystallinity and Schottky diode characteristics of the GaAs/Si. Although the forward and reverse I-V characteristics of the Schottky

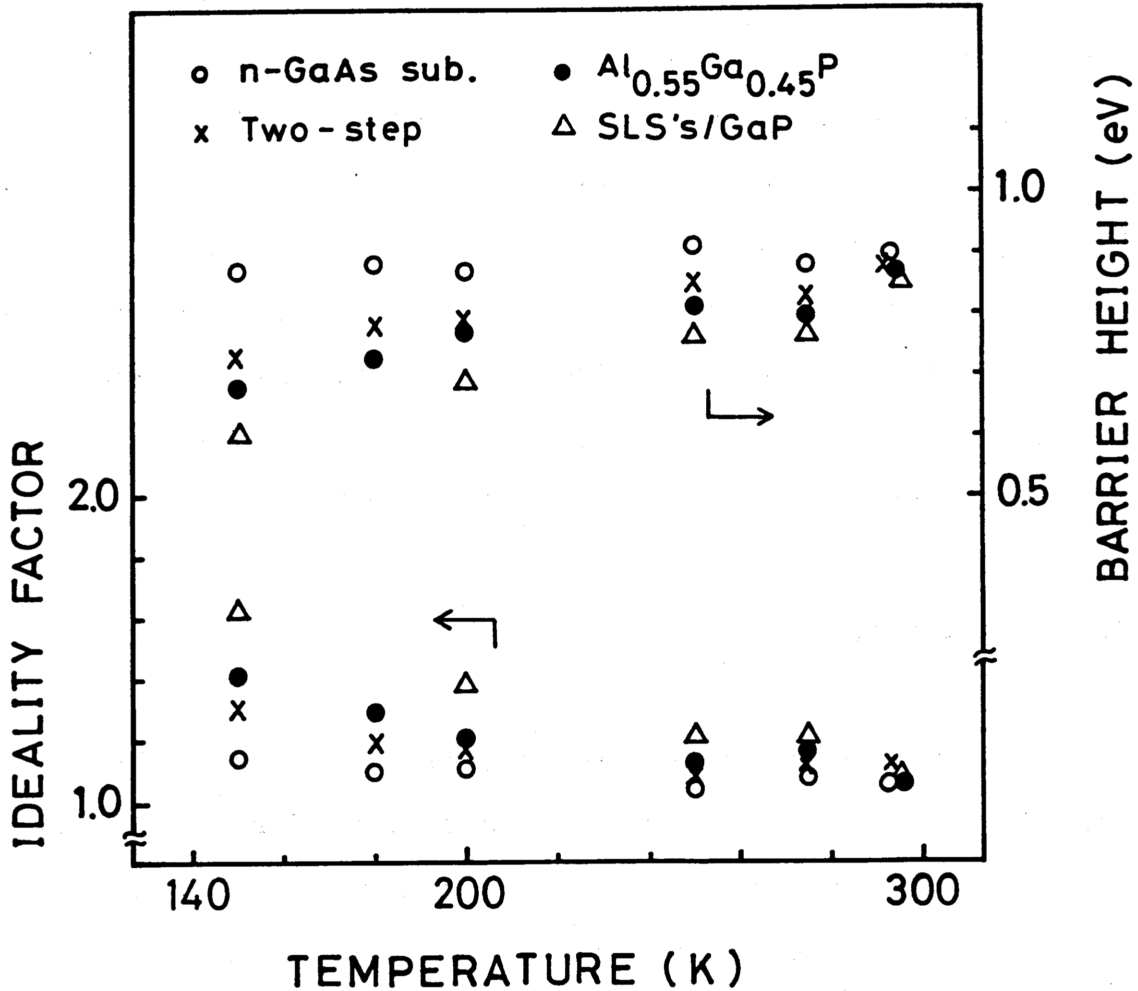


Fig. 4.10. Temperature dependence of ideality factors and I-V barrier heights for n-type GaAs substrate and GaAs/Si grown by two-step growth, SLSs/GaP and $Al_{0.55}Ga_{0.45}P$ techniques. The area of the Schottky diode is 7.85×10^{-3} cm^2.

diodes fabricated on the GaAs/Si with the $Al_{0.55}Ga_{0.45}P$ intermediate layer are good, significant leakage current is observed under reverse and small forward bias, in contrast to the n-type GaAs substrate. The leakage current under reverse and small forward bias is unique to the GaAs/Si. The leakage current is caused by recombination and generation centers associated with the high density of dislocations in the GaAs/Si.

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Chapter 5. GaAs MESFET's Grown on Si

5.1 Introduction

Although GaAs/Si still has problems such as a high density of dislocations[1,2] and unintentional Si autodoping[3-6], GaAs metal-semiconductor field-effect transistors (MESFET's)[6-15] and high electron mobility transistors (HEMT's)[16-18] have been fabricated on Si by metalorganic chemical vapor deposition (MOCVD) or molecular beam epitaxy (MBE). Numerous potential applications of the GaAs/Si can be achieved by the successful fabrication of GaAs MESFET's or HEMT's as well as laser diodes[2,19-21]. Choi et al.[8] have first reported that a GaAs MESFET is fabricated on a Ge coated Si substrate by MBE with a maximum transconductance of 105 mS/mm for a gate length of 2.1 μm. Shichijo et al.[12] have reported that the 1-kbit static RAM is fabricated on Si by MBE. In spite of this progress, there has been little data on the characteristics of MOCVD-grown GaAs MESFET's on Si. In particular, realization of high-performance GaAs LSI's on Si is necessary in order to obtain a good pinch-off characteristic, suppress the sidegating effect and obtain uniform threshold voltage of GaAs MESFET's on Si. The pinch-off characteristics of GaAs MESFET's and HEMT's grown on Si by MOCVD are often degraded by unintentional Si autodoping in undoped layers[6]. To ease this problem, Nonaka et al.[7] and Ishida et al.[9] doped GaAs

layers with vanadium, and Lee et al.[13] lowered growth temperature to increase resistivity of undoped GaAs layers. Major problems limiting a GaAs LSI's are the sidegating effect[22-24] and the variation of the threshold voltage[25,26], which are expected to be affected by the defects. The sidegating effect, where the biasing conditions of one device influence the output currents of its neighbors, must be minimized in order to increase the complexity. In general, higher growth temperature improves the crystallinity of the GaAs/Si and is thought to reduce the sidegating effect. However, an undoped GaAs layer grown on Si at high temperature by MOCVD has a high electron concentration due to enhanced Si incorporation,[3-5] which degrades the pinch-off characteristic of a MESFET on Si[6].

In this chapter, GaAs MESFET's characteristics in terms of pinch-off, the sidegating effect and the microscopic uniformity of sheet resistance, which are basic characteristics for a GaAs LSI's on Si, are described. This chapter is organized as follows: Epitaxial growth and fabrication process are presented in section 5.2. In section 5.3, DC characteristics are described. Sidegating effect and microscopic uniformity of electrical property are presented in section 5.4 and 5.5, respectively. This chapter is concluded in section 5.6.

5.2 Epitaxial Growth and Fabrication Process

All epitaxial layers were grown on (100) p-type (B-doped, 1.7 Ω-cm) Si substrates oriented 2° off toward [011] in an RF-heated horizontal MOCVD reactor at atmospheric pressure using the two-step growth technique. The back of some substrates were coated with 720-nm-thick sputtered SiO_2 films. The source materials were trimethylgallium (TMG), trimethylaluminum (TMA) and arsine (AsH_3). The substrates were degreased in organic solvents and then cleaned in $4H_2SO_4+H_2O_2$ and $HF+4H_2O$ solutions. Prior to the growth, the substrates were heated in H_2 atmosphere at 1000 ^{o}C for 10 min to remove native oxide from the substrate surfaces. For MESFET's, the following layers were successively grown on p-Si substrates with and without a 720-nm-thick sputtered SiO_2 back coating: a 12.5-nm-thick GaAs nucleation layer at 400 ^{o}C, a 0.8-μm-thick undoped GaAs buffer layer at 700 ^{o}C, a 1-μm-thick p-$Al_{0.3}Ga_{0.7}As$ layer at 700 ^{o}C, a 1-μm-thick undoped GaAs layer at 650, 700 and 750 ^{o}C, a 0.3-μm-thick channel layer doped with Se to $3x10^{17}$ cm^{-3} at 750 ^{o}C, and a 60-nm-thick ohmic contact layer doped with Se to $1x10^{18}$ cm^{-3} at 750 ^{o}C. The p-$Al_{0.3}Ga_{0.7}As$ layer was not inserted for some MESFET's characterized for the transmission line model (TLM).

MESFET's were fabricated using the recessed gate technique. The fabrication process is shown in Fig. 5.1. A 0.1-μm-thick SiO_2 film was sputtered on the top n^+-GaAs

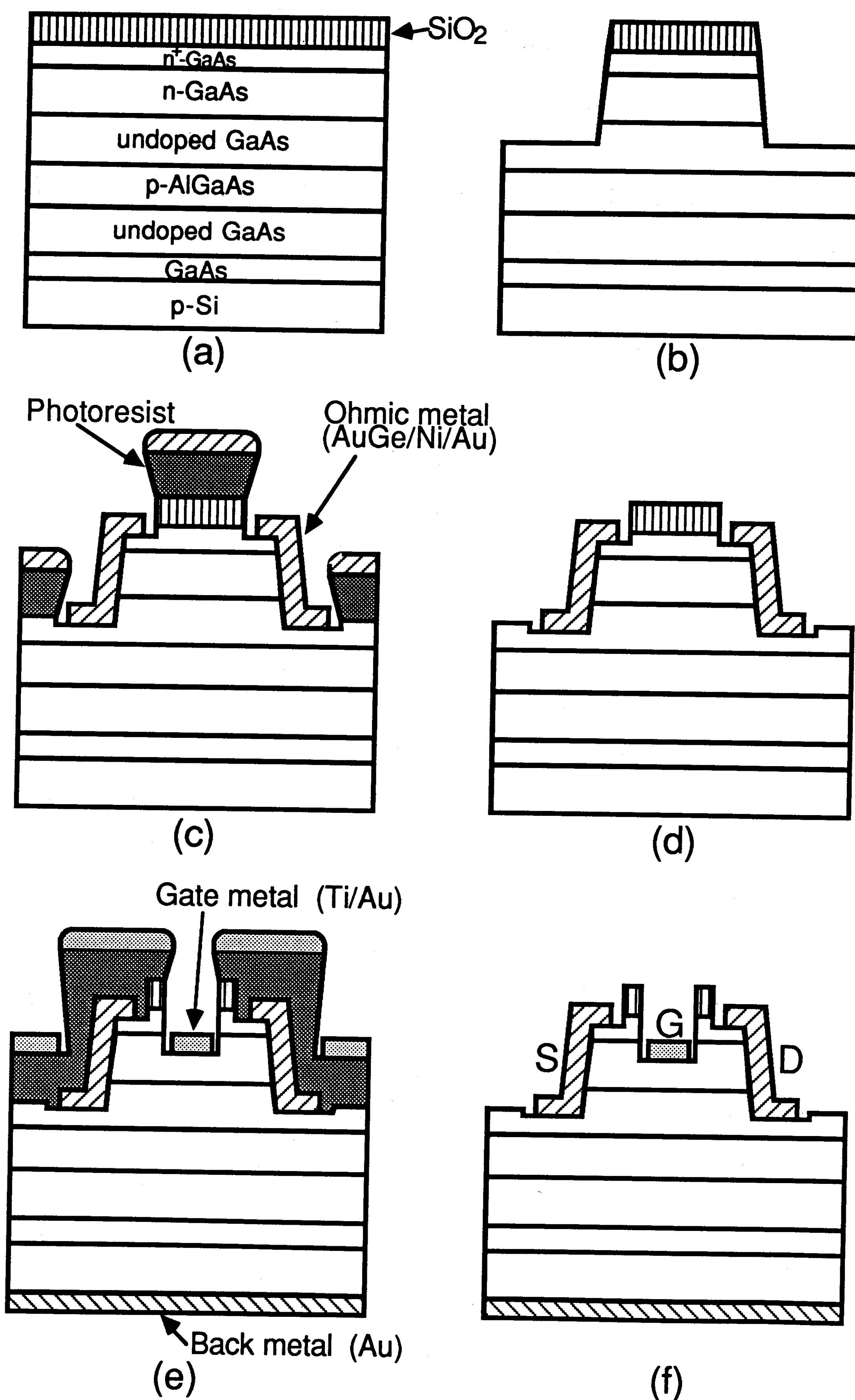


Fig. 5.1. Stages in the fabrication of the GaAs MESFET on Si.

layer, and a 0.8-μm-deep mesa isolation was performed by chemical etching. AuGe/Ni/Au source and drain ohmic contacts were formed by evaporation/liftoff and alloyed at 380 ^{o}C for 1 min in flowing N_2 gas. The gate region was recessed to the depth of about 0.2 μm by chemical etching, and the gate contact was made by evaporation/liftoff of Ti/Au. A schematic cross section of the fabricated MESFET structure on the GaAs/Si is shown in Fig. 5.2. Figure 5.3 shows low- and high-magnification Nomarski micrographs of the MESFET fabricated on the GaAs/Si. The gate length and width are 2.5 and 15 μm, respectively. The test pattern for the device isolation consists of two 80-μm-long ohmic contacts to the n^+-GaAs layer regions separated by 8 μm with the etched isolation. As shown in Fig. 5.4, the test pattern of the TLM, which consists of 80 μm x 80 μm ohmic contacts to the n^+-GaAs layer with various spacings from 10 μm to 160 μm, was used to study the laterally spreading current flow. The test structure for the sidegating effect is illustrated in Fig. 5.5. A 200-μm-wide MESFET with a 2.5-μm gate length and a 270-μm-wide sidegate electrode were placed 5-30 μm away from each other. The sidegate electrode consisted of an ohmic contact onto the n^+-GaAs layer. This n^+-GaAs layer and the MESFET active channel were separated by the isolation etching. The test pattern, which consists of the n^+-GaAs layers arrayed by 50-μm pitch, was used to study the microscopic uniformity of the electrical property. Carrier concentration profiles were obtained by

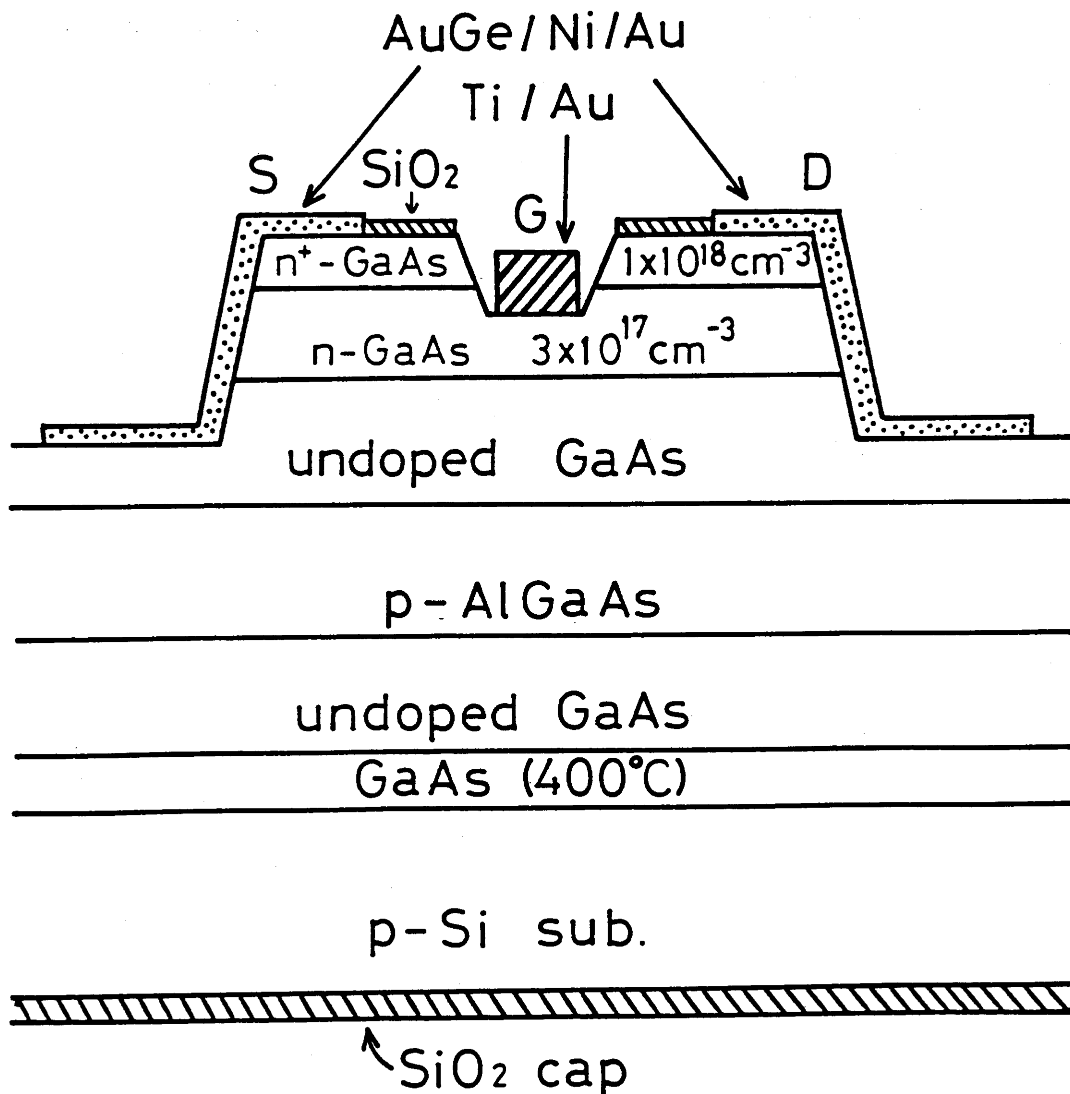
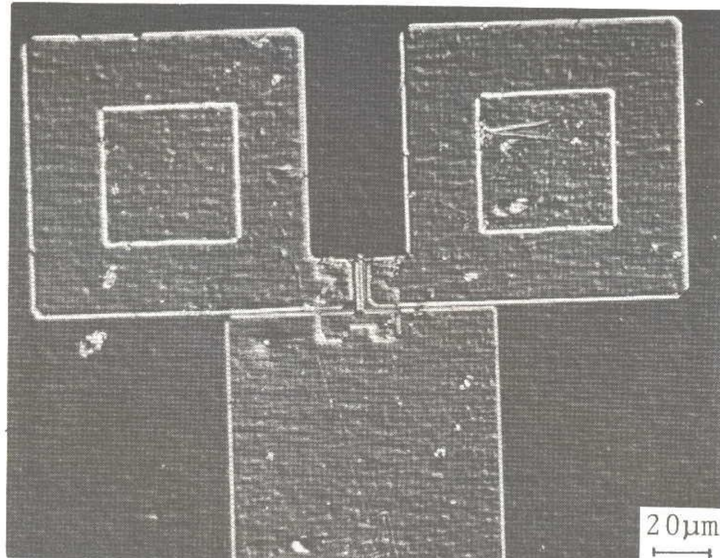


Fig. 5.2. Schematic cross section of the fabricated GaAs MESFET on SiO_2 back-coated Si using the recess gate technique.



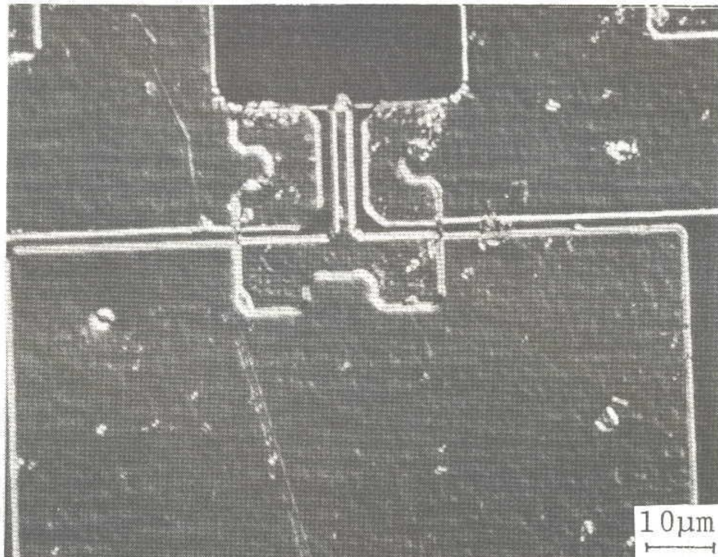


Fig. 5.3. Low- and high-magnification Nomarski micrographs of the GaAs MESFET on Si. The gate length and width are 2.5 and 15 μm, respectively.

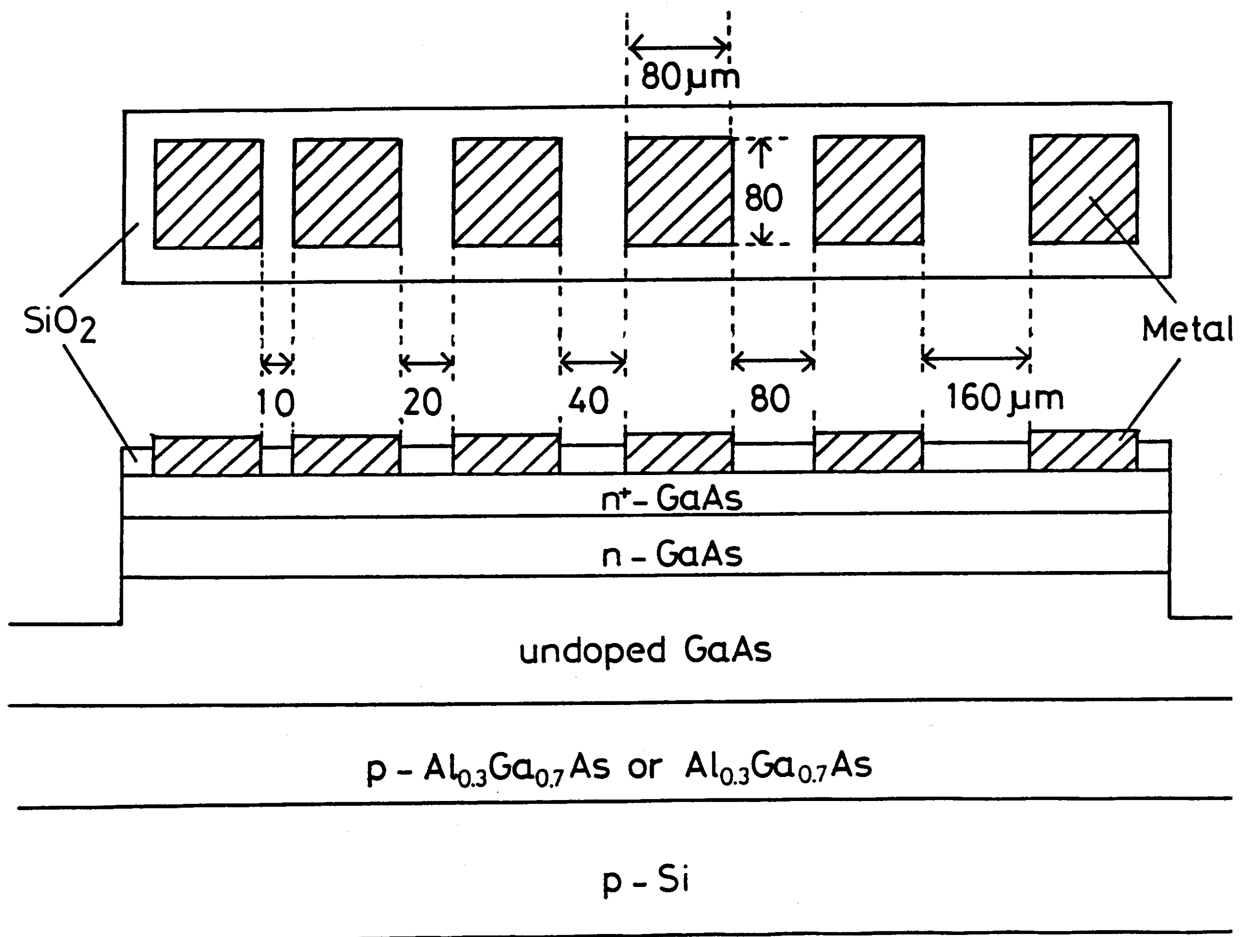


Fig. 5.4. Test pattern for the transmission line model (TLM) measurement.

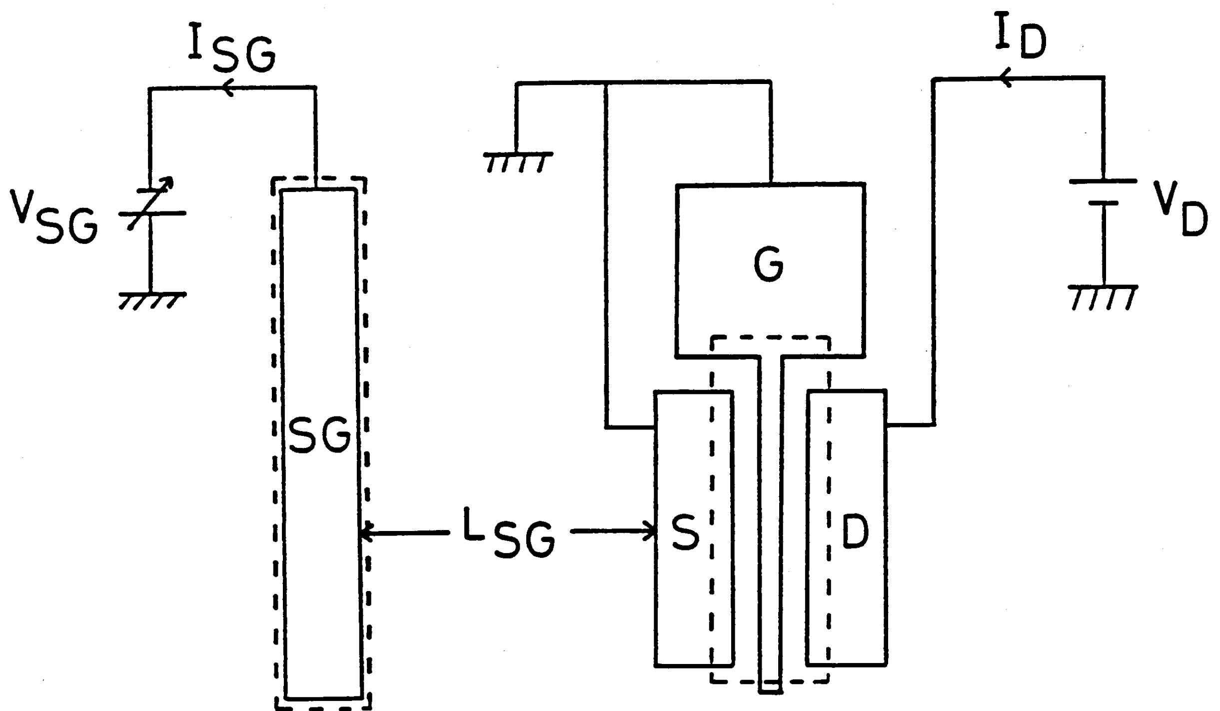


Fig. 5.5. Test pattern for the sidegating effect.

electrochemical capacitance-voltage (C-V) measurement using a Polaron model PN 4200 system.

5.3 DC Characteristics[6)]

Figure 5.6 shows the electron concentration profiles of MESFET's grown at 750 ^{o}C on the "passivated" and "unpassivated" Si substrates. In the "passivated" Si substrate, the back and side edges of Si were covered with a Si_3N_4/SiO_2 stacked layer to suppress the gas phase transport of Si from the Si substrate during growth. As seen in the figure, the electron concentration of the undoped GaAs layer beneath the channel layer for the "passivated" Si is $3x10^{14}$ cm^{-3}, as low as that of the undoped GaAs layer grown on GaAs. However, for simplicity in the experiments, MESFET's discussed below were fabricated on Si substrates where only the back was covered with a 720-nm-thick sputtered SiO_2 film. These Si substrates back-coated with a sputtered SiO_2 film have side edges still exposed to the ambient and are less effective in suppressing the gas phase transport of Si during the growth. Nevertheless, as described in section 2.5, the electron concentration of an undoped GaAs layer grown at 750 ^{o}C has been reduced to $1x10^{15}$ cm^{-3} from $1x10^{17}$ cm^{-3} using the Si back-coated with a 720-nm-thick sputtered SiO_2 film.

The isolation leakage currents in the undoped GaAs layers measured at 0.1 V are shown in Fig. 5.7. The undoped

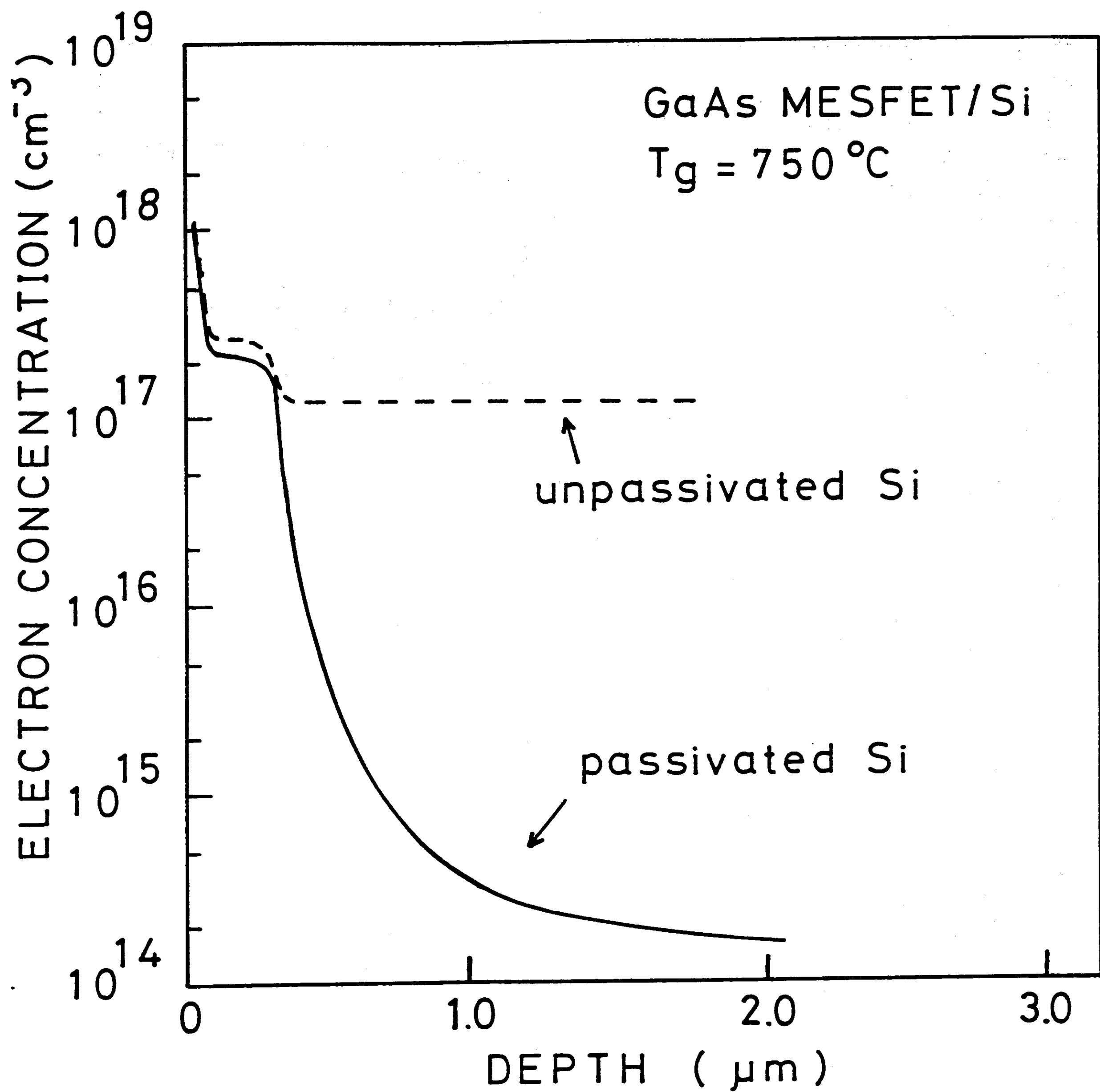


Fig. 5.6. Electron concentration profiles of MESFET structures grown at 750 ^{o}C on the "passivated" and the "unpassivated" Si. In the "passivated" Si, the back and side edges were covered with a Si_3N_4/SiO_2 stacked layer.

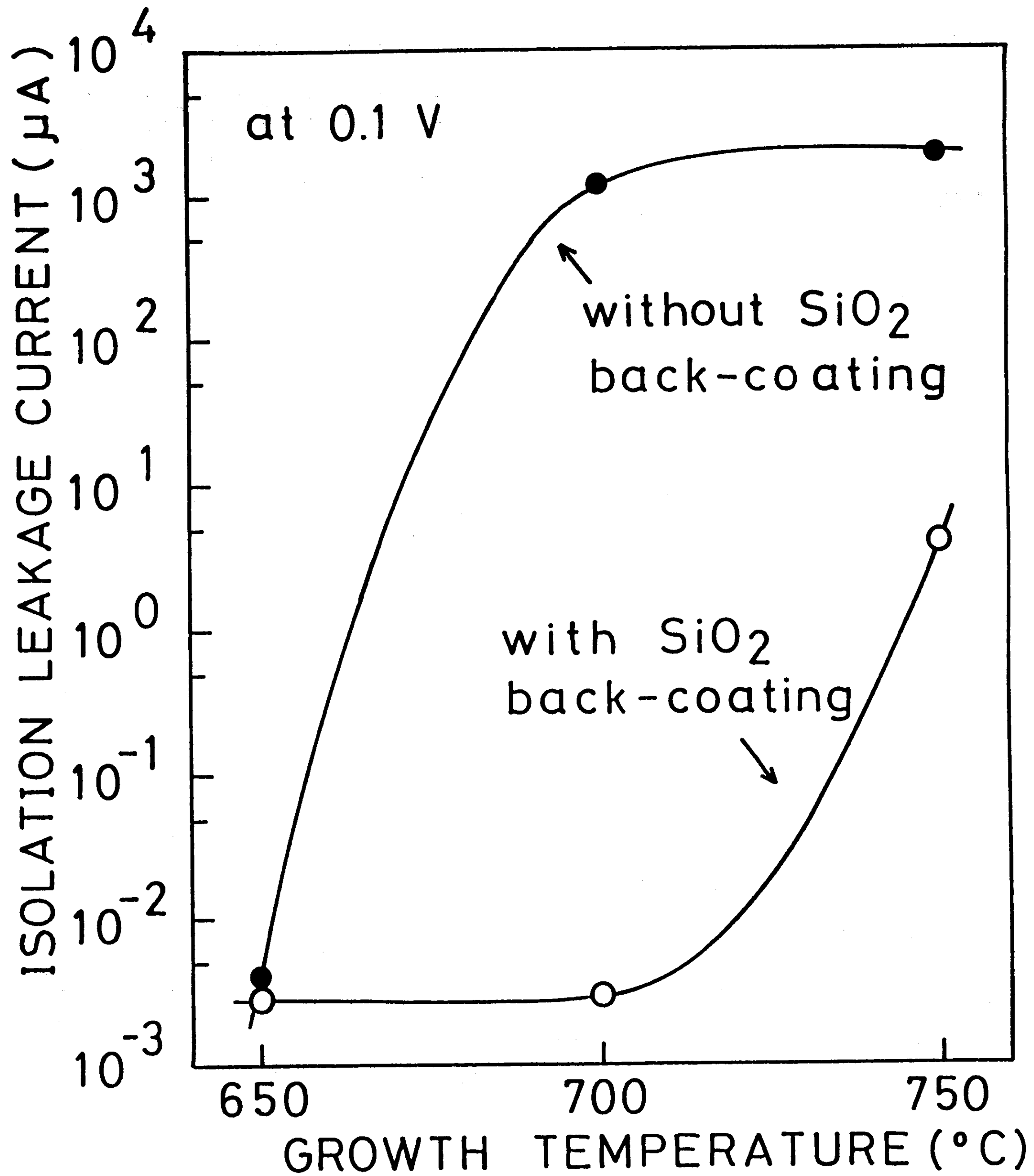


Fig. 5.7. Isolation leakage currents in the undoped GaAs layers beneath the channel layers grown at 650, 700 and 750 °C on Si with and without 720-nm-thick SiO_2 back coatings. The samples have a MESFET structure with a p-$Al_{0.3}Ga_{0.7}As$ layer.

GaAs layers were grown at 650, 700 and 750 °C on Si with and without 720 nm-thick SiO_2 back coating. The isolation leakage is determined by conduction paths in the undoped layer beneath the channel and near the GaAs/Si interface. The inserted p-$Al_{0.3}Ga_{0.7}As$ prevents the current reaching the GaAs/Si interface, as will be discussed in detail later. If the undoped layer beneath the channel is of high resistivity, the isolation leakage current should be negligibly small. This measurement tests whether the resistance of the undoped layer is high enough to isolate two MESFET's. Without SiO_2 back coating, the isolation leakage current greatly increases from 4 nA to 1900 μA when growth temperature increases from 650 to 750 °C. An increase of the leakage current reflects an increase of the electron concentration of the undoped GaAs layer with increasing growth temperature. With SiO_2 back coating, however, it remains less than 4 μA, even when the growth temperature is as high as 750 °C. The larger leakage observed for the growth temperature of 750 °C suggests that the Si incorporation into a GaAs layer by the gas phase transport of Si from the side edges exposed to the ambient seems more significant than at lower temperatures.

The resistance (R) between the ohmic metal pads measured in the TLM pattern is shown as a function of spacing (L) in Fig. 5.8. The calculated specific contact resistance is also shown. A linear dependence of R on L is found for GaAs and Si substrates back-coated with SiO_2 when

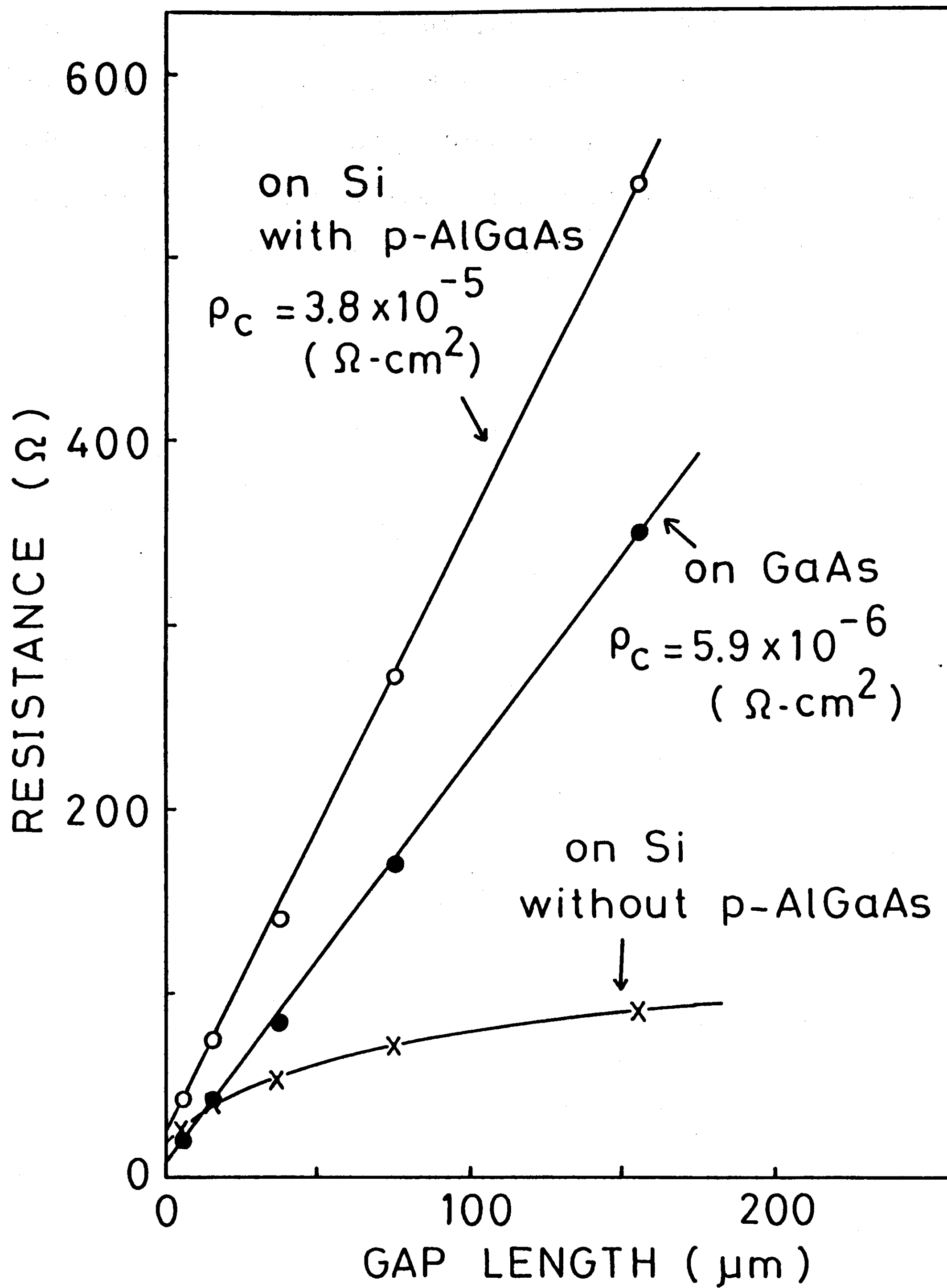


Fig. 5.8. Resistance (R) between the ohmic metal pads as a function of the spacing (L) in MESFET's grown on GaAs and Si. The Si substrate was back-coated with SiO_2. The MESFET on GaAs does not have a p-$Al_{0.3}Ga_{0.7}As$ buffer layer.

a p-$Al_{0.3}Ga_{0.7}As$ buffer layer was grown beneath the undoped GaAs layer. The current reaching the GaAs/Si interface, which still has a high electron concentration, can flow laterally to the ohmic metal pad. Use of a Si substrate back-coated with SiO_2 cannot prevent such current. Creating a barrier by inserting a p-$Al_{0.3}Ga_{0.7}As$ layer prevents the current reaching the interface. As long as a p-$Al_{0.3}Ga_{0.7}As$ is inserted, whether the Si substrate is back-coated or not does not show a great difference in the plot, although only a plot for back-coated Si is shown in Fig. 5.8. The TLM pattern consists of the ohmic metal pads deposited onto the n^+-GaAs ohmic-contact layer which is not mesa-etched. Therefore, the main current flow is in the n^+-GaAs ohmic-contact layer, which has a much higher conductivity than the channel or the undoped layer. However, the conductivity near the GaAs/Si is comparable to that of the n^+-GaAs layer, and the current reaching the interface can create a parallel conduction path. As a result, the lineality of the plot is strongly affected by the current reaching the interface rather than the current flowing laterally in the undoped GaAs layer. The specific contact resistance, ρ_c, for a Si substrate with or without the back coating is one order higher than for GaAs substrate, which may be related to the rough surface of the n^+-GaAs on Si.

Figure 5.9 shows the relationship between the gate bias and the square root of the source-drain current of MESFET's on Si with and without SiO_2 back coating. The undoped GaAs

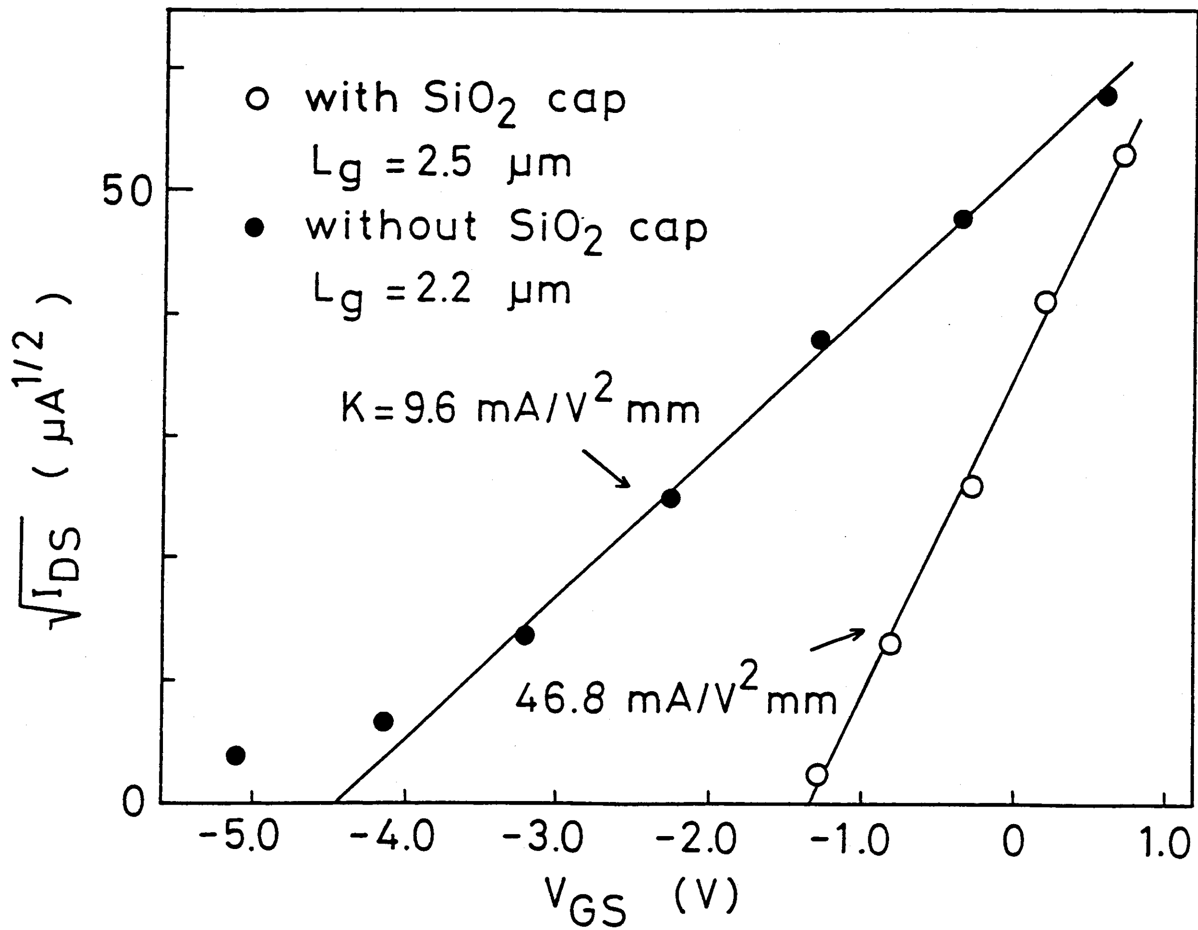


Fig. 5.9. Relationship between the gate bias and the square root of the source-drain current of the MESFET's with 15-µm gate width on Si with and without SiO_2 back coating. The MESFET's have p-$Al_{0.3}Ga_{0.7}As$ buffer layers.

layers beneath the channel layers were grown at 700 ^{o}C. The drain current-voltage (I-V) characteristic of the MESFET on Si with SiO_2 back coating is shown in Fig. 5.10. The MESFET structures were grown on the p-$Al_{0.3}Ga_{0.7}As$ buffer layer discussed above. The undoped GaAs layers beneath the channel layers were grown at 700 ^{o}C. The MESFET on Si with SiO_2 back coating has an improved pinch-off characteristic because lateral current flow in the undoped GaAs layer beneath the channel layer is suppressed by the SiO_2 back coating. Another significant improvement from the use of SiO_2 back coating is observed in the K-value determined from

$$I_{DS} = K(V_{GS} - V_{th})^2$$

where $K=\mu\varepsilon Z/2La_{eff}$. Here a_{eff} is the effective channel thickness, L is the length, Z is the width of the channel, μ is the electron mobility in the channel, ε is the dielectric constant of GaAs, I_{DS} is the drain saturation current, V_{GS} is the gate bias, and V_{th} is the threshold voltage. The V_{th}, the maximum transconductance (g_{mmax}) and the K-value are -4.4 V, 74 mS/mm and 9.6 mA/V^2mm, respectively, for a MESFET with a 2.2x15 μm gate on Si without the back coating. However, a MESFET on Si with the back coating shows better pinch-off and a higher K-value. For a MESFET with a 2.5x15 μm gate on Si with SiO_2 back coating, the V_{th}, the g_{mmax} and the K-value are -1.3 V, 160 mS/mm and 46.8 mA/V^2mm, respectively. A reason for the higher g_{mmax} and K-value is

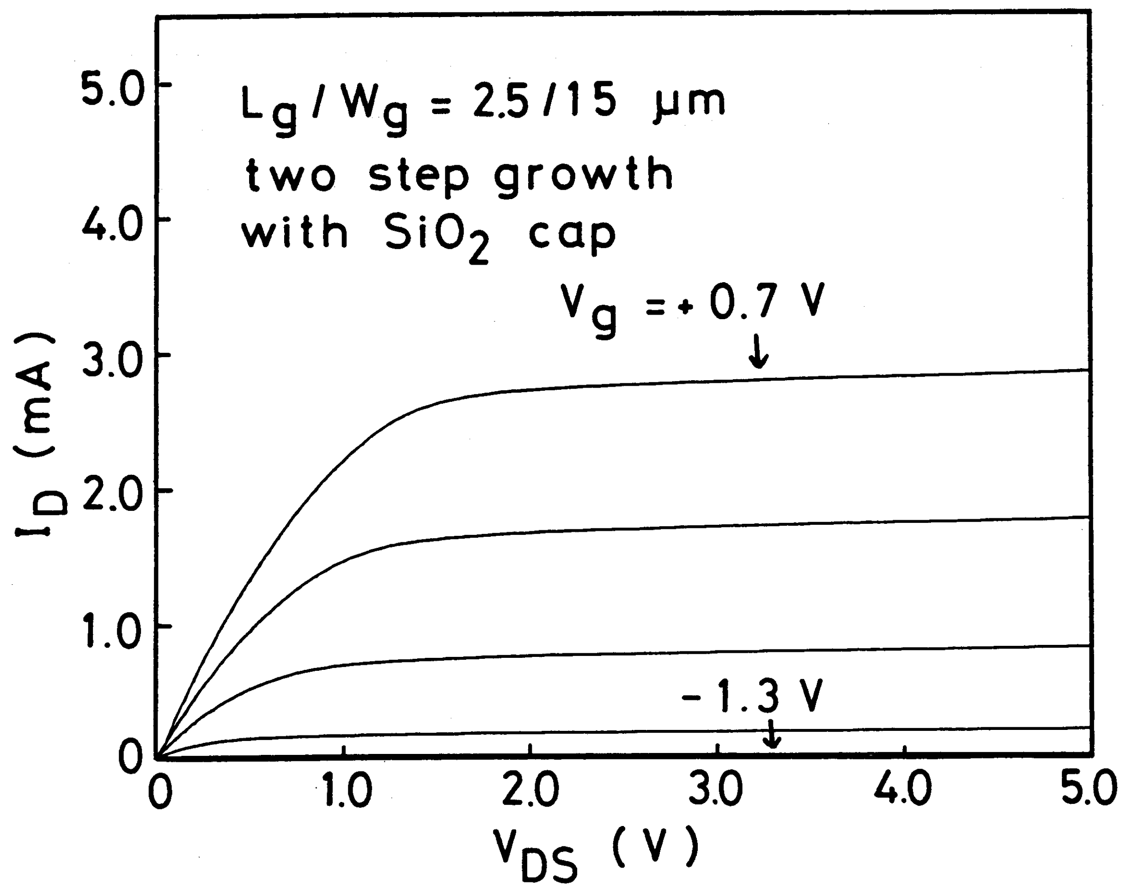


Fig. 5.10. Drain I-V characteristic of a GaAs MESFET grown on SiO_2 back-coated Si. The MESFET has a p-$Al_{0.3}Ga_{0.7}As$ buffer layer.

that the current flow in the undoped GaAs layer beneath the channel layer is suppressed because of its higher resistance.

5.4 Sidegating Effect

The influence of bias on the drain I-V characteristics of the neighboring devices is termed the sidegating effect. Figure 5.11 shows the normalized drain saturation current at the gate bias (V_{GS}) of 0 V as a function of the sidegate bias (V_{sg}) for the MESFET on SiO_2 back-coated Si. The undoped GaAs layers beneath the channel layers were grown at 650, 700 and 750 ^oC. The currents are normalized to their values at V_{sg}=0 V. The sidegating pad is located 30 μm away from the source of the device. As can be seen from Fig. 5.11, higher growth temperature of the undoped GaAs layer beneath the channel layer reduces the sidegating effect. At a growth temperature of 750 ^oC, the reduction in the drain current is less than 4 %, even when -10 V is applied to the sidegate pad. The sidegating effect is strongly affected by the crystallinity of the undoped GaAs layer beneath the channel layer. Higher growth temperature improves crystallinity and reduces the sidegating effect. The mechanism responsible for the sidegating effect is thought to be related to the presence of electron traps at the interface between the channel layer and the undoped GaAs layer beneath the channel layer. The presence of these

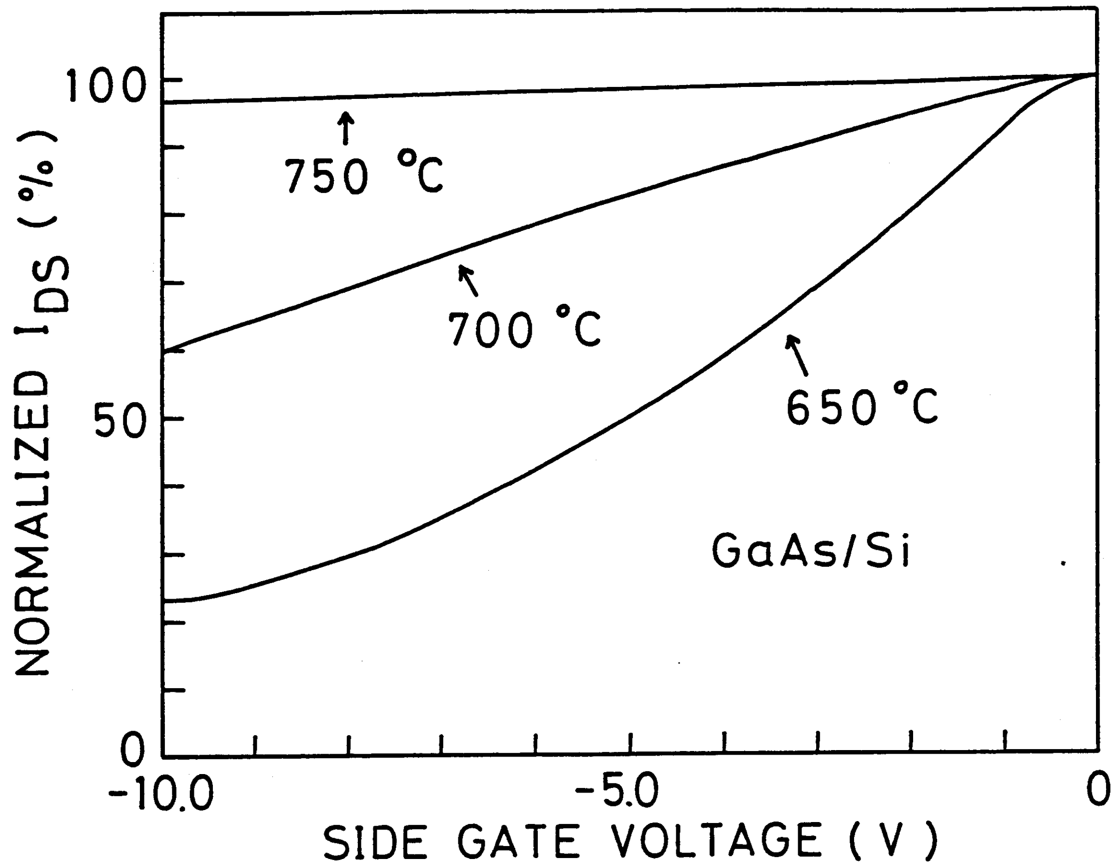


Fig. 5.11. Comparison of the drain saturation currents at V_{GS}=0 V as a function of the V_{sg} for a MESFET on SiO_2 back-coated Si. The undoped GaAs layers beneath the channel layers were grown at 650, 700 and 750 ^{o}C. The currents are normalized to their respective values at V_{sg}=0 V.

traps creates a negative space charge layer which is balanced by positive charge from the channel layer. The application of a negative bias to a sidegate pad modulates the width of this space charge layer with a corresponding decrease in the channel layer width and the drain saturation current. Figure 5.12 shows the normalized drain saturation current as a function of the sidegate bias V_{sg} for various sidegate pad spacing of the MESFET's on GaAs and Si. The undoped GaAs layers beneath the channel layers were grown at 750°C. For the MESFET on GaAs, the reduction in the drain current is less than 8 % at the sidegate bias of -10 V and with the sidegate pad spacing as small as 10 μm. For the MESFET on Si, in contrast, the reduction in the drain current becomes larger with decreases in the sidegate pad spacing.

5.5 Microscopic Uniformity of Electrical Property

The effect of dislocations on the threshold voltage uniformity of the GaAs MESFET's is an important factor for the GaAs LSI's. The electrical properties such as the threshold voltage and the sheet resistance of the GaAs MESFET's, which are fabricated on liquid encapsulated Czochralski (LEC)-grown undoped semi-insulating GaAs substrates by means of Si ion implantation, depend on the distance from a neighboring dislocation[25,26]. There is a strong correlation between the threshold voltage and

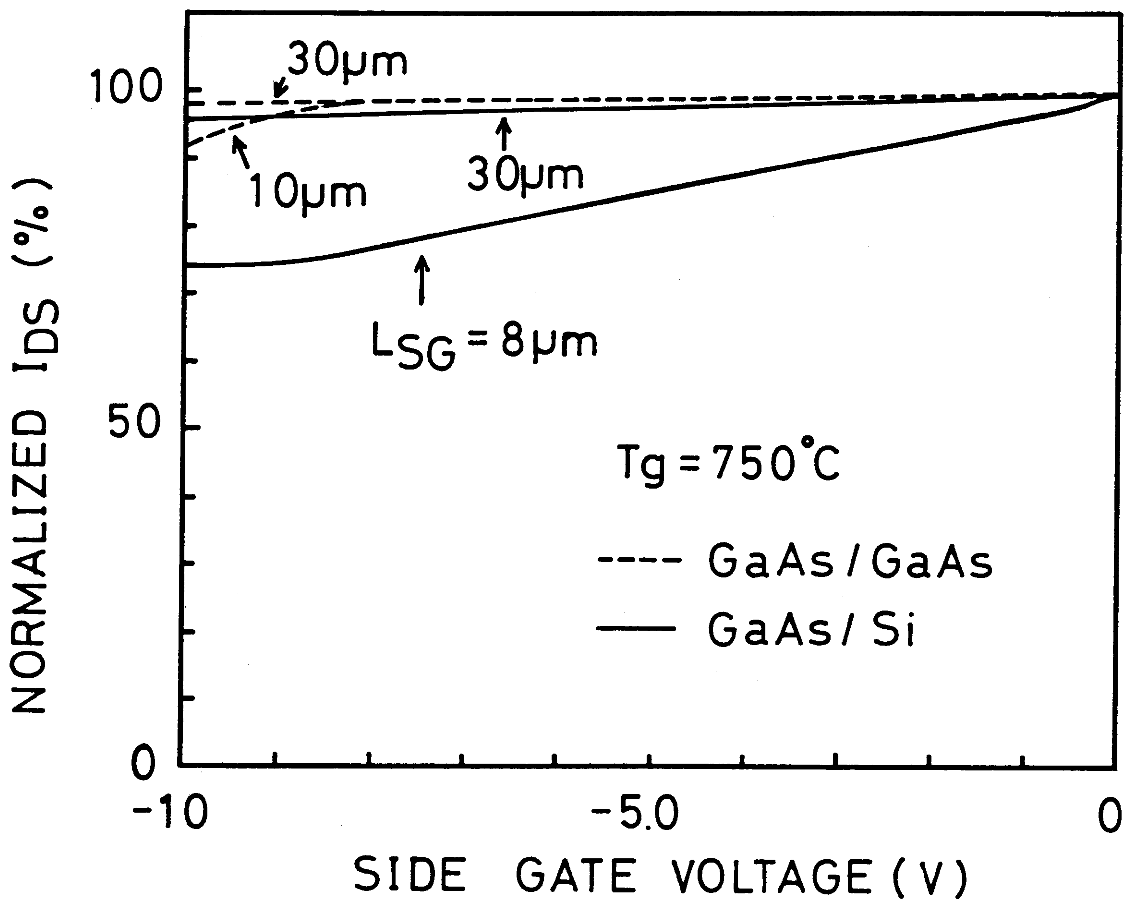


Fig. 5.12. Comparison of the drain saturation currents at V_{GS}=0 V as a function of the V_{sg} for various sidegate pad spacing of MESFET's on GaAs and Si. The undoped GaAs layers beneath the channel layers were grown at 750 ^{o}C. The currents are normalized to their respective values at V_{sg}=0 V.

dislocation distribution. This dependence can be explained on the mass action low. The higher carrier density near a dislocation is a direct result of a higher activation of Si atoms as a donor, because of a higher probability of occupying the Ga site. Since the threshold voltage is a function of activated donor concentration, the higher is the electron concentration, the lower becomes threshold voltage.

To study the effect of a high density of dislocations in the GaAs/Si on the electrical properties, the variation of sheet resistance was measured for the n^+-GaAs layers arrayed by 50-μm pitch. The microscopic variation for the sheet resistance of the n^+-GaAs layers on GaAs and Si substrates are shown in Fig. 5.13. Note that the standard deviations of the sheet resistance figures are 17.5 Ω/□ for the GaAs/GaAs and 16.6 Ω/□ for the GaAs/Si, respectively, which indicate that a high density of dislocations in the GaAs/Si do not significantly affect the uniformity of electrical property. Figures 5. 14 (a) and (b) show Nomarski micrographs of molten KOH etched surface for the LEC-grown GaAs substrate and the GaAs/Si, respectively. The EPD is $5x10^4$ cm^{-2} for the GaAs substrate and $9x10^7$ cm^{-2} for the GaAs/Si, respectively. Note that a networked structure is clearly observed in the GaAs substrate, but the etch pits in the GaAs/Si are uniformly distributed. In spite of a high density of dislocations in the GaAs/Si, the reason for obtaining the uniform distribution of the sheet resistance on the GaAs/Si is that the dislocations in the GaAs/Si are

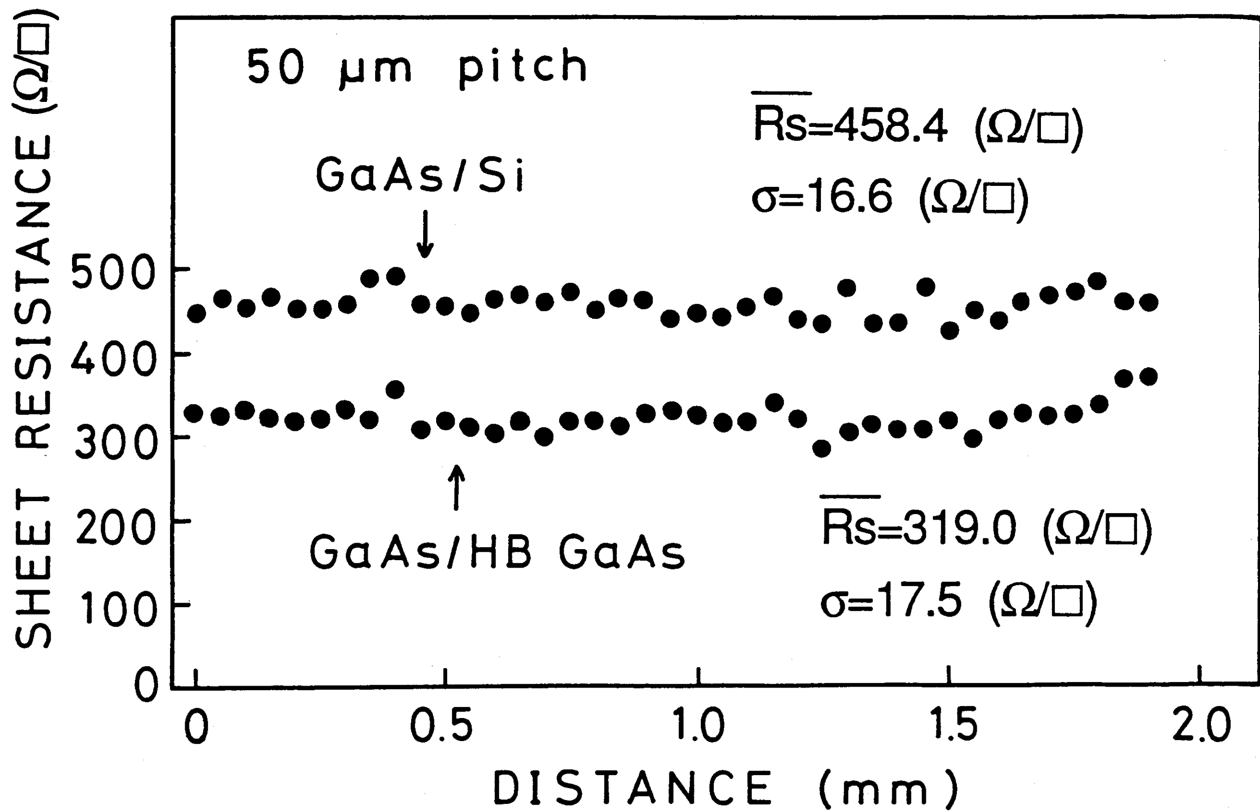


Fig. 5.13. Microscopic variation for the sheet resistance of the n^+-GaAs layers on GaAs and SiO_2 back-coated Si.

(a) LEC-grown GaAs substrate

(b) GaAs/Si

Fig. 5.14. Nomarski micrographs of molten KOH etched surface for (a) the LEC-grown GaAs substrate and (b) the GaAs/Si.

uniformly distributed.

5.6 Conclusions

GaAs MESFET's have been fabricated on Si with and without a sputtered SiO_2 back coating. The characteristics in terms of pinch-off, sidegating effect and microscopic uniformity, which are important for the GaAs LSI's on Si, are compared. The back coating suppresses the gas phase transport of Si from the substrate and reduces Si incorporation into an undoped GaAs layer during the MOCVD growth even at high temperature. Since the undoped GaAs layer beneath the channel grown even at high temperature has a low electron concentration, the pinch-off characteristic of the MESFET has been improved by the back coating of Si substrates with SiO_2. The undoped GaAs layer grown at high temperature is of good crystallinity and suppresses the sidegating effect. The threshold voltage of -1.3 V, the maximum transconductance of 160 mS/mm and the K-value of 46.8 mA/V^2mm have been obtained for a MESFET with a 2.5x15 μm gate on Si with SiO_2 back coating. The reduction in the drain current of a MESFET on a SiO_2 back-coated Si substrate is less than 4 %, even when the sidegate bias is -10 V and the sidegate pad spacing is 30 μm. The standard deviation of 16.6 Ω/□ has been obtained for the sheet resistance of the 50-μm pitch arrayed n^+-GaAs layer on Si. The characteristics of a MESFET on a Si substrate with SiO_2 back

coating are comparable to those of a MESFET on GaAs.

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Chapter 6. Summary

In the last few years considerable scientific and engineering resources have been devoted worldwide to the heteroepitaxial growth of GaAs on Si by molecular beam epitaxy (MBE) or metalorganic chemical vapor deposition (MOCVD). Numerous material advances have been reported; the two-step growth technique, the use of off-angle substrates to suppress antiphase domain formation, dislocation reduction techniques using superlattice buffer layers, selective area growth and in-situ or ex-situ annealing. Also, various types of optical and electronic devices such as lasers, solar cells, light emitting diodes (LED's), metal-semiconductor field-effect transistors (MESFET's) and high electron mobility transistors (HEMT's) have been fabricated on Si. The most impressive results using the GaAs/Si as yet are room-temperature cw operation of an AlGaAs/GaAs laser, the integration of a GaAs LED with a Si MOSFET and a GaAs 1-kbit SRAM grown by MBE or a combination of MBE and MOCVD. For practical applications, however, it would be advantageous to grow the entire device structure by MOCVD, which is generally regarded as a more promising technique than MBE for high-volume production.

In this research, the heteroepitaxial growth of GaAs on Si by MOCVD and its application to optical and electronic devices have been studied. The most noticeable results in this research are the successful fabrication of room-

temperature cw operation of AlGaAs/GaAs SQW lasers and GaAs MESFET's on Si grown entirely by MOCVD. These results are important for the realization of GaAs/Si technology.

In chapter 1, the background and purpose of this research, and the current status of GaAs/Si materials and devices were presented.

The important results in this research are summarized in the following paragraphs.

In chapter 2, the heteroepitaxial growth and characterization of GaAs layers on Si by MOCVD were presented. It is clear that the crystallinity of the GaAs/Si is improved by using the $Al_{0.5}Ga_{0.5}As/Al_xGa_{1-x}P$ intermediate layers and affected by the composition of x in the $Al_xGa_{1-x}P$ intermediate layer. The $Al_xGa_{1-x}P$ layer grows two-dimensionally on Si when the composition (x) is greater than or equal to 0.45. In spite of a large lattice mismatch (3.5 %) between $Al_{0.5}Ga_{0.5}As$ and $Al_{0.55}Ga_{0.45}P$, the $Al_{0.5}Ga_{0.5}As$ layer grows two-dimensionally on the $Al_{0.55}Ga_{0.45}P$/Si. The best crystallinity has been obtained for the GaAs/$Al_{0.5}Ga_{0.5}As/Al_{0.55}Ga_{0.45}P$/Si structure, which has a specular surface morphology. The full width at half maximum of the X-ray is 126 arcs by thermal cycle annealing.

The quantum wells on Si grown with the $Al_{0.5}Ga_{0.5}As/Al_{0.55}Ga_{0.45}P$ intermediate layers show smoother heterointerfaces than those grown by the two-step growth technique. The causes of the fluctuation in the quantum well thickness of the GaAs/Si are three-dimensional growth

at the initial stage and propagation of dislocations.

The effect of selective area growth on the reduction in the EPD of the GaAs layers selectively grown on Si was studied. The EPD decreases with the narrowing of the selective area. By using a combination of strained layer superlattice and thermal cycle annealing, a minimum EPD of $1.4x10^6$ cm^{-2} has been obtained.

The use of a SiO_2 back-coated Si substrate is effective in obtaining a low background electron concentration in the undoped GaAs layer grown on Si, particularly at high temperature by MOCVD. Using SiO_2 back-coated Si, the undoped GaAs layer with an electron concentration as low as $1x10^{15}$ cm^{-3} has been grown even at 750 ^oC. The back coating suppresses the gas phase transport of Si from the substrate and reduces Si incorporation into the undoped GaAs layer during the growth, even at high temperatures.

In chapter 3, the characteristics of all-MOCVD-grown DH and SQW lasers on Si were studied. The DH laser on Si has a pulsed threshold current of 250 mA (8.87 kA/cm^2) at room temperature. The cw operation with a threshold current of 100 mA (3.55 kA/cm^2) has been achieved below 130 K. The polarization of the DH laser can be controlled by the Al composition in the $Al_xGa_{1-x}As$ cladding layer.

By using the techniques of thermal cycle annealing and SiO_2 back-coated Si, room-temperature cw operation has been achieved for all-MOCVD-grown SQW lasers on Si. The SiO_2 back coating is effective in obtaining the excellent I-V

characteristic. The thermal cycle annealing is also found to improve the crystallinity of the GaAs/Si and contribute to room-temperature cw operation. Compared with the laser on Si grown by the two-step growth technique, the laser characteristics have been improved by the use of the $Al_{0.5}Ga_{0.5}As/Al_{0.55}Ga_{0.45}P$ intermediate layers, which are caused by the smoother heterointerfaces. The laser on Si grown with the $Al_{0.5}Ga_{0.5}As/Al_{0.55}Ga_{0.45}P$ intermediate layers exhibits a cw threshold current as low as 60 mA (1.72 kA/cm^2) and a differential quantum efficiency as high as 67 % at room temperature. However, the lasers on Si still have a problem with lifetime, due to many threading dislocations. Major improvements in the material quality are necessary in order to increase the reliability to the level required for practical applications.

In chapter 4, the relationship between the crystallinity of MOCVD-grown GaAs/Si and the characteristics of Schottky diodes fabricated on the GaAs/Si with various intermediate layers was investigated. Schottky diode characteristics, which depend on the intermediate layer, are superior for the GaAs/Si with the $Al_{0.55}Ga_{0.45}P$ intermediate layer to those for the GaAs/Si fabricated by the two-step growth technique and using the SLSs/GaP intermediate layers. It is clear that the intermediate layer plays an important role in improving the crystallinity and the Schottky diode characteristics of the GaAs/Si. The Schottky diode on the GaAs/Si with the $Al_{0.55}Ga_{0.45}P$ intermediate layer shows good

forward and reverse I-V characteristics with an ideality factor of 1.06, which is as good as for an n-type GaAs substrate. However, unique to the GaAs/Si, significant leakage current is observed under reverse and small forward bias. This leakage current is caused by recombination and generation centers related to a high density of dislocations in the GaAs/Si.

In chapter 5, the characteristics of GaAs MESFET's grown by MOCVD on Si with and without SiO_2 back coating were studied. The SiO_2 back coating suppresses the gas phase transport of Si atoms from the substrate and reduces Si incorporation into an undoped GaAs layer during the growth, even at high temperatures. Since the undoped GaAs layer beneath the channel grown even at a high temperature has a low electron concentration, the pinch-off characteristic of the MESFET has been improved by the use of the SiO_2 back-coated Si. The undoped GaAs layer grown at high temperature is of good crystallinity and suppresses the sidegating effect. Threshold voltage of -1.3 V, maximum transconductance of 160 mS/mm and a K-value of 46.8 mA/V^2mm were obtained for a 2.5-μm-gate-length MESFET on SiO_2 back-coated Si. The reduction of the drain current of a MESFET on SiO_2 back-coated Si is less than 4 %, even when the sidegate bias is -10 V and the sidegate pad spacing is 30 μm. The standard deviation of 16.6 Ω/□ has been obtained for the sheet resistance of the 50-μm pitch arrayed n^+-GaAs layer on Si. The characteristics of the MESFET's grown at

high temperature on Si with SiO_2 back coating are comparable to those of the MESFET's on GaAs.

Scope for Future Work

The heteroepitaxial growth of GaAs on Si by MOCVD and its applications to optical and electrical devices were studied. Room-temperature cw operation of AlGaAs/GaAs SQW lasers and GaAs MESFET's on Si have been grown entirely by MOCVD. The successful fabrication of lasers and MESFET's on Si grown entirely by MOCVD makes sense as a first step towards transforming GaAs/Si technology into reality.

For minority carrier devices such as lasers, LED's and solar cells, further work is needed to improve the reliability of the devices. The main obstacles which degrade the reliability of optical devices are a high density of dislocations and stress in the GaAs/Si. The degradation is attributed to a high density of non-radiative recombination centers associated by dislocations. The lasers are one of the most challenging, demanding a low dislocation density (less than 1×10^4 cm^{-2}) and a low stress (less than 10^8 dyn/cm^2). The lasers would require a significant breakthrough in the material properties to attain room-temperature cw operation of 20000-100000 hours which is at least a factor of 1000 above the current best result. One possible technique to improve the reliability of lasers is the selective area growth method, which reduces

the dislocations and stress in the GaAs/Si.

In contrast, majority carrier devices such as MESFET's and HEMT's are less susceptible to dislocations. The effects of dislocations and stress on the electrical properties and the yield of GaAs LSI's on Si have not been studied in detail. For example, it is expected that a significant influence might occur due to piezoelectricity, which affects the threshold voltage of GaAs MESFET's on Si.

Undoubtedly, a significant progress in the heteroepitaxial growth has already been made in both the material and the device applications. Promising and potentially useful devices have also been made from other mismatched heteroepitaxy (InP/Si, InP/GaAs, etc.). Indeed, a deeper understanding of the art and science of mismatched heteroepitaxial growth is needed to turn the potential into reality.

Acknowledgments

The research for the present dissertation was carried out under the direction of Professor M. Umeno of Department of Electrical and Computer Engineering, Nagoya Institute of Technology. The author wishes to express his sincere gratitude to Professor M. Umeno for his constant guidance and encouragement on the present study.

The author would like to express his deep thanks to Professor M. Saji and Professor K. Nakashima of Department of Electrical and Computer Engineering, Nagoya Institute of Technology, for their fruitful suggestions.

The author wishes to express his sincere thanks to Associate Professor T. Jimbo and Dr. T. Soga of Department of Electrical and Computer Engineering, Nagoya Institute of Technology, for their encouragement during the study.

The author is deeply indebted to Dr. S. Nozaki of Intel Corporation and Mr. N. Noto of Shin-Etsu Handotai Corporation for their valuable discussions. The author wishes to express his thanks to Dr. T. George, Jet Propulsion Laboratory, for cross-sectional TEM observation, and Dr. J. J. Murray, Intel Corporation, for the SIMS measurement.

Sincere thanks are also expressed to my collaborators, especially Mr. H. Tada of Mitsubishi Electric Corporation, Mr. Y. Kobayashi, M. Taoka, D. Imanishi, Y. Hayashi and Mr. Y. Agata of Nagoya Institute of Technology.

List of Publications

Papers and Letters

(1) "The Dependence of Threshold Voltage Scattering of GaAs MESFET on Annealing Method" T. Egawa, Y. Sano, H. Nakamura, T. Ishida and K. Kaminishi, Jpn. J. Appl. Phys. **24**, L35 (1985).

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Oral Presentation

応用物理学会

1）"ＭＯＣＶＤ法による高純度ＧａＡｓエピ層へのシリコンイオン注入（Ⅱ）"　江川 他　(1983).

2）"ＧａＡｓ　ＭＥＳＦＥＴのV_{th}のアニール法依存性について"　江川 他　(1985).

3）"アルシン中での熱処理によるＧａＡｓ基板表面上のＥＰＤの減少効果"　江川 他　(1985).

4）"半絶縁性ＧａＡｓ基板における転位とV_{th}のミクロ分布との相関（Ｉ）"　江川 他　(1986).

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6）"半絶縁性ＧａＡｓ基板における転位とV_{th}のミクロ分布との相関（Ⅲ）"　江川 他　(1987).

7）"インゴットアニール基板上に成長したＭＢＥ　ＧａＡｓエピ層の評価"　江川 他　(1987).

8）"ＭＯＣＶＤ法によるＳｉ上ＤＨレーザの低温での偏光特性"　江川 他　(1988).

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