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Deep Level Characterization and Electrochemical Processing for Single Crystalline Silicon Carbide

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Abstract

This thesis describes deep level characterization for silicon carbide crystal and electrochemical technique for fabrication processes of silicon carbide electronic devices.

The author characterized deep levels in the band gap of 3C-SiC by deep level transient spectroscopy (DLTS), capacitance transient spectroscopy (CTS) and optical CTS (O-CTS). It is found that a deep level located at Ec-0.34 eV commonly exists in 3C-SiC, and it is named the ND1 center. A configuration coordinate diagram for the ND1 center is drawn from the results of DLTS, CTS and O-CTS. Deep levels with thermal activation energy of 0.35-0.75 eV are also observed, while no deep level with 0.75-1.0 eV thermal activation energy is observed. In addition, small density of deep levels with optical threshold energy of about 1.4 eV is observed.

Hydrogen passivation effects for the defects in 3C-SiC are also investigated. It is found that the ND1 center and other defects can be passivated by a hydrogen plasma treatment. However, the hydrogen plasma treatment also introduces damages in 3C-SiC. By inserting a grid between plasma source and 3C-SiC, the damages can be suppressed. 3C-SiC with the lowest deep level concentration within this work is obtained by a treatment of the hydrogen plasma with the grid and subsequent annealing at 300°C.

Deep levels in 4H-SiC epitaxial layer on substrates with non-ordinal inclined direction toward $< 1\bar{1}00 >$ are investigated. Deep level densities in the epitaxial layers do not depend on the substrate inclination but epitaxial layer thickness. The epitaxial 4H-SiC layers on the substrates with inclination toward $< 1\bar{1}00 >$ have the same crystalline quality as epitaxial layers on the substrates with inclination toward $< 11\bar{2}0 >$.

Anodic oxidation of 6H-SiC has been performed in order to investigate possibility of the usage as sacrificial oxidation. The anodic oxidation method can form silicon dioxide layer on 6H-SiC. The oxidation rate is much higher than that for thermal oxidation, but apparent consumed SiC layer is only 1/8 of the oxide thickness. By using the anodic oxidation as a sacrificial oxidation before contact formation, Al ohmic contact resistance is reduced and Schottky barrier heights of Au and Ni contacts become higher than those on as-received surfaces. These contact properties are similar with the contact properties on the surface after sacrificial thermal oxidation. The results show that sacrificial anodic oxidation is expected to substitute for sacrificial thermal oxidation.

Anodic etching of 6H-SiC has been performed. This etching method can disclose crystalline defects as etch pits in a certain etching condition. The etch pits have a peculiar shape and seem to reflect crystal growth mechanism. The etch pits would originate from micropipes and screw dislocations existing in the crystal. And under

another etching condition, etched surfaces do not show observable roughness and etch pits even seeing through a microscope. By using this etching condition, patterned structures on 6H-SiC surfaces are fabricated.

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Chapter 1

Introduction

1.1 Background

In present days, electronics is very important for our life. We use a lot of electronic devices, such as mobile phones, computers, compact disc (CD) players and so on, day after day. A core of the electronics is a semiconductor technology. Most of electronic devices operate with semiconductor electronic circuits. Diodes and transistors are common semiconductor electronic devices, and integrated circuits (IC) and large scale integrated circuits (LSI) are very small scaled electrical circuits fabricated by semiconductors. Solar cells and light emitting diodes (LED) are also important semiconductor devices, because a large number of electronic device products are equipped with them.

Semiconductor devices are made of solid-state crystals, such as Ge, Si, GaAs. The most popular semiconductor crystal is Si, because most of the IC and the LSI, which have very large commercial market, have been fabricated from this material. And switching devices, which control high power electricity, have also been fabricated from Si. A Si semiconductor technology has been established and developed in 20th century. Now, in 21st century, Si semiconductor devices encounter capability limitations due to the material properties. Energy efficiency of the Si high power devices is not so high and power output of Si high frequency devices is also not so high. The energy efficiency should be increased as high as possible in environmental view, and higher power output devices make the system including them small. In addition, the Si devices cannot operate in high temperature conditions. Thus, alternative materials which can overcome these problems are widely researched. One of the candidates of the alternative materials is silicon carbide (SiC).

1.2 Silicon Carbide

SiC is a compound crystal with bonding between silicon and carbon. A semiconducting property of this material has been expected since 1900's [1]. However, because of the difficulty of the material synthesis, researches for use of this material as a semiconductor have not been active for the long time. After development of the modified Lely method

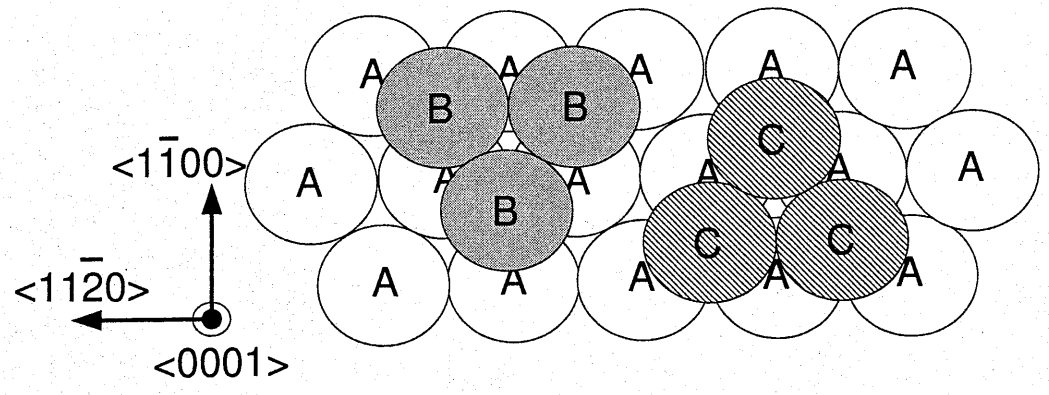

Figure 1.1: Close-packed structure filled up with many balls.

[2,3], which can grow SiC crystal with large size boule, and the chemical vapor deposition (CVD) method on Si substrates [4,5], research activities became lively. Now, SiC wafers are commercially available and SiC Schottky diodes are also commercially available. It seems that SiC semiconductor devices will be spread rapidly in our life.

Material properties of SiC are based on tight binding between silicon and carbon atoms, which is 88% covalent and 12% ionic. This strong bond leads to a wide band gap, high thermal conductivity, and physical and chemical stability. The band gaps for 3C-SiC and 4H-SiC are 2.2 eV and 3.2 eV, respectively, and those values are two or three times larger than that for silicon. Another feature of SiC is polytypism. The polytypism means that the crystals have the same chemical composition but different atomic periodical arrangements. SiC has a large number of polytypes, such as 3C, 4H, 6H and so on. The these notations are called the Ramsdell's notation and indicate crystalline structures [6]. Imagine that a crystal has a close-packed structure, which is filled up with many balls as shown in Fig. 1.1, and each the ball consists of a silicon and carbon atom pair. The balls can locate three kinds of positions in the stacking direction with arbitrary notations of A, B and C. If order of stacking is "ABCABC", the crystal structure is called "3C", which has periodicity of *3* layers and a *Cubic* structure. If stacking order is "ABACABAC", the crystal structure is called "4H", which has periodicity of *4* layers and a *Hexagonal* structure. Figure 1.2 shows stacking order for typical SiC polytypes.

1.2.1 3C-SiC

As mentioned above, 3C-SiC has a cubic structure and "ABCABC" sequence to the stacking direction (the stacking direction is the same as $< 111 >$ or $< 0001 >$ direction in crystallography). This polytype has the lowest band gap energy in SiC polytypes and has isotropic physical properties, such as the electron mobility and the dielectric constant, due to the its cubic structure. This polytype is usually fabricated by the CVD method on Si (100) or (111) substrates. Figure 1.3 shows a furnace for the CVD. In the

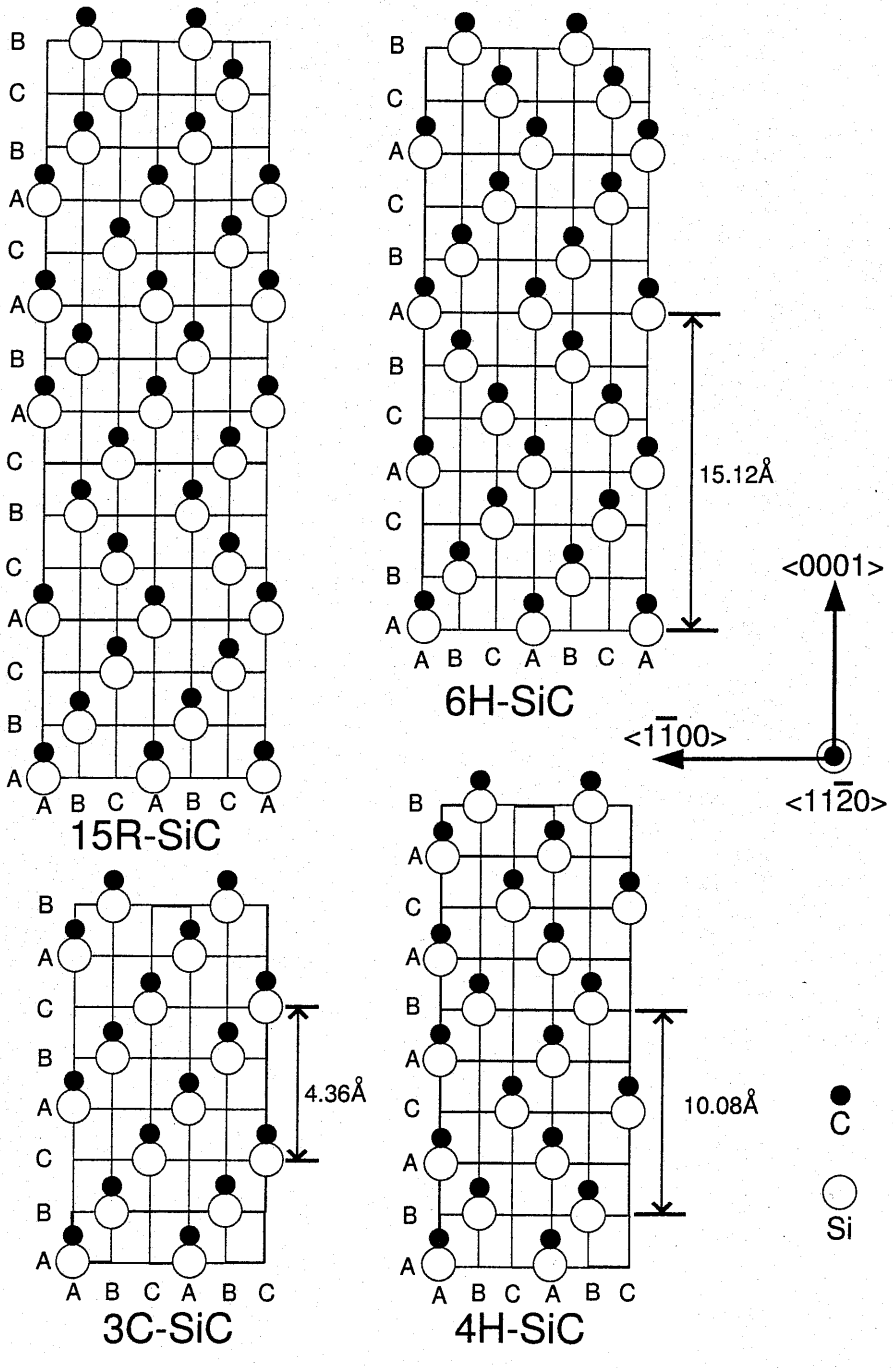

Figure 1.2: Stacking order of 3C-, 4H-, 6H- and 15R-SiC.

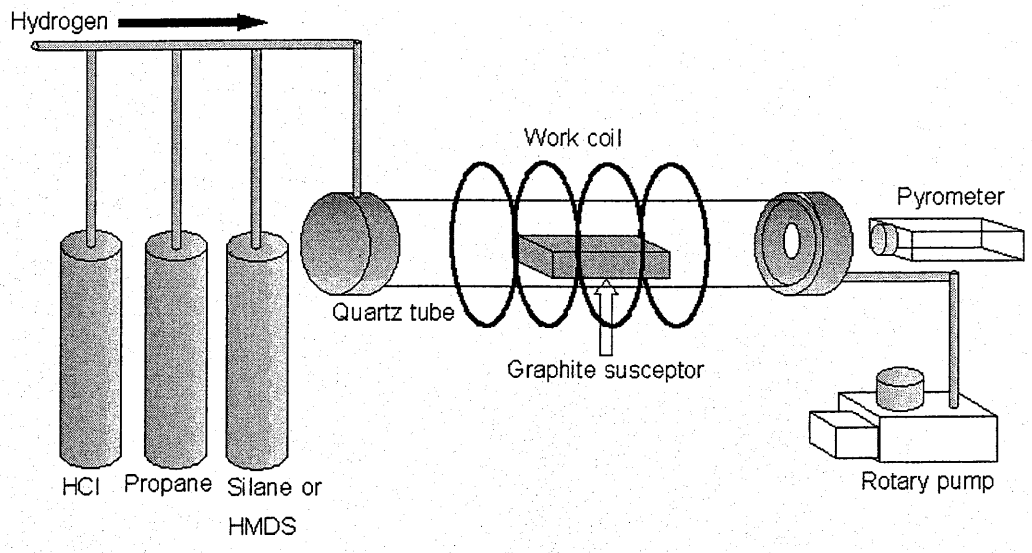

Figure 1.3: CVD furnace for 3C-SiC epitaxial growth with a horizontal configuration.

following paragraph, growth processes for 3C-SiC on Si are briefly explained.

At first, a graphite susceptor coated by SiC is baked in the quartz tube in order to remove the contaminant in the susceptor. Then a Si substrate is put on the susceptor, and the susceptor is inserted in the quartz tube again. In the quartz tube, the graphite susceptor is inductively heated by high frequency magnetic fields, which are formed by induction coils with high frequency AC current. Temperature of the susceptor is monitored by a pyrometer. Before the growth, the Si substrate is etched by HCl gas at the temperature of 1175°C. After that, the HCl gas is evacuated and temperature is decreased to room temperature. Then, for carbonization of the Si substrate, propane is introduced into the tube and temperature is increased to 1350°C. There are two kinds of source gas systems, the one is a mixture gas system of Si and C sources (two source system), such as silane + propane and Si_2Cl_6 + propane, the other is one source gas system for the Si and C source (one source system), such as hexamethyldisilane (HMDS) and tetramethylsilane. In the case of two source system, Si source is introduced together with propane into the tube, while in the case of one source system, propane flow is stopped and source gas is introduced into the tube. All of the gases are introduced with H_2 carrier gas. 3C-SiC is grown during this process. After the growth, all of the source gases are evacuated, and Ar gas is introduced in order to avoid the etching by source gas at lower temperature. Then temperature is decreased to room temperature and the CVD process is finished.

Generally, CVD grown 3C-SiC on Si has very high density of anti phase boundaries (APBs) and twins [7–9]. The APBs formation is a common problem for growth of a polar crystal on a non-polar crystal, and the twin is formed if two dimensional nucleation is dominant during the first growth step. Both the planar defects deteriorate crystalline

quality and device performance. Up to now (Dec. 2002), commercial 3C-SiC wafers are not available due to the defect problem. Recently a method for elimination of these two defects has been established by using undulant Si (100) substrates [10, 11]. However, 3C-SiC employed in this work is a conventional CVD layer and has a large number of such kinds of defects.

1.2.2 4H- and 6H-SiC

4H- and 6H-SiC have hexagonal crystalline structures, and wafers having these polytypes are commercially available. The wafers are generally fabricated by a sublimation method with seed crystals, so called the modified Lely method [2,3]. A schematic of the sublimation furnace is shown in Fig. 1.4. The key point of this method is sublimation of SiC source powder and re-crystallization of the source at the seed crystal position. The source powder is introduced at the bottom of a graphite crucible and the seed crystal is stuck at top of the crucible. The crucible has low impedance and is covered by a high impedance graphite thermal insulator. Then the crucible is inserted in a quartz tube. Around the quartz tube, an induction coil which can conduct large current is placed. High frequency voltage is applied to the coil and then the crucible in the tube is heated inductively. By controlling voltage and current, a lower part and an upper part of the crucible are heated up to around 2500°C and 2200°C, respectively. This temperature gradient makes source the powder sublimated and transported to the seed crystal position.

Generally, sublimation grown SiC crystals have relatively poor crystallinity. There are many structural defects in the crystals. One example for the structural defects is a micropipe, which is a hollow core threading through the crystal. For fabrication of SiC electronic devices, the micropipe formation is a major problem and thus many researchers have been engaged in elimination of the micropipe. In addition, control of the doping concentration is also difficult in the sublimation growth. Thus CVD homoepitaxial growth of SiC, which can grow crystal with low defect density and desirable doping concentration, is frequently performed on SiC substrates. Instruments for the CVD homoepitaxial growth are the almost same as that for heteroepitaxial growth of 3C-SiC which is shown in Fig. 1.3. Differences between them are growth temperature and substrates. In homoepitaxial case, the growth temperature is around 1500-1600°C and the substrates are sublimation-grown 6H- or 4H-SiC which has a (0001) polished face with inclination. The inclination leads the epitaxial growth to a step-flow growth mode [12–19], and thus high quality epitaxial layers are grown at 1500-1600°C. (Without inclination, epitaxial layer surfaces show mosaic patterns.) A large number of electronic devices have been fabricated by many research groups by using epitaxial SiC layers [20–27].

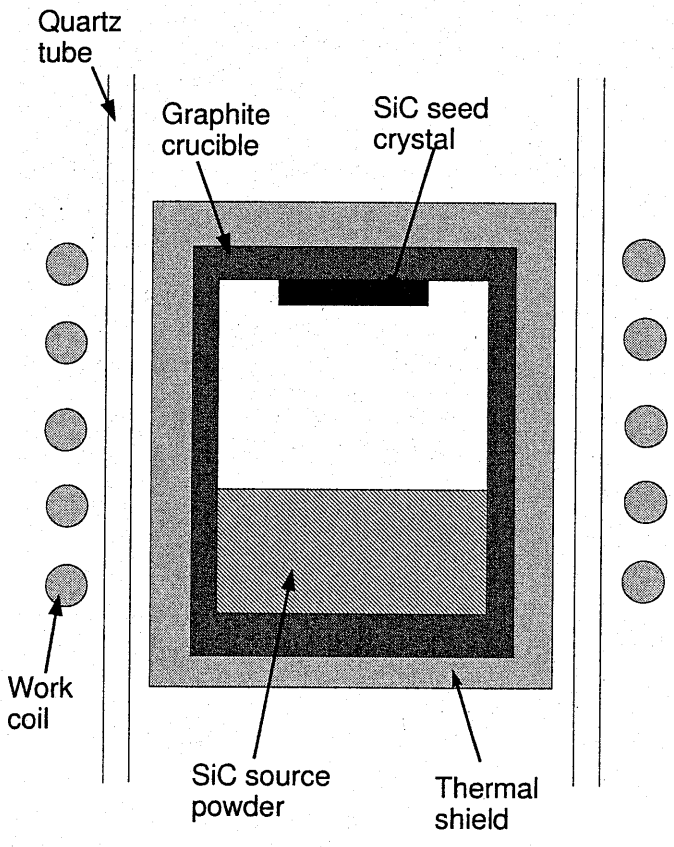

Figure 1.4: Sublimation furnace for the bulk hexagonal SiC growth.

1.3 Prospects of SiC electronic devices

The most prospective polytype for power electronic devices is 4H-SiC. In this section, material properties between 4H-SiC and Si are compared. 4H-SiC has band gap of 3.2 eV, which is about three times larger than that of Si. A breakdown electric field for 4H-SiC is 2×10^6 V/cm, which is about one order of magnitude larger than that for Si. Thermal conductivity for 4H-SiC is 4.9 W/cm·K, while that for Si is 1.5 W/cm·K. The large band gap ensures operation of electronic devices in high temperature conditions. The large band gap and thermal conductivity make the devices stable in high power operation. And 4H-SiC has the large electron saturated velocity, which determines the limit for high frequency operation. The electron saturated velocity for 4H-SiC is 2.7×10^7 cm/s, which is about three times larger than that for Si. Considering all the excellent properties, 4H-SiC power electronic devices can operate with power loss of 1/100 compared to Si devices, and 4H-SiC device size becomes 10 times lower than Si device size.

At present, devices operating with such theoretical values have never been realized. There are many problems for fabrication of "good" devices. In the crystal growth, crystalline quality must be improved, and impurity concentration must be more controllable. In the device fabrication processes, insulation layer formation technique must be improved, and ohmic contact resistance must be decreased and pattern formation methods must be also improved. The process temperature should be decreased, because high temperature processes affect negatively results of earlier stage processes. In order to achieve these improvements, basic researches for SiC properties, SiC crystal growth and crystal characterization are desired, and researches for device fabrication processes are also important.

1.4 Contents of this thesis

In order to overcome the problems mentioned in the previous section, electrical characterization of SiC crystal was carried out in this research work. Deep levels in the band gap were detected by using capacitance transient methods. The deep level detection gives important information for crystalline quality improvement and for expectation of device characteristics. This thesis also deals with deep level passivation. If deep level defects in crystal are passivated, the defects no longer deteriorate the device operation. This is an effective method for the improvement of device performance. Another highlight of this thesis is low temperature processes for SiC device fabrication. The low temperature processes were carried out in an electrochemical reaction. An oxide film on SiC is important because the oxide film is used as gate and field insulation layers. Generally an oxidation process for SiC is performed under high temperature condition about 1100°C. By using the electrochemical method, an oxide film can be formed on SiC at room temperature. Another usage of the electrochemical method is an etching process. The etching of SiC is difficult due to its chemical stability. Dry etching methods have been employed for etching process in device fabrication processes. However,

the dry etching processes introduce damage layers in near SiC surface regions. The electrochemical etching can etch SiC at room temperature and the resulting etched surface has no damages. In addition, the etching can be used as crystal characterization. The defects in the crystal are decorated after the electrochemical etching. The decorated defects can be observed by a microscope, and thus defect density can be evaluated.

Chapter 2 deals with deep levels in 3C-SiC detected by a deep level transient spectroscopy (DLTS), which is a very common method to observe deep level defects in semiconductor crystal [28]. The deep levels are also measured by capacitance transient spectroscopy (CTS) and optical capacitance transient spectroscopy (O-CTS). From the DLTS method, thermal excitation of electrons from deep centers can be observed conveniently. From the CTS method, thermal excitation can be observed at relatively low temperatures. From the O-CTS method, optical excitation from deep levels can be observed. By using these three methods, the energy structure for the deep levels is investigated. In chapter 3, it is reported that the deep levels in 3C-SiC are passivated by hydrogen on the basis of the DLTS observation. Hydrogen is introduced in 3C-SiC by hydrogen plasma, and then its thermal stability is observed. In chapter 4, deep levels in 4H- and 6H-SiC epilayer are investigated. The 4H-SiC samples characterized have different inclined direction from ordinary epitaxial layers. The deep level information about such epitaxial layers helps disclosure of mechanism of deep level formation. In chapter 5, a low temperature oxidation process for 6H-SiC is described. The process is anodic oxidation, which is one of the electrochemical methods. It is convenient to form an oxide film on silicon carbide at low temperature. In chapter 6, the electrochemical etching of 6H-SiC is reported. At first, the etching method is used for characterization of crystalline defects. After the etching, crystalline defects are decorated with a peculiar shape. Second, the etching in a resulting flat surface is tried and patterned structures are fabricated using this method. A possibility of this method to alter conventional dry etching methods is discussed. In chapter 7, summaries of this thesis are given.

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Chapter 2

Deep Level Observation in 3C-SiC

2.1 Introduction

3C-SiC is generally grown on Si substrates by the CVD method as described in the previous chapter. There are large differences in thermal expansion coefficients (~8%) and lattice constants (~20%) between 3C-SiC and Si. These differences introduce many crystalline defects, such as APBs and twins [1, 2]. Other defects and many impurities are unintentionally included in the crystal. For device fabrication using this material, characterization of the defects and the impurities is important. The DLTS is one of the powerful tools for detecting the defects and impurities [3]. In the appendix A, theory of the DLTS is briefly explained.

For 4H- and 6H-SiC, the DLTS measurements from low temperature of about 100 K to high temperature of 700 K have been reported [4–7]. However, for 3C-SiC, DLTS studies in the temperature range up to high temperature were limited [8–11]. Only a few reports studied high temperature DLTS measurements for 3C-SiC on 6H-SiC [12, 13]. The DLTS measurements below the room temperature are equivalent to the energy range of less than 0.6 eV, if the typical capture cross section of 10^{-16} cm^2 is assumed. It is considered that the most important deep level for device operation locates near midgap states, which act frequently as generation and recombination centers and increase junction tunneling current. Thus, so far, the most important energy region in 3C-SiC on Si has never observed by the DLTS. In this chapter, firstly, deep levels in 3C-SiC grown from silane and propane were discussed by DLTS and CTS measurements at high temperature region.

There are a few reports about 3C-SiC grown from HMDS [14–17]. The information about deep levels in 3C-SiC grown from HMDS is very limited, although gas system difference may lead the difference of the deep levels. In this chapter, secondly, DLTS results for 3C-SiC grown from HMDS was discussed and the source gas system difference was also discussed.

Optical excitation measurements of the carrier from deep levels have never reported in 3C-SiC. The optical properties of the deep levels are very important to see the characteristics of the defects. O-CTS measurement can detect the optical cross section and the optical threshold energy of the deep levels by excitation from light [18]. Furthermore,

Table 2.1: Growth conditions for 3C-SiC grown from silane and propane.

Sample name	Silane flow	Propane flow	Growth time	Film thickness
silane A	7.5 sccm	4.5 sccm	2h. 20min	~5 μm
silane B	5 sccm	3 sccm	3h.	~10 μm
silane C	2.5 sccm	1.5 sccm	5h.	~10 μm

the O-CTS measurements can reveal very deep levels, which cannot excite thermally due to requirement of very high temperature measurement. In this chapter, finally, O-CTS measurements for 3C-SiC grown from silane and propane were dealt with.

2.2 Experiment

2.2.1 3C-SiC grown from silane and propane

3C-SiC samples grown from silane and propane were grown on p-type Si (100) substrates. The growth was done under atmospheric pressure and at 1350°C, and carrier gas for source gases was H_2. Three samples were grown with different gas flow rates and growth times as shown in Table 2.1. The samples were named as in this table. Conductivity of the samples confirmed by Hall measurements was n-type. Polytype and crystal orientation of the samples were confirmed as 3C-SiC (100) crystals by the Raman scattering spectroscopy. All of the samples had net donor concentrations of approximately 4×10^{16} cm^{-3}.

2.2.2 3C-SiC grown from HMDS

3C-SiC grown from HMDS were grown on n-type Si (100) substrates by atmospheric pressure CVD with H_2 carrier gas. The HMDS flow rate was 0.5 sccm and growth temperature was 1350°C. The growth time was varied to obtain samples with various thicknesses, which are listed in Table 2.2 along with net donor concentrations. The samples were named as in this table. Polytype and crystal orientation of the grown samples were confirmed as 3C-SiC (100) crystals by the Raman scattering spectroscopy and reflective high energy electron diffraction (RHEED). Hall measurements for the samples revealed that the samples were n-type.

2.2.3 Capacitance transient methods for deep level detection

In order to fabricate Schottky diodes for measurements, Au and Al contacts were evaporated on all the samples as Schottky and ohmic contacts. The Schottky contacts areas were 1 and 0.28 mm^2 for the samples grown from silane and propane and those grown from HMDS, respectively. Capacitance-voltage measurements were performed to see net

Table 2.2: Thicknesses and net donor concentrations for 3C-SiC grown from HMDS. ("-" indicates that the net donor concentration could not be measured due to leaky Schottky contacts.)

Sample name	Film thickness (μm)	Net donor concentration (cm^{-3})
HMDS0.65	0.65	1.2×10^{18}
HMDS1.0	1.0	1.1×10^{18}
HMDS2.2	2.2	3.8×10^{17}
HMDS2.6	2.6	6.5×10^{17}
HMDS3.2	3.2	3.8×10^{17}
HMDS4.3	4.3	-
HMDS6.6	6.6	4.4×10^{17}
HMDS8.0	8.0	-
HMDS17	17	-

donor concentrations. DLTS measurements were carried out using the bipolar rectangular weighting function [19]. A detail of the principle of the DLTS and CTS is explained in appendix A. A block diagram for the DLTS system used in this study is shown in Fig. 2.1. As shown in this figure, in the case of CTS measurements, a temperature controller is required and a part of the electronic circuits is not used. The bias condition for the DLTS, CTS and O-CTS measurements were -1 and 0 V for reverse and injection bias, respectively. All the DLTS spectra shown in this chapter are for rate window of 105 s^{-1}. The O-CTS measurement observes capacitance transient signal caused by optical excitation of carriers from deep levels. The measurements are performed at lower temperature than the temperature at which carrier excitation from deep levels occurs due to thermal excitation. Light sources for optical excitation are monochromatic lights. For O-CTS measurements, a white light source from a 300 W Xe lamp are separated to a monochromatic light by a monochromator. Emission rates by the optical excitation are in proportional to a photon flux of the light subjected to this equation, $\tau = 1/\phi \cdot \sigma_o$, where ϕ is the photon flux and σ_o is the optical cross section. A large photon flux is required to see an O-CTS signal during appropriate measurement time. Since, in order to get a large photon flux, slits of the monochromator are fixed with large width, resolution of output wavelength from the monochromator is not so high. An energy range of the monochromatic light is 0.5-2.1 eV, and the lamp current was adjusted so that the excitation light has a constant photon flux for a series of the spectra. Depending on the source emission spectrum, two different levels of photon flux were adopted, one is 2×10^{15} $cm^{-2}s^{-1}$ for 0.50-0.73 eV and the other is 6×10^{15} $cm^{-2}s^{-1}$ for 0.73-2.1 eV. The monochromatic lights were illuminated to the samples through the Schottky contacts. Thus, for this measurements, the thin Au Schottky contacts (~50 nm) were formed on the samples.

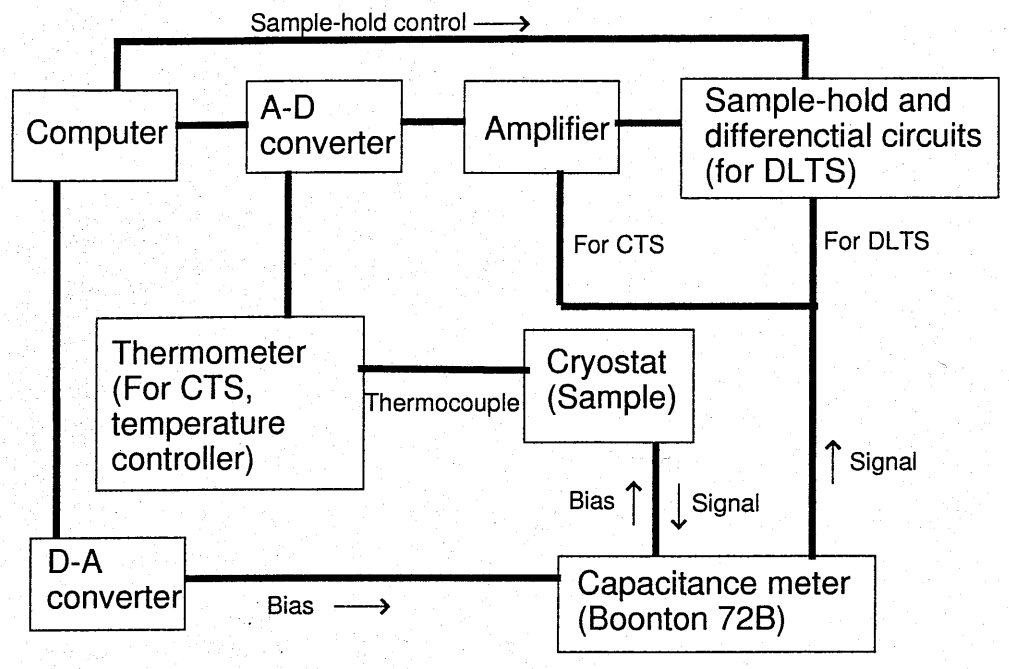

Figure 2.1: A block diagram for the DLTS and CTS system.

2.3 Results

2.3.1 DLTS and CTS measurements for 3C-SiC grown from silane and propane

DLTS and CTS results for 3C-SiC grown from silane and propane are shown. Figure 2.2 shows DLTS spectra for the samples named silane A, B and C. All the samples show sharp peaks around 150 K, which correspond to the deep levels with activation of 0.27-0.33 eV. Except for this peak, the silane A shows no peak at the entire temperature range. For the silane B, a small and broad peak is observed near room temperature. Furthermore, the silane C exhibits a large and broad peak around room temperature. The temperature range of the very broad peak in the silane C is roughly equivalent to the activation energy of 0.35-0.75 eV when the typical capture cross section is assumed.

For the temperature range above 400 K, there is no peak in the DLTS spectra for these sample. High temperature measurements are important for observation of midgap levels. However, at temperature above 500 K, accurate DLTS measurements are not possible, because the diodes show large leakage current at this temperature range. Thus, we measured CTS at the highest temperature at which the leakage current is small enough for accurate capacitance measurements. Figure 2.3 shows CTS spectra for the silane A, B and C. For CTS spectrum at 450 K, the time constant of 10^3 ms corresponds to an activation energy of 0.93 eV, if a capture cross section at infinite temperature is 10^{-16} cm^2. On the other hand, for CTS spectra at 400 K and 500

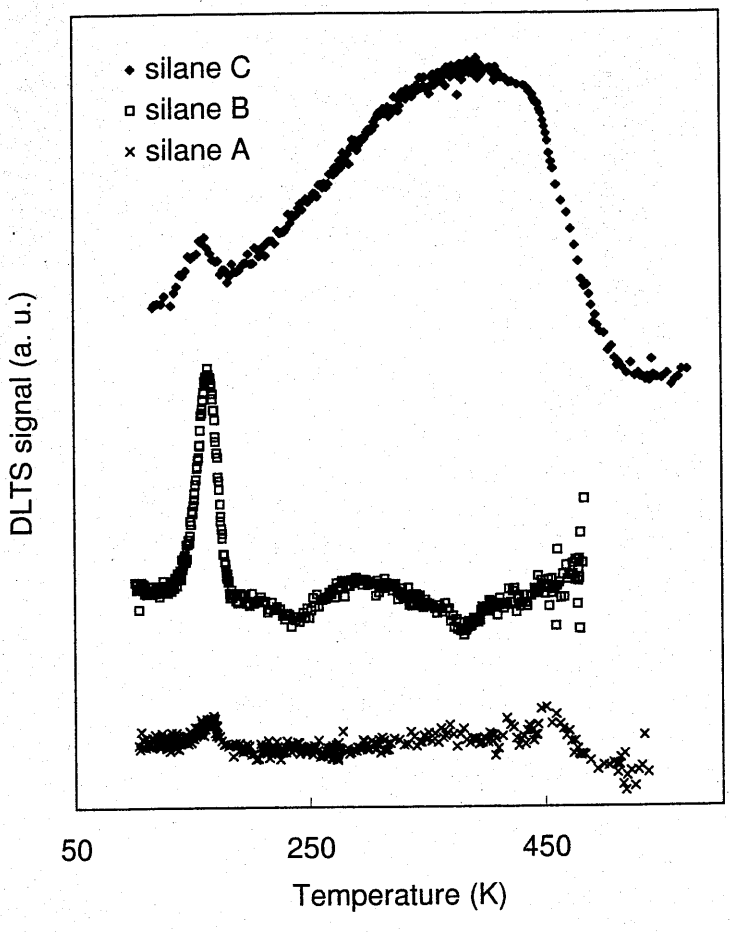

Figure 2.2: DLTS spectra for 3C-SiC grown from silane and propane.

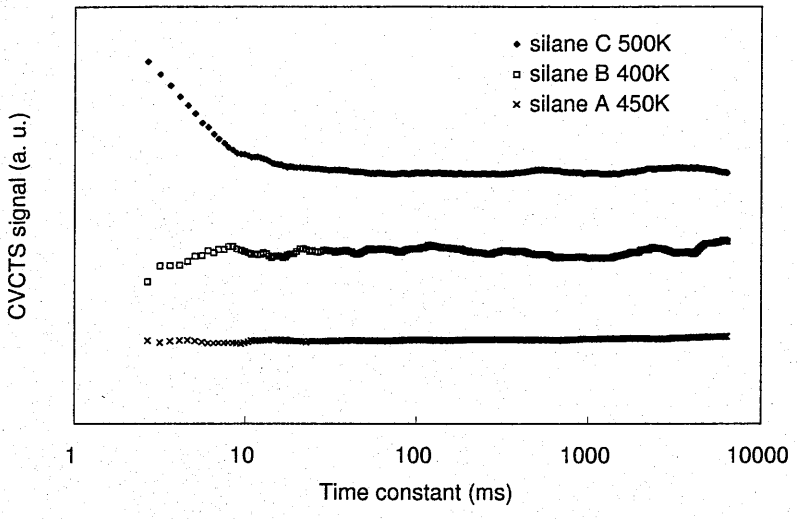

Figure 2.3: CTS spectra for 3C-SiC grown from silane and propane.

K, the time constant of 10^3 ms corresponds to activation energies of 0.82 and 1.0 eV, respectively. No CTS peak appears in all the CTS spectra, except for time region of less than 10 ms in the silane C which corresponds to broad peak around room temperature in the DLTS spectrum. Thus no new peak was detected.

In this study, the detection limit of DLTS and CTS measurements is approximately 1/1000 of the carrier concentration. Thus, the concentration of near midgap defects is less than 10^{13} cm^{-3} in the observed samples. However, in fact, it cannot be concluded that no midgap defects in 3C-SiC commonly exist, because it is not clear that the observed samples are typical 3C-SiC or not. In order to clarify this, more samples must be investigated.

Saddow *et al.* and Schmitt *et al.* reported DLTS data in a temperature range of about 100 to 700 K for 3C-SiC [12,13], but their data are very different from the data in this work. The sample measured by Saddow *et al.* was CVD grown 3C-SiC on 6H-SiC, and the sample measured by Schmitt *et al.* was molecular beam epitaxial (MBE) grown 3C-SiC film on 6H-SiC. Therefore, substrates and growth methods used in their works were different from this work. 6H-SiC has almost same thermal expansion coefficient and lattice constant with 3C-SiC. The grown films on 6H-SiC would have different kind of defects compared with those on Si.

2.3.2 DLTS measurements for 3C-SiC grown from HMDS

The Au contacts on the thick 3C-SiC (>8.0 μm) grown from HMDS showed ohmic characteristics, while those on the thinner samples had a tendency to show the Schottky

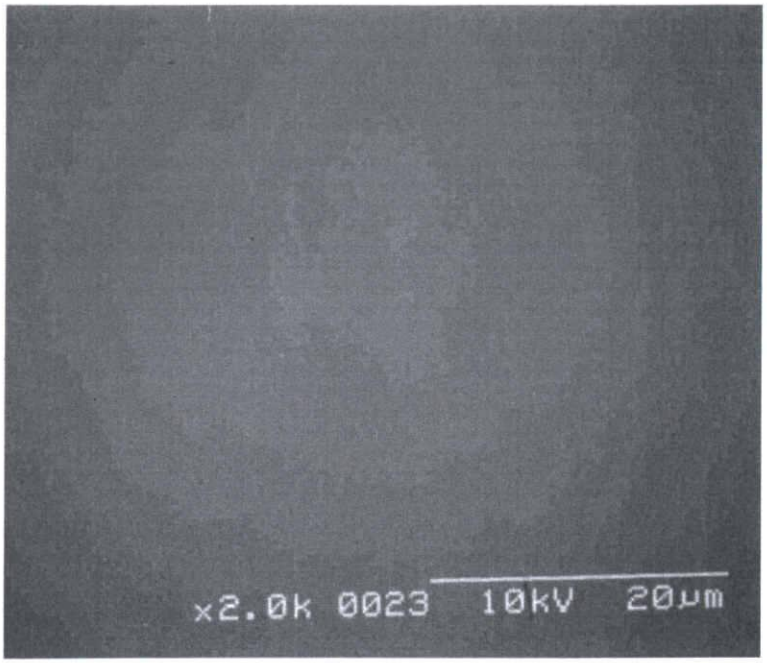

Figure 2.4: SEM micrograph for the HMDS0.65 (the 0.65 μm thick 3C-SiC grown from HMDS).

characteristics. The main reason for this seems to be the surface roughness, which increases with sample thickness. Figure 2.4 shows a scanning electron microscope (SEM) picture for the surface of the HMDS0.65, for which the Schottky contacts were obtained. There was no significant roughness on the surface. Figure 2.5 shows the SEM micrograph for the surface of the HMDS8.0. The Schottky contacts were not obtained on this sample and it had significant roughness on the surface. Since an edge part of the rough surface under the Au contacts suffers an electric field concentration, which leads to immature breakdown of the junction, the Au contacts on the rough surface would show the ohmic characteristic.

The DLTS spectrum for the HMDS0.65 is shown in Fig. 2.6. Only one peak is apparently observed around 300 K, but capacitance transient signals are observed over the entire temperature range and the flat part of the spectrum is raised from the zero level. The flat part is the superposition of numerous peaks distributed at various temperature positions or is due to defects which have an emission behavior deviating from an exponential form. The capacitance transient signals for the flat part are discussed later.

Figure 2.7 shows the DLTS spectrum for the HMDS1.0. This spectrum is similar to that for the HMDS0.65, and capacitance transient signals are also observed in the entire temperature range. Figure 2.8 shows the DLTS spectrum for the HMDS2.2. In contrast to the HMDS0.65 and the HMDS1.0, this spectrum exhibits a peak near 130 K, and the flat part is almost at zero. The DLTS spectrum for the HMDS3.2 is shown in Fig. 2.9. This spectrum also has only one peak near 130 K. The DLTS spectra for

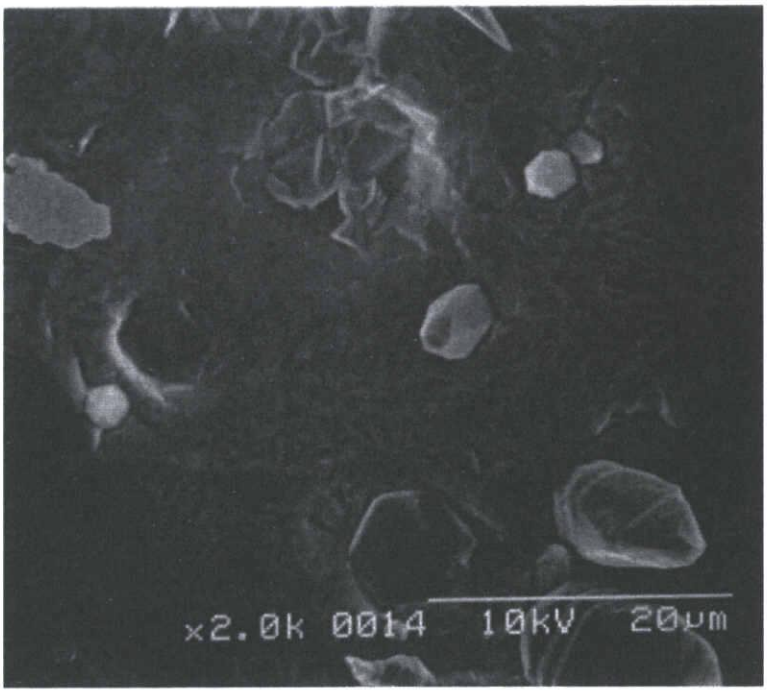

Figure 2.5: SEM micrograph for the HMDS8.0 (the 8.0 μm thick 3C-SiC grown from HMDS).

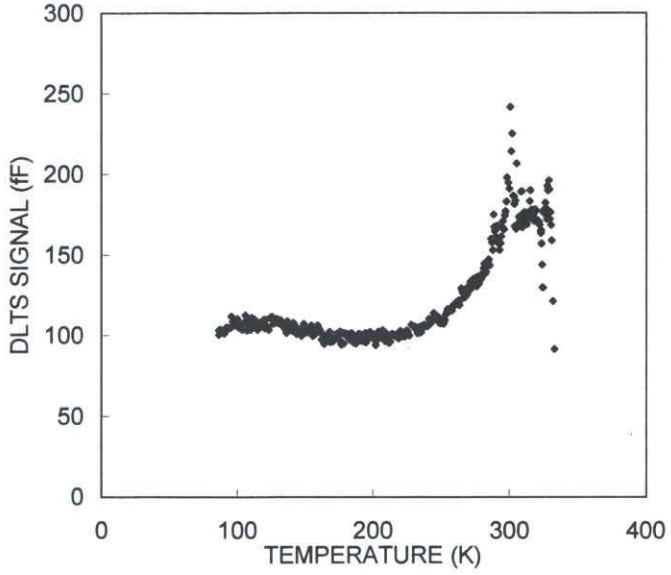

Figure 2.6: DLTS spectrum for the HMDS0.65 (the 0.65 μm thick 3C-SiC grown from HMDS).

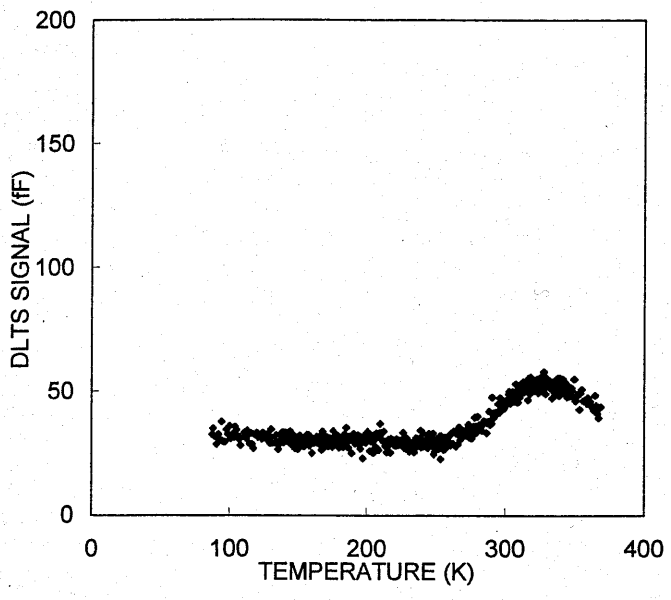

Figure 2.7: DLTS spectrum for the HMDS1.0 (the 1.0 μm thick 3C-SiC grown from HMDS).

the HMDS2.6 and the HMDS6.6 are not shown, since these spectra also show only one peak near 130 K.

The spectra of the 2.2-6.6 μm thick epilayers show no capacitance transient signals at any temperature except for near 130 K. Figure 2.10 shows the Arrhenius plots of τT^2 for the peaks near 130 K. The parameters for these peaks estimated from the Arrhenius plots are listed in Table 2.3. Although the capture cross sections at infinite temperature are different among the samples, the difference would be due to poor accuracy of the extrapolation procedure in the Arrhenius plot. It is considered that these defects are identical.

The DLTS signals for the HMDS0.65 and the HMDS1.0 have a flat part, as described above. Figure 2.11 shows the capacitance transient signal for the 0.65 μm thick sample at 190 K, which corresponds to a flat region in the spectrum, and similar signals are also observed at other temperatures. The transient signal cannot be fitted by an exponential function but by a logarithmic function, as shown in Fig. 2.11. Usually, such a signal is interpreted by the model with the carrier emission from distributed energy levels. Here, another model to explain this transient behavior is examined. Similar transient behavior has been reported to occur at photoconductive decay [20], and has been interpreted by considering a barrier which separates the electrons and holes. Since there are a large number of dislocations in the present 3C-SiC samples caused by the heterointerface, a dislocation space charge pipe model is introduced [21], in which physically localized

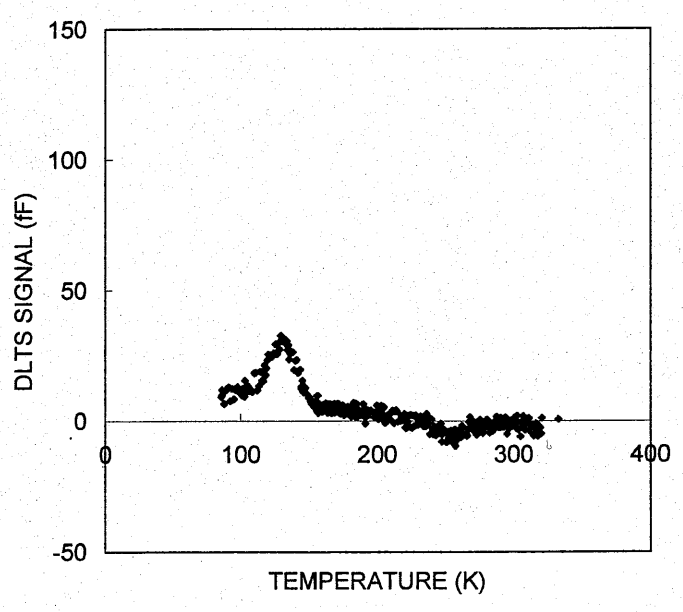

Figure 2.8: DLTS spectrum for the HMDS2.2 (the 2.2 μm thick 3C-SiC grown from HMDS).

Table 2.3: Trap parameters of the peaks near 130 K for 3C-SiC grown from HMDS and trap parameters of the peaks near 150 K for 3C-SiC grown from silane and propane.

Sample name	Activation energy (eV)	Capture cross section at infinite temperature (cm^2)	Defect density (cm^{-3})
HMDS2.2	0.26	5.9×10^{-14}	9×10^{14}
HMDS2.6	0.21	6.8×10^{-16}	2×10^{15}
HMDS3.2	0.24	6.7×10^{-15}	7×10^{14}
HMDS6.6	0.25	1.2×10^{-14}	2×10^{15}
silane B	0.33	3.4×10^{-14}	2×10^{14}

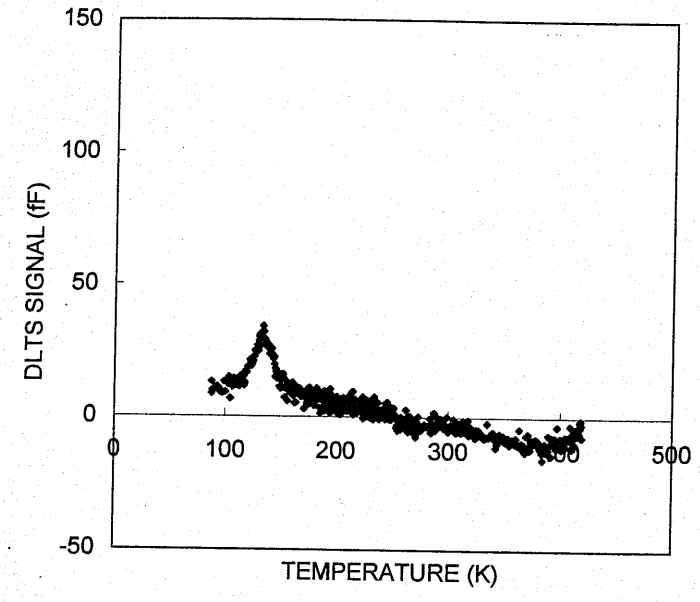

Figure 2.9: DLTS spectrum for the HMDS3.2 (the 3.2 μm thick 3C-SiC grown from HMDS).

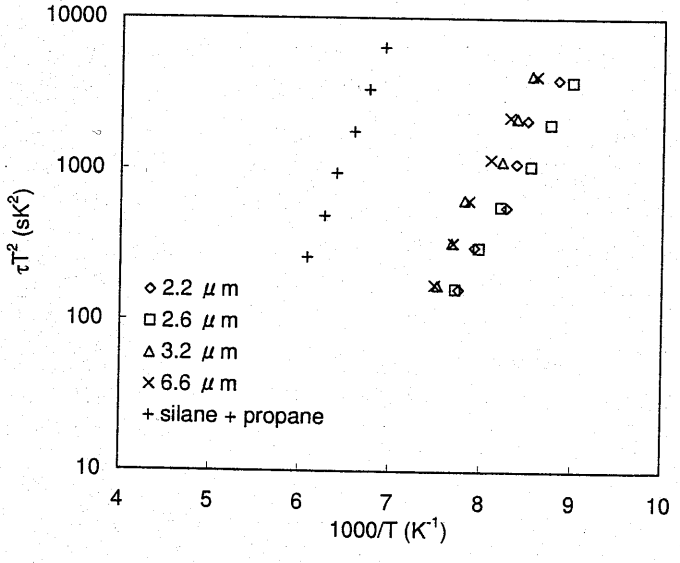

Figure 2.10: Arrhenius plots of τT^2 for the peaks around 130 K in the DLTS spectra for 3C-SiC grown from HMDS and the peak around 150 K in the DLTS spectrum for 3C-SiC grown from silane and propane (silane B).

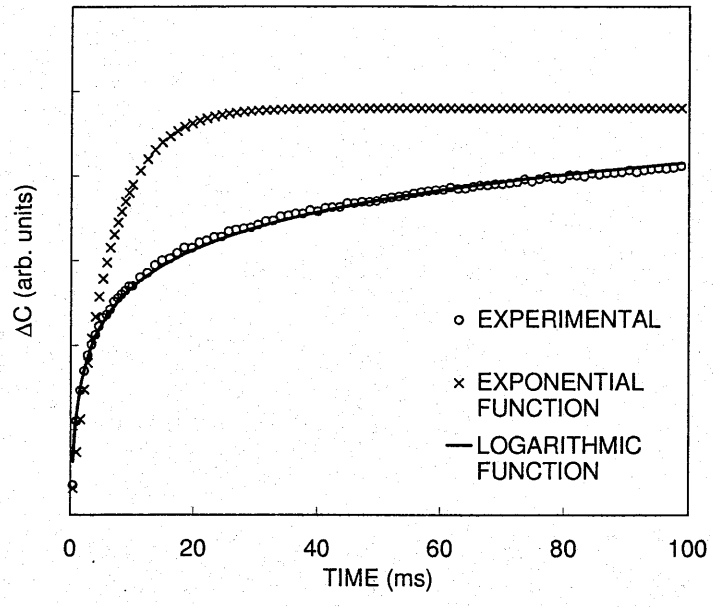

Figure 2.11: Capacitance transient signal for the HMDS0.65 at 190 K with exponential and logarithmic functions.

and a discrete defect level forms a potential valley around the defect by charges at this level. When electrons are emitted from the levels, the depth of the potential valley increases and the electron emission rate decreases. Then the apparent activation energy of emission depends on the number of trapped electrons, and the emission behavior deviates from the exponential form. Using this model, the emission behavior is simulated and compared with the experimental data. However, this calculation data could be fitted to the experimental data only at a single temperature and the entire DLTS spectrum could not be reproduced. Thus, it is concluded that this model is not proper and the carrier emission would be caused by the energy levels distributed over a wide energy range.

Comparison of the DLTS results for the 3C-SiC grown from HMDS with the those grown from silane and propane is discussed. In Fig. 2.10, the Arrhenius plot for the peak observed from the silane B is shown. From the plot, the activation energy for the peak is determined to be 0.33 eV as listed in Table 2.3. Zhou *et al.* discovered two defects having activation energies of 0.34 eV and 0.68 eV from a DLTS study for 3C-SiC/Si grown from silane and propane [8]. Zekentes *et al.* detected four kinds of defects having activation energies of 0.25 eV, 0.32 eV, 0.54 eV and 0.57 eV [9]. Ichimura *et al.* observed two defects with activation energies of 0.34 eV and 0.52 eV [10]. All of these DLTS studies show that defects with an activation energy of about 0.3 eV are present in 3C-SiC/Si, but the energy values are slightly different among the samples. It

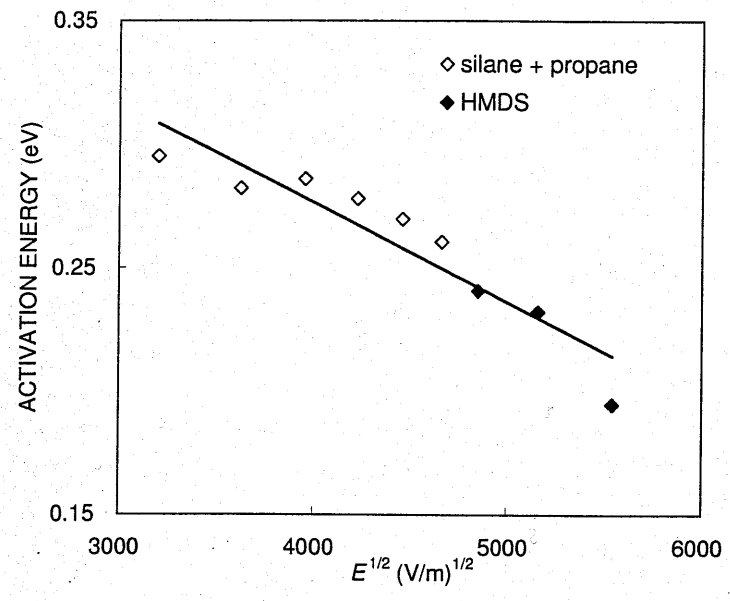

Figure 2.12: Activation energy for the defects in the HMDS2.6 and the silane B as a function of $E^{1/2}$, where E is the magnitude of the electric field.

is considered that the main cause of these differences is the electric field dependence of the carrier emission, *i.e.*, the Poole-Frenkel effect [22]. The activation energy for a donor defect decreases with increasing electric field. Figure 2.12 shows the activation energies for the defects in HMDS2.6 and the silane B against $E^{1/2}$, where E is the magnitude of the electric field. The activation energies were measured by double correlation DLTS (DDLTS) measurements for silane B. For HMDS2.6, the peaks are too small to perform the DDLTS measurements and thus the electric field averaged in the carrier emission region is adopted for the plot. There is a linear relationship between $E^{1/2}$ and activation energy for both the gas systems, and thus it is confirmed that this defect level is donor-like and influenced by the Poole-Frenkel effect. Generally, the 3C-SiC grown from silane and propane has a net donor concentration of the order of 10^{16} cm^{-3} [8–10], while that of the 3C-SiC grown from HMDS is of the order of 10^{17} cm^{-3}, which leads to the increase in the electric field in the depletion region. Thus, although the apparent activation energies for the defects are different, these defects would be identical, and hereafter we call these defects ND1. From the extrapolation of the line in Fig. 2.12, the activation energy of about 0.44 eV is obtained for the ND1 center at zero electric field.

Ichimura *et al.* have reported temperature dependence of the capture cross section for the ND1 center [10]. The capture cross section at infinite temperature, σ_∞, and capture cross section at 150 K, σ_T, for the ND1 center are 6×10^{-14} cm^2 and 2.2×10^{-17} cm^2, respectively [10]. (In that paper, an error was made in calculation of σ_∞. Although

it is given as 6×10^{-17} cm^2, it is correctly 6×10^{-14} cm^2.) In this case, it is assummed that the ND1 center has the multiphonon-emission process for the carreir capture [22]. When peak temperature is T, σ_T is given by

$$\sigma_T = \sigma_\infty \exp\left(-\frac{E_{cap}}{kT}\right), \tag{2.1}$$

where E_{cap} and k are the energy barrier of the carrier capture and the Boltzman constant, respectively. From this equation, the ND1 center has an energy barrier of the carrier capture of about 0.1 eV. Therefore, at zero electric field, the ND1 center is located at E_C-0.34 eV.

From the DLTS measurements described above, two kinds of defects were found. One was observed in the layers with less than 1.0 μm thickness and showed the broad DLTS signal in a wide temperature range. The other (ND1) was observed in the layers having more than 2.2 μm thickness. Since the former was observed only in the thin layers, it is assumed to originate from the interface. The defects at the interface can be observed by measuring the DLTS from the sample backside. Si substrates were chemically etched and contacts were evaporated on the substrate side of the sample. However Au contacts on the substrate side show ohmic characteristics as shown in Fig. 2.13 and DLTS measurements could not be performed. The substrate side of the sample should be very smooth because the epitaxial growth was carried out on the thoroughly polished Si substrates. The failure of the Schottky contact fabrication would not be due to the roughness under the contact, but defects at the heterointerface. Thus the heterointerface seems to have high density defects. The defects generated at the heterointerface can propagate into the epilayer bulk. The region measured by DLTS was about 0.04-0.06 μm from the sample surface, and thus even for the 0.65 μm thick sample it is measured only in the region >0.5 μm from the interface. The defects originating from the interface were not detected in the epilayers of more than 2.2 μm thickness, therefore they are eliminated in the region 1.0-2.2 μm from the interface. It has been reported that the density of APBs and twin boundaries generated at the interface decreases as the epilayer thickness increases [23, 24]. Generally, extended defects, such as APBs and twins, have continuously distributed energy levels. Hence the defects found in the thin layers could be extended defects. Masuda *et al.* investigated residual stress in 3C-SiC grown from HMDS by Raman spectroscopy [17]. They observed that the tensile stress decreases as the film thickness increase. This implies that the extended defect density decreases with increasing distance from the interface. Choyke *et al.* observed the G band in photoluminescence measurements for 3C-SiC/Si [25]. They described that the G band is related to dislocations and extended defects from the interface, since the G band intensity is strong at the 3C-SiC/Si interface side and weak near the surface side. This also shows that the extended defects tend to be localized near the interface. Choyke *et al.* have also reported D1 centers which appear only for over 3 μm thick 3C-SiC in photoluminescence measurements [25]. Since the film thickness dependence is similar with the ND1 center, and thus there is a possibility that the ND1 and the D1 centers are identical.

As already noted, 3C-SiC grown from HMDS has a higher net donor concentrations

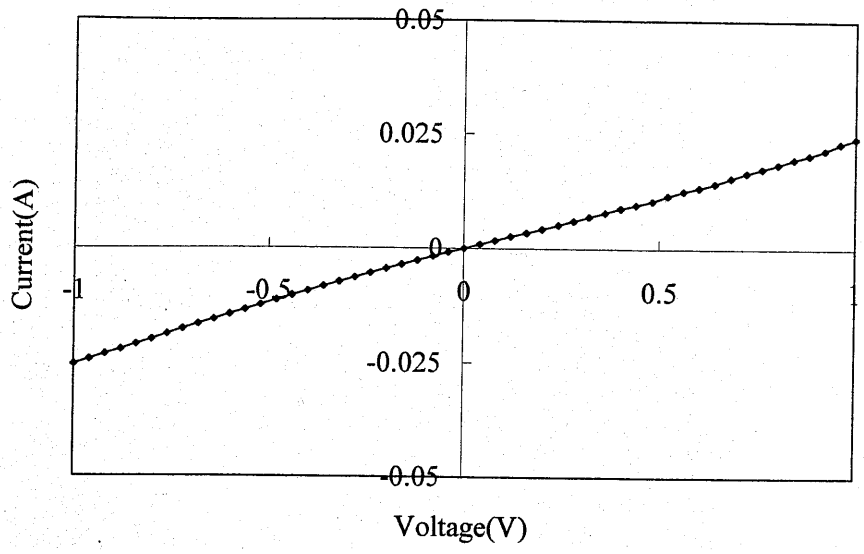

Figure 2.13: Current-Voltage characteristics for the Au contacts formed on the interface side of the sample.

than 3C-SiC grown from silane and propane. Matsuura *et al.* reported that 3C-SiC grown from HMDS has a lower donor concentration and a much lower compensation ratio of about 0.03 than that of 3C-SiC grown from silane and propane, as determined by Hall measurement data [26]. For 3C-SiC grown from silane and propane, the compensation ratio is about 0.9 [27, 28]. Matsuura *et al.* noted that the lower compensation ratio for 3C-SiC grown from HMDS leads to the higher net donor concentration, and they concluded that 3C-SiC grown from HMDS has better crystalline quality [26]. However, the ND1 centers are present in 3C-SiC grown from HMDS at one order of magnitude higher concentration, as listed in Table 2.3. Thus, it is difficult to say which crystals grown from those two gas systems have lower defects density.

2.3.3 O-CTS measurements for 3C-SiC grown from silane and propane

O-CTS measurements were performed to the silane B in order to clarify the energy level structure of the peak around 150 K (the ND1 center) in the DLTS spectrum and to detect more deep levels by optical excitation. In the DLTS spectrum for silane B, there are peaks for the ND1 center and broad peak around 340 K, which results from overlap of a large number of peaks with activation energy of 0.35-0.75 eV. The O-CTS

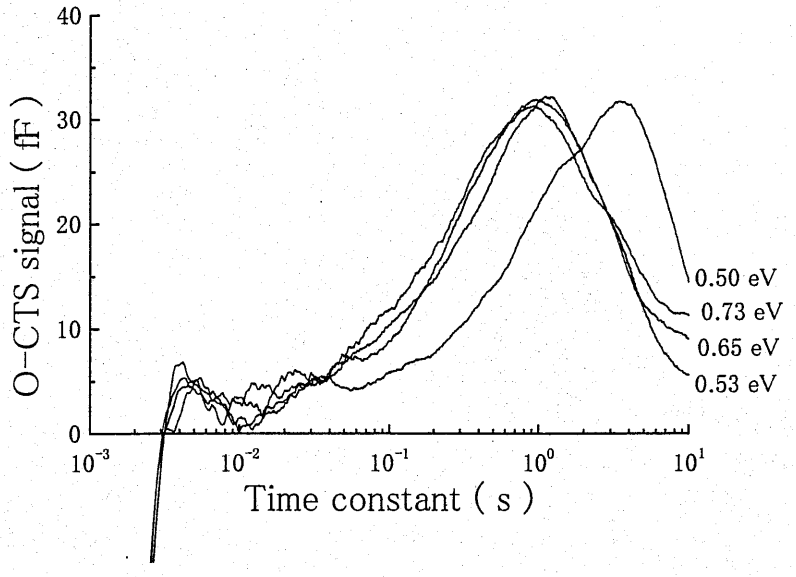

Figure 2.14: O-CTS spectra for the silane B with 0.50-0.73 eV photon energy at 90 K. (Photon flux is 2×10^{15} $cm^{-2}s^{-1}$.)

measurements for the silane B at measurement temperature of 90 K with 0.50-0.73 eV photon energy were performed in order to observe optical excitation of electrons from the ND1 center as shown in Fig. 2.14. With 0.5 eV illumination, a peak is observed around time constant of 3 s. This peak has the same height as the peak observed near 150 K in the DLTS spectrum. Thus the peak observed in the O-CTS spectrum with 0.5 eV illumination is identical with the peak around 150 K in the DLTS spectrum, which originates from the ND1 center. With 0.54 eV illumination, the time constant of the peak becomes small. This means an increase in optical cross section for the ND1 center.

Figure 2.15 shows O-CTS spectra in the range of 0.73-2.1 eV. The photon flux is constant for all the spectra in Fig. 2.15 but is different from that adopted in Fig. 2.14. With 0.73 eV illumination, the peak around 0.4 s is caused by the ND1 center. With increasing photon energy, the time constant of the peak increases.

From these results, the optical cross section for the ND1 center is plotted in Fig. 2.16. The optical cross section for the ND1 center increases with increasing photon energy up to 0.6 eV and then decreases with increasing photon energy at higher photon energy. The apparent photoionization threshold energy is about 0.47 eV as shown in Fig. 2.16.

The ND1 center has a thermal activation energy of 0.44 eV at zero electric field, and the capture barrier is about 0.1 eV as discussed in section 2.3.2. Therefore the ND1 center has an energy level of 0.34 eV from the conduction band edge. On the basis of the

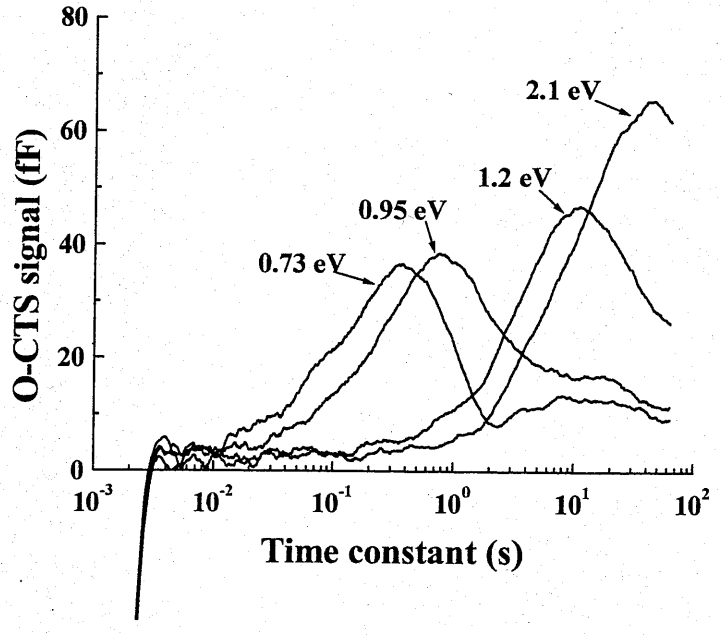

Figure 2.15: O-CTS spectra for the silane B with 0.73-2.1 eV photon energy at 90 K. (Photon flux is 6×10^{15} $cm^{-2}s^{-1}$.)

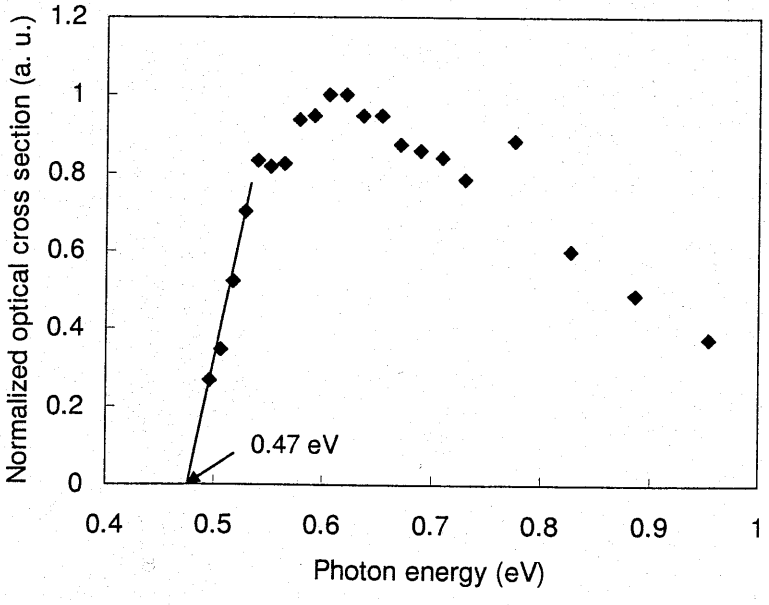

Figure 2.16: Optical cross section for the ND1 center.

results described above, the configuration coordinate diagram is drawn in Fig. 2.17 [29]. From this figure, the Franck-Condon shift, which indicates strength of the interaction between an electron and the lattice around the defect, d_{FC} of 0.13 eV is deduced.

With 0.73 eV illumination, a broad peak was observed at time constant of around 10 s as shown in Fig. 2.15. The broad peak is the overlap of a number of the small peaks with optical threshold energies of less than 0.73 eV. In the DLTS spectrum (Fig. 2.2), the peak with activation energy below 0.73 eV is only the broad peak around room temperature, and thus the peak observed at time constant of 10 s would be identical with the broad peak around room temperature in the DLTS spectrum. With 2.1 eV illumination, a peak with larger intensity than the ND1 center is observed at 30 s. Comparison of this peak with theoretical curve reveals that this peak is broader than normal single peak. Therefore another peak is overlapping the peak due to the ND1 center, to result in the large broad peak. For investigation of this overlapping peak, we performed O-CTS measurements at 180 K at which the ND1 center is thermally ionized at very short time constant and thus the other peak is separated from the ND1 center peak, as shown in Fig. 2.18. From this figure, the signal observed at less than 10^{-2} s is caused by thermal excitation from the ND1 center, and time constant of this peak does not change with photon energy. Without illumination, no peaks are observed except for the ND1 center. With 1.4 eV illumination, the shoulder of the peak appears at time constant of 50 s. With increasing photon energy this peak becomes intense and its time constant becomes short. With 2.1 eV illumination, the broad peak is observed at about 20 s.

Figure 2.19 shows sum of this broad peak and the theoretical curve for the ND1 center at time constant of 40 s along with the O-CTS spectrum at 85 K with 2.1 eV illumination. Both the curves agree very well and thus, the large peak observed at 85 K with 2.1 eV illumination is, in fact, due to overlap of the two peaks. The optical threshold energy for the deeper level is roughly estimated to be around 1.4 eV from Fig. 2.18.

2.4 Conclusion

Deep levels in 3C-SiC grown from two gas systems were observed by DLTS, CTS and O-CTS methods. 3C-SiC grown from silane and propane have defects with an activation energy of about 0.3 eV and with distributed activation energies of 0.35-0.75 eV. No deep level with activation energy from 0.75 eV to 1.0 eV is observed in the samples, if capture cross section was assumed at 10^{-16} cm^2.

3C-SiC grown from HMDS have two kinds of defects. The one is observed in thinner 3C-SiC samples (<1.0 μm) and it has widely distributed activation energies. This defect would originate from the heterointerface of 3C-SiC/Si. The other is observed in thicker 3C-SiC samples (>2.2 μm). This defect has an activation energy of about 0.25 eV, and it is a donor-like defect. This is the same defect observed in the 3C-SiC grown from silane and propane with an activation energy of about 0.3 eV and is named ND1. The ND1 center would have an activation energy of 0.44 eV in the absence of an electric

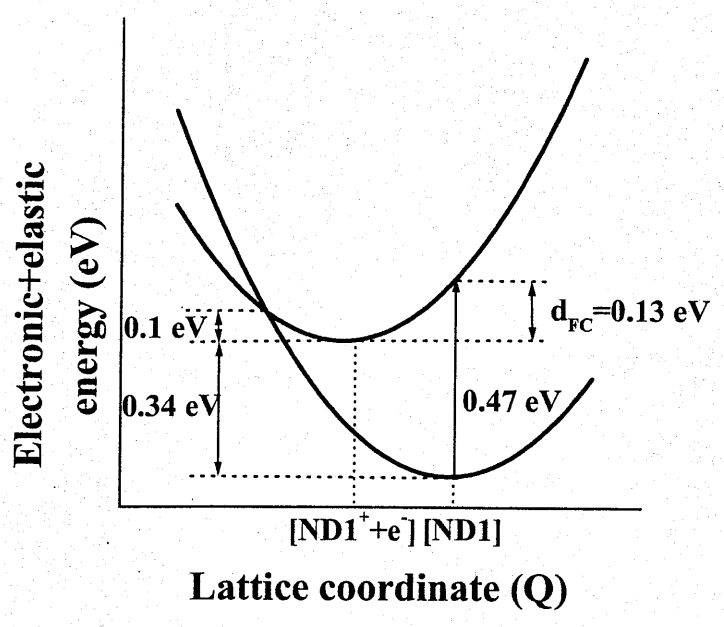

Figure 2.17: The configuration coordinate diagram for the ND1 center.

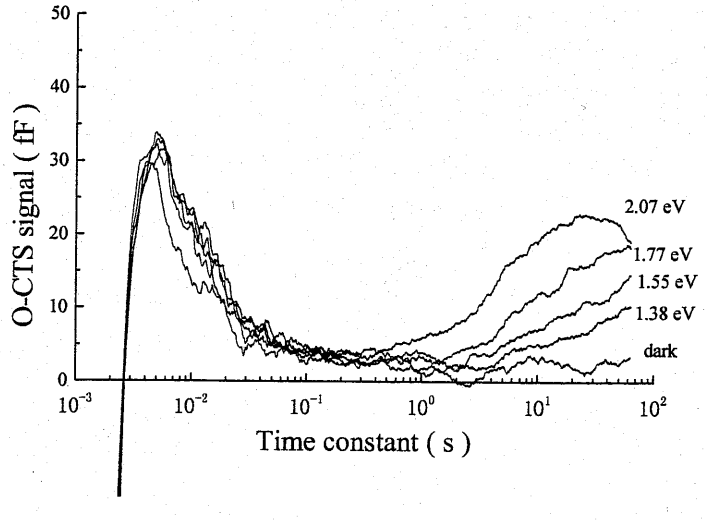

Figure 2.18: O-CTS spectra at 180 K. (Photon flux is 6×10^{15} $cm^{-2}s^{-1}$.)

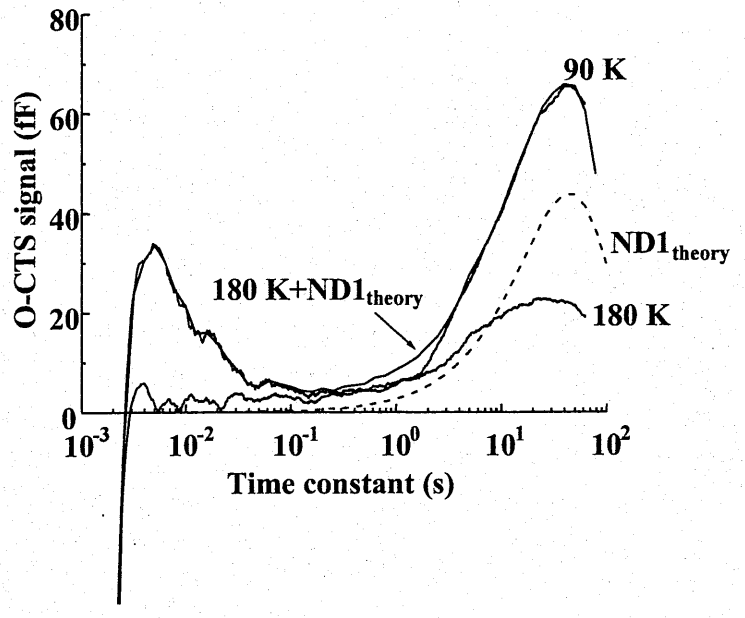

Figure 2.19: Comparison of the O-CTS spectra at 90 K with 2.1 eV and sum of theoretical curve and the O-CTS spectrum at 180 K.

field. Since an energy barrier for the carrier capture of the ND1 center is about 0.1 eV, the ND1 center is located at E_C-0.34 eV in the band gap.

O-CTS measurements reveal the configuration coordinate diagram of the ND1 center. The ND1 center has an optical threshold energy of 0.47 eV and it has an activation energy of 0.44 eV and an energy barrier for the carrier capture of 0.1 eV. Thus the Frank-Condon shift for the ND1 center is 0.13 eV. In addition, it is revealed that there are deeper level defects which have optical threshold energy of around 1.4 eV in 3C-SiC grown from silane and propane, even though there is no deep level with activation energy of 0.75-1.0 eV.

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Chapter 3

Passivation of Deep Levels in 3C-SiC

3.1 Introduction

3C-SiC on Si has a large number of defects originated from the 3C-SiC/Si heterointerface. If the defects are electrically active, they cause negative effects on device operation. Thus the electrically active defects must be decreased in practical devices. Hydrogen is known to be able to passivate donor, acceptor and electrically active defects [1]. A few works for passivation of donor and acceptor in SiC have been reported [2–4], and H^+ implantation effects for SiC have been investigated by photoluminescence [5–7]. However passivation of deep levels in SiC has never been reported. The purpose of this work is to passivate electrically active defects in 3C-SiC on Si by hydrogen. Hydrogen would be incorporated into crystals by several methods, *e.g.*, hydrogen plasma treatment, ion implantation and annealing in hydrogen ambient. In this work, it is attempted to introduce hydrogen into 3C-SiC by the hydrogen plasma treatment. This hydrogen plasma would introduce hydrogen and damages simultaneously at the sample surface. The damages are caused by bombardment of high-energy ions into the sample during the treatment, and they should be reduced for practical use of this method. In order to reduce the damages, a grid is inserted between the sample and the plasma source. The grid can suppress the ion flux reaching the sample surface. Effects of the hydrogen plasma treatment with grid are observed by DLTS. Then the results are compared with those for the sample treated without the grid.

3.2 Experiment

A sample used in this work is the same as the silane B described in the previous chapter. The sample was cut into two pieces, and they were characterized by C-V and DLTS measurements before the plasma treatments. For these measurements, Schottky diodes were fabricated on each sample by evaporating Au and Al for the Schottky and ohmic contacts, respectively. All of the diodes showed almost the same carrier concentrations of

about 4×10^{16} cm^{-3} and almost the same DLTS spectra. After removal of the electrodes, one of the sample was treated by hydrogen plasma without a grid. Another sample was treated by hydrogen plasma with the grid. Both the hydrogen plasma treatments were performed for 2 hours at a substrate temperature of 300°C in a remote RF plasma system (0.3 Torr, 50 W RF power). The grid was inserted 5 cm away from the sample and the sample and the grid bias were 0 V. Then the electrodes were formed on the samples and the C-V and DLTS measurements were performed once again. After that, the samples were annealed under N_2 flow for 1 hour at several temperatures (300, 400, 500, 600 and 700°C; 300°C annealing is only for the sample treated with the grid, while 700°C annealing is only for the sample treated without the grid). The electrodes were removed prior to each annealing step, and they were formed after each annealing step. The DLTS and C-V measurements were performed at each step.

3.3 Results

Figure 3.1 shows the DLTS spectrum for the sample. All of DLTS spectra in this chapter are for a time constant of 38 ms. Measurement region is 0.07-0.14 μm and peaks are detected around 150 K and 300 K. The peak around 150 K corresponds to a defect having an activation energy of 0.31 eV and is named the ND1 center in the previous chapter. The concentration of the ND1 center varies within 2-9$\times10^{14}$ cm^{-3} from sample to sample, and it has homogeneous depth profile. The peak around 300 K is broad and some of the diodes do not show this peak. Therefore, defect parameters for this peak are not estimated, but it is supposed from the peak temperature position that this peak has an activation energy of 0.5-0.7 eV.

Figure 3.2 shows the DLTS spectra for the sample treated by hydrogen plasma with and without the grid. The injection and emission bias are 0 V and -1 V, respectively, and the corresponding measured region is about 0.07-0.14 μm from the sample surfaces. The spectrum for the sample treated without the grid has a very broad peak around 200-300 K. This peak would consist of many peaks with different temperature positions. Thus, several energy levels are formed by the hydrogen plasma. The spectrum for the sample treated with the grid has only one peak around 330 K. Parameters for the peak are extracted from the Arrhenius plot, and the activation energy for the peak is 0.77 eV. Distribution of this peak is localized at very near surface region (shallower than 0.08 μm from surface), and by taking into account of this localization the concentration of this peak is larger than 3×10^{15} cm^{-3}. These peaks observed in both the samples are caused by damages of the plasma treatments, because these peaks do not appear in the spectrum for the as-grown sample. Figure 3.2 clearly shows that the grid decreases the damages at the sample surface. Trap parameters for the peaks in the sample treated with the grid are listed in Table 3.1.

Figure 3.3 shows the DLTS spectra for an about 0.15-0.18 μm region of the sample treated by hydrogen plasma with and without the grid. The bias conditions are -1 V and -2 V for injection and emission bias, respectively. As shown in this figure, both the spectra show no peak in the entire temperature range. This indicates that in both the

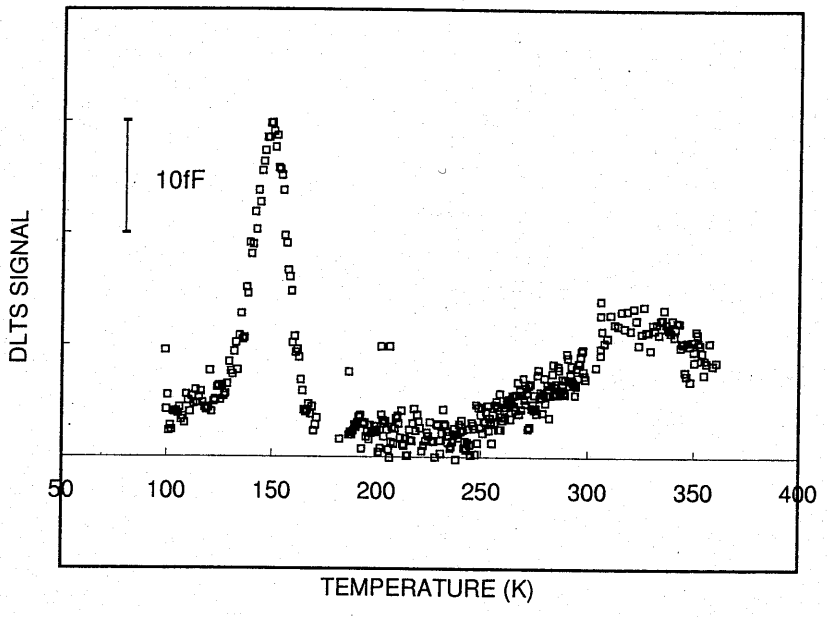

Figure 3.1: DLTS spectrum for the as-grown 3C-SiC (silane B).

Table 3.1: Trap parameter for the peaks from 3C-SiC treated by hydrogen plasma with the grid.

Peak position	150 K (ND1)	260 K	330 K
Activation energy (eV)	0.31	0.68	0.77
Capture cross section at infinite temperature (cm^2)	1.6×10^{-14}	6.6×10^{-13}	1.8×10^{-13}

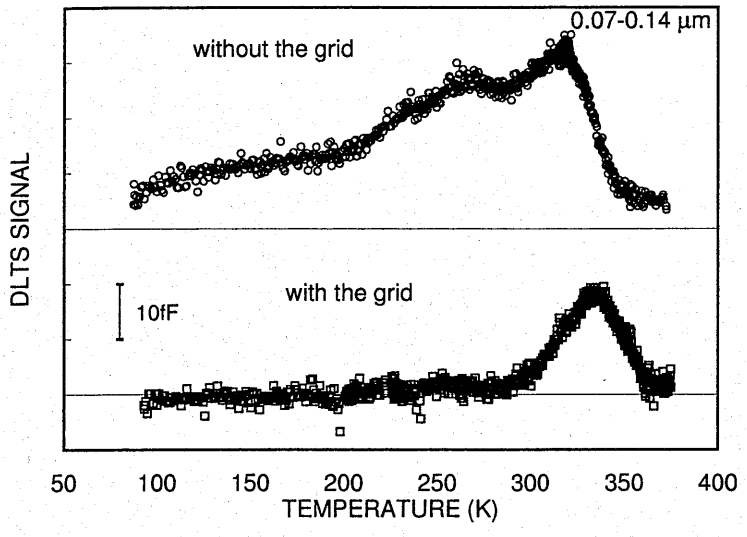

Figure 3.2: DLTS spectra for the 0.07-0.14 μm depth region of the hydrogen plasma treated 3C-SiC with and without a grid.

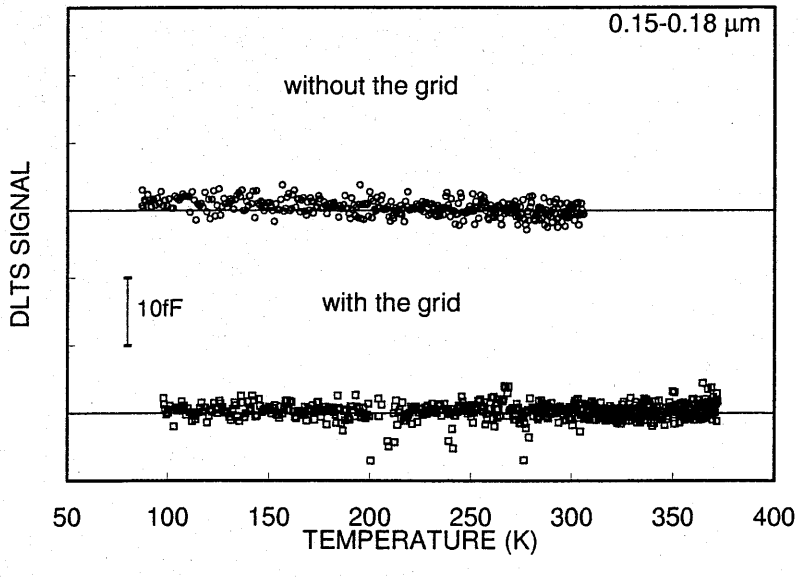

Figure 3.3: DLTS spectra for the 0.15-0.18 μm depth region of the hydrogen plasma treated 3C-SiC with and without the grid.

samples, hydrogen passivates the deep levels observed in the as-grown sample, and no damages exist in the region more than 0.14 μm away from the sample surfaces.

In order to investigate thermal stability of hydrogen passivation and to anneal out the damages, the samples were annealed at several temperatures. Figure 3.4 shows DLTS spectra for the sample treated without the grid at each annealing step. The measured regions are about 0.07-0.14 μm from the sample surface for all the spectra. The spectrum for the 400°C annealed sample has two weak peaks around 150 K and 230 K, and the broad peak observed for the as-treated sample disappears. Thus the plasma damages causing the broad peak were annealed out. Parameters for the peaks around 150 K and 230 K cannot be obtained from the Arrhenius plot due to their weak intensities, but from the peak position, the peak around 150 K is the ND1 center observed in the as-grown sample. Therefore, by 400°C annealing, some hydrogen atoms which passivated the ND1 center become free, and some of the ND1 centers are re-activated. The spectrum for the 500°C annealed sample exhibits the same peaks as observed for the 400°C annealed sample, and their intensities are larger than for the 400°C annealed sample. This indicates that more hydrogen atoms bonded to the ND1 center go away from the defect sites and more ND1 centers are re-activated. The spectrum for the 600°C annealed sample shows so a intense peak around 260 K that the spectrum is shown in a reduced scale. Since an intensity of the peak around 150 K is almost the same as that for the 500°C annealed sample, the ND1 centers are almost completely re-activated at 500°C annealing. The peak around 230 K observed at the 500°C annealed sample may be hidden by a very large peak around 260 K. Annealing at 700°C for the sample is also performed, but the spectrum does not exhibit any change from that for the 600°C annealed sample (not shown). All of hydrogen atoms seem to be out-diffused at the 600°C annealing. Double correlation DLTS (DDLTS) measurements were performed for the ND1 center and the peak around 260 K. The ND1 center shows electric field dependence for the emission rate as described in the previous chapter, while the peak around 260 K shows no electric field dependence for the emission rate. Thus the ND1 center is donor-like, but the peak around 260 K is acceptor-like.

Figure 3.5 shows the DLTS spectra for the deeper (about 0.15-0.18 μm) region of the sample treated without the grid at each annealing step. The spectrum for the 400°C annealed sample shows only a very faint peak around 150 K. In this region, most of the ND1 centers are passivated by hydrogen and no peaks from the damages are observed. On the other hand, the spectrum for the 500°C annealed sample shows a peak from ND1 center with almost the same intensity as observed in the as-grown sample. At this temperature, the ND1 centers are completely re-activated in this region. The spectrum for the 600°C annealed sample shows the ND1 peak and a small peak around 260 K, which is considered to be the same peak as observed in the 0.07-0.14 μm region of this sample.

Figure 3.6 shows the DLTS spectra for the sample treated with the grid at each annealing step. The measured regions are about 0.05-0.15 μm from the sample surface. The spectrum for the sample annealed at 300°C shows a very weak peak around 230 K. Although the parameters for this peak cannot be obtained owing to its weak intensity, it is considered that this peak is the same as that observed for the sample treated without

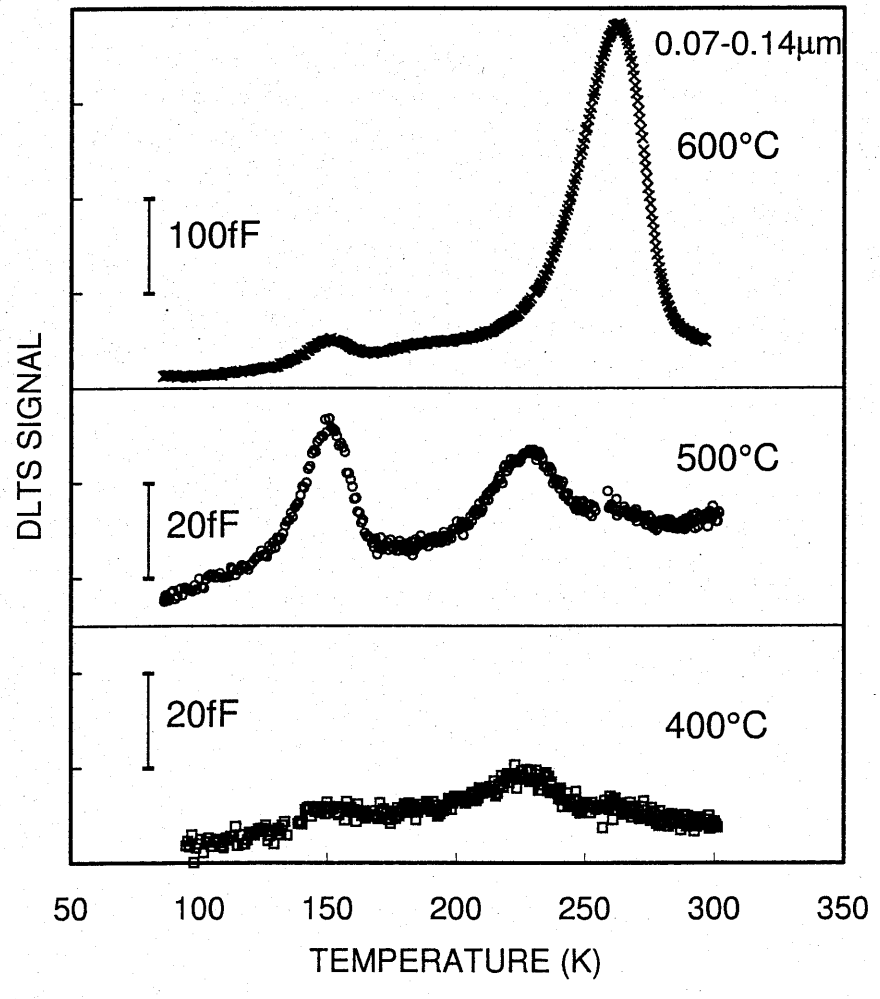

Figure 3.4: DLTS spectra for the 3C-SiC after the hydrogen plasma treatment without the grid and several annealing steps. (Note that an intensity of the spectrum for after 600°C annealed sample is reduced to 1/5.)

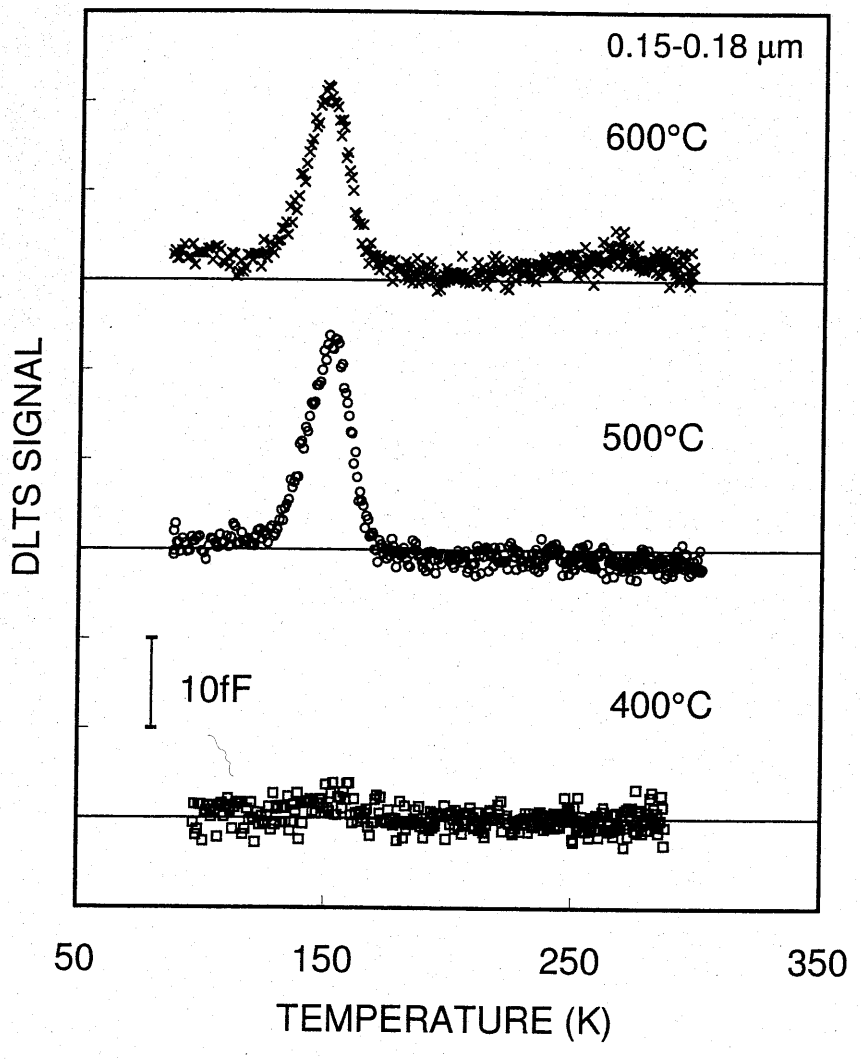

Figure 3.5: DLTS spectra for the 0.15-0.18 μm depth region of the 3C-SiC after the hydrogen plasma treatment without the grid and several annealing steps.

the grid and annealed at 400°C and 500°C. The trap concentration for this peak is less than 10^{14} cm^{-3}. The spectrum for the sample annealed at 400°C shows two weak peaks around 150 K and 230 K. The intensity of the peak around 230 K remains similar to that for a previous annealing step. On the other hand, some of the ND1 centers are re-activated at this temperature annealing, as for the sample treated without the grid. In the spectrum for the sample annealed at 500°C, the ND1 center seems to be almost completely re-activated. The peak around 230 K has twice larger intensity than that for a previous annealing step, and a new very weak peak is found around 270 K. However, the peaks around 230-270 K are not so intense compared with the sample treated without the grid. The spectrum for the sample annealed at 600°C shows peaks around 150 K and 260 K. The peak intensity for the ND1 center remains the same as that for a previous annealing step, while the peak around 260 K becomes as intense as the peak for the ND1 center. The intensity of the 260 K peak shows prominent difference from the sample treated by hydrogen plasma without the grid and annealed at 600°C. The reliable defect density for this peak cannot be obtained due to localization of the defect as well as the peak around 330 K observed in the 300°C annealed sample, but the peak intensity is 6 times smaller than that for the sample treated without the grid. This clearly shows that the grid greatly reduces concentration of this defect.

Figure 3.7 shows the DLTS spectra for the about 0.15-0.20 μm region of the sample treated with the grid and annealed at each temperature. The 300°C annealed sample shows no DLTS peaks in this region. Re-activation of the defects does not occur at this temperature annealing. In the spectrum for the 400°C annealed sample, a weak peak is observed around 150 K. This indicates that some ND1 centers are re-activated at this temperature. The DLTS spectrum for the sample annealed at 500°C exhibits one peak around 150 K, and the DLTS spectrum for the sample annealed at 600°C shows a peak around 150 K and a faint peak around 260 K. The ND1 centers are completely re-activated by above 500°C annealing. These results are almost the same as the DLTS spectrum for the similar region (0.15-0.18 μm) of the sample treated without the grid.

Two types of new defects are detected in the sample treated by hydrogen plasma. One is observed just after the hydrogen plasma treatment (the broad peak around 200-330 K), and the other is observed after the subsequent annealing above 500°C (the peaks around 220-270 K). The as-treated sample without the grid shows a very broad peak. For the sample treated with the grid, some parts of this broad signal do not appear, and thus the grid suppresses the damages related to this peak. The damages of the plasma treatment are created by bombardments of high-energy particles to the crystal lattice. Therefore the defects formed are expected to be intrinsic-type defects, such as C vacancy V_C, Si vacancy V_{Si}, dislocations or hydrogen related defects. This broad peak is annealed out at 300°C or 400°C. This low annealing temperature suggests that this broad peak is originated from simple point defects or hydrogen related defects. Itoh *et al.* have reported that V_C in 3C-SiC is annealed at 300°C [8], and theoretical studies have shown that V_C acts as a donor at E_C-0.8 eV [9, 10]. This annealing behaviour and the energy state are similar to the peak observed at 330 K just after the plasma treatment with the grid, and thus this peak could be assigned to V_C. The peaks around 260 K observed in both over 500°C annealed samples are also caused by the plasma

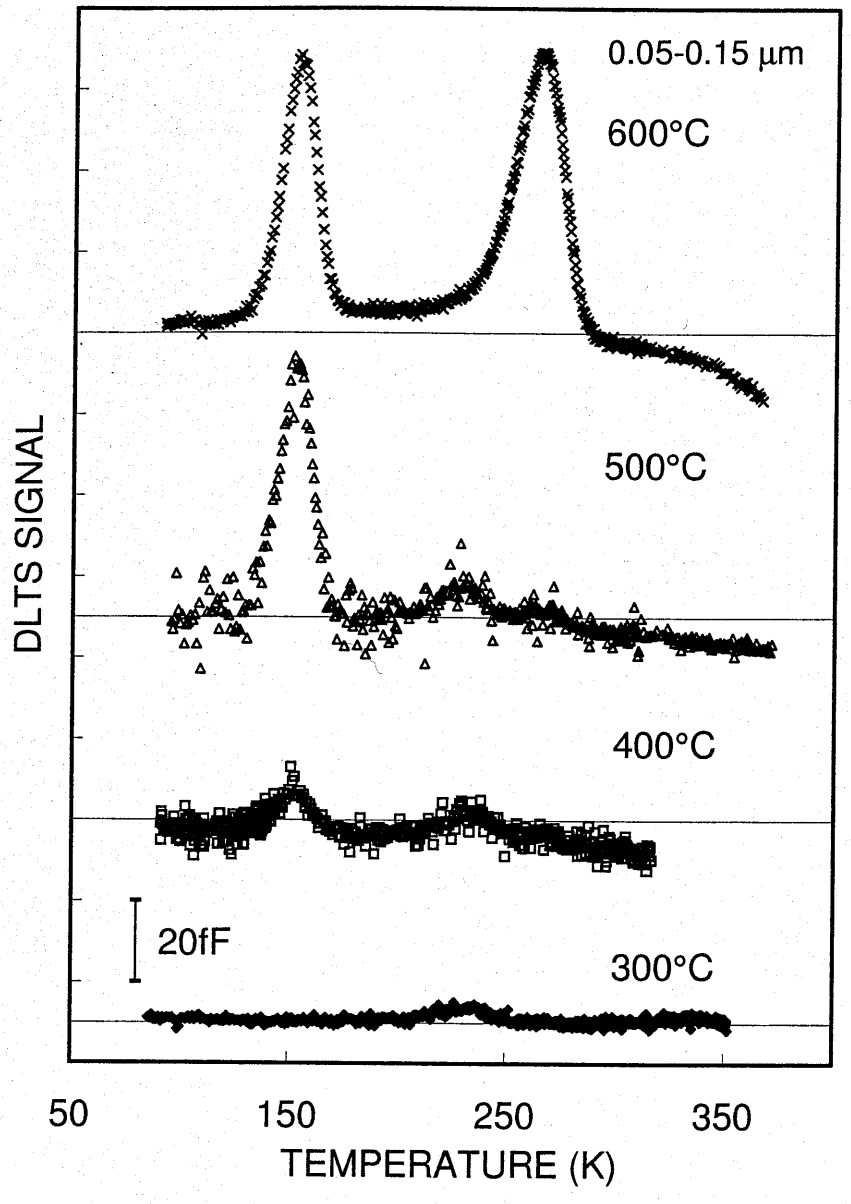

Figure 3.6: DLTS spectra for the 3C-SiC after the hydrogen plasma treatment with the grid and several annealing steps.

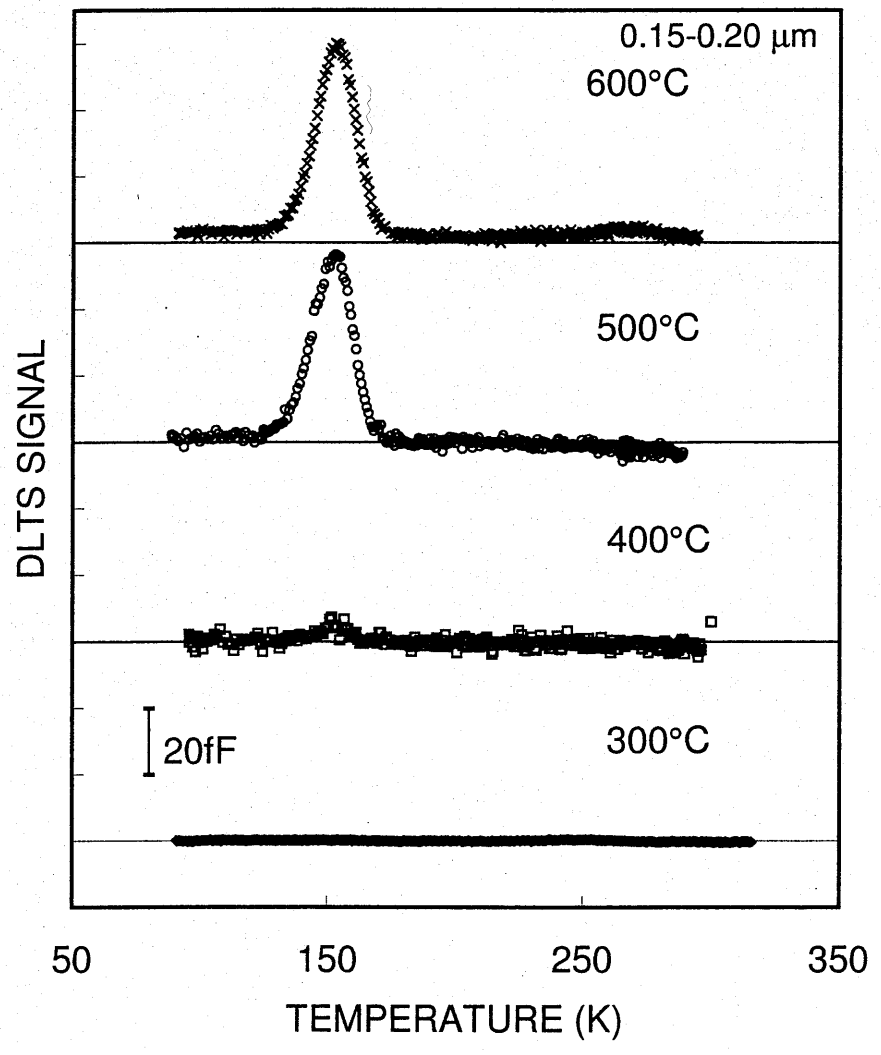

Figure 3.7: DLTS spectra for the 0.15-0.18 μm depth region of the 3C-SiC after the hydrogen plasma treatment with the grid and several annealing steps.

damages. Since the hydrogen plasma treatment would make a large number of point defects, the 260 K peak can be assigned to complex defects. As can be seen from Figs. 3.4 and 3.6, the grid greatly reduces this peak intensity.

The concentration of the ND1 center returned to the initial value after the treatment and subsequent annealing over 500°C. As mentioned above, the plasma treatment would form many intrinsic-type defects and apparently these defects do not interact with the ND1 center. It is speculated that the ND1 center includes some impurities so that its concentration is not affected by the intrinsic defects. Aboelfotoh *et al.* have reported that deuterium implantation does not have any effects on deep levels [11]. They have observed deep levels immediately after this implantation and after subsequent annealing at 800°C. Thus, the deep levels in their samples seem different from the ND1 center, which are passivated by hydrogen. Since they argue that their observed defects are a Si vacancy and C vacancies, the ND1 center seems not to be these simple vacancy, which does not conflict with the speculation described above.

It has been reported that V_{Si} + H complex in 3C-SiC is amphoteric and has energy levels of 0.32 (+/0) and 0.66 (0/-) eV above the top of the valence band from a theoretical calculation [12]. In this study, n-type sample was used so that these levels could not be observed.

The samples show net donor concentrations of about 4×10^{16} cm^{-3} independent of the treatment. This indicates that hydrogen does not passivate shallow donor levels. This result is consistent with deuterium passivation effects for 6H-SiC reported by Achtziger *et al.* [2], who have reported that deuterium passivates only acceptors, not donors.

3.4 Conclusion

Hydrogen was introduced into 3C-SiC by plasma treatments, and the effects of hydrogen were investigated by DLTS measurements. DLTS results indicated that hydrogen passivates deep centers in the as-grown sample, and that the treatment forms damages at the sample surface region. By inserting a grid between the sample and the plasma source, the damages were reduced retaining the passivation effects. The defect concentration is less than 10^{14} cm^{-3} for the sample treated by the hydrogen plasma with the grid and subsequently annealed at 300°C.

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Chapter 4

Deep Level Observation in Hexagonal SiC

4.1 Introduction

Generally, hexagonal SiC epitaxial layers are grown on SiC (0001) Si face substrates with inclination toward $< 11\bar{2}0 >$ direction. Epitaxial growth on the inclined substrates proceeds in the step-flow mode so that high quality epitaxial layers are obtained at a relatively low growth temperature, 1500-1600°C [1–8]. In the 6H-SiC growth, the inclined direction is important, since it has been reported that epitaxial growth on (0001) Si substrates with inclination toward $< 1\bar{1}00 >$ causes poorer crystalline quality than the substrates with inclination toward $< 11\bar{2}0 >$ direction. On the contrary, recent studies show that, in the 4H-SiC case, epitaxial growth on the substrates with inclination toward $< 1\bar{1}00 >$ direction produces the same good quality films as the films on the substrates with inclination toward $< 11\bar{2}0 >$ direction [9, 10]. In this study, deep level defects in epitaxial films grown on the substrates inclined toward these two directions are compared by DLTS.

4.2 Experiment

4H-SiC (0001) Si face polished substrates with inclination toward $< 11\bar{2}0 >$ and $< 1\bar{1}00 >$ by 8 degree were purchased from Sterling Semiconductor Inc. 4H-SiC epilayers were grown on the substrates by the cold wall chemical vapor deposition method in atmospheric pressure. Source gases were Si_2Cl_6 and C_3H_8 with H_2 carrier gas, and growth temperature was 1550°C. Si/C ratio for source gases is approximately 0.1. Before the growth, the substrates were etched by HCl at 1300°C. 6 and 20 μm thick 4H-SiC epitaxial film pairs were grown. The each pair was simultaneously grown in a furnace in order to avoid fluctuation from run to run. At the growth, 6H-SiC epilayer was also grown simultaneously on 6H-SiC (0001) Si face substrate with inclination toward $< 11\bar{2}0 >$ by 3.5 degree, in order to see the difference between 6H-SiC and 4H-SiC. Morphology of these samples was reported in ref. [10]. After the growth, Ni was evaporated on the C

face of the samples and the samples were annealed in order to form ohmic contacts. Au was evaporated on the epitaxial layer surface as the Schottky contacts. Using these contacts, current voltage (I-V), capacitance voltage (C-V) and DLTS measurements were performed. The DLTS measurements were done with reverse bias of -1.0 V and injection bias of 0 V which corresponds to measurement region of less than 1 μm from the epilayer surface. All the DLTS spectra shown in this paper are for time constant of 38 ms.

4.3 Results

From C-V measurements, all the samples have net donor concentrations of 2-4$\times 10^{15}$ cm^{-3}. The concentrations were constant within the observed region (<2 μm) from the surface for all the samples. Figure 4.1 shows DLTS spectra for the 4H-SiC sample pair with 6 μm thickness. The two spectra are similar except for a temperature range above 550 K. The spectrum for the sample with inclination toward $< 11\bar{2}0 >$ shows four peaks below 550 K and large signal above 550 K. On the other hand, the spectrum for the sample with inclination toward $< 1\bar{1}00 >$ shows six peaks. Peak positions for both the spectra are almost the same and the peak around 250-300 K is broad in both the spectra. Activation energies for the peaks are listed in Table 4.1. Calculated deep level concentrations for all the peaks are below 2×10^{13} cm^{-3} for both the samples. The parameters for the large signal above 550 K in the spectrum for the sample with inclination toward $< 11\bar{2}0 >$ cannot be estimated, but it is expected that it originates from high concentration (>10^{13} cm^{-3}) of deep levels.

Figure 4.2 shows DLTS spectra for the 4H-SiC sample pair with 20 μm thickness. In these spectra, peak positions are similar to the spectra for the 6 μm thick samples. However, it can be seen from peak height that concentrations of the deep levels are obviously smaller than those in 6 μm thick samples. All of the peaks correspond to deep level concentrations below 3×10^{12} cm^{-3}. From the above two figures, defect activation energies and concentrations seem not to depend on the substrate inclined direction, but the defect concentration depends on the epilayer thickness.

Sum of the deep level concentrations for each sample along with net donor concentrations were plotted in Fig. 4.3. For the 4H-SiC 6 μm thick sample with inclination toward $< 11\bar{2}0 >$, the large signal above 550 K was not included in the summation, and thus the actual total defect concentration is larger than plotted in Fig. 4.3, as indicated by the arrow. From this figure, in each 4H-SiC sample pair with the same thickness, defect concentrations for the sample with inclination toward $< 1\bar{1}00 >$ seems to have lower defect concentration than those for the sample with inclination toward $< 11\bar{2}0 >$. However, the difference is too small to prove the inclined direction dependence conclusively. The 20 μm thick sample pair has lower total deep level concentrations than the 6 μm thick sample pair. Thus the defect concentration strongly depends on the epilayer thickness rather than on the substrate inclined direction.

The 20 μm thick 6H-SiC sample with inclination toward $< 11\bar{2}0 >$ was also investigated by DLTS. A DLTS spectrum for this sample is shown in Fig. 4.4. For comparison,

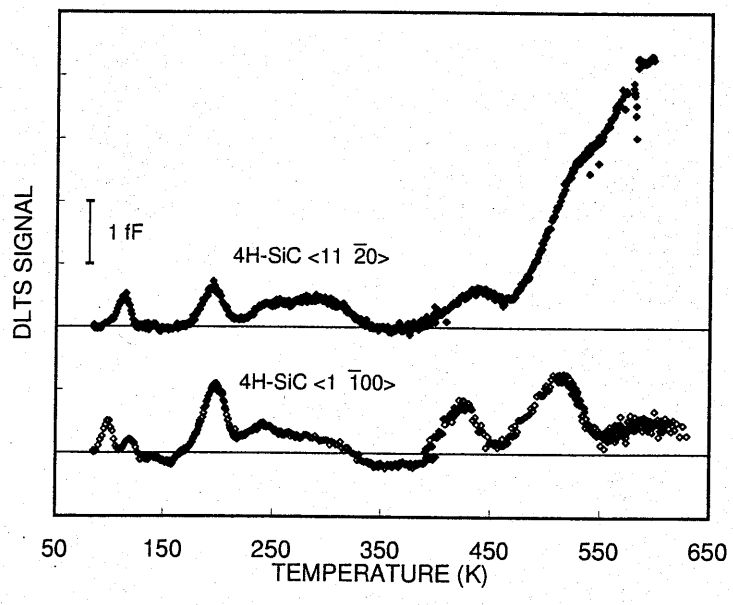

Figure 4.1: DLTS spectra for the 4H-SiC sample pair with 6 μm thickness.

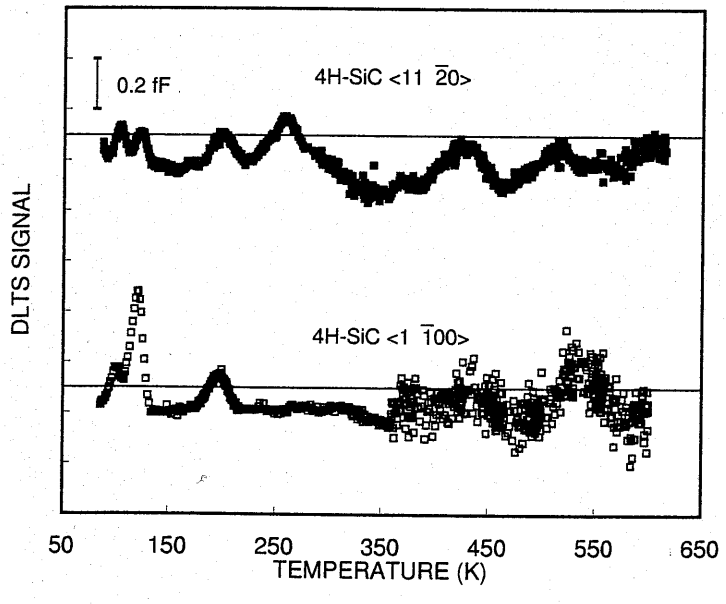

Figure 4.2: DLTS spectra for the 4H-SiC sample pair with 20 μm thickness.

Table 4.1: Activation energy for the deep levels in 4H-SiC epilayers. ("NE" means that although the peak is observed, the activation energy cannot be evaluated. "-" means that the peak is not observed.)

Approximate peak temperature	Sample condition				Correspondence to published data [11]
	< 1120 > 6 μm	< 1100 > 6 μm	< 1120 > 20 μm	< 1100 > 20 μm	
100 K	-	0.15 eV	0.23 eV	0.14 eV	ID_1
120 K	0.18 eV	0.22 eV	0.22 eV	0.18 eV	P_1/P_2
200 K	0.34 eV	0.33 eV	0.35 eV	0.38 eV	P_3
260 K	NE	NE	NE	-	
430 K	1.2 eV	1.0 eV	0.99 eV	NE	RD_1
500 K	NE	0.95 eV	1.0 eV	NE	RD_2

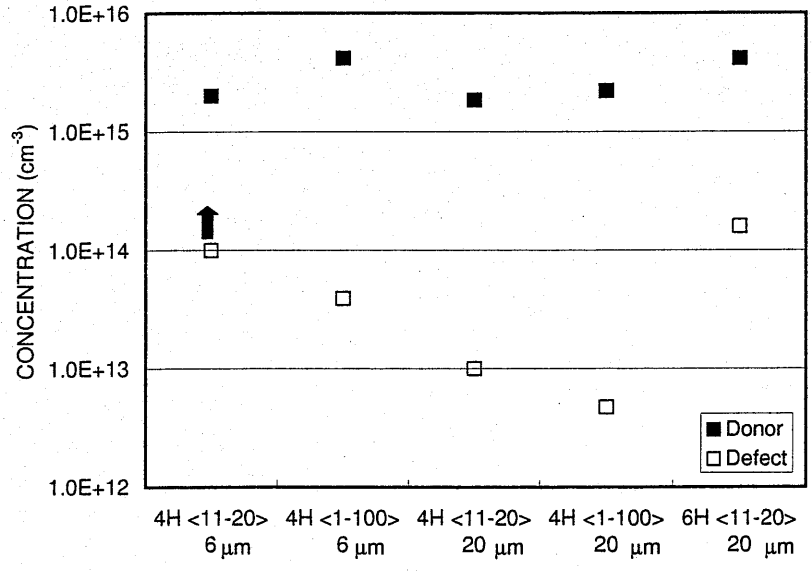

Figure 4.3: Sum of the deep level concentrations and net donor concentrations.

the DLTS spectrum for the 20 μm thick 4H-SiC sample with inclination toward $< 11\bar{2}0 >$ is also shown in Fig. 4.4. This figure shows a clear difference between these two spectra. The spectrum for the 6H-SiC sample shows three large peaks. From the activation energies deduced from an Arrhenius plot, the peak at the lowest temperature is considered as the E_1/E_2 center and the peak at the highest temperature is considered as the R center observed in ref. [11]. The defect concentrations are of the order of 10^{13} cm^{-3}, which is one order of magnitude higher than the deep level concentrations in the 4H-SiC samples. Both the samples were grown simultaneously in the furnace and have the same substrate inclined direction. Thus it is concluded that the higher concentration is due to the polytype difference.

Schottky barrier height and leakage current at reverse bias of 20 V were evaluated by C-V and I-V measurements, respectively. The results are shown in Fig. 4.5. The data were taken from 5-15 Schottky contacts for each sample. Average, minimum and maximum values are plotted in this figure. The barrier height and leakage current seem to have relation with the defect concentration shown in Fig. 4.3. The sample with a higher defect concentration shows a lower Schottky barrier height except for the 6H-SiC sample. Although the leakage current values are scattered, the sample with a higher defect concentration tends to have a higher averaged leakage current value. The sample with a high defect concentration may have high density of surface states. The surface states would pin the surface Fermi level near the conduction band, reduce the barrier height, and increase the leakage current.

Finally, it is compared the DLTS peaks observed in these 4H-SiC samples with DLTS peaks reported so far. The Z_1 center (now it is called $Z_{1/2}$ after the observation of two peaks in DLTS signal followed by optical excitation [12]) with an activation energy of 0.63-0.68 eV has been observed in as-grown epitaxial 4H-SiC samples [11, 13]. It has been reported that the $Z_{1/2}$ center originates from a silicon vacancy-related defect [14]. The samples investigated in this work show no $Z_{1/2}$ center signal over a detection limit of the DLTS system used in this study ($\sim 10^{12}$ cm^{-3}). In this study, samples were grown from Si_2Cl_6 and C_3H_8, while the samples having the $Z_{1/2}$ center have been grown from SiH_4 and C_3H_8 [11, 13]. This difference in source gas seems to cause the $Z_{1/2}$ center concentration difference. However, in 6H-SiC grown from the same condition, the $E_{1/2}$ center, which is considered as corresponding to the $Z_{1/2}$ center in 4H-SiC [14, 15], is observed with relatively high concentration. Since, in the same growth condition, defects would be created as the same manner in both the 4H- and 6H-SiC, the $Z_{1/2}$ and the $E_{1/2}$ would also be included as the same manner in 4H- and 6H-SiC, respectively. Considering these discussion, it cannot be concluded that presence of the $Z_{1/2}$ center depends on source gases.

Most of the peaks observed in the studied samples have parameters which resemble those reported in ref. [11] and [16]. Deep levels in 4H-SiC created by He implantation were reported in ref. [11] and those created by proton irradiation were reported in ref. [16]. The correspondence between the present and the previous results is shown in Table 4.1. This indicates that the defects in the samples are also intrinsic defects. The deep level concentration in the samples is larger for a thinner epilayer. Deep levels originating from impurity atoms in the source gas would show no film thickness

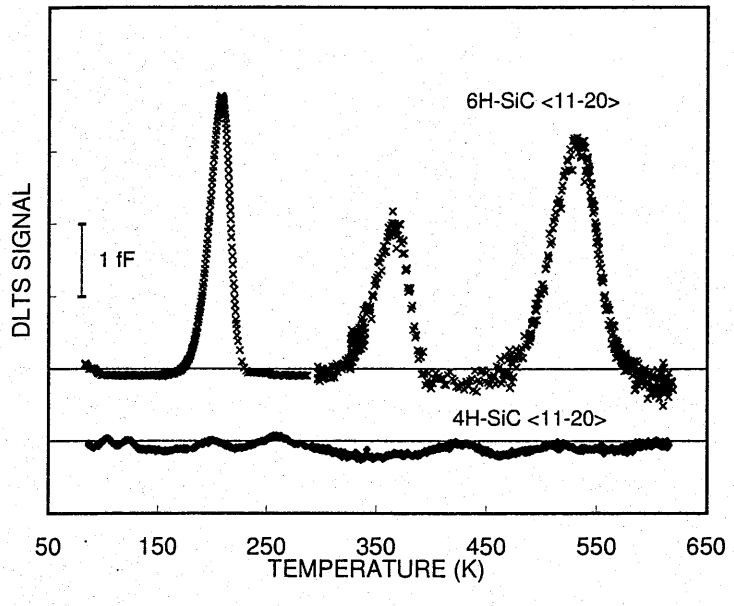

Figure 4.4: DLTS spectra for the 20 μm thick 6H- and 4H-SiC samples with inclination toward $< 11\bar{2}0 >$.

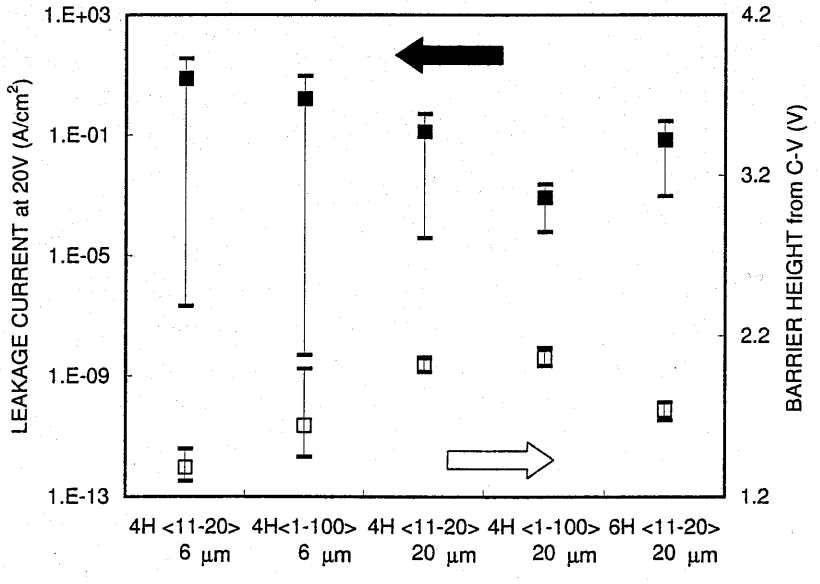

Figure 4.5: Schottky barrier height and leakage current at reverse bias of 20 V.

dependence. Thus, this film thickness dependence supports the supposition that most of peaks in the samples originate from intrinsic defects.

4.4 Conclusion

4H-SiC epitaxial layers on the substrates with two inclined directions of $< 1\bar{1}00 >$ and $< 11\bar{2}0 >$ were grown and they were characterized by DLTS. Deep level concentrations show no substrate dependence but film thickness dependence. Growth on 4H-SiC substrates with inclination toward $< 1\bar{1}00 >$ can result in the same quality epilayer as that on the substrates with inclination toward $< 11\bar{2}0 >$.

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Chapter 5

Anodic Oxidation of 6H-SiC

5.1 Introduction

6H- and 4H-SiC electronic devices are usually fabricated on the (0001) Si face, and oxide formation processes, such as field oxide formation, gate oxide formation for a metal-oxide-semiconductor (MOS) structure and sacrificial oxidation as surface preparation, are important in electronic device fabrication. However, the thermal oxidation rate for SiC is typically low even at high temperatures, especially 6H-SiC (0001) Si face [1]. This situation is the same in the case of 4H-SiC. The low oxidation rate makes the oxidation process time-consuming and 4H-, 6H-SiC devices costly. Therefore, alternative methods for oxidation have been extensively investigated [2, 3]. In this work, it is attempted to form oxide films on 6H-SiC by an anodic oxidation method, that has been widely studied for several semiconductor materials [4, 5]. So far, the anodic oxidation of SiC has been employed to fabricate porous SiC [6–8], and limited information about anodic oxide on 3C-SiC has been reported by Shor *et al.* [9]. There has been no attempt to substitute anodic oxidation for thermal oxidation in hexagonal SiC device processes. The anodic oxidation method can be performed with inexpensive and simple instruments at room temperature. This is a great advantage in the SiC device processing. In this work, the anodic oxidation is applied to sacrificial oxidation process.

Here, the anodic oxidation (or etching) process is briefly described. Figure 5.1 shows band diagram of an interface between SiC and an electrolyte. The semiconductor (SiC) energy band is bent in order to adjust its Fermi level to electrochemical potential of the electrolyte. This band structure and resulting charge transfer processes are similar with the Schottky contact. If there is a hole at the semiconductor surface, the hole can react with an anion in the electrolyte. The holes can be created by thermal excitation, light illumination or impact ionization. When the electrolyte has hydroxyl ions as anions, oxidation of semiconductor occurs together with the anion-hole reaction. In the case of SiC, Si and C atoms are oxidized to SiO_x and CO_x. SiO_2, which is an electrically insulating and solid state material, is the most possible material formed by the Si oxidation, and it would cover the exposed SiC surfaces. CO or CO_2, which are vapor phase materials, are the most possible materials formed by the C oxidation. Thus a SiO_2 film is grown on SiC by the anodic oxidation. This chapter treats this anodic

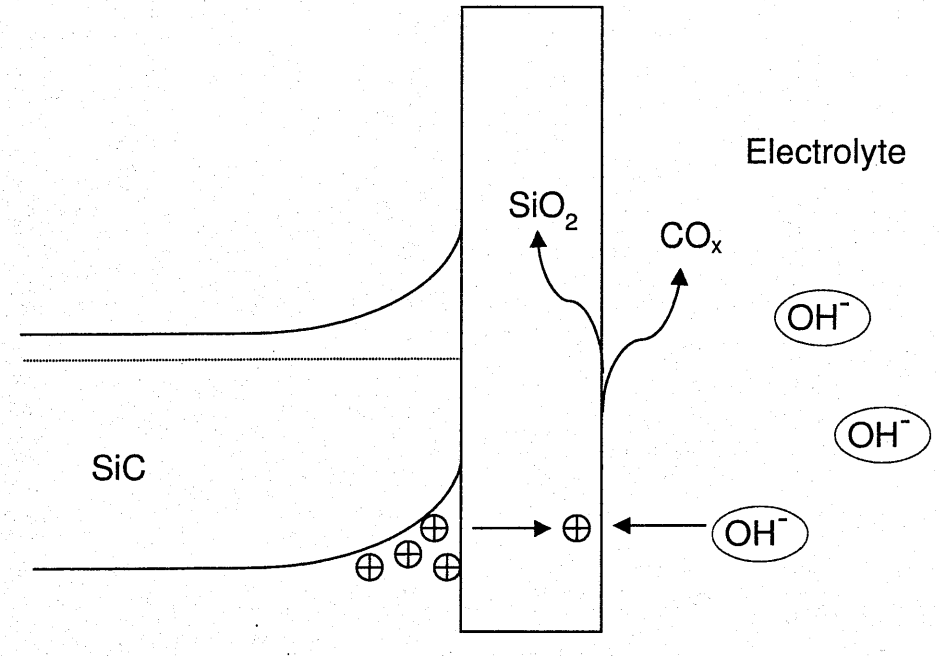

Figure 5.1: Band diagram of the interface between the semiconductor and the electrolyte.

oxidation. If, during the anodization, the oxide film is removed or SiO_x, which can dissolve in the electrolyte, is formed, the anodic etching is observed. The next chapter treats this anodic etching.

5.2 Experiment

Bulk n-type 6H-SiC (0001) on-axis wafers with a net donor concentration of 1×10^{18} cm^{-3} were purchased from Sterling Semiconductor Inc. Before the anodic oxidation, Al was evaporated on the Si face of the samples as ohmic contacts. The electrolyte for the anodic oxidation was a mixed solution of 300 cc ethylene glycol, 7.5 cc water and 1.2 g KNO_3, which has been widely used for the anodic oxidation of Si [10]. The samples were stuck on plastic plates. Part of the Si face of the sample was exposed to the electrolyte and the other parts of the sample were coated with silicone resin or wax. A Pt electrode was used as the cathode, and voltage was applied between the sample and the Pt electrode using the constant current method. The current density was set at 1 mA/cm^2 and the oxidation time was 4, 20 or 100 min. Schematic for experimental setup for anodic oxidation is shown in Fig. 5.2 This setup has also been used for electrochemical etching experiments described in the next chapter.

In order to confirm the effect of the anodic sacrificial oxidation, oxide films formed on the sample surfaces were etched by HF. Ni, Au and Al metals on the anodically oxidized-etched surfaces, where Ni and Au are for the Schottky contacts and Al is for the ohmic contacts, were evaporated. All of the contacts were not annealed. The contact area

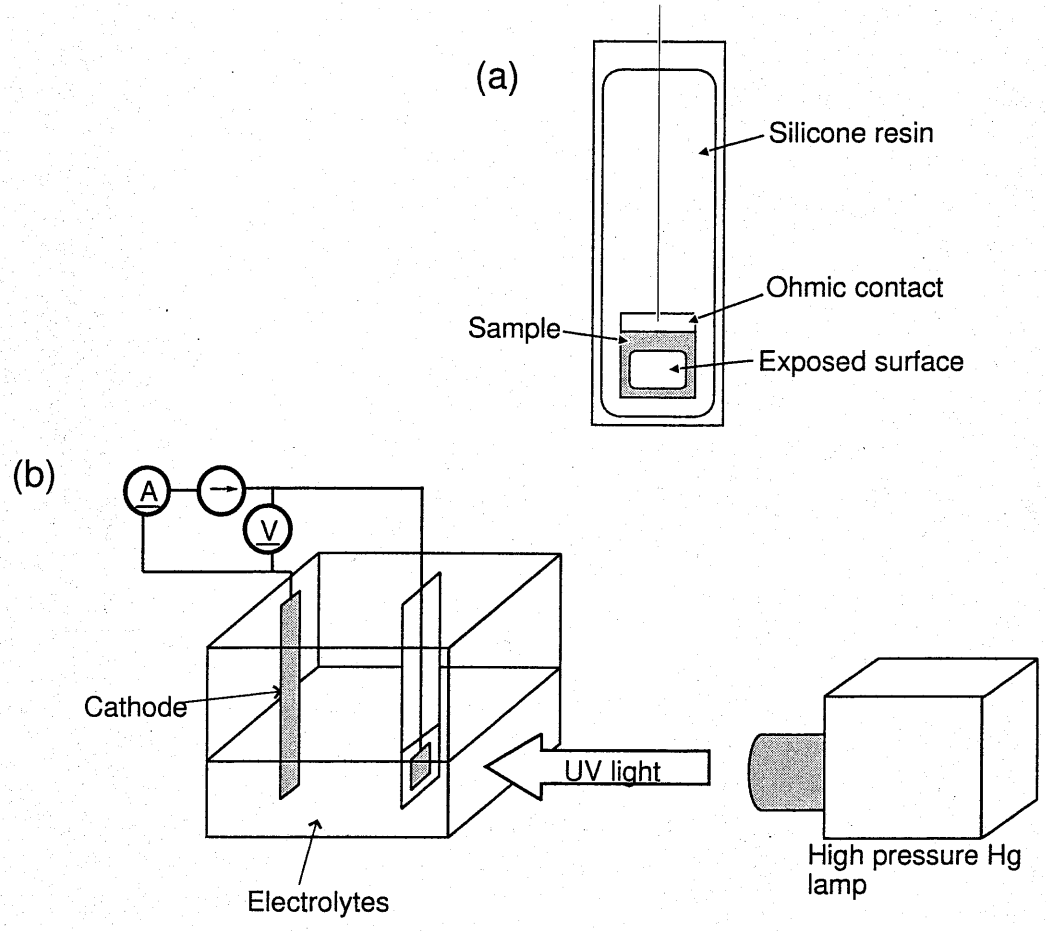

Figure 5.2: Schematic for experimental setup for anodic oxidation. (a) is a plastic plate with a stuck sample, and (b) is an electrochemical cell and block diagram for electrical connections. (The High pressure Hg lamp is not used in anodic oxidation, but in the electrochemical etching described in the next chapter)

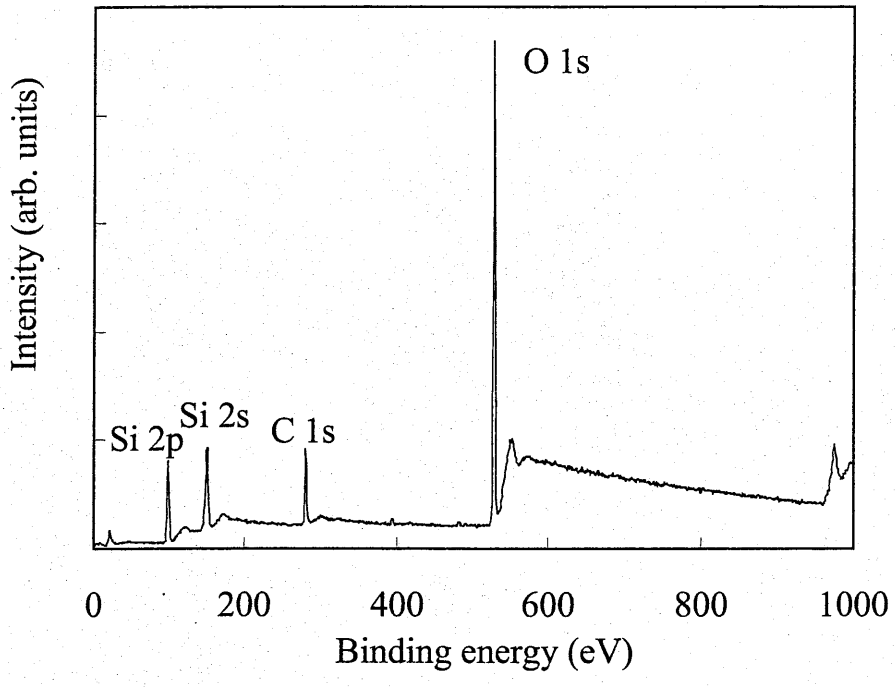

Figure 5.3: XPS spectrum for the anodic oxide film.

for all the contacts was 0.283 mm^2. As references, the metals were also evaporated on an as-received surface and a thermally oxidized-etched surface with removed sacrificial layer thickness of 30 nm. Before the evaporation, all the samples were dipped in HF and then were dipped in boiling water. Current-voltage (I-V) and C-V characteristics for the Schottky contacts were measured and contact resistances for the Al ohmic contacts were evaluated by the 4-point-probe-pattern method. Auger electron spectroscopy (AES) measurements were also performed in order to evaluate composition at each surface.

5.3 Results

5.3.1 Anodic oxide

The X-ray photoelectron spectroscopy (XPS) spectrum for the anodic oxide film of approximately 250 nm thickness is shown in Fig. 5.3, where peaks for Si, C and O appear. The C 1s peak has an intensity comparable to the Si peak and thus the film is not pure SiO_2. The peak-energy positions for Si 2p, C 1s and O 1s are 109.0 eV, 290.4 eV and 538.3 eV, respectively. The oxide film is not thin enough to avoid charge-up of the film during the measurement. Therefore, all of the peak positions are shifted due to the charge-up, making it difficult to discuss the chemical shifts of the peak positions.

The oxide was easily etched by HF. Step heights between oxide-etched surfaces and

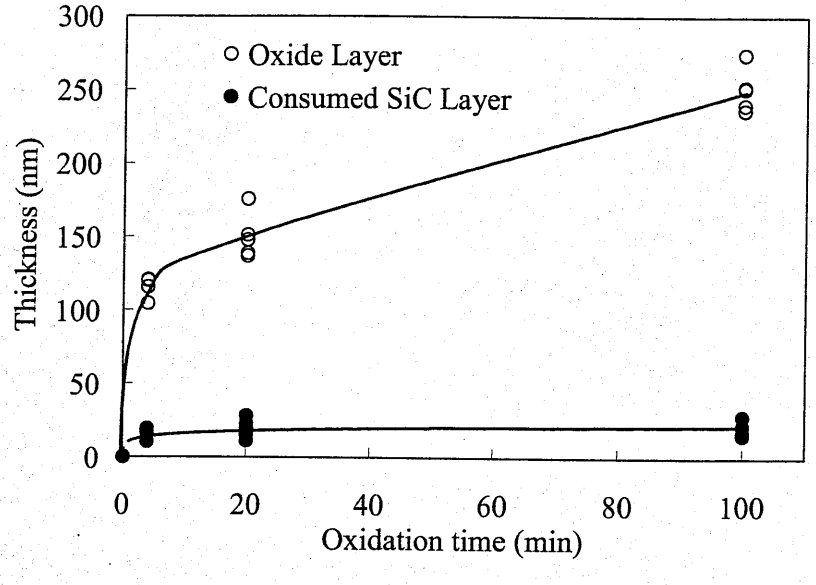

Figure 5.4: Thickness of the oxide film and consumed SiC layer against oxidation time.

oxide surfaces as well as between oxide-etched surfaces and non oxidized (as-received) surfaces were measured using a profilometer. It was defined that the former is oxide film thickness and the latter is consumed SiC layer thickness, and they are plotted in Fig. 5.4 as a function of time. As shown in this figure, the oxide with a thickness of more than 100 nm was formed after only 4 min of anodic oxidation. The oxide thickness seems to saturate after 10-20 min of anodic oxidation. It takes about 5 h to form an oxide film of more than 100 nm thickness on the 6H-SiC (0001) Si face by thermal oxidation at 1000°C under wet O_2 ambient [1]. Therefore, the oxide formation rate for anodic oxidation is much higher than that for thermal oxidation. On the other hand, the consumed SiC layer thickness after 4 min of anodic oxidation is only about 15 nm, 1/8 of the oxide thickness. The consumed layer thickness also seems to saturate with time.

The anodic oxide film was etched by HF and the morphology of an oxide-etched surface using an atomic force microscope (AFM) was observed. As reference, the morphologies of an as-received surface and a thermal-oxide-etched surface were also observed. Here, thermal oxidation was performed at 1100°C for 2 h under wet O_2 ambient, and the consumed SiC layer thickness was about 30 nm. Figure 5.5 shows the AFM images for these surfaces. The average roughness Ra and root-mean-square roughness Rms are given in the figure. Only the anodic-oxide-etched surface after 4 min of anodic oxidation is shown, since all of the anodic-oxide-etched surfaces show similar morpholo-

gies. As shown in this figure, the as-received wafer has the flattest surface and shows a little undulation with less than 10 nm peak-to-valley height, which may be caused by polishing. The thermal-oxide-etched surface also shows the undulation, and its flatness is slightly degraded compared with the as-received surface. On the other hand, the anodic-oxide-etched surface shows microroughness with an approximately 100 nm peak-to-valley height. The Ra and Rms values for the anodic-oxide-etched surface are more than one order of magnitude larger than those for the other two surfaces. Thus, thermal oxidation can form a flatter SiC/SiO_2 interface than anodic oxidation.

As mentioned above, the anodic oxide film thickness is about eight times larger than the consumed SiC thickness. The SiC/SiO_2 interface roughness shown above causes underestimation of the consumed SiC thickness. The oxide film thickness and the consumed SiC layer thickness were measured using a profilometer. The profilometer can measure step heights on the way traced by its probe. The tip of the probe is not small enough to enter the fine valleys of the rough surface, whose depth is about 100 nm against the peaks. Therefore, the probe traces only on the peaks. Thus, the actual volume of the consumed SiC is larger than expected from the consumed SiC layer thickness measured by the profilometer. Furthermore, oxide films would be porous because of CO_2 bubble formation, as reported in the case of 3C-SiC using an electrolyte of H_2SO_4 [9].

The roughness at an anodic-oxide-etched surface as observed by AFM is thought to be due to defects at the surface. Since bulk SiC crystals were employed, there are many defects in the crystal. It has been reported for anodic oxidation of SiC using HF that anodization rate at the defect site is different from that at the other regions [11]. As the anodic oxidation proceeds, the defect sites are selectively oxidized. After the oxidation and the oxide film removal, the defective regions are preferentially removed and the resulting surface is rough. This implies that the anodic oxidation and etching can be utilized as defect characterization techniques. If epitaxial SiC crystals with low defect density are employed, the roughness may be suppressed.

5.3.2 Sacrificial anodic oxidation

Sacrificial anodic oxidation was performed before contact formation. Ni, Au and Al contacts were evaporated on the as-received, anodic-oxide-etched and thermal-oxide-etched surfaces. Figure 5.6 shows the forward biased I-V characteristics for the Ni Schottky contacts on each surface. The Ni contacts on the as-received surface have an average ideality factor n of 1.1. Those on the surfaces after the sacrificial anodic oxidation show ideality factors n scattered within 1.1-1.4, and those on the surface after the sacrificial thermal oxidation show n of about 1.1. The horizontal shift of I-V curves means Schottky barrier height difference of the diodes. The barrier heights ϕ_{I-V} obtained from I-V curves are 0.95 V for the as-received surface and 1.0-1.3 V for both the oxidized-etched surfaces. The estimation of ϕ_{I-V} is somewhat unreliable due to deviation of the n value from 1.

Figure 5.7 shows barrier heights measured from C-V characteristics, ϕ_{C-V}, and leakage current densities at a reverse bias of 20 V for the Ni Schottky contacts. The values of ϕ_{C-V} show the same trend as ϕ_{I-V}; the Ni contacts on the as-received surface have

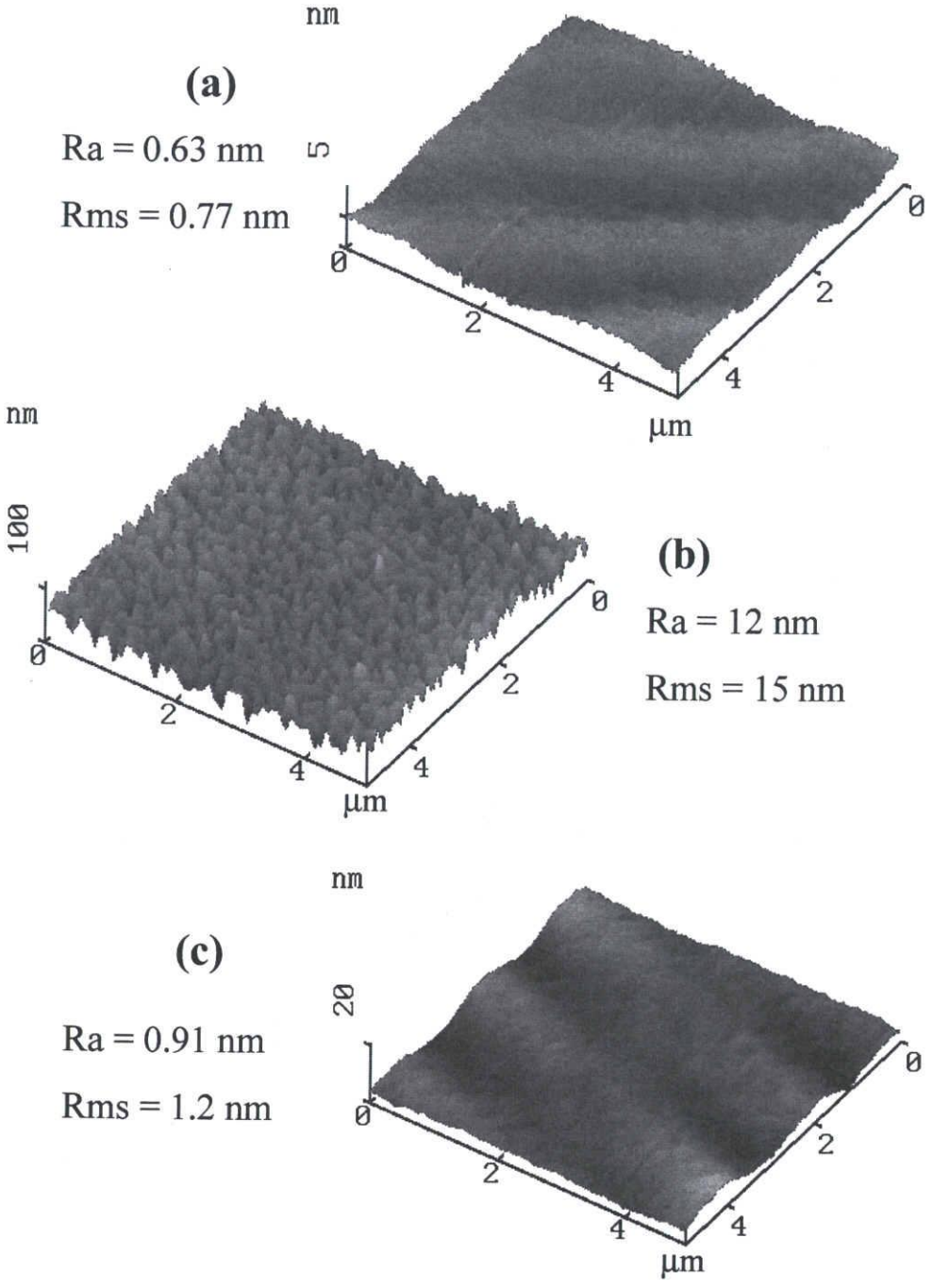

Figure 5.5: AFM images for (a) the as-received surface, (b) the 4 min anodically oxidized and etched sample surface and (c) the thermally oxidized and etched sample surface.

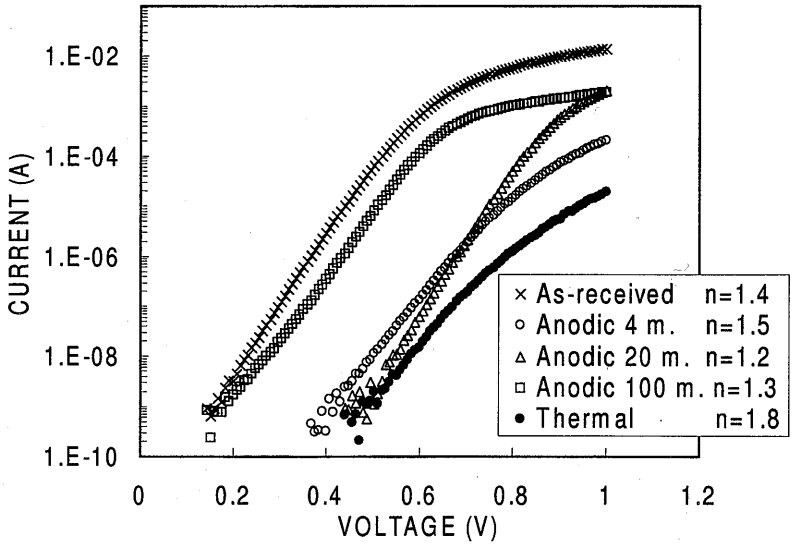

Figure 5.6: Forward biased I-V characteristics for the Ni Schottky contacts on each surface.

the lowest ϕ_{C-V} of 0.9 V, while those on the other surfaces have ϕ_{C-V} of about 1.2 V, except for those on the 100 min anodically oxidized-etched surface. The leakage current densities for all the surfaces are of the order of 10^{-1} A/cm^2.

Figure 5.8 shows the forward biased I-V characteristics for the Au Schottky contacts on each surface. The n values for the Au contacts are larger than those for the Ni contacts, in a range of 1.2-1.8. The ϕ_{I-V} for the Au contacts on the as-received surface shows the lowest value of 0.90 V as in the case for the Ni contacts, while it is within 0.98-1.3 V for both the oxidized-etched surfaces.

Figure 5.9 shows the ϕ_{C-V} values and leakage current densities at a reverse bias of 20 V for the Au Schottky contacts. ϕ_{C-V} also increased by the oxidation and subsequent etching. For the as-received surface, ϕ_{C-V} is 1.1 V, while for the other surfaces, ϕ_{C-V} is about 1.7 V except for the 20 min anodically oxidized-etched surface. The leakage current densities at a reverse bias of 20 V for all the Au contacts are of the order of 1 A/cm^2, which is one order of magnitude larger than that for the Ni contacts. The deviation of n value from 1 for the Ni and Au Schottky diodes means that forward current has not only the diffusion current component but also other current components such as tunneling current. After the sacrificial oxidation, the barrier height for the contacts become larger. Thus, the diffusion current becomes relatively small, and the tunneling current will tend to be dominant. This leads to higher n value.

Figure 5.10 shows contact resistances for the Al contacts on each surface. The contact resistances are 1-10 Ωcm^2 on the as-received surface and 10^{-2}-10^{-1} Ωcm^2 on the oxidized-

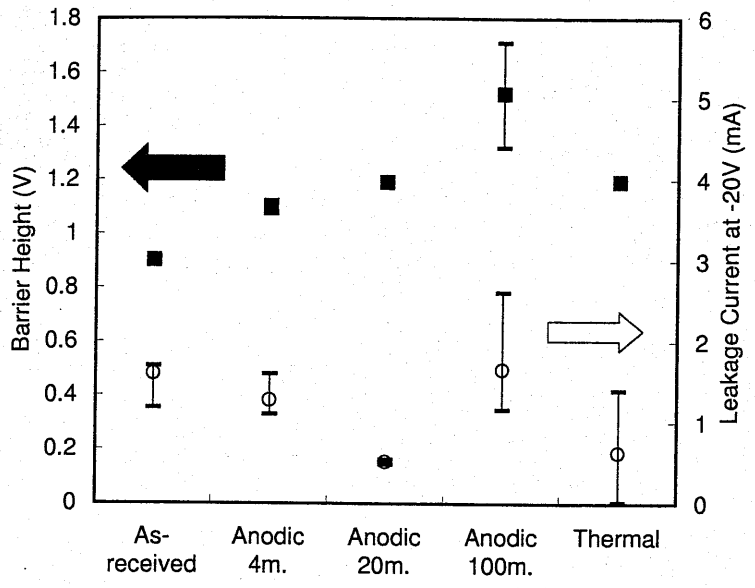

Figure 5.7: Barrier heights from C-V measurements and leakage current at reverse bias of 20 V for the Ni Schottky contacts on each surface.

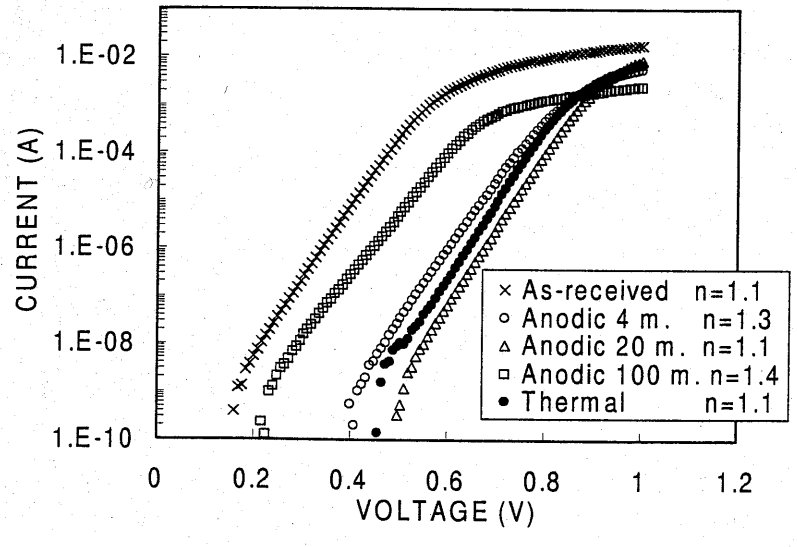

Figure 5.8: Forward biased I-V characteristics for the Au Schottky contacts on each surface.

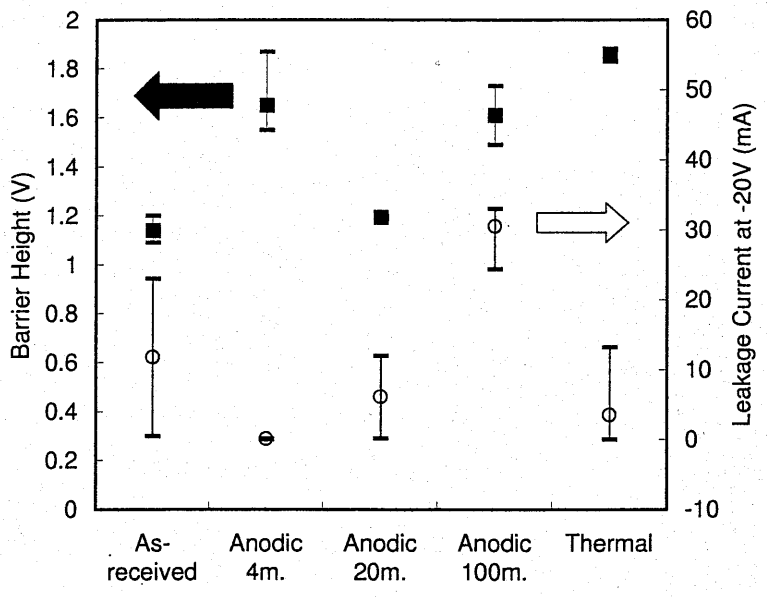

Figure 5.9: Barrier heights from C-V measurements and leakage current at reverse bias of 20 V for the Au Schottky contacts on each surface.

etched surfaces. Thus both the anodic and thermal oxidation-etching processes reduce the Al contact resistance by about two orders of magnitude. These Al contact resistance values are relatively high in comparison with the best value reported so far [12, 13]. However, the contact resistance values would depend on the crystalline quality of SiC. The samples cut from a single piece of wafer were employed in this work and comparison between treatments is focused on. Thus it can be concluded that both the sacrificial oxidation processes reduce the Al contact resistances.

The above results show that both the anodic and thermal sacrificial oxidation processes have similar effects on the properties of the contacts. It has been reported that the sacrificial thermal oxidation removes a low crystallinity layer at the SiC surface [14]. In order to confirm presence and removal of this low crystallinity layer, AES measurements for the as-received, 4 min anodically oxidized-etched and thermally oxidized-etched surfaces were performed. Prior to the measurements, the samples were cleaned by the same manner as before the contact formation. The AES spectra were taken as soon as possible after the cleaning in order to avoid contamination from the environment. Figure 5.11 shows AES spectra for each surface. Each spectrum is normalized by Si_{KLL} peak intensities. As shown in this figure, both the sacrificial oxidized-etched surfaces show very similar spectra. On the other hand, the spectrum for the as-received surface has larger intensity of the C_{KLL} peak than those for the others. This implies that there is a C-rich layer at the as-received sample surface. It has been reported that the contact resistance

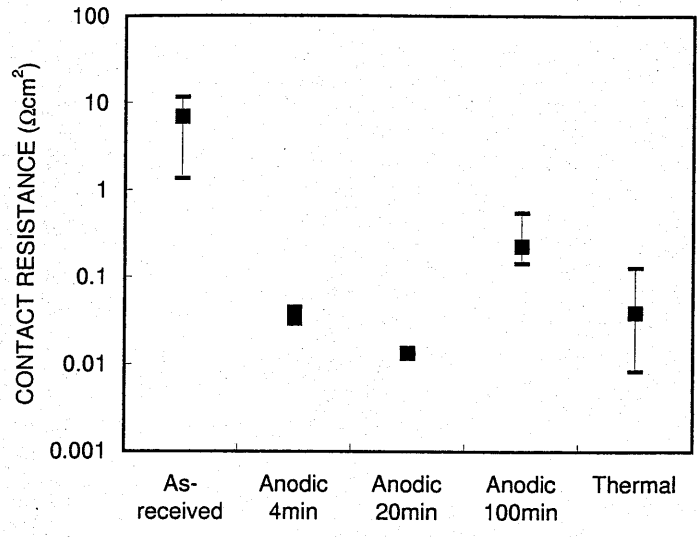

Figure 5.10: Contact resistances for Al ohmic contacts on each surface.

is lower for a less C-rich surface [15]. After both the sacrificial oxidation processes, the C-rich layer was removed, which results in a lower contact resistance, as shown in Fig. 5.10. As shown in Fig. 5.5, it is found from atomic force microscopy that the anodically oxidized-etched surface has one order of magnitude larger root-mean-square roughness (10-15 nm) than that for the as-received and thermally oxidized-etched surface (less than 1 nm). Even on such rough surfaces, contact properties after sacrificial anodic oxidation are similar to those after sacrificial thermal oxidation. This implies that crystallinity of the surface layer, rather than surface morphology, is influential for the contact properties.

5.4 Conclusion

Oxide films on 6H-SiC are formed by an anodic oxidation method. The films are easily etched by HF, but not pure SiO_2. The oxidation rate is much higher than the thermal oxidation rate, but the apparent consumed SiC layer thickness is only 1/8 of the oxide thickness. The anodic oxidation method is applied to the sacrificial oxidation before the contact formation on the 6H-SiC (0001) Si face. The sacrificial anodic oxidation has similar effects to the sacrificial thermal oxidation on both the Schottky and ohmic contact properties. AES measurements reveal that the surfaces after both the sacrificial oxidation processes do not have a C-rich layer. Thus, the C-rich low-crystallinity layer,

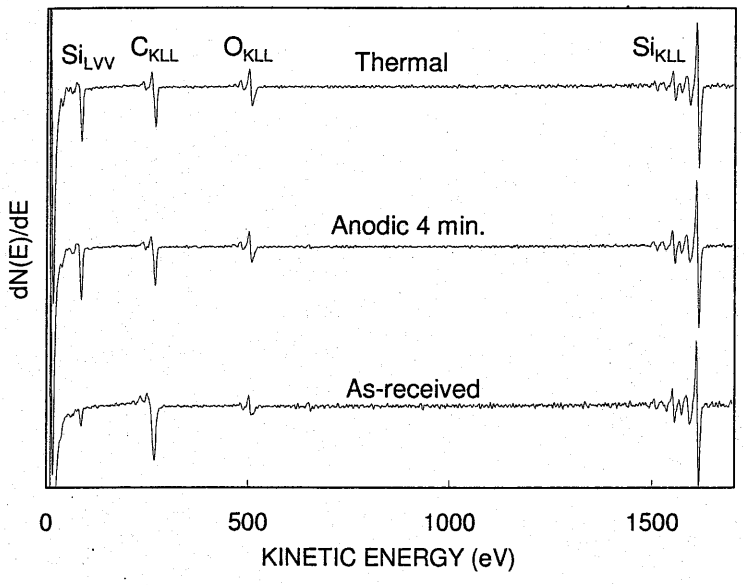

Figure 5.11: AES spectra for each surface.

which is detrimental for the contact, was removed by the anodic oxidation and etching. The results indicate that the sacrificial anodic oxidation is expected to substitute for the sacrificial thermal oxidation.

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Chapter 6

Anodic Etching of 6H-SiC

6.1 Introduction

Silicon carbide has excellent physical and chemical stability. The stability makes SiC devices promising for operating in harsh environments. However, because of the stability, it is hard to apply conventional characterization and processing methods, which have been established in semiconductor industry so far. Etching of SiC is one of the most difficult techniques. Although etching can be used for characterization of crystalline quality and a device fabrication process, there is no chemical etchant for SiC at room temperature. The high temperature molten salt etching is the only way to etch SiC with solely chemical process. Dry etching methods have been employed for the etching of SiC in device fabrication processes. In this chapter, an electrochemical etching method is applied to a characterization method and device fabrication processes.

SiC crystal has many structural defects which deteriorate performance of the devices. The most well-known structural defect observed in SiC is micropipe, which is a hollow core threading through the entire SiC wafer. Other structural defects in SiC are dislocation, void, inclusion and so on. All kinds of structural defects should be eliminated for electronic device fabrication and usage as substrates for epitaxial growth of GaN and SiC. In order to eliminate these defects, defect characterization is important. Usually, structural defects in SiC crystals are revealed by molten KOH etching [1–10]. This etching proceeds preferentially at a structural defect position and thus defects such as micropipes and dislocations appear as etch pits [1, 10]. One of the subjects in this chapter is to employ the electrochemical etching method for characterization of the defects. The electrochemical etching of SiC using an aqueous KOH solution has been reported in ref. [11]. The etching mechanism of the electrochemical method differs from the molten KOH etching, and resulting etched surfaces will also be different between them. Etch pit morphology is observed on the electrochemically etched SiC sample surfaces and compared it with molten KOH etched surfaces.

For an industrial device fabrication process, dry etching methods are employed and widely researched [12–18]. However, the dry etching methods introduce damages near the surface in SiC. The damages deteriorate performance of SiC electronic devices. On the other hand, the electrochemical method is combination of chemical and electrical

processes and can etch SiC at room temperature without causing damages in it. This method is frequently used for fabrication of porous SiC [19–33]. Another subject in this chapter is to develop an electrochemical etching technique applicable for the device fabrication process. In this view, the etched surface morphology must be smooth, and masking and patterning are required. In order to form patterned structure, porous structure formation and subsequent thermal oxidation and etching methods have been proposed, [34,35] and trench structure formation by photoelectrochemical etching with laser scan has also been proposed. [36] However, these procedures are time-consuming and thus hard to apply to an industrial process. The patterned structures without porous layer formation, which would be less time-consuming and applicable for the device fabrication process, is proposed in a latter part of this chapter.

6.2 Experiment

6.2.1 Characterization of structural defects

The electrochemical etching was performed for commercially available n-type 6H-SiC (0001) wafers with both sides polished. The net donor concentration of the wafers is approximately 10^{18} cm^{-3}. The wafers were cut into small pieces with dimension of 5 mm$\times$1 cm. Before the etching, ohmic Al contacts were evaporated on the Si face of the samples. Each sample was placed on a plastic plate, and its edge part, the contacts and the lead wire were covered with silicone resin as well as procedures described in previous chapter. The content of KOH in the aqueous solution for an electrolyte was 50 wt.%. The SiC samples and a Pt electrode were dipped in the electrolyte as an anode and a cathode, respectively. The voltage was applied between them at a constant current mode. The etching temperature was room temperature. Current density at the sample surface was fixed at 5 mA/cm^2 and etching time was 30 min. After the etching, the silicone resin was removed by a mixed solution of HF and HNO_3. The etching was done for both the Si face and the C face of the samples under the same condition. Etched surfaces were observed by a Nomarski microscope, SEM and AFM. In order to clarify the micropipe positions in the as-received sample, an optical microscope with crossed polarizer, which can reveal stress fields introduced by micropipes [37,38], was employed. After the electrochemical etching, one sample was etched by molten KOH etching at 490°C for 10 min.

6.2.2 Application to device fabrication

Samples and preparation before the etching were almost the same as those described in the previous subsection, but ohmic contacts were Al or alloyed Ni. In order to investigate the best etching condition for device fabrication, concentration of KOH in electrolytes, etching temperature, sample polarity, UV light illumination and current density were varied. The electrolytes were aqueous KOH solutions with various concentration (0.1-50 wt.%). Voltage was applied between them with constant current of 5 mA/cm^2 unless

otherwise stated, and the exposed region of the samples was etched. The etching was performed with or without light illumination which generates electron-hole pairs in the samples for enhancement of the etching reaction. The light source was a high pressure Hg lamp with a power supply of 500 W. After the etching the silicone resin was removed by HF:HNO_3, and then we characterized the etched depth by a stylus profilometer and etched surface morphology by the Nomarski microscope, SEM and AFM. For patterned etching experiments, Ni metal was employed as a mask material and patterned structures were observed by SEM.

6.3 Results

6.3.1 Characterization of structural defects

As-received sample surfaces show no obvious structural defects or polishing scratch even in observation by the Nomarski microscope. During the electrochemical etching, applied voltage was around 25 V under the constant current condition described above for all the samples. On the electrochemical etched surfaces, scratches and many etch pits with a peculiar shape are found as shown in Fig. 6.1 (a). This figure is for the Si face of the sample. Since the results in this study were almost the same for the Si and C faces, in this paper, data are shown only for the Si face. In this etching condition, the etched depth measured by the profilometer is approximately 30 nm which is almost unchanged with increasing etching time because the etching proceeds with porous formation as described later. A white color region at the left hand side in Fig. 6.1 (a) was covered by silicone resin during the etching. After the etching, the scratches are clearly observed as seen in Fig. 6.1 (a). This implies that the sample has damages originating from polishing even though no scratches are observed before the etching. Figure 6.1 (b) is a magnified picture of the etch pit. From Fig. 6.1 (a), each of the etch pits seems to consist of a crescent pit (or sometimes circle pit) and a triangle pit, and all the etch pits have almost the same size; the diameter of the crescent pit and the side of the triangle pit are about 10 μm. There is a dark point in the region surrounded by the crescent pit as shown in Fig. 6.1 (b), and it is a small circular pit. In the etch pits in Fig. 6.1 (a), some of the etch pits have the dark point and the other seem not to have the dark point. The crescent pit and the triangle pit align in the same direction for all the etch pits in Fig. 6.1 (a). It has been reported that only round shape etch pits are formed by an electrochemical etching [11, 39], and to the best of my knowledge, etch pit with this kind of shape has never been reported in the molten KOH etching [1–10].

The electrochemical etching has been performed in the same condition for SiC wafers supplied from four different venders. This kind of etch pit was observed for the wafers from two of the four venders. Thus, although that peculiar etch pit is not specific to one vender, the etch pit appearance may depend on crystal growth conditions. The results were reproducible for different wafers from the same vender.

As shown in Fig. 6.1 (a), the electrochemical etching revealed the scratches originating from polishing. Thus this etching method can detect the polishing damages even

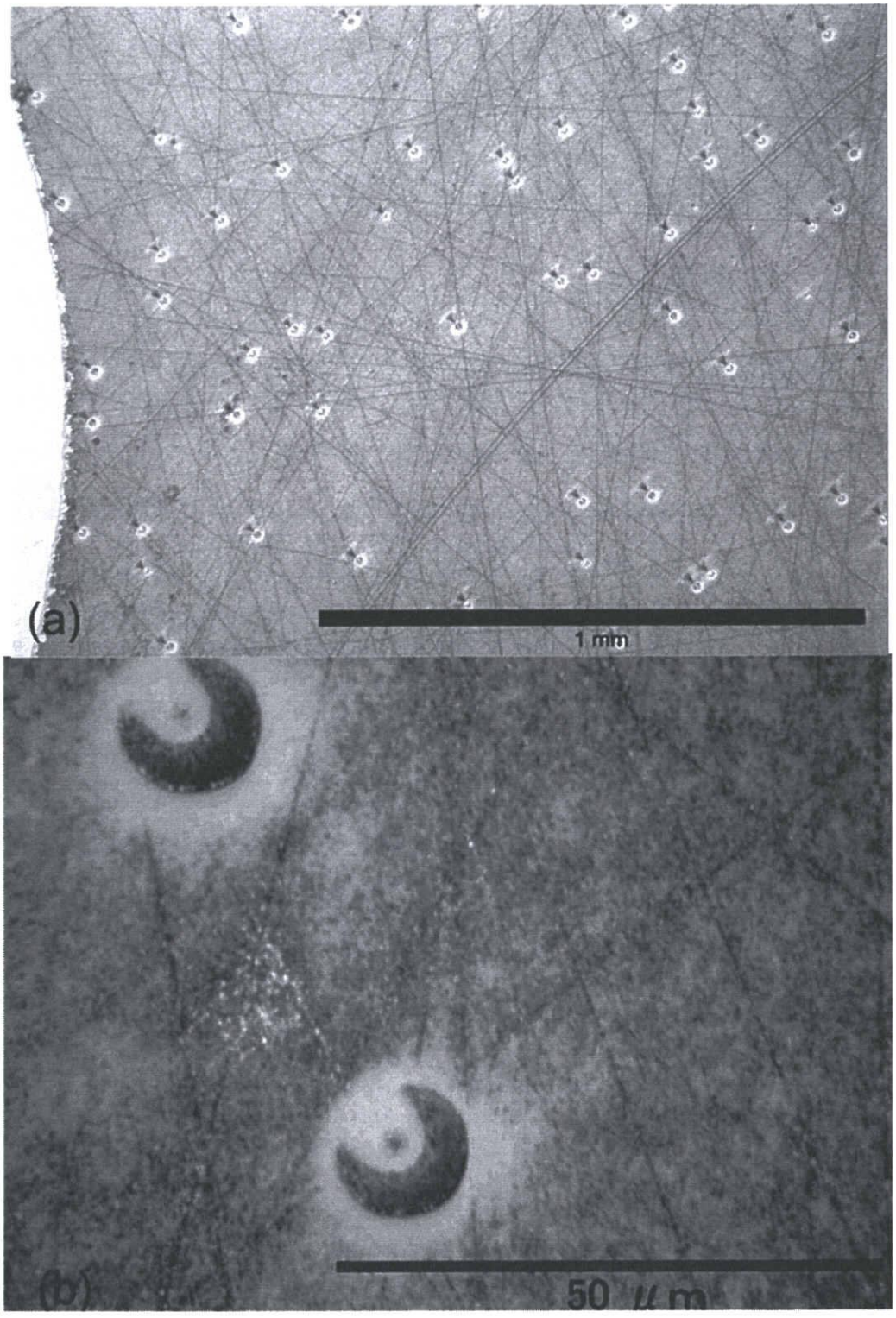

Figure 6.1: Optical micrographs for electrochemically etched 6H-SiC: (a) overview of the etched surface and (b) magnified view at the etch pit point.

though the damages are invisible before the etching. These scratches on the wafers from the four venders were observed, and the concentration of the scratches was different among venders.

Figures 6.2 (a) and (b) show SEM micrographs for the etch pit. Figure 6.2 (a) is a picture of perpendicular view and Fig. 6.2 (b) is an inclined view. Almost all the surface areas become porous except for the region around the crescent pit. It seems that the dark point surrounded by the crescent pit observed in Fig. 6.1 (b) has a porous structure. Boundary of the triangle pit is not clear especially in Fig. 6.2. In order to see rise and fall around the etch pits in detail, an AFM image around the etch pit with a cross section profile was taken as shown in Fig. 6.3. The cross section line AB (the left hand side of the figure) corresponds to the line AB in the AFM image (the right hand side of the figure). From this figure, the crescent pit is mostly depressed, but there is an uplifted region in the middle part of the crescent pit. In Fig. 6.2 (b) no such uplifted region is observed in the crescent pit. Therefore the crescent pits are usually just depressed but some of them have uplifted regions in it. The triangle pit is depressed by 250 nm at its vertex part near the crescent pit.

It has been performed that the etching under other conditions, *i.e.*, at lower KOH concentrations and higher or lower temperature ranges. The crescent or circle pits appeared in the other etching conditions but the triangle pits did not appear. In addition, the etching under the condition described above reveals crescent or circle pits most clearly and makes the etched surfaces most porous. Thus it is considered that the etch pit shape is related to the porosity.

The etch pit density ($<10^3$ cm^{-2}) is one order of magnitude larger than the micropipe density nominally announced by the wafer vender (<100 cm^{-2}). In order to clarify correlation between the etch pits and micropipes, optical micrography with the crossed polarizer was observed for the as-received sample and for the same sample after the electrochemical etching. Figures 6.4 (a) and (b) show the optical micrographs with crossed polarizer for the as-received surface and for the etched surface, respectively. Both the images are for the same position within the sample. In Fig. 6.4 (a), three bright spots are observed. The center of these spots corresponds to the micropipe positions [37,38]. In Fig. 6.4 (b), the dark area is the etched part, and many white points corresponding to the etch pits appear there. By comparing the micropipe positions with the etch pit positions in these figures, we can see that all the micropipes become the etch pits after the electrochemical etching. Thus, all the micropipes become the etch pits. However, the number of the etch pits is obviously larger than that of the micropipes. Therefore the etch pits originate not only from micropipes but also from other kinds of defects. Figure 6.4 (c) shows the molten KOH etched surface for the same area of the sample. Etch pits density revealed by the molten KOH etching is almost the same as the nominal etch pit density announced from the wafer vender ($<10^4$ cm^{-2}) and is larger by one order of magnitude than those revealed by the electrochemical etching. From these figures, it cannot be clearly seen that the defects revealed by the electrochemical etching correspond the etch pits in the molten KOH etching, because the etch pit density after the molten KOH etching is too high to confirm the one-to-one correspondence.

The direction of the paired etch pits formed by the electrochemical etching is almost

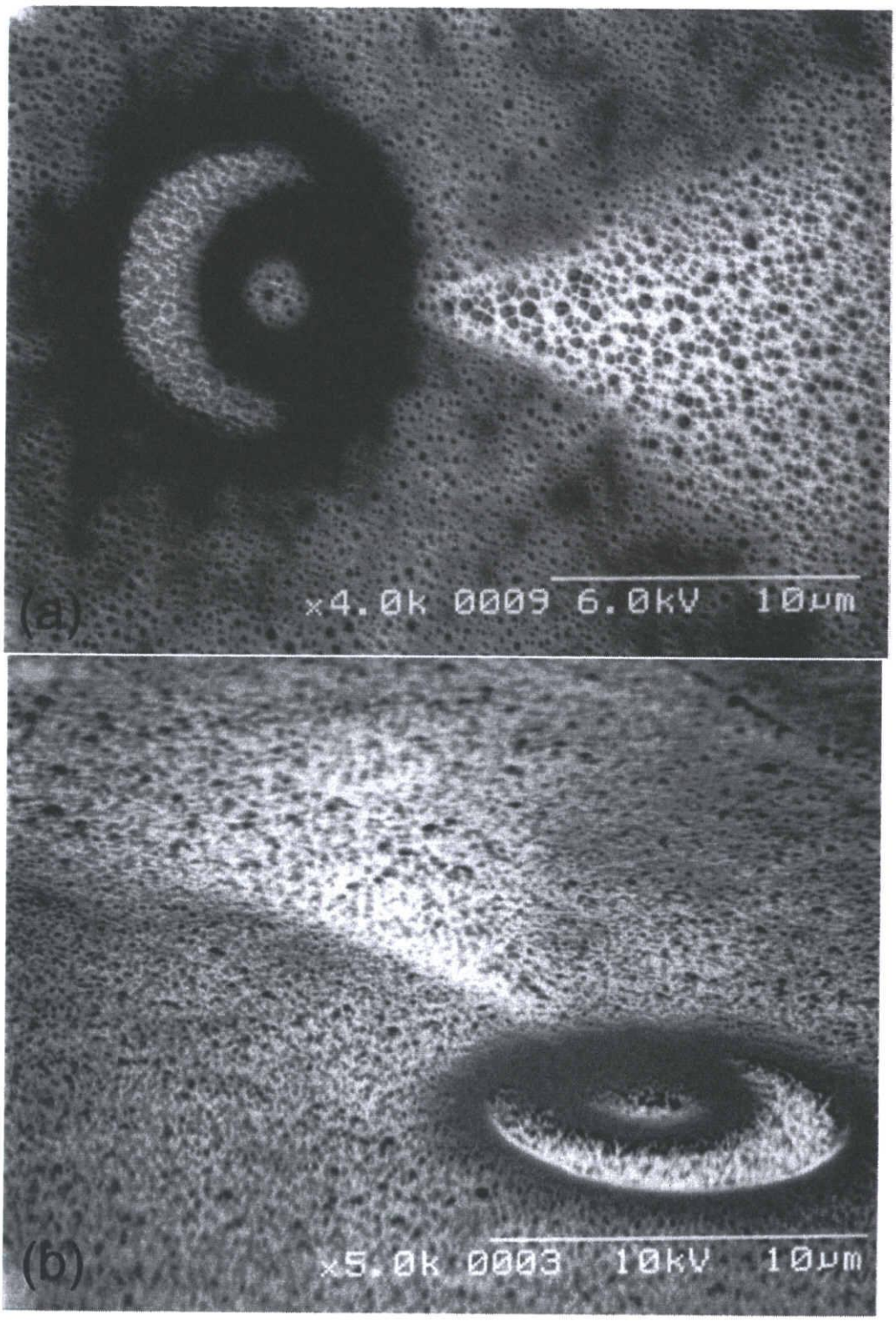

Figure 6.2: SEM micrographs for the etch pit: (a) perpendicular view from the surface and (b) inclined view of the same etch pit.

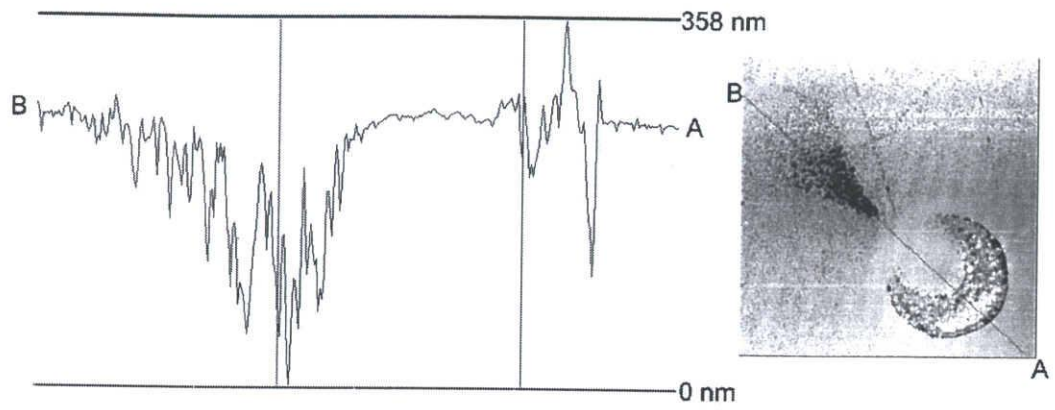

Figure 6.3: Cross sectional profile for the etch pit taken by AFM.

the same within one sample as shown in Fig. 6.1 (a). However, from the observation of many pieces cut from one wafer, it was found that the paired etch pits align in the radial direction from the wafer center irrespective of Si face or C face as illustrated in Fig. 6.5 (b). The arrows in Fig. 6.5 (b) indicate the direction of the etch pits, which is defined in Fig. 6.5 (a). From this fact, a hypothesis about the cause of this peculiar shape etch pit can be made. If the SiC crystal grows at steps of the spiral originating from a screw dislocation at the center of the wafer according to the BCF theory [40], the growth proceeds from the center of the wafer to its perimeter with migrating steps. When there are obstacles, for example micropipes or inclusions, on the growing surface, the migration of steps will be stopped there. A schematic diagram of this situation is drawn in Fig. 6.6. As a result, in a region near the obstacles in the lower terrace, the crystal does not grow in the step-flow mode. In that region, which would have almost triangle shape, the crystalline quality would differ from the normal step-flow growth region. The electrochemical etching would disclose the crystalline quality difference originating from the growth mode difference. The pinning of steps by the screw dislocation was observed for 6H-SiC [9, 41]. From the data and these reports, it is most probable that the screw dislocations as well as micropipes cause the electrochemical etch pits. The screw dislocations form a vertical step on the step-flowing terrace, which can be the obstacles for the step-flow growth, but threading edge dislocations do not form such steps since their Burgers vectors are parallel to the surface. Sanchez *et al.* have reported that the screw dislocation density is one or two order of magnitude lower than

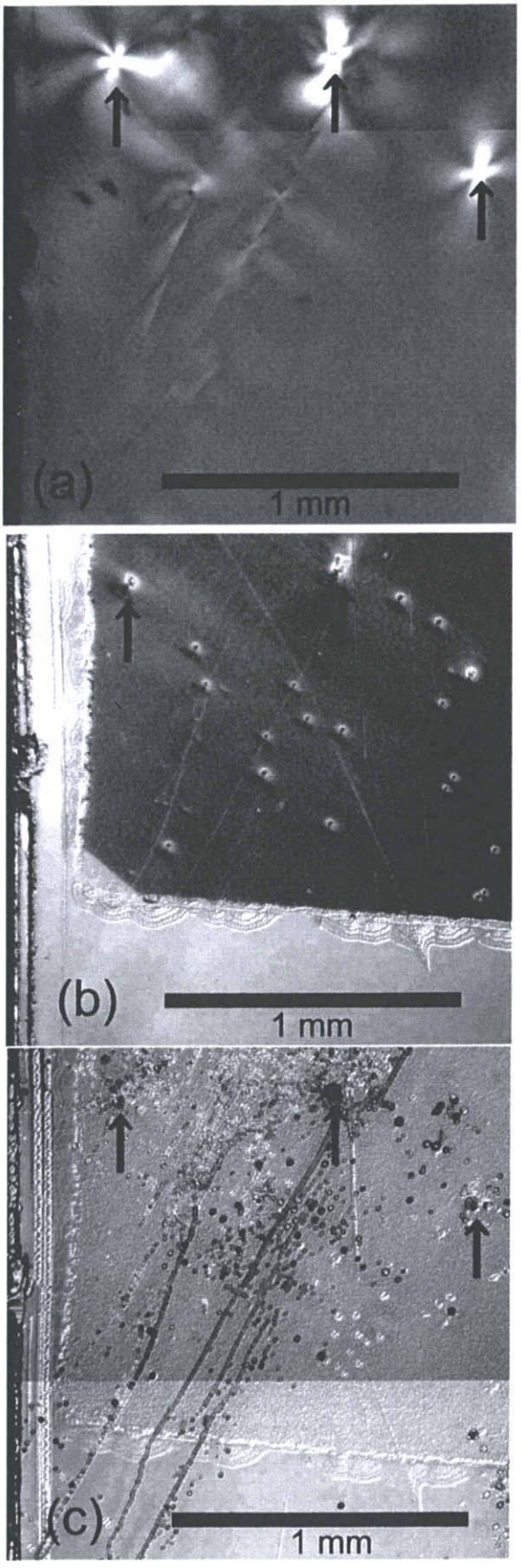

Figure 6.4: Optical micrograph for 6H-SiC: (a) the as-received surface observed with the crossed polarizer, (b) the electrochemically etched surface for the same region and (c) the molten KOH etched surface for the same region. The arrows indicate the position of micropipes.

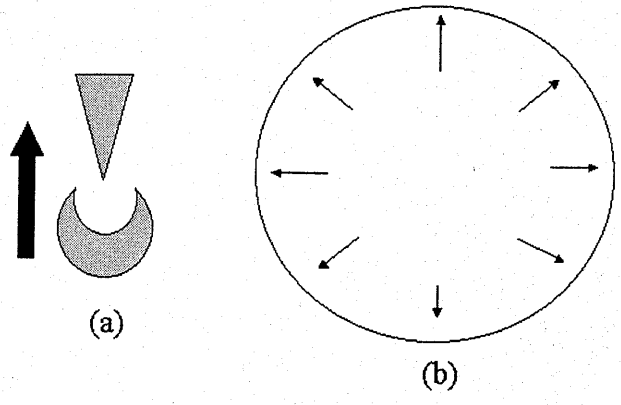

Figure 6.5: Schematic diagram of the direction of the etch pits.

the edge dislocation density [41]. As noted above, the electrochemical etch pit density is one order of magnitude lower than the molten KOH etch pit density. This density difference can be consistently explained considering that although both the edge and screw dislocations are revealed by the molten KOH etching, only the screw dislocations become etch pits in the electrochemical etching.

Although it was tried to clarify the difference between the pit region and the rest by microscope Raman scattering, any Raman peak shifts were not found for both TO and LO modes, whose wave numbers depend on the stress and the carrier concentration in the crystal, respectively [42]. Therefore it cannot be confirmed that the stress and carrier concentration differences in the crystal are the cause of the triangle shape pits.

In the electrochemical etching, reaction species at the semiconductor-electrolyte interfaces are usually positive holes and negative charged hydroxyl ions [43–46]. Thus etching reaction requires holes at the semiconductor surfaces. In this study, since any light sources to generate electron-hole pairs in the sample surfaces were not used, holes would be produced by another process in the samples. Since SiC has a wide band gap, thermal generation of the electron-hole pairs hardly occurs at room temperature. Another possible hole creation mechanism is an impact ionization process. As noted earlier, this etching was performed at applied voltage of about 25 V. For 6H-SiC with donor concentration of 10^{18} cm^{-3}, this voltage makes an electric field high enough (3×10^6 V/cm) to cause the impact ionization at the sample surfaces, if the sample-electrolyte interfaces has an ideal Schottky barrier [47, 48]. In fact, at a lower anodic voltage of 10 V, for

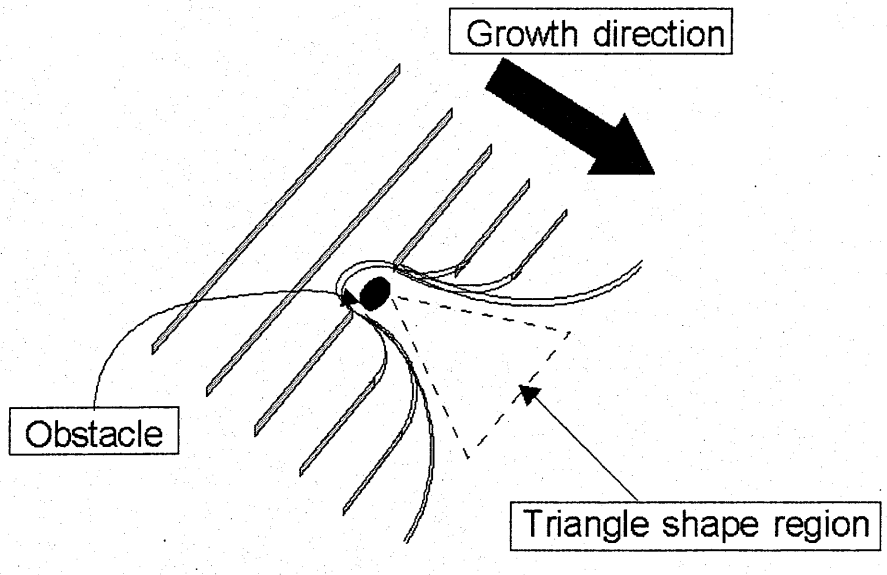

Figure 6.6: Schematic diagram for the creation mechanism of the triangle shape with different crystallinity from the other region during the crystal growth.

example, no etching phenomenon was observed. Thus, it is considered that the etching proceeds with the hole creation by the impact ionization process. The appearance of the etch pits implies that the impact ionization coefficient at the etch pit points is different from that in the rest of the surface. If the etch pits originate from the positions with the enhanced impact ionization coefficient, it is natural that they can be observed after the electrochemical etching but not after the molten KOH etching. It is not clear that what kinds of defects give rise to the enhancement of the impact ionization. Considering the results of the microscope Raman measurements, the enhancement would be due to some subtle differences in crystallinity or impurity concentration. Even in the electrochemical etching, when the KOH concentration or temperature were changed, the etch pits did not appear. Since the impact ionization coefficient depends on temperature and the electric field, its difference seems clear only in the etching under the condition employed in this paper.

Kayambaki *et al.* have reported that electrochemical etching with an aqueous KOH solution results in quite different morphologies between the Si and C faces for 4H- and 6H-SiC [11]. However, it was not found significant difference between the Si and C faces in the present etching condition. Kayambaki *et al.* have also reported that round shape etch pits appear after the electrochemical etching [11]. Their results and results from this study are quite different. Their data for Si face etching are for epitaxial layer etching, but the samples used in this study are bulk 6H-SiC. They employed p-type SiC

while the samples used in this study are n-type SiC. Since p-type SiC has a large number of positive holes in thermal equilibrium, the impact ionization process is not necessary for the reaction with hydroxyl ions. And they employed a 0.05 M KOH electrolytic solution, which is of two order of magnitude lower concentration than that employed in this study. It is expected that these differences cause the large differences in the experimental results.

6.3.2 Application to device fabrication

Firstly, the best etching condition for making smooth etched surfaces with an acceptable etching rate has been investigated by changing KOH concentration, crystal polarity, light illumination and temperature. The current density was fixed at 5 mA/cm^2 and etching rates at many etching conditions were observed. Figure 6.7 shows etching rates for Si and C faces both with and without light illumination at room temperature for 5 mA/cm^2. The etching rates for both the Si and C faces are increased by the light illumination. The etching rates for the C face are higher than those for the Si face as in the case of molten KOH etching [49, 50]. Except for the etching for the C face without light illumination, the etching rates show maximum at a KOH concentration of 1 wt.%. At high KOH concentration (>10 wt.%), SEM observation revealed that etched surfaces have porous structures. The porous structure results in apparently low etching rates, because the etching rates from etched depth measurements were measured by a profilometer which cannot probe the bottom of small diameter pores.

Figure 6.8 shows the etching rates in the temperature range of 5-10°C. The etching rates become lower than those at room temperature. In this case, at 10 wt.% KOH concentration, the highest etching rates are obtained for all the conditions. At 0.1 wt.% KOH concentration without light, direct etching did not occur but anodic oxidation of SiC seemed to occur, because during the experiments the voltage increased with time, which means that the resistance of the SiC-electrolyte interface increased. After the experiments, the surface showed interference color due to a transparent film on it. The films were removed before the characterization, because a $HF:HNO_3$ solution was employed in order to remove silicone resin.

Figure 6.9 shows etching rates in the temperature range of 50-55°C. The etching rates become around 20-50 nm/min but the etched surfaces have large roughness especially at high KOH concentrations. The roughness becomes the same order of magnitude as the etched depth for higher than 10 wt.% KOH concentration and leads to poorly reliable estimation of the etching rates because of difficulty in profiling a step between the etched and non-etched surfaces. In this temperature range, the light illumination does not always enhance the etching rates and the etching rates for the C face are not necessarily larger than those for the Si face. Thus the etching reaction may differ from that in the lower temperature range.

In most of the etching conditions described above, the etching seems to proceed with repeat of oxide film growth and removal, because the periodical oscillation of voltage during the etching was observed at or below room temperature. The voltage oscillation during the etching is shown in Fig. 6.10. The oscillation of voltage and

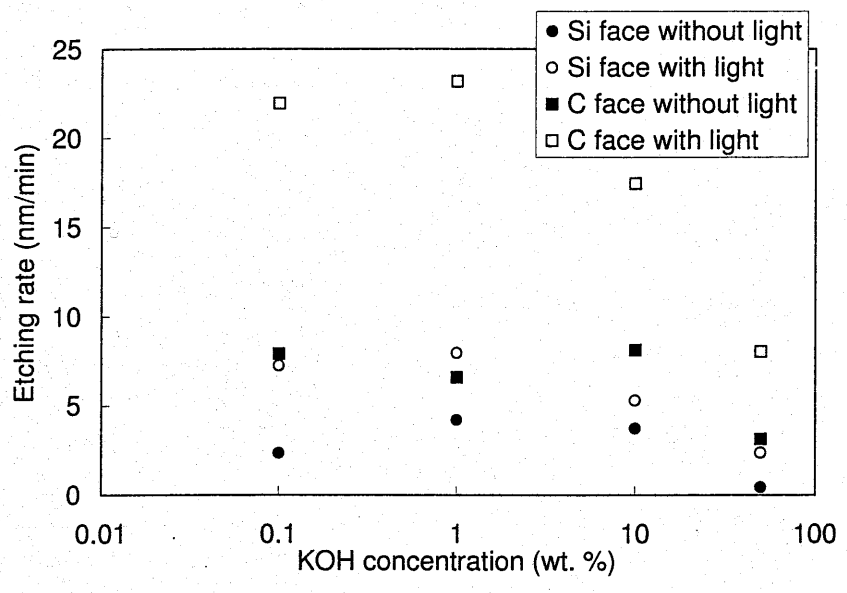

Figure 6.7: Electrochemical etching rates for 6H-SiC for various KOH concentrations at room temperature.

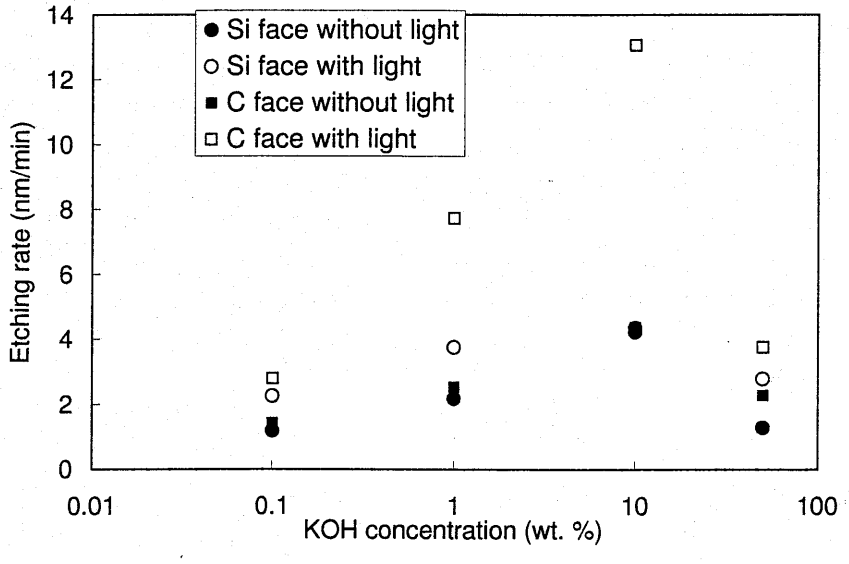

Figure 6.8: Electrochemical etching rates in the temperature range of 5-10°C.

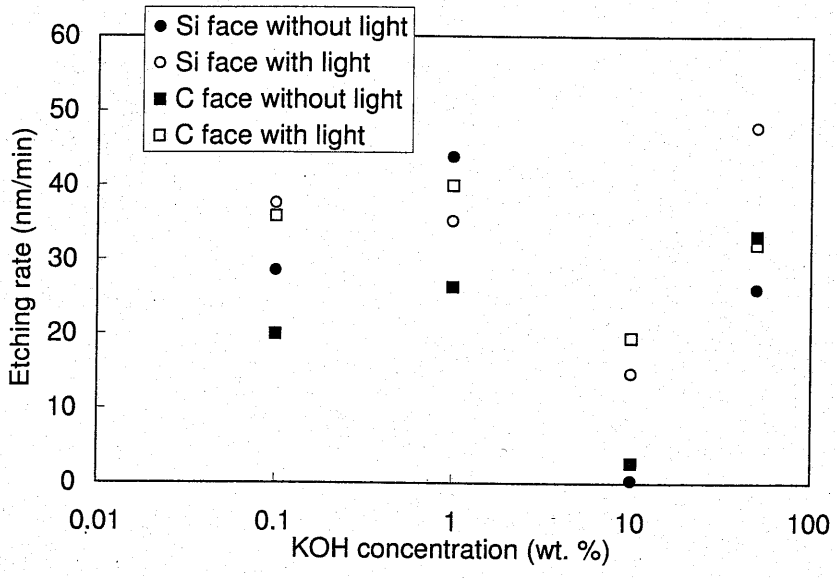

Figure 6.9: Electrochemical etching rates in the temperature range of 50-55°C.

the repeat of oxide growth and removal has been observed in anodization of Si [51]. Under the high temperature conditions, there was no voltage oscillation during the etching and the voltage was almost zero as shown in Fig. 6.10. The silicon oxide has high solubility in high temperature alkaline solutions [52]. Thus under the high temperature conditions, oxide films did not grow but dissolved into the electrolytes. Bubble formation at the exposed surface during the etching was also observed at all the temperature ranges. This implies that C atoms might become CO_2 or CO gas during the etching. It has been reported that the oxygen has a essential role even in the molten KOH etching [49, 50]. Thus it is considered that the oxidation process plays an important role in the electrochemical etching.

In the etching conditions with current density of 5 mA/cm^2, etched surfaces were no longer mirror-like. Figure 6.11 shows an example of the roughened surface. There are many grooves and circular pits in the etched surface. The grooves can be separated by two groups. The one is high contrast and straight grooves, which seems parallel with $< 1\bar{1}00 >$ orientation. This phenomenon is similar with the etch pits row appearance in the molten KOH etching, [53] This etch pits row is also parallel with $< 1\bar{1}00 >$ orientation and considered that its origin is the subgrain boundary. [53] Therefore, these high contrast and straight grooves in Fig. 6.11 could originate from the subgrain boundary. The other kind of grooves are curved and has low contrast. The origin of these grooves is unclear, but it may be dislocation loop.

In order to improve the flatness of the etched surface, the current density was de-

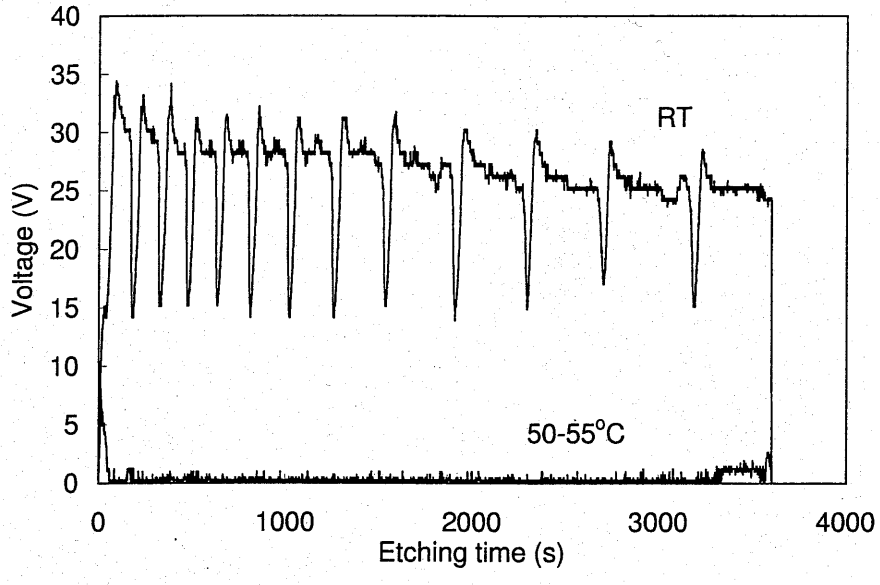

Figure 6.10: Voltage variation for the etching in 10 wt.% KOH with light illumination for the C face at room temperature and 50-55°C.

creased from 5 to 1 mA/cm^2. At this current density, a temperature of 50-55°C, 1 wt.% KOH concentration and with light illumination, a flat and mirror-like etched surface was obtained for the Si face. Figure 6.12 shows a Nomarski microscope picture for the surface etched in the above mentioned condition. An etched depth and time were 1.3 μm and 1 hour, respectively, and thus etching rate is 22 nm/min. The etched region is a lower part of the figure and there is no prominent roughness in it. The root mean square (Rms) roughness within 5 mm^2 area is evaluated by AFM. The Rms for the etched surface is 9.6 nm, which is larger than that for the non-etched (as-received) surface, 0.21 nm. In an atomic scale, the etched surface becomes rough.

Patterned structures were fabricated by using this etching method. A Ni metal was employed as a mask material and the etching condition is the same as that described in Fig. 6.12 except for the etching time, which was increased to 4 hours. SEM micrographs for the patterned structures are shown in Fig. 6.13. The patterned structures were observed, and thus Ni metal is effective as a mask material. Since Ni metal becomes a mask not only for the chemical attack by the electrolytes but also light illumination which enhances the etching by generating holes, the masked region seemed not to be etched. However, even though the mask metal has a fine pattern with its minimum length of 10 μm before the etching, the etched pattern is not so fine and smaller than the mask pattern, and the side wall at masked region is rough. The reason of this is that generated holes diffuse into under the masked region and enhance lateral overetching.

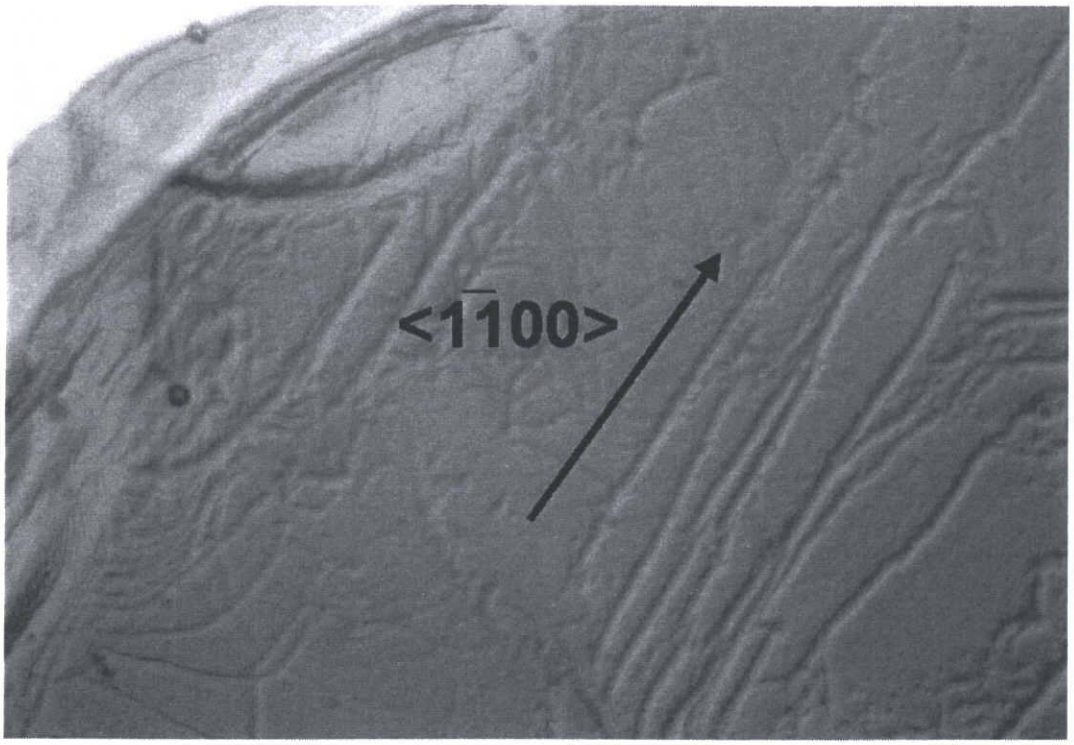

Figure 6.11: Optical micrograph for the C face surface etched in 10 wt.% KOH at 50-55°C with light illumination using 5 mA/cm^2 current density for 1 hour.

The diffusion length of holes, Lp, is roughly calculated as following. The Lp is expressed by $Lp = (Dp \times \tau_p)^{1/2}$, where Dp is the diffusion coefficient of holes and τ_p is the hole lifetime. The Dp can be calculated from the Einstein relationship by using hole mobility data. The reported hole mobilities are 40-100 cm^2/V·s and the data from the sample with the nearest impurity concentration is 83 cm^2/V·s [54]. From this value, Dp is calculated to 2.4 cm^2/s. And τ_p has been reported as 0.03-0.3 μs in epitaxial layer [55]. In this calculation, since samples used in this study were bulk crystal, the shortest time of 0.03 μm is adopted as τ_p . From these value, the calculated hole diffusion length is 2.7 μm, which is the same order of magnitude as the pattern scale. Thus it is considered that diffusion of holes is the most serious problem for success of fine patterned electrochemical etching. If we use the etching method for better crystalline quality epitaxial SiC, the diffusion coefficient and hole lifetime would be larger. Unfortunately the fine patterned etching is difficult for the good crystal.

For device fabrication, we must take care about contamination. In this etching method, K atom is thought to a major contaminant. AES measurements were performed to the etched surface to see K contamination, and no K peak was observed. The AES spectrum was taken after exposure in HF:HNO_3. This chemical cleaning may remove the K atoms, and the contamination is less than the detection limit of the AES measurement.

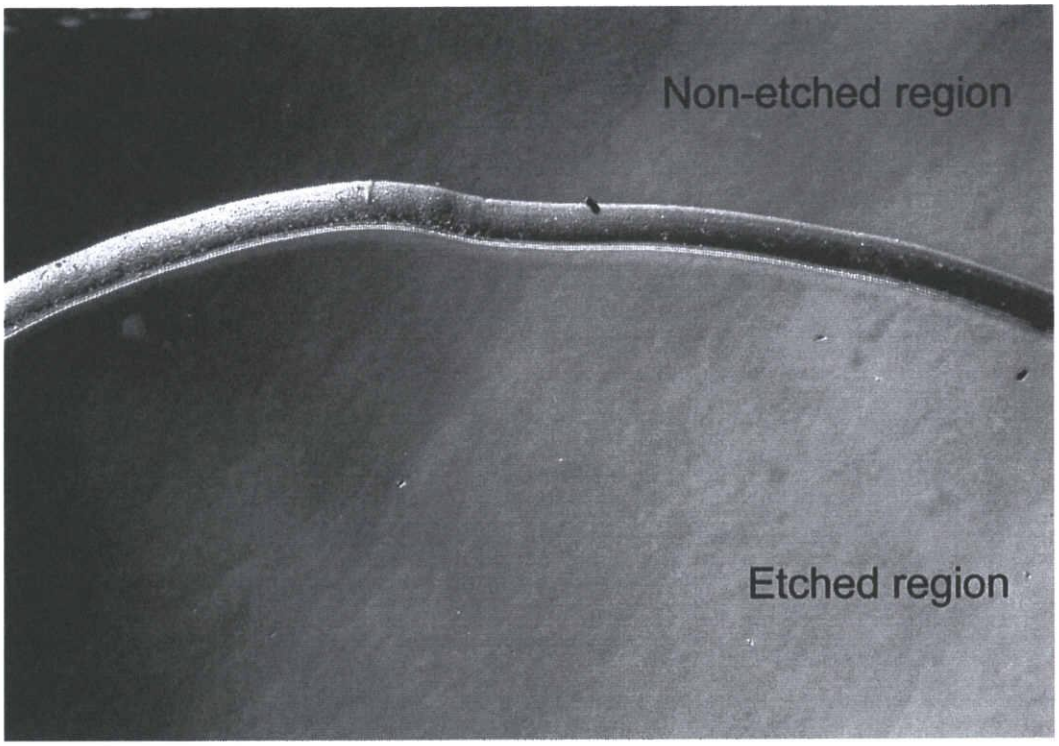

Figure 6.12: Optical micrograph for the Si face surface etched in 1 wt.% KOH at 50-55°C with light illumination using 1 mA/cm^2 current density for 1 hour.

6.4 Conclusion

n-type 6H-SiC samples were electrochemically etched using an aqueous KOH solutions as electrolytes. In a condition of 50 wt.% KOH concentration and current density of 5 mA/cm^2 without light illumination at room temperature, etched surfaces showed many triangle etch pits accompanied with a crescent or circle etch pit. The paired pits aligned in the radial direction from the wafer center. The triangle pit was in the wafer perimeter side with its base facing the perimeter. From the optical microscope observation with the crossed polarizer, the origin of the etch-pit was not only micropipe but also other kinds of defects, most probably screw dislocation.

In all the etching condition, the etching rates depended on surface polarity, KOH concentration, temperature and light illumination. At high temperatures (50-55°C), the etching rates were high but the surfaces become rough. At a decreased current density (1 mA/cm^2), surface roughness after the etching was suppressed. The patterned structures were fabricated by using a Ni mask and this etching method.

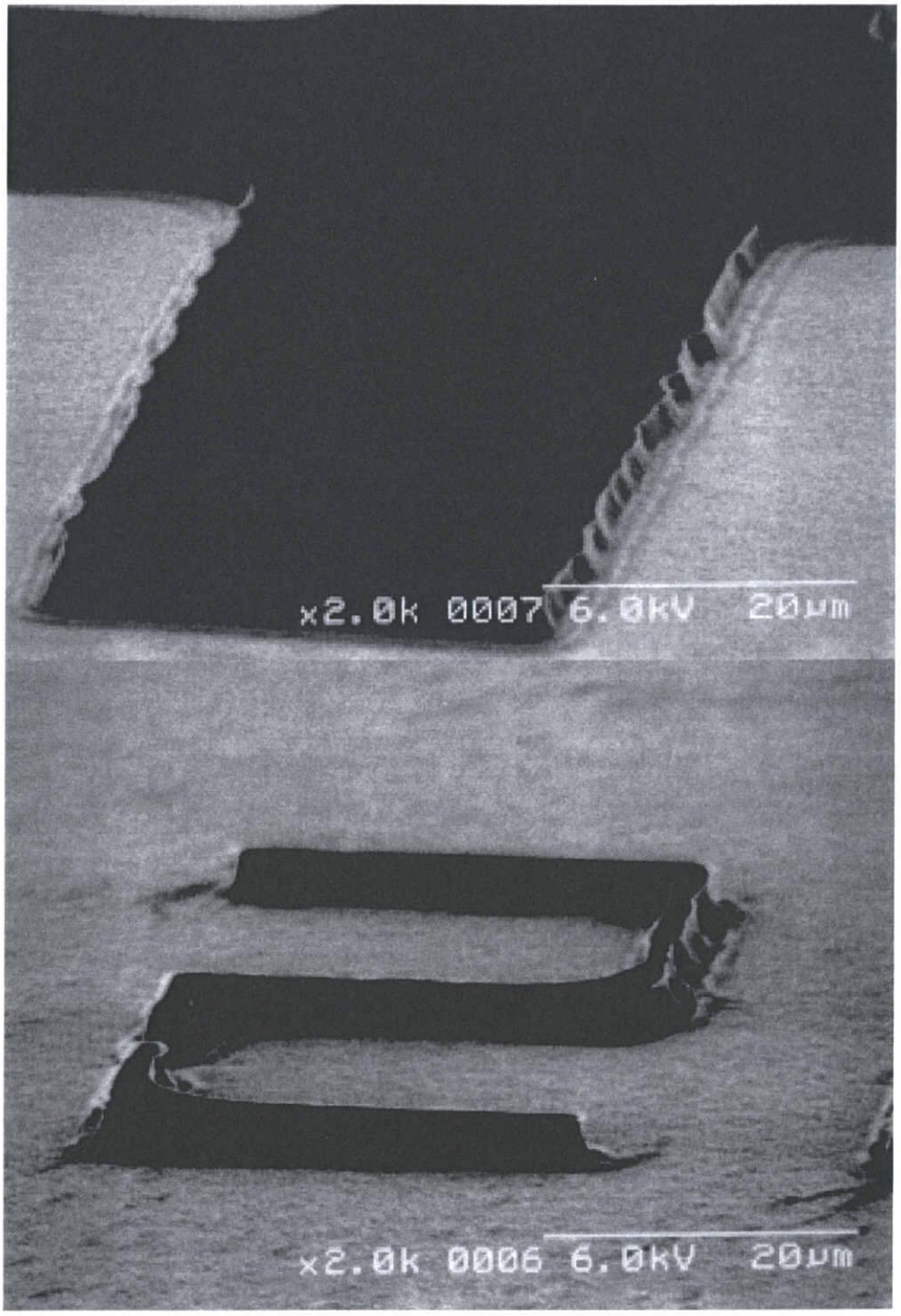

Figure 6.13: Patterned structure fabricated by the electrochemical etching with a Ni metal mask. (The pictures were taken after Ni mask removal.) Etching condition is the same as that described in Fig. 6.12.

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Chapter 7

Conclusion

7.1 Conclusion of this work

In this work, DLTS, CTS and O-CTS measurements have been employed for characterization of SiC and electrochemical techniques were used for oxidation and etching of SiC. Following results have been obtained.

Deep levels in the band gap of 3C-SiC were characterized by DLTS, CTS and O-CTS. It is found that a deep level commonly exists in 3C-SiC, and it is named the ND1 center which is a donor-like defect and has a thermal activation energy of 0.44 eV with zero electric field and an optical threshold energy of 0.47 eV. The Frank-Condon shift for the ND1 center is 0.13 eV and a configuration coordinate diagram for the ND1 center is drawn. (In fact, recent experiments and comparison with theoretical equation reveal that the actual optical threshold energy is 0.51 eV, and thus the Frank-Condon shift for the ND1 center is 0.17 eV [1, 2].) Deep levels with thermal activation energy of 0.35-0.75 eV are also observed and no deep level with 0.75-1.0 eV thermal activation energy is observed. In addition, small density of deep levels with optical threshold energy of about 1.4 eV is observed.

Hydrogen passivation effects for the deep levels in 3C-SiC are investigated. It is found that the ND1 center and other defects can be passivated by a hydrogen plasma treatment. However, the hydrogen plasma treatment also introduces damages in the sample surface. By inserting a grid between plasma source and 3C-SiC, the damages are suppressed. The hydrogen plasma treatment with the grid and subsequent annealing at 300°C makes 3C-SiC with the lowest deep level concentration of less than 10^{14} cm^{-3} within this work.

Deep levels in 4H-SiC epitaxial layers grown on substrates with inclination toward $< 1\bar{1}00 >$ are investigated. Deep level densities do not depend on the substrate inclined direction but epitaxial layer thickness and they decrease with increase of epilayer thickness. The epitaxial 4H-SiC layers on the substrates with inclination toward $< 1\bar{1}00 >$ have the same crystalline quality as epitaxial layers on the substrates with inclination toward $< 11\bar{2}0 >$.

Anodic oxidation of 6H-SiC has been performed. The anodic oxidation method can form silicon dioxide layer on 6H-SiC. The oxidation rate for the anodic oxidation is

much higher than that for thermal oxidation but apparent consumed SiC layer during oxidation is only 1/8 of the oxide thickness. By using the anodic oxidation as a sacrificial oxidation before contact formation, Al ohmic contact resistance is reduced and Schottky barrier heights of Au and Ni contacts become higher than those on surfaces without sacrificial oxidation. These contacts properties are similar with the contact properties on the surface after sacrificial thermal oxidation. The results show that sacrificial anodic oxidation is expected to substitute for sacrificial thermal oxidation.

Anodic etching of 6H-SiC has been performed. This etching method can disclose crystalline defects as etch pits in a particular etching condition. The etch pits have a peculiar shape and seem to reflect crystal growth mechanism. The etch pits would originate from micropipes and screw dislocations existing in the crystal. And etching in another condition with a lower current density, etched surfaces do not show observable roughness even seeing through a microscope. By using this etching condition, patterned structures on 6H-SiC surfaces are fabricated. It would be useful for fabrication of devices, which requires an etching process.

7.2 Suggestions for future works

In fact, 3C-SiC samples characterized in this study have relatively poor crystalline quality. The samples have high density of APB's and twins. Thus, I'm not sure that the observed information is general trend in 3C-SiC. As described in chapter 1, it has been reported that 3C-SiC with very low density of APB's and twins can be produced by growing on undulant Si substrates [3,4]. Deep level concentration in such a good crystal might be small and observable deep level may be different from those observed in this study. The difference should be compared and we should establish common information about deep levels in 3C-SiC.

Hydrogen passivation effects on deep levels in 3C-SiC were observed in this study, but the effects on deep levels in 4H-SiC have never been studied. 4H-SiC is the most prospective polytype for device application. The hydrogen effects on 4H-SiC should be investigated for getting information about defect passivation.

In epitaxial 4H-SiC, there is a very common deep level named a $Z_{1/2}$ center [5–7]. In this study, the $Z_{1/2}$ center is not observed in 4H-SiC samples. Properties of this center have not been fully revealed and an optical threshold energy for this center is not clear. It should be important to investigate its optical threshold energy by the O-CTS method.

In this study, it is proposed that the electrochemical method can be substitution for conventional processes. The usage for anodic oxidation suggested in this paper is sacrificial oxidation. However, typical usage of the oxidation process is to form insulating oxide films for gate and field oxide layers. If anodic oxide can be used to make good insulating films, the anodic oxidation process becomes prospective for making gate and field oxide layers.

Peculiar shape etch pits appear after the electrochemical etching under a certain condition. A reason of the peculiar shape formation is suggested but the suggested mechanism does not completely solve its formation process. I hope the mechanism will

be solved in future.

By using the electrochemical etching technique, patterned structures were fabricated. However, the pattern shape would not be fine enough for device fabrication. The limitation of the pattern precision was expected, and thus we should take into account that limitation and consider usage of this method. In my opinion, this method can be used for removal of subsurface damages caused by polishing or plasma etching.

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Appendix A

Principle of Capacitance Transient Measurements

A.1 Capacitance transient at the junction

Generally, in order to investigate deep levels in a semiconductor, we observe charge states at the junction, which are varied from the carrier emission, capture, recombination or generation accompanied by temperature, light illumination or bias condition change. At first, imagine p^+n junction (it is almost the same case as the Schottky junction) of a semiconductor. In this case, a depletion layer of the junction expand to n-type region. It is assumed that there is a deep level above a half of the band gap and it acts as an electron trap. A time dependent electron density at the deep level is defined from the Shockley-Read-Hall (SRH) statistics as a following equation.

$$\frac{dn_t}{dt} = c_n(N_t - n_t) - e_n n_t - c_p p n_t + e_p(N_t - n_t), \tag{A.1}$$

where c_n and e_n are capture and emission rates for electrons, respectively, c_p and e_p are capture and emission rates for holes, respectively, n is a electron density in the conduction band, p is a hole density in the valence band, and N_t is a density of the deep level. In Fig A.1, charge state change at the junction accompanied by bias condition change is shown. Figure A.1 (a) indicates a band diagram at a low reverse bias condition in which deep levels below the Fermi level trap electrons. The depletion layer width is relatively short. The bias making this condition is called injection bias (or electron filling pulse) in DLTS measurements. Figure A.1 (b) indicates a condition of the diode immediately after applying high reverse bias. In this condition, depletion layer width is expanded, and the Fermi level energy in n-type region is lowered in comparison with that at the low bias condition (the Fermi level in this condition is, in fact, the pseudo-Fermi level). A part of deep levels which is trapping electrons becomes located above the pseudo-Fermi level. The electrons in this part will be emitted to conduction band as following equation (because of $c_n = c_p = 0$).

$$\frac{dn_t}{dt} = -(e_n + e_p)n_t + e_p N_t. \tag{A.2}$$

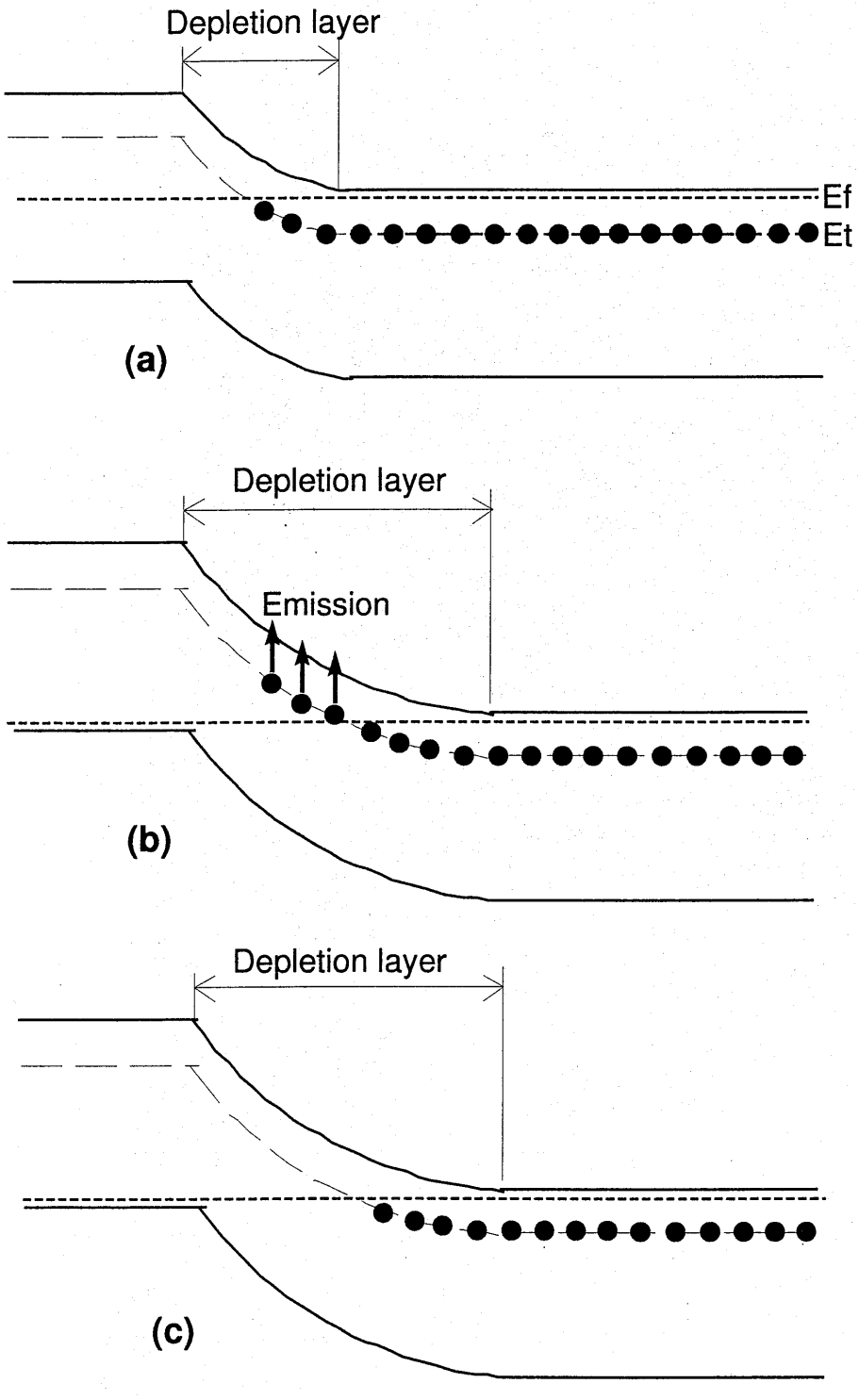

Figure A.1: Band diagrams of the Schottky diode with different bias conditions (a) a relatively low reverse bias condition (b) a condition immediately after high reverse bias (c) a stable reverse bias condition after the electron emission.

After the emission, the diode condition becomes stable at $t = \infty$, and the deep levels above the pseudo-Fermi level have no electron as well as the condition of Fig. A.1 (a). Thus, we can define the boundary condition of $n_t = N_t \mid_{t=0}, n_t = 0 \mid_{t=\infty}$, and by using them the equation A.2 is solved as,

$$n_t = \frac{e_p}{e_n + e_p} N_t + \frac{e_n}{e_n + e_p} \exp\{-(e_n + e_p)t\}. \tag{A.3}$$

Here, since we are considering the electron trap, the equation A.3 is approximated by using $e_n \gg e_p$ as following.

$$n_t = N_t \exp(-e_n t). \tag{A.4}$$

The e_n can be rewritten as τ^{-1} and thus

$$n_t = N_t \exp\left(-\frac{t}{\tau}\right). \tag{A.5}$$

From this equation, the deep level located above the pseudo-Fermi emits electrons with time constant of τ. Here, a capacitance originating from the junction is expressed as

$$C = \frac{\varepsilon A}{W} = \left\{\frac{q\varepsilon N_d}{2(V_b + V_r)}\right\}^{1/2} A, \tag{A.6}$$

where ε is the dielectric constant of the semiconductor material, A is the cross section of the junction, W is the depletion layer width, q is the charge of an electron, N_d is the net donor concentration in the depletion layer, V_b is the built in potential of the junction and V_r is applied reverse bias voltage. Since the capacitance depends on net charge in the depletion layer, it depends on time because of the electron emission from deep level as indicated by equation A.5. Thus, when the deep level is a donor-like,

$$C(t) = \left[\frac{q\varepsilon\{N_d - n_t(t)\}}{2(V_b + V_r)}\right]^{1/2} A. \tag{A.7}$$

When $N_t \gg N_d$, this equation can be approximated as following,

$$C(t) = \left\{\frac{q\varepsilon N_d}{2(V_b + V_r)}\right\}^{1/2} A\left\{1 - \frac{N_t}{2N_d}\exp\left(-\frac{t}{\tau}\right)\right\}. \tag{A.8}$$

From this equation, the capacitance change caused by application of the reverse bias is exponential with the same time constant as that of the electron emission, τ. If we define the capacitance at $t = 0$ and $t = \infty$ as C_0 and C_∞, respectively, we can obtain

$$C_0 = \left\{\frac{q\varepsilon N_d}{2(V_b + V_r)}\right\}^{1/2} A\left(1 - \frac{N_t}{2N_d}\right) \tag{A.9}$$

and

$$C_\infty = \left\{\frac{q\varepsilon N_d}{2(V_b + V_r)}\right\}^{1/2} A. \tag{A.10}$$

The net capacitance change $\Delta C = C_\infty - C_0$ is expressed as

$$\Delta C = \left\{ \frac{q\varepsilon N_d}{2(V_b + V_r)} \right\}^{1/2} A \frac{N_t}{2N_d} = C_\infty \frac{N_t}{2N_d}. \tag{A.11}$$

Thus we can obtain the deep level concentration, $N_t = 2N_d(\Delta C/C_\infty)$. And equation A.8 is written by using C_0 and C_∞ as

$$C(t) = C_\infty - \Delta C \exp\left(-\frac{t}{\tau}\right) \tag{A.12}$$

From above equations we can see the electron emission rate from the deep level and the deep level concentration by observation of the capacitance transient.

A.2 Deep level transient spectroscopy (DLTS)

Figure A.2 shows a basic idea of the DLTS measurement [1]. Figure A.2 (a) shows capacitance transient signals at various temperature accompanied by a bias change shown in Fig. A.2 (c). This capacitance transient is expressed as equation A.12. *tau* in this equation strongly depends on temperature. At high temperature, τ is relatively small and while at low temperature τ is relatively large as shown in Fig. A.2 (a). We observe capacitance at time t_1 and t_2 normalized by the time of reverse bias application. If we subtract $C(t_1)$ from $C(t_2)$, we can get a DLTS signal of corresponding temperature,

$$dC = \Delta C \left\{ \exp\left(-\frac{t_1}{\tau}\right) - \exp\left(-\frac{t_2}{\tau}\right) \right\}. \tag{A.13}$$

This signal vary with temperature as shown in Fig. A.2 (b). A time constant for maximum DLTS signal, τ_{max}, is

$$\tau_{max} = \frac{t_1 - t_2}{\log \frac{t_1}{t_2}}. \tag{A.14}$$

τ_{max} is determined by t_1 and t_2. A value of $t_1 - t_2$ is called as the rate window. When we measure DLTS signal with various rate windows, the peak temperature corresponding with the rate windows, T_{max}, is obtained, and we can see temperature dependence of τ_{max}. The peak height also provides the deep level concentration.

In this work, t_1 and t_2 sampling was not employed in the DLTS measurements, but the bipolar rectangular weighting function was employed [2]. This weighting function improves S/N because of its signal integration procedure. Figure A.3 shows bias change, capacitance change and the weighting function, where t_p is time of the filling pulse, t_d is a delay time after the reverse bias application for waiting of the response time of the capacitance meter, t_w is a time for weighting function application to the signal. At the first half of t_w, the weight is +1 and, at second half of t_w, the weight is -1 as shown in Fig. A.3 (c). By applying this weighting function at equation A.12, we can obtain the DLTS signal as

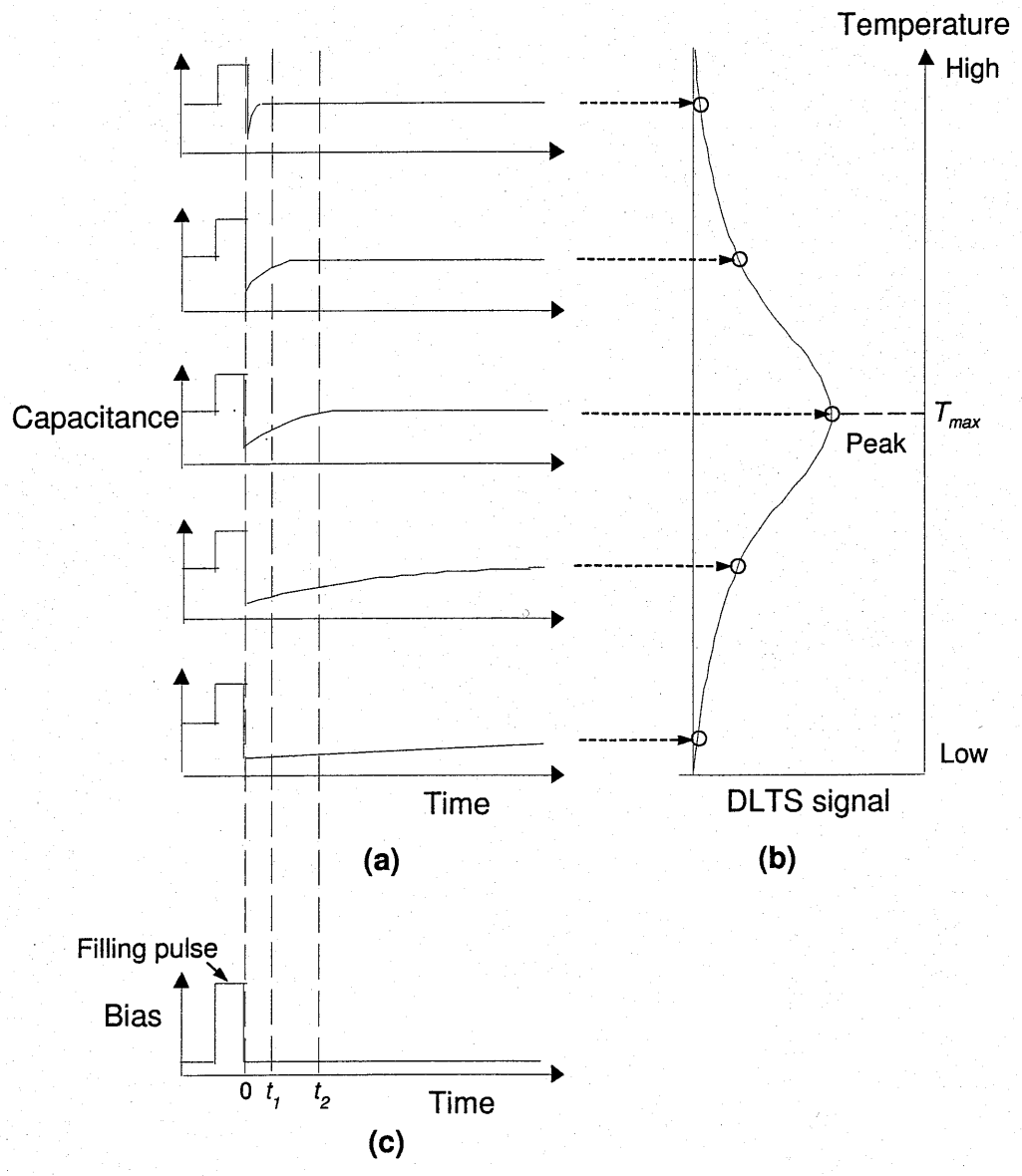

Figure A.2: A basic idea of the DLTS measurement. (a) Capacitance transient signals at various temperature. (b) DLTS signals deduced from the capacitance transient signals. (c) Bias change to lead the capacitance transient.

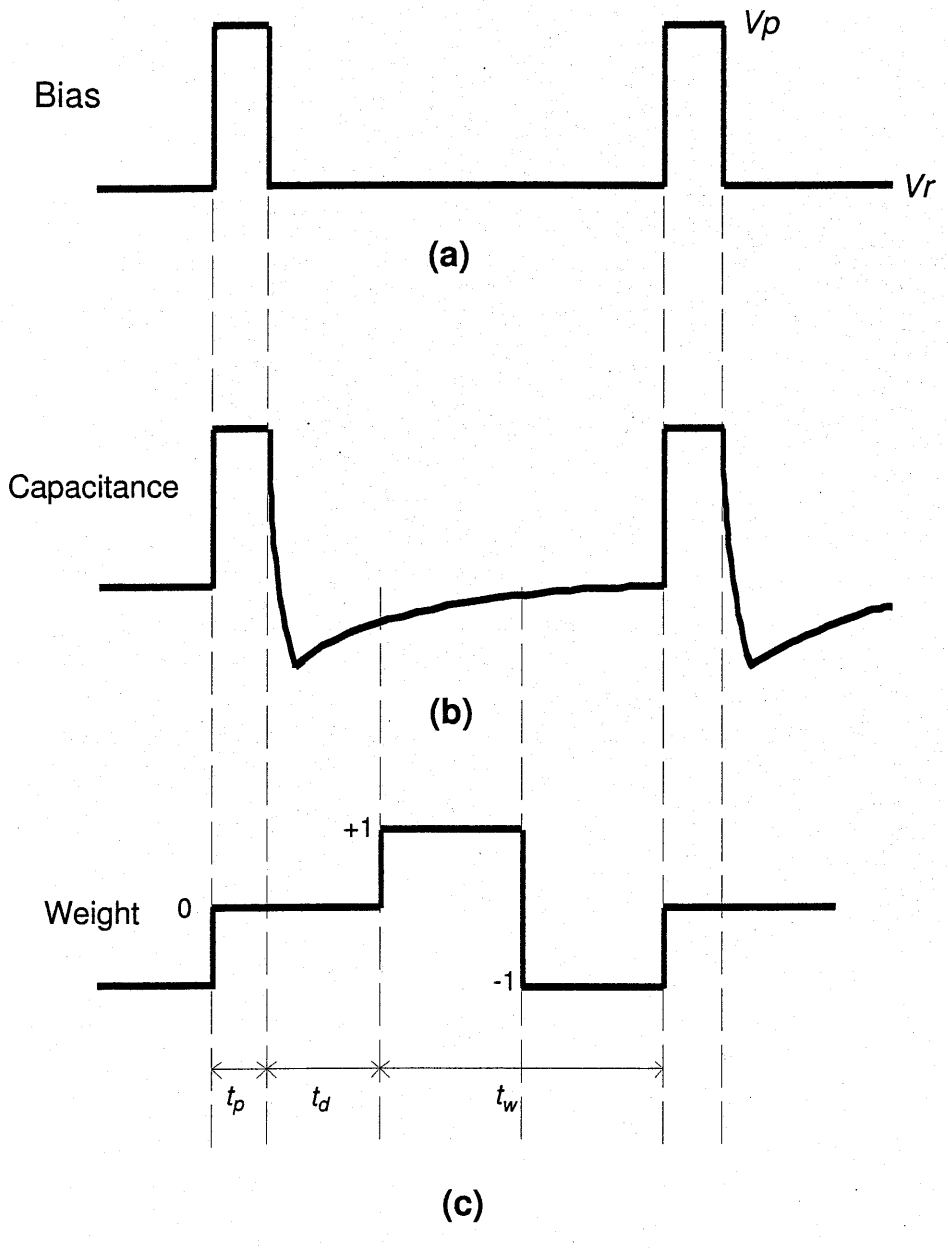

Figure A.3: Schematic of the bipolar rectangular weighting function. (a) Bias change to lead capacitance transient. (b) Capacitance transient signals. (c) Weighting function.

$$V_0 = \frac{1}{t_w}\left\{\int_{t_d}^{t_d+\frac{t_w}{2}} C(t)dt - \int_{t_d+\frac{t_w}{2}}^{t_d+t_w} C(t)dt\right\} = -\frac{\Delta C\tau}{t_w}\exp\left(-\frac{t_d}{\tau}\right)\left\{1-\exp\left(-\frac{t_w}{2\tau}\right)\right\}. \tag{A.15}$$

τ_{max} is deduced from $dV_0/\tau = 0$,

$$\exp\left(\frac{t_w}{2\tau_{max}}\right) = \frac{1+\frac{t_d}{\tau_{max}}+\frac{t_w}{\tau_{max}}}{1+\frac{t_d}{\tau_{max}}}. \tag{A.16}$$

By substituting t_d and t_w, τ_{max} can be obtained from this equation. In this work, t_d/t_w has been fixed at $1/2$, and in this case $\tau_{max} = t_d/0.523$.

In this work, the capacitance transient spectroscopy (CTS) is performed in chater 2. The difference of this method from the DLTS is that the DLTS signals are obtained for several fixed τ_{max} calculated from equation A.16 with scanning temperature, while the CTS signals are obtained for several fixed temperature with scanning t_d and t_w, which determine τ_{max} [3]. We can get the same information from these two measurements, but the DLTS has an advantage for observation of a wide energy range while the CTS has advantages for S/N ratio and separation of superimposed peaks in a DLTS spectrum. The CTS method is almost the same as other capacitance transient measurements, so called the isothermal capacitance transient spectroscopy (ICTS) and time analyzed transient spectroscopy (TATS) [4–6]. Differences among them are only signal treatment method, and thus information taken from these measurements are completely the same.

A.3 Evaluation of energy levels

The DLTS and CTS measurements give τ due to thermal excitation of carrier. τ is expressed as

$$\frac{1}{\tau} = \sigma v_T N_c \exp\left(-\frac{E_t}{kT}\right), \tag{A.17}$$

where σ is the capture cross section for the deep level, v_T is the thermal velocity of the carrier, N_c is the effective density of states for the conduction band, E_t is absolute energy of the deep level from the conduction (or valence) band and k is the Boltzmann constant. Here $v_T \propto T^{1/2}$ and $N_c \propto T^{3/2}$, thus equation A.17 becomes

$$\frac{1}{\tau T^2} = \text{const.} \cdot \sigma \exp\left(-\frac{E_t}{kT}\right) \tag{A.18}$$

From this equation, if σ has no temperature dependence, we can plot τT^2 as a function of $1/T$. The plot become straight line, and its slope provides the energy level and its intercept at $T = \infty$ provides capture cross section at infinite temperature. In experiments, for getting the exact energy level, we must consider temperature dependence of the capture cross section.

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