Investigation of MIS-type GaN- based HEMT grown by MOCVD on silicon (111) substrate

（MOCVD 法を用いて成長したシリコン基板(111)上 MIS 型窒化ガリウム系 HEMT に関する研究）

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Joseph J. Freedsman

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Abstract

In this study, metal-organic chemical vapor disposition (MOCVD) grown GaN based metal-insulator/oxide-semiconductor high-electron-mobility transistors (MIS-HEMTs) on silicon (111) substrate are presented. In order to reduce the AlGaN/GaN heterostructure related traps, thicker super-lattice structures (SLS) were employed. A detailed XRC and Hall measurements of the AlGaN/GaN HEMT heterostructures grown using thicker SLS showed reduced edge dislocation densities and increased Hall mobilities. Trap characterization by frequency dependent conductance analyses (FDCA) showed a remarkable decrease in fast traps related to the AlGaN/GaN layers confirming improvements in the AlGaN/GaN heterostructures.

A process compatible Al_2O_3 based AlGaN/GaN MOS-HEMT was discussed. The device characteristics of MOS-HEMT compared with the normal HEMT shows reduced gate leakage and higher breakdown voltage (BV). The BV and power device figure-of-merit (FOM) for Al_2O_3/AlGaN/GaN MOS-HEMT was 431 V and 1.89 x 10^8 $V^2\Omega^{-1}cm^{-2}$ respectively. The trapping characteristics by FDCA on the MOS-HEMT showed the surface related slow traps (~ms) has been passivated by Al_2O_3 layer.

The importance of using a thin *in-situ* MOCVD grown AlN as a passivating layer for AlGaN/GaN MIS-HEMTs on Si was also discussed. The trapping analyses and device characterizations revealed that low growth temperature of AlN layer favor less defect AlN/AlGaN/GaN MIS-HEMT structures.

Therefore, the AlGaN/GaN heterostructure related traps can be minimized by growing the AlGaN/GaN heterostructures on thick buffer layers and the surface related traps can be minimized by using a passivating material or a high~κ insulating layer.

Chapter 1

Introduction

1.1. Foreword

The beginning of 21st century has seen enormous progress and advancements in the solid state electronics and its applications in the areas of wireless and tele-communications, information technology as well as radar and satellite appliances. The progress in electronics industry although could always compete with the demands and requirements of the global market. These requirements may include aspects of ultra-high power, high efficiency, high linearity, high operating frequency and high-speed switching devices. To meet the broad necessity, the integrated circuit with as many transistors with sub-micron sizes should be closely packed. The Moore's law even predicted that the number of silicon transistors per chip has doubled ever since its invention in early 1970's as a progress of very-large-scale-integration (VLSI). These demands have made the researchers to push the operating power performance in the pioneer silicon and later Ge and GaAs based electronic devices closed to theoretical limits. SiC then widely believed to be a better candidate, although it appeared to be not truly microwave technology in terms of its relatively low carrier transport properties.

Further, these challenges also opened up wide band gap GaN based materials to be suitable alternative workhorse and promising candidates to compete or over-run the race with the predecessors. The advantages in Al_xGaN/GaN based devices includes cost effective, large bandgap (3.4 eV), high breakdown limit ($\geq$ 3 MV/cm), high electron mobility ($\geq$ 1300 cm^2/vs at 300 K) and very high carrier saturation velocity ($v_{sat} \cong 2 \times 10^7$ cm/s). The various applications of GaN based high power and high frequency devices are

shown in fig. 1.1. These applications range from solid state lightings to space modules. As shown in the figure 1.1, GaN based high power radio frequency (rf) amplifiers find applications in satellites, wireless base stations and radio communications. Further, they find importance in defense and military warfare utilities and space modules etc. GaN based high voltage devices are used for power transmission purposes and grids. Other potential applications include Monolithic Microwave Integrated Circuits (MMICs) and high power amplifiers.

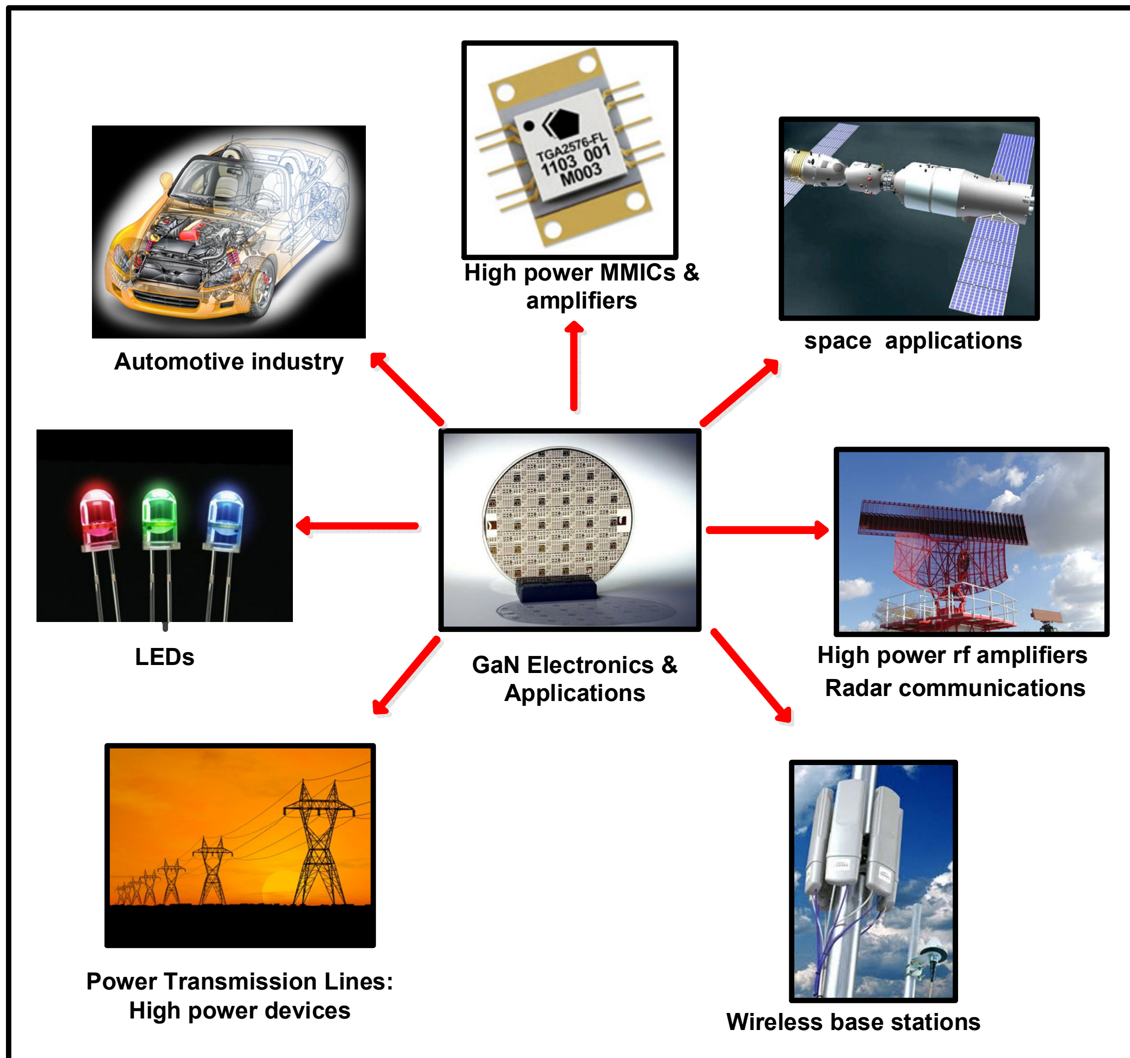

FIG. 1.1. Application areas of GaN based electronics.

1.2. Perspectives of GaN materials

Gallium Nitride and its related alloy materials are very promising for both active electronic devices as well as optoelectronic applications. The III-V nitride system such as GaN, AlN, InN and their alloys are all wide-band gap materials and are crystallized in the form mostly of Wurtzite (fig. 1.2) or Zincblende types.

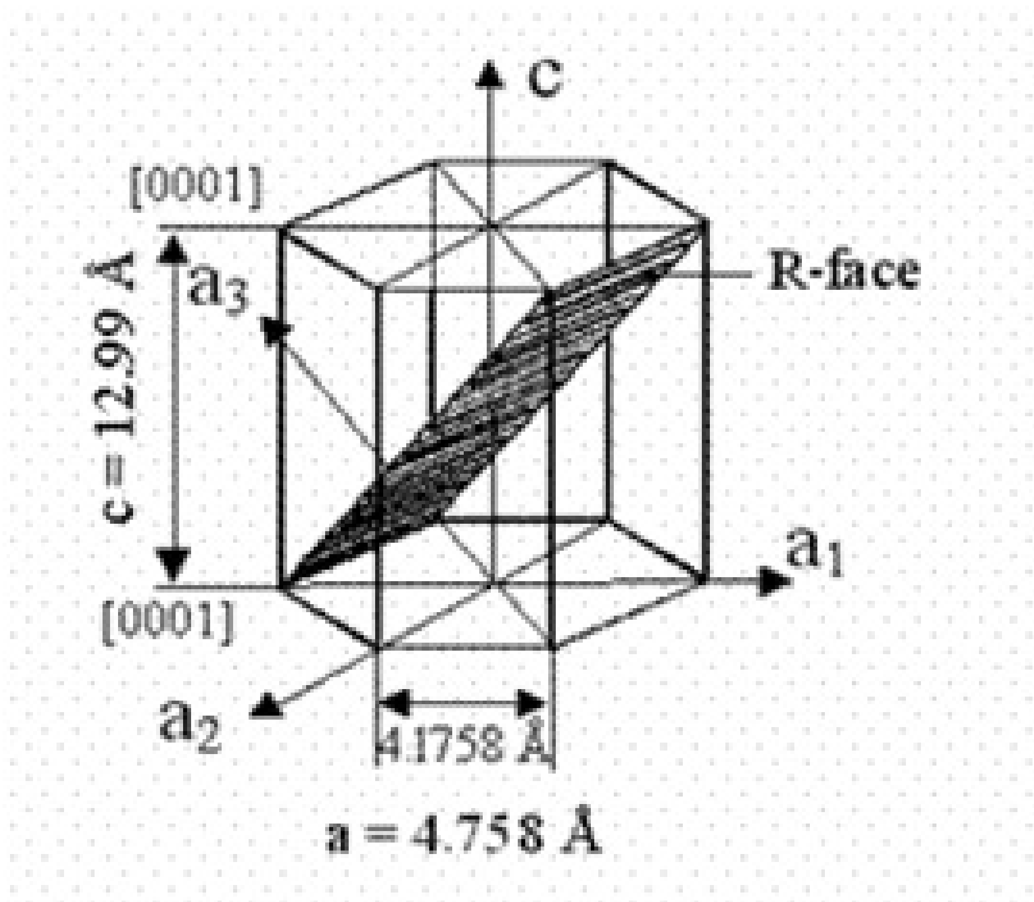

FIG. 1.2. Crystal structure of Wurtzite Gallium Nitride

Wurtzite AlN, GaN and InN have direct band gap energies of 6.2, 3.4 and 0.7 eV respectively (see fig. 1.3) for potential application in a broad spectrum of wavelength. Bandgap engineering and suitable alloy composition of the nitrides makes them favorable

candidates for blue-green and ultraviolet (UV) light emitting diodes (LEDs) [1-3], UV-lasers [4] and active photo detectors in the wavelength between visible and UV regions [5-6].

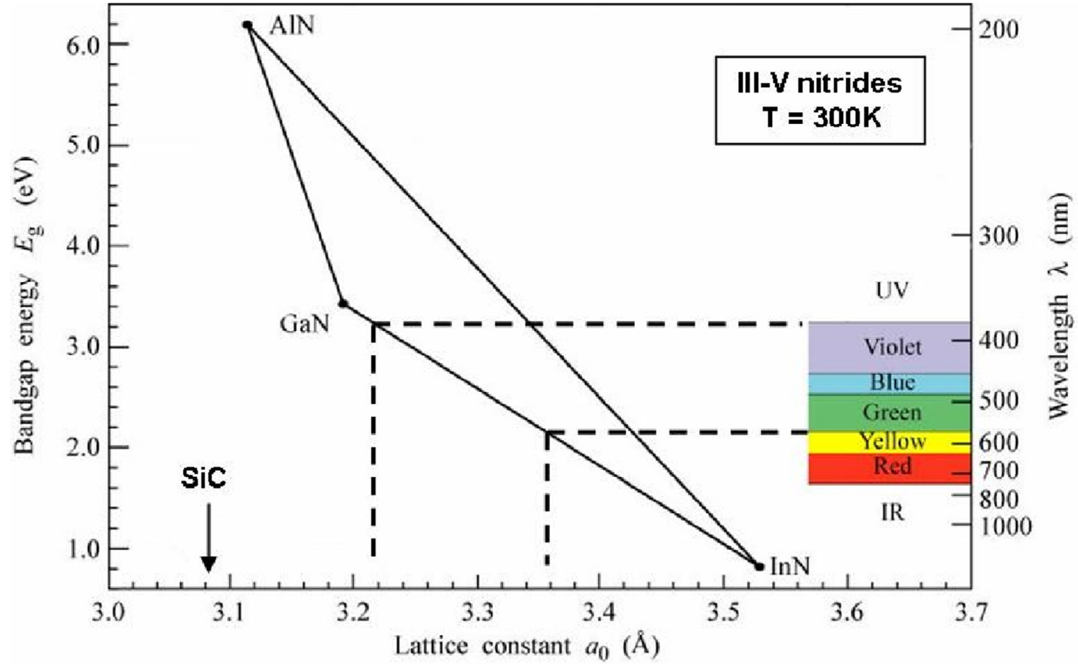

FIG. 1.3. Band gap energy and corresponding wavelength guide of wurtzite AlN, GaN, InN and their alloys versus their lattice constant (a) at room temperature.

Other promising prospects of GaN devices are that, they offer high power, high frequency and high temperature electronics. Again the wide band gap makes the GaN materials more favourable for high temperature applications, since they go intrinsic at elevated temperatures compared to the counterparts like Si, Ge and GaAs. The critical breakdown field of the GaN is approximately the square of the band gap energy and it has been theoretically estimated to be ≥ 3 MV/cm which is ten folds higher than the small bandgap semiconductors like Si and GaAs with relatively low breakdown values of 0.3

and 0.4 MV/cm respevtively [7]. This simply means that GaN devices can be used for high power applications which can operate at elevated temperature. Therfore less cooling is required and involves cost effective process to dissipiate the heat generated. Alongside, GaN has excellent carrier transport properities such as good moblity and drift velocity which are highly desirable for high speed switching devices and microwave rectifiers etc. The comparision of electronic properties of GaN with other leading semicondutor materials are presented in table. 1.1 [8-11]. With a high combined figure of merit (CFOM) value, it is unambiguously believed that GaN devices can deliver high power, high temperature and high frequency future needs.

Table. 1.1. Comparison of electronic properties of various semiconductors at 300 K.

Property	Si	GaAs	6H-SiC	4H-SiC	GaN
Bandgap E_g (eV)	1.12	1.43	2.86	3.02	3.39
Breakdown Field E_B (MV/cm)	0.3	0.4	2.4	2.2	3.0
Electron Mobility μ (cm^2/Vs)	1500	8500	800	460	2000
Drift Velocity $\upsilon_{s\text{-}max}$ (10^7 cm/s)	1.0	2.0	2.0	2.7	3.0
Thermal Conductivity χ (W/cmK)	1.5	0.5	4.9	4.9	1.5
Dielectric Constant ε	11.8	12.8	10	9.7	9.5
CFOM = $\chi.\varepsilon.\mu.\upsilon_s E_B{}^2/(\chi.\varepsilon.\mu.\upsilon_s. E_B{}^2)_{Si}$	1	7	295	222	290

(CFOM = Combined Figure Of Merit for high temperature, high power and high frequency applications)

The most amazing feature or property of wurtzite III-nitrides is the quantum well (see fig. 1.4) formed at the hetero-interface between GaN and AlGaN layers. A high concentration of two dimensional electron gas (2-DEG) is accumulated at the quantum well near the AlGaN/GaN heterointerface due to large conduction band discontinuity and

built-in piezoelectric (P_{Pe}) and spontaneous polarization (P_{Sp}) effects in AlGaN/GaN material system. This property makes the AlGaN/GaN heterostructure system more suitable for high power and high frequency electronics.

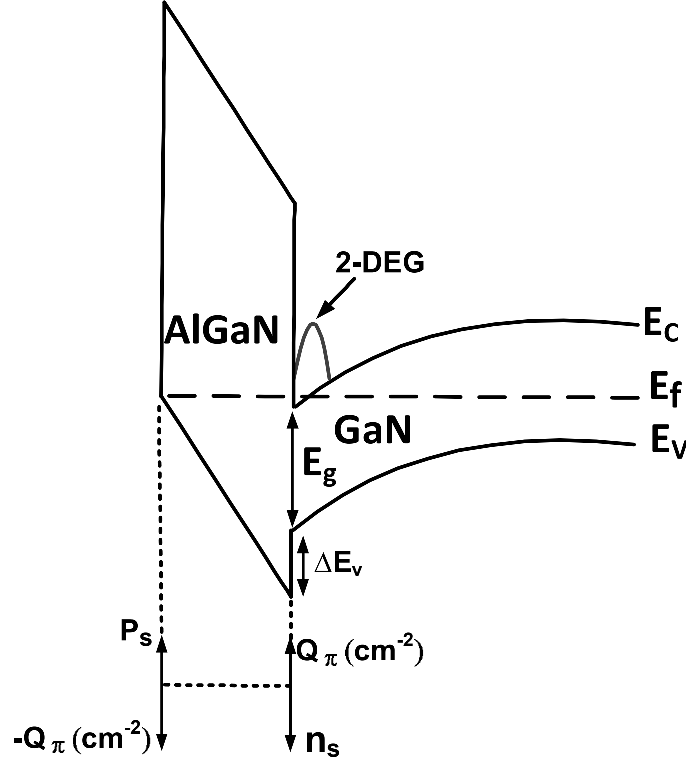

FIG. 1.4. Band diagram of AlGaN/GaN heterostructures with conduction band-discontinuity and formation of 2-DEG in the AlGaN/GaN quantum well.

The maximum output power (see fig. 1.5.) for the high power electronic device is given by the equation 1.1,

$$P_{max} = \frac{1}{8} V_{max}.\, I_{max} \tag{1.1}$$

$$I_{max} = V.n_s.\, \upsilon_{sat} \tag{1.2}$$

Therefore for maximum output power (P_{max}), maximum current (I_{max}) and maximum voltage (V_{max}) are required. As given in equation 1.2, the drain current density can be pushed to the maximum by utilizing the advantages of P_{Pe} and P_{Sp} polarization effects, as

mentioned before and consequently increasing the sheet carrier concentration (n_s) [12]. This can be easily achieved by increasing the mole fraction of Al in the barrier layer without strain relaxation. Further, the v_{sat} of the carriers can also be improved by minimizing the gate width and the gate length extension. The mobility of these hetero-structures can be maximized by reducing the carriers scattering. Eventually, this can be achieved by reducing the dislocation densities and interface roughness. For this very reason, owing to the increased carrier concentration near the hetero-interface along with good mobility, the AlGaN/GaN heterostructure based field-effect transistors (FETs) are otherwise termed as AlGaN/GaN High-Electron-Mobility transistors (HEMTs).

The advantage of wide band gap GaN devices are its increased power density, improved efficiency, reliability and compact size making them highly recommendable for high power and high frequency amplifier modules. Thus, altogether contributes to a superior performance at a low cost compared to the competing GaAs or SiC technology.

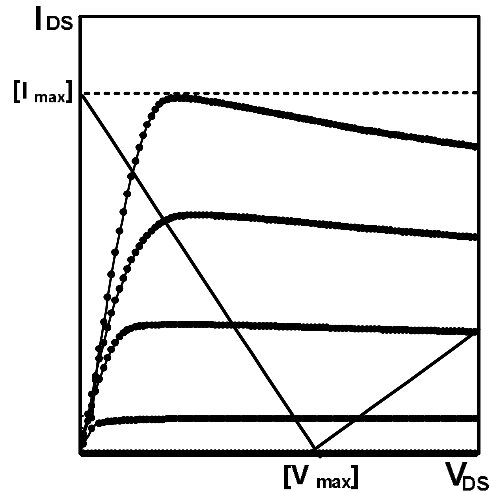

FIG. 1.5. Schematic representation of drain current density (I_{DS}) versus applied voltage (V_{DS}) of AlGaN/GaN HEMT device.

1.3. Progress in GaN technology: Present status and issues

Extensive research has been made for the development of easily growable Si and GaAs smiconductors. While Si and GaAs reseach reached its peak and pushed to their theoretical limits, the growth of III-nitrides emerged its infant stage in the late 1960s. Although, GaN devices seems to be highly promising, at present it has its own challenges even after the first successful evoultion of AlGaN/GaN HEMTs [13]. One among the technological difficulty is the lack of large size ideal substrate to grow the GaN based devices. Even after forty years ever since its evolution, finding a better substrate suitable for the epitaxial growth of GaN is still challenging to meet all the requirements (see fig. 1.6). An ideal substrate candidate for the epitaxial growth of GaN is the one which satisfies or requires the following criterias [14-17],

- ✓ low cost availability of large sized substrates
- ✓ less lattice mismatch with bulk GaN
- ✓ low thermal expansion (TEC) when bulk GaN crystals are grown.

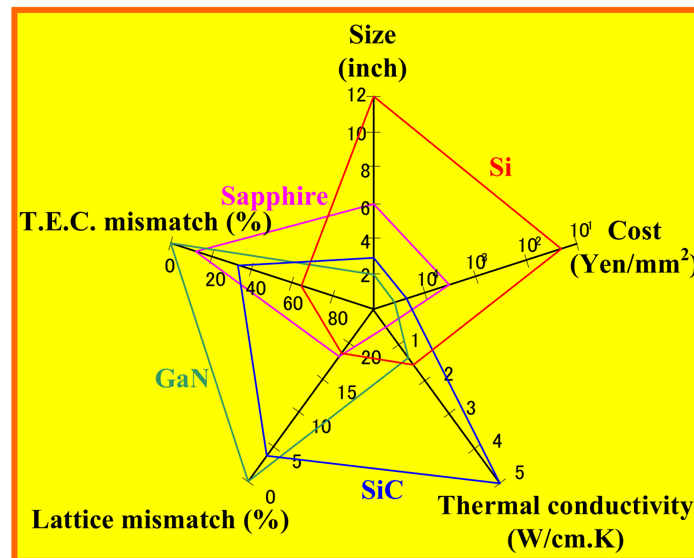

FIG.1.6. Schematic representation of various substrates available and their properties relative with GaN.

As shown in the fig. 1.6, homo-epitaxial growth of GaN on free-standing GaN substrate has negligible lattice mismatch and low dislocation densities in the order of 10^6 cm^{-2} [18]. However, the limited availability of such substrate with large diameter is further hindered by its high cost. While 6H-SiC substrates are available in small size, yet their costs are too high for large scale commercial production of GaN wafers. While large size sapphire substrates are available at expensive costs, their poor thermal conductivity makes GaN devices difficult to dissipate heat generated during high power operations. Amano *et al*., showed the growth of high quality GaN films on sapphire substrates using a low-temperature AlN buffer layer grown using metal organic vapor phase epitaxial growth [19].

On the other hand, availability of less expense and large scale Si substrates are the center of the attraction for GaN power electronics. However, the growth of high quality GaN on silicon substrates has its own challenges, such as high dislocation densities (10^9~10^{11} cm^{-2}) [19], cracks and deep pits [20] due to large lattice mismatch (17 %). Also, there is a large difference in thermal mismatch coefficients (~55%) between GaN and Si. These challenges have to be overcome in order to realize high quality GaN based optoelectronic and electronic devices on silicon substrates. From a point of view for better device operation, a highly resistive substrate with low defects are favorable for low leakage, high breakdown and less current collapse. To realize the mass production of GaN electronic devices on large sized wafers for high power and high frequency applications the epitaxial growth conditions of GaN on Si substrates has to be improved. Such improvements in the heteroepitaxial growth conditions and their application in GaN HEMT technology will be further discussed in detail in the coming chapters.

1.4. State of the art: Focus on GaN HEMT technology

The research on GaN and its alloy based HEMT technology had made considerable attention, progress and development in the last decade. The expansion of GaN based power amplifiers brings higher-power and higher-gain features to microwave designers that reduces heat-sink requirements with smaller part counts and enables smaller systems with higher power performance and efficiency. Furthermore, the future radio frequency modulation schemes for satellite and radar communications requires very high linearity power amplifiers, which in turn depends on power transistors with excellent thermal stability and increasingly higher frequency response. GaN devices can invariably meet these requirements due to its inherently higher transconductance which gives higher linearity, good thermal management and high cut-off frequencies. Apart from being advantageous in optoelectronic devices, GaN based HEMT on Si technology is also promising in the areas of high power and high frequency applications as shown in fig. 1.7.

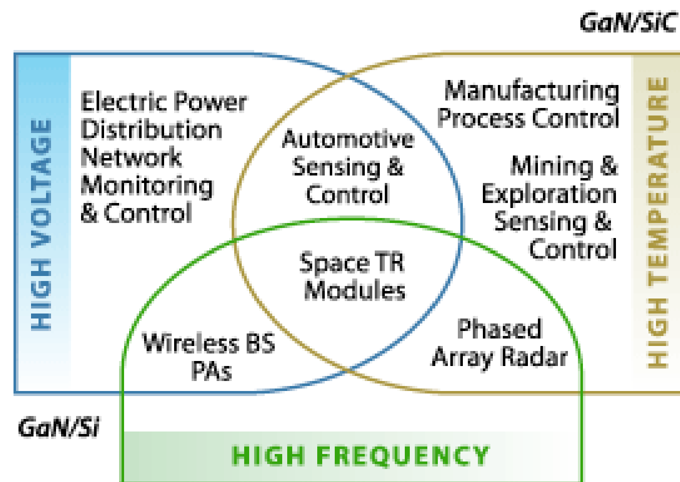

FIG. 1.7. A block diagram showing the high power and high frequency applications of GaN devices on Si and SiC respectively.

1.5. Scope of the present work: Background and motivation

Although, GaN HEMT technology finds extensive applications in the areas of high temperature, high power and high frequency, there are few serious issues which are yet to be solved. One among the serious issues is the trap states at different locations existing in AlGaN/GaN HEMTs as shown in the figs. 1.8. (a) and (b) respectively. The location of these trap states can be identified as AlGaN surface, the AlGaN/GaN hetero-interface and the deep level buffer traps [22, 23]. The origin of these trap states can be due to various factors such as interruption of crystal periodicity, dangling bonds, interface roughness, dislocation, impurities and defects well known to exist in group III-nitrides.

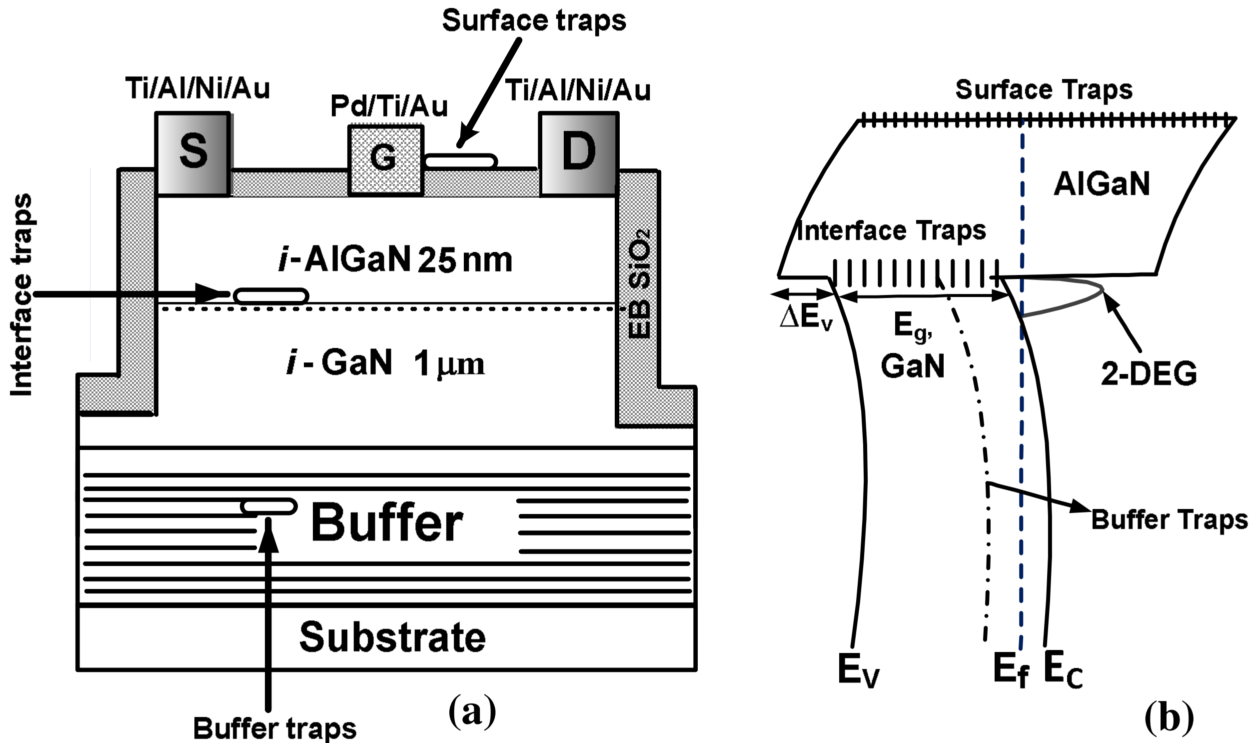

FIG. 1.8. (a) Schematic representation of typical AlGaN/GaN HEMT. (b) Corresponding energy band diagram with various traps and their location in the AlGaN/GaN HEMT heterostructure.

The trap is itself a serious problem and therefore can deteriorate the transistor performance in DC and RF conditions. The origin of the surface traps can sometimes be due to the device process such as plasma damages while mesa-etching and exposure of semiconductor surface to acids and alkalis. The traps can act as trapping centers and can partially deplete the 2-DEG. The hetero-interface trap states can scatter the 2-DEG there by limiting the mobility of the carriers. The presence of surface traps can act as virtual gate depleting the channel electrons as well extending the depleting region [24]. Excess amount of these unwanted traps would eventually limit the maximum current available from a device during a microwave power measurement because of discharging of this virtual gate. As a result, there is current collapse in the AlGaN/GaN HEMTs. The presence of positive charges on the AlGaN surface induced by process damages such as nitrogen vacancies would in-turn enhance the Schottky leakage and limit the breakdown voltage [25]. Because of these problems, if the device is not good at DC operation, it is rather not going to be good at RF. Hence, the presence of the traps irrespective of its location is a serious pertinent problem that needs to be focused and improved.

1.6. Research goal and objectives

The main purpose and objective of this research is therefore

(i) to study the location and nature of these traps, and

(ii) to minimize the trap density.

a) To locate and minimize hetero-interface traps (D_{it}):

There can be considerable amount of hetero-interface traps (D_{it}) around the AlGaN layer adjacent to the GaN channel as shown in figs. 1.8. (a) and (b) respectively. These traps can be electrically active and have specific time constant for trapping and

detrapping of carriers. The exact origin of this hetero-interface trap has not yet been fully understood. However these can represent material imperfections such as impurities, dislocations, point defects etc. Even the small lattice mismatch (~2.2 %) between GaN channel and AlGaN barrier layer can cause the existence of hetero-interface traps. The presence of these traps can seriously deteriorate the carrier reduction and mobilities. These traps cannot be quantitatively identified by conventional capacitance-voltage (*CV*) techniques. Further, the most commonly used Terman method cannot be extended to the AlGaN/GaN heterostructures and hence suitable measurements are needed for the qualitative examination and quantitative estimation of these traps. Hence, in this work frequency dependent conductance analyses which can simultaneously estimate both the hetero-interface traps and surface traps will be employed.

b) To locate and minimize surface-related traps:

There are also AlGaN surface-related traps present in the AlGaN/GaN based HEMTs. The origin of these surface states can be due to process such as exposure of AlGaN surface to alkalis and acids while processing. Further, the nitrogen vacancies, ionized impurities and the dangling bonds caused during the plasma based mesa-etching can mostly cause the existence of surface states. The surface related trap states have time constants in the order of ~ ms.

The presence of these surface related traps can eventually form virtual gate and can partially deplete the 2-DEG which can cause the drain current slump. This can seriously deteriorate the performance of AlGaN/GaN HEMT operation in DC and RF conditions [24, 25]. Hence there is a serious necessary to identify and minimize the surface states for effective high power and high frequency operations. While quantitative

analysis of the surface states is itself a challenging issue, the next obstacle to overcome is the reduction of surface traps. The ultimate solution is the realization of AlGaN/GaN based MOS/MIS-HEMTs. Utilization of a good quality oxide/insulator layer would in-turn alleviate or minimize the existence of surface-related slow traps. On the other hand, if the interface formed between the oxide/insulator and the AlGaN is not of best quality, it can also limit MOS-devices from efficient operation. Therefore, choosing a good insulator/oxide and appropriate deposition condition is very essential for AlGaN/GaN based MOS-HEMTs. Apart from the surface and hetero-interface traps there can be buffer related traps which can also affect the performance of HEMTs if present in large volume. These buffer traps can be identified using deep level transient spectroscopy techniques [26].

In general the buffer traps/deep traps and hetero-interface traps can be minimized by careful epitaxial design and growth, whereas the surface traps can be reduced by utilizing suitable oxide/insulator and appropriate post deposition conditions. The preview of this dissertation follows as,

Chapter 2 mainly focuses on the current challenges and critical issues that prevail in the epitaxial growth technology of metal-organic chemical vapor deposition (MOCVD) grown AlGaN/GaN HEMTs on Si. It also describes about the improvements needed for the MOCVD grown AlGaN/GaN heterostructures on Si. The techniques employed to overcome those challenges in order to attain high-quality heteroepitaxial AlGaN/GaN layers on Si are also briefly discussed.

Chapter 3 gives the overview MOCVD growth of AlGaN/GaN heterostructures on Si using thick buffer layers or the super lattice structures (SLS) and consequent

improvements in crystal quality and current transport properties are presented. The concept and theory of AlGaN/GaN HEMT is introduced in this section. The device characterizations of AlGaN/GaN HEMTs fabricated on the heterostructures grown using super lattice structure (SLS) are discussed in detail. The trapping characteristics of the AlGaN/GaN HEMT structures measured using frequency dependent conductance method are also neatly presented.

Chapter 4 will mainly consists of the efforts to minimize the surface traps using a passivation material like an oxide/insulator. The concept of metal-insulator/oxide-semiconductor (MIS/MOS) HEMT is introduced along with their device characteristics and principles. A detailed description of the method of preparation of the oxide layer and its characterization is also presented. Further, the device characteristics of thermally oxidized Al_2O_3 based AlGaN/GaN MOS-HEMT will be compared with the conventional HEMT characteristics.

Chapter 5 describes about the potential utilization of using a thin *in-situ* MOCVD grown AlN layer as a passivating layer for AlGaN/GaN MIS-HEMTs on Si substrates. The influence of AlN layer's growth temperature on traps and their role in device characteristics are briefly discussed.

Finally **chapter 6** summarizes the conclusions drawn from the present work mainly based on the trapping characteristics in GaN based devices and the improvements made to minimize the hetero-interface and surface traps respectively. Furthermore, the potential future work and directions will conclude this dissertation.

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Chapter 2

MOCVD growth of AlGaN/GaN HEMT structures on 4-inch silicon substrates

2.1 Introduction

Most of the III-V Nitrides and its related compounds are either grown using MOCVD or molecular beam epitaxial (MBE) method. The most widely used technique for the high quality growth of GaN is the MOCVD. The advantages of MOCVD grown nitrides are i) faster growth than MBE, few microns of epilayers can be grown per hour, ii) multi-wafer capability easily achievable (4 to 6 wafers can be grown), iii) higher growth temperature, which favors highly thermodynamically stable product and iv) quality of epitaxial layer (atomically sharp interface) is always better than the MBE [1-5]. However, few disadvantages may include difficulty in monitoring the growth rate exactly since no *in-situ* RHEED measurements are possible due to high pressure. Also, post growth cooling can sometimes introduces structural defects.

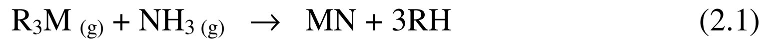
The advantage of MBE includes the ability to monitor the growth by *in-situ* RHEED measurements, low temperature growth and the possibilities to use plasma or laser assisted growth. Nevertheless, the disadvantages are need ultra-high vaccum, low growth rate and very expensive. Other less commonly used technique for the growth of III-V semiconductors are liquid phase epitaxy (LPE) and hydride vapor pressure epitaxy (HVPE) [6-9] which produce reasonable quality GaN epitaxial films with no sharp atomic interfaces.

Overall, the MOCVD technique has produced the highest quality GaN based devices till date. Because of the economy and flexibility of the process, the quality of the materials produced, and the scalability of the technology, MOCVD has come to dominate

the heteroepitaxial growth of III-V semiconductors. It is clear that the future development of large scale profitable production of lighting and electronics relies on the further improvements in MOCVD and purity in its organometallic precursors.

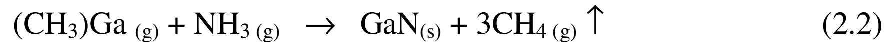
2.2. MOCVD growth of AlGaN/GaN HEMT structures

The general reaction for MOCVD grown III-V binary or ternary nitrides is based on the pure gas phase chemical reaction between highly volatile organometallic chemical precursors with nitride source. The vapor phase chemical reaction lead to the highly stable III-V nitride compound with highly volatile by-products. The general chemical reaction [10-11] between organometallic III-precursor and NH_3 gas is given by equation 2.1,



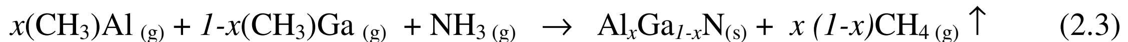
$$R_3M_{(g)} + NH_{3\,(g)} \rightarrow MN + 3RH \qquad (2.1)$$

where R is alkyl group like CH_3 or C_2H_5 and M is group III metal atoms like Al, Ga or In. The MOCVD growth of GaN is widely done by introducing the metal-alkyl precursor Trimethyl Gallium (TMG) and ammonia (NH_3) into the reaction chamber with the substrate heated at elevated temperature (≥ 1000 °C). The reaction is represented by the equation 2.2,



$$(CH_3)Ga_{(g)} + NH_{3\,(g)} \rightarrow GaN_{(s)} + 3CH_{4\,(g)}\uparrow \qquad (2.2)$$

Similarly, heterostructures involving ternary compounds such as $Al_xGa_{1-x}N$ or $In_xGa_{1-x}N$ can be grown by the reaction of respective metal-alkyls and ammonia as given in the equation 2.3,



$$x(CH_3)Al_{(g)} + 1\text{-}x(CH_3)Ga_{(g)} + NH_{3\,(g)} \rightarrow Al_xGa_{1-x}N_{(s)} + x\,(1\text{-}x)CH_{4\,(g)}\uparrow \qquad (2.3)$$

In this MOCVD process, growth can take place as high as 1000-1200 °C. The growth can be optimized based on the substrate used that is SiC, sapphire or Si where the

nucleation layers can be varied depending on the substrate's property. For example, two pretreatment steps are essential for the growth of high quality GaN films on sapphire substrates, a high temperature nitridation of the sapphire surface followed by the deposition of buffer layer [12]. The nitridation of the sapphire was found to result in the formation of relaxed AlN layer, which acts subsequently as a buffer layer. Some of the substrate property and its consequences in the MOCVD GaN epitaxial growth are; (i) Lateral lattice constant (a) mismatch will lead to high dislocation density, (ii) Vertical lattice constant (c) mismatch can lead to anti-phase boundaries and inversion domain boundaries, (iii) Co-efficient of thermal expansion mismatch will lead to thermally induced stress and cracks in epitaxial layer and (iv) Low thermal conductivity can make poor heat conduction which is unfavorable for high power devices.

Alongside with the substrate properties, the growth of high quality MOCVD epitaxial films also depends on the temperature and III-V flux ratio. If the temperature is too high it might result in desorption and nitrogen vacancies whereas, the low temperature growth can result in impurities incorporation and structural defects. Similarly, III-V flux ratio when too high, there will be low surface mobility for the III-metallic atoms leading to structural defects. On the other hand, too low III-V flux ratio will ultimately result in nitrogen vacancies and auto background doping. Therefore, for good MOCVD grown epitaxial layer the III-V flux ratio and temperature should be optimized in addition to finding a better substrate candidate. The MOCVD growth will always result in polarizing *c*-plane of GaN which is preferable for III-V electronic devices. Thus, the state-of-the-art MOCVD GaN based HEMT technology relies in less-defect AlGaN/GaN epilayers. The MOCVD growth of GaN on free standing GaN, sapphire and SiC are

considered to be expensive ones and well established. There are many demands for the technological improvements for GaN grown on large size and less expensive Si.

2.3 Present challenges in MOCVD growth of AlGaN/GaN structures on silicon

Silicon can be a promising substrate for the MOCVD growth of GaN due substrate's large size availability (upto 12″), low cost and large thermal conductivity. However, there is large lattice mismatch (~17 %) and difference in thermal expansion coefficient (~55%) for GaN on Si that leads to a high defect density like pits and cracks. Figure 2.1 (a) and (b) shows the schematic representation of how cracks or deep pits are formed and how cracks and pits free epilayers are grown using SLS. The thermal expansion of GaN is much larger than that of Si, so the epi-wafer becomes concave shape, and a tensile stress is applied to the GaN epilayer, mostly resulting in cracks. The formation of deep pits is believed to be due to the melt-back etching of Gallium atoms into Si substrate, while the cracks are due to the tensile stress [13-14].

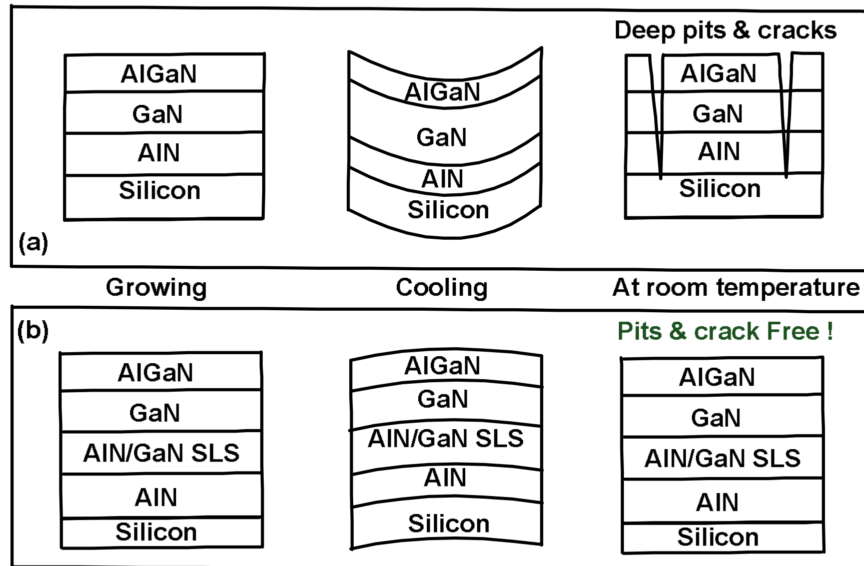


FIG. 2.1. (a) Schematic representation of cracks and pits formation during the MOCVD growth of AlGaN/GaN/Si HEMT. (b) Pits and crack free AlGaN/GaN/Si HEMT structures using AlN/GaN based super lattice structures (SLS).

The presence of these pits tends to degrade the optical and electrical properties such as increased sheet carrier density and decreased carrier mobilities in GaN devices [15]. The deep pits are clearly visible on the AlGaN surface as shown in fig. 2.2 (a) optical microscopic view and in fig. 2.2. (b) AFM view. Apart from these pits and cracks, there can be large concentration of treading edge dislocations owing to the aforementioned lattice mismatch for GaN on Si. GaN epitaxial layer on Si can have dislocation densities of the order of 10^8-10^{11} cm^{-2} depending on the growth and buffer layers involved [16].

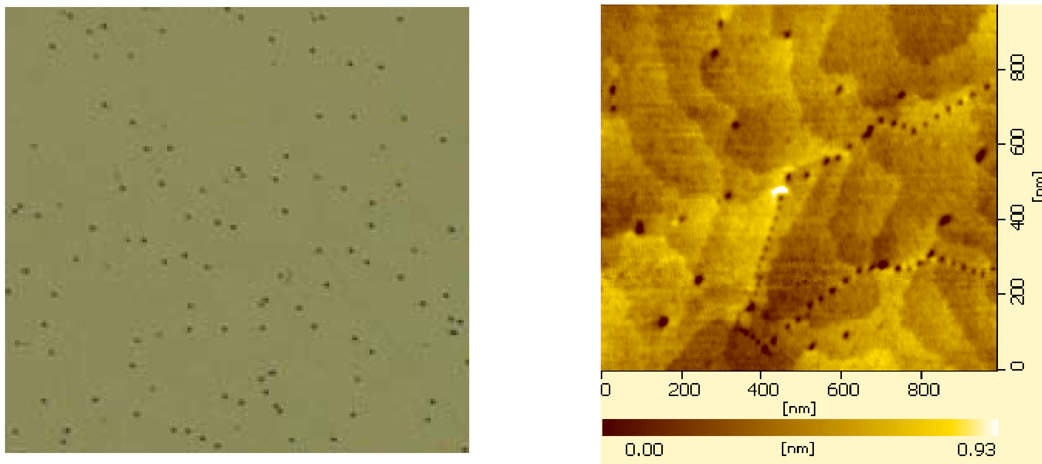


FIG. 2.2. (a) Optical microscopic view of pits in AlGaN surface. (b) AFM view of pits on the AlGaN surface.

Furthermore, the deep pits can increase the leakage currents in the GaN based HEMT devices, which in turn can limit the breakdown voltage, hampering the high power operations [13]. Therefore, these deep pits have to be eliminated in order to increase the transport properties of the GaN HEMT structures and to enhance the high

power applications. This can be done by careful design of the nucleation layer for GaN on Si with high resistive buffer layers.

As mentioned, the origin of deep pits is found to be the silicon surface (~a) and the pits extend vertically through the buffer layers (~b) and to the GaN/AlGaN heterostructure (~c) as shown in figs. 2.3 (a) and (b) respectively. Whenever the dislocations reach the surface it ends in a pit. This makes it possible for AFM to record dislocations due to equilibrium between surface tension and line tension. Further, the presence of these pits and cracks can seriously affect the device characteristics such as Schottky gate leakage and current collapse. Various transport mechanisms such as conduction through dislocation states by hopping and tunneling assisted by the dislocation states are accounted for the gate leakage. However, the formations of these kinds of deep pits and cracks can be eliminated by canceling the tensile stress in the GaN layer by using thick multipairs of GaN/AlN super lattice structure.

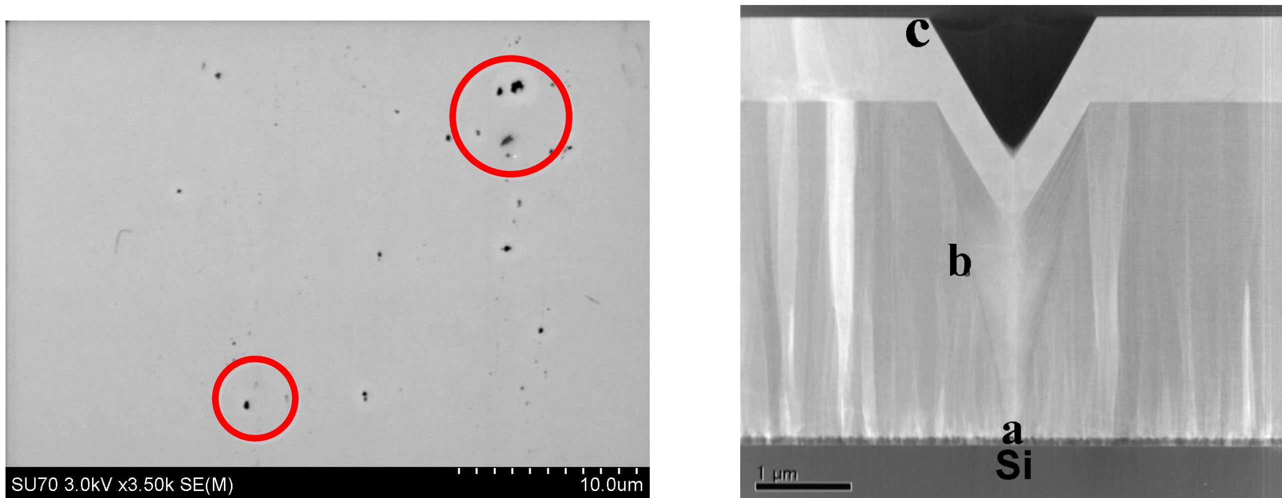


FIG. 2.3. (a) SEM micrograph of pits present on the AlGaN surface. (b) Cross-sectional TEM image showing the origin of deep pit from Si substrate.

2.4. Improvements in the growth of AlGaN/GaN structures on silicon

As discussed in the earlier section, the lack of highly resistive GaN with low defect density on low cost silicon substrate is a serious problem and has to be improved. Different approaches have been made to achieve device grade AlGaN/GaN heterostructures. One such approach is the transition metal especially Fe doping in the GaN layer [17]. For Fe doped GaN layer, Ferrocene was explored as a precursor. It is found that the doping of Fe results in semi-insulating GaN layer. Improved breakdown voltage with degraded drain current characteristics was also reported using Fe doped GaN on silicon substrate [18]. Nevertheless, the photoluminescence spectral studies showed two kinds of $Fe^{3+/2+}$ acceptor level traps located at 2.6 eV and 3.17 eV respectively above the valence band maximum [19,20]. These acceptor levels can act as buffer traps and can partially deplete the 2-DEG channel causing a current slum called the current collapse. Another tedious approach called the substrate transfer technology was employed to improve the breakdown voltage. In this method the processed AlGaN/GaN/Si HEMTs were transferred to glass substrate. There was considerable drain current degradation in this case too [21]. Neither of the above two techniques could demonstrate higher breakdown voltage without compromising the drain current characteristics.

Therefore, an alternative approach for the growth of highly resistive and low defect GaN layer on Si without degrading the device characteristics is very much essential for high power and high frequency applications. As mentioned, the use of thick multi-pairs of AlN/GaN would be a suitable alternative approach to realize the high quality GaN on Si. The crack free thick GaN epilayers can be grown by converting the strain from tensile to a compressive state simply by inserting thin AlN/GaN super lattice

structures (SLS) inter-layers. The other advantages of growing thicker buffer layers include lattice mismatch relaxation with the substrate, reduced dislocations, defects and smoother interface [22-25].

As shown in HR-TEM images in figs. 2.4. (a) and (b), the edge dislocations are minimized by using multipairs of AlN/GaN SLS. The use of these SLS layers helps to attain a highly resistive GaN layer with reduced dislocation densities by overcoming the large lattice mismatch with the substrate. A difference in dislocation density is clearly visible above and below the SLS layers as indicated by a triangle and circle. Hence, MOCVD growth of GaN using thick SLS results in a highly resistive GaN layer with reduced dislocations as well as crack and pit free as aforementioned. Such a low dislocation, crack and pit free GaN epilayers on Si are very promising candidates for HEMT device fabrication.

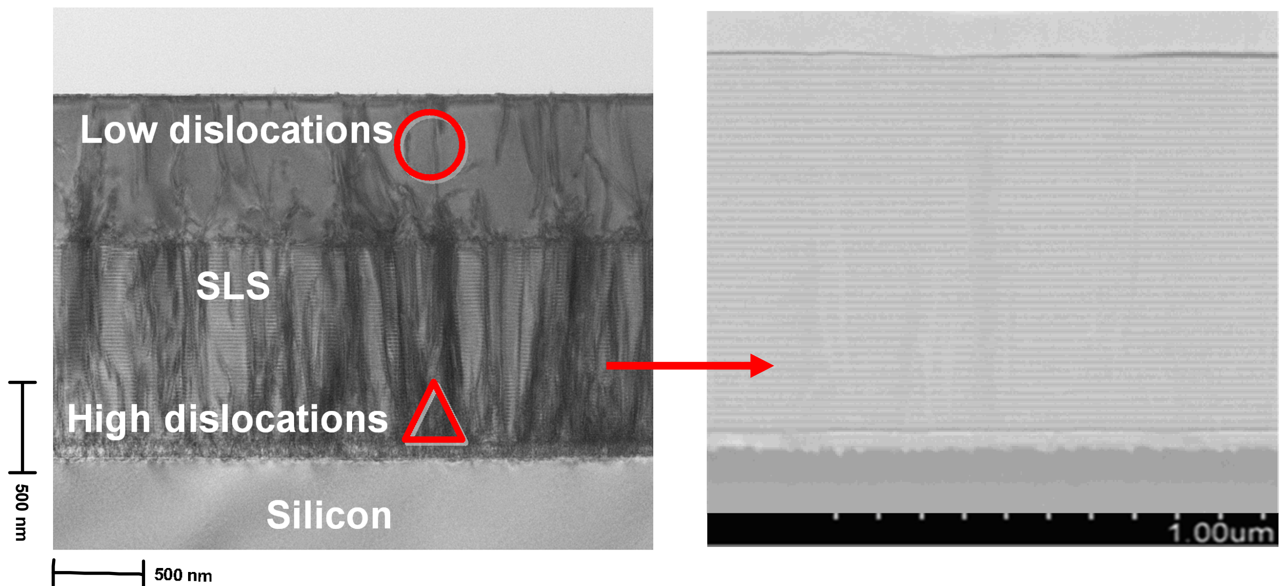


FIG. 2.4. (a) Cross-sectional TEM image of AlGaN/GaN grown on Si with SLS. A low dislocation density (circle) was observed on AlGaN/GaN layers compared to region of high dislocation (triangle) near Si/nucleation layers. (b) Cross-sectional SEM image also revealing periodicity in SLS.

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Chapter 3

Characterization and HEMT fabrication on MOCVD grown AlGaN/GaN heterostructures on Si (111) with thick buffer layers

3.1. Introduction

The epilayer design serves as the key factor for the device characteristics such as the drain current density, the channel conductance, leakage and breakdown voltage mechanisms. Therefore, proper design of the AlGaN/GaN heterostructure is crucial for the subsequent fabrication process [1-3]. In this study, the AlGaN/GaN heterostructures involved were all grown by Taiyo Nippon Sanso SR-4000 MOCVD system. The HEMT structures were grown on 4” p-type Si substrate by using various (AlN/GaN) buffer layers thickness (T_{buff}). The thickness ratio of the AlN/GaN multipairs was 1:4. The T_{buff} was between 1.25 to 5 μm in order to study the influence buffer layers on the heterostructures and their device characterisistics. The growth of these graded buffer layers is to overcome the large lattice mismatch with the Si substrate and to lower the defects arising due to it.

Further high quality and high resistive GaN layer can elevate the dislocation governed buffer leakage and improve the device breakdown voltage. The AlGaN barrier thickness and Al composition for the hetero structures were fixed as 25 nm and 26 % respectively. The unintentionally doped GaN channel layer was also fixed as 1 μm for the heterostructures. All the heterostructures layers including the buffers were grown at high temperature (≥ 1000 °C). Crack and pit free AlGaN/GaN epilayers were successfully grown on 4-inch p-type Si substrate as shown in fig. 3.1.

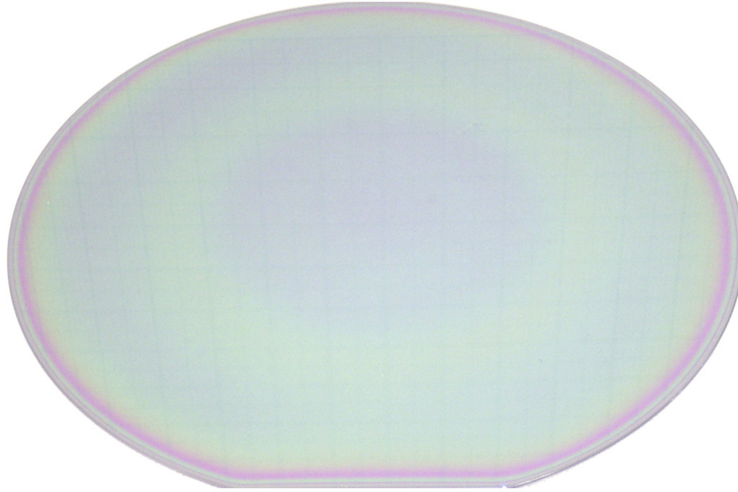

FIG. 3.1. Photograph of crack and pit free AlGaN/GaN HEMT wafer grown on 4” p-type Si (111) substrate.

3.2. Characterization of MOCVD grown AlGaN/GaN HEMT structures on Si (111) with thick buffer layers

The as grown MOCVD AlGaN/GaN heterostructures were subjected to material and carrier characterization prior to the device fabrication.

3.2.1. HR-XRC characterization method

The crystal quality of MOCVD grown GaN layer with increasing T_{buff} were analyzed by measuring (004) and (100) crystallographic reflections from high-resolution X-ray rocking curve (HR-XRC) measurements using Philips X`pert x-ray diffractometer. Screw and edge dislocation components in GaN layers can be calculated by using the full-width at half-maximum (FWHM) values of 004 and 100 planes respectively. The densities of line defect can directly influence the ω-scan which in turn affects the FWHM line width. Any increase of screw and mixed component of the dislocation density will increase the tilt component in *c*-plane GaN, and hence increase the FWHM line width of symmetric reflection in (004) diffraction peak. The threading edge dislocation densities

can be derived from the FWHM values by scanning the symmetric reflection in (100) diffraction peak. Increase in FWHM value will reveal the edge dislocation component of *c*-plane GaN layer [4-5]. The screw and edge dislocation components are given according to the equations 3.1 and 3.2,

$$(D_{screw}) = \frac{\alpha_{004}^{2}}{4.35.c_{screw}^{2}} \tag{3.1}$$

$$(D_{edge}) = \frac{\alpha_{100}^{2}}{4.35.c_{edge}^{2}} \tag{3.2}$$

In these equations, α is the FWHM (in radian) at respective reflection and c is the Burger's constant. The values of c for screw and edge components are 0.5185 and 0.3189 A° respectively. The calculated screw dislocation density for AlGaN/GaN heterostructures with various T_{tot} was around ~1.5 x 10^{9} cm^{-2}. Meanwhile, the FWHM value corresponding to 100 reflection decreased significantly (see highlighted text by a red ink in table 3.1) as the buffer thickness increased. And the calculated edge dislocation density ($D_{D\text{-}edge}$) was found to decrease considerably with increasing $T_{tot.}$ Furthermore, it was found that increasing the T_{buff}, reduced the edge dislocation densities while increasing the GaN layer thickness reduced the screw dislocation densities. Hence, growing thick GaN layers using thick buffers is an effective way to reduce both edge and screw dislocation densities.

3.2.2. Surface analyses: AFM characterization

The morphological investigations of the AlGaN/GaN HEMT heterostructures grown with increasing T_{buff} were carried out using Seiko SP 300 Sound Proof Housing AFM system. Using AFM, images with very good atomic resolution have been obtained for the HEMT samples as shown in fig. 3.2.

As seen, it was found that increasing the T_{buff}, results in better surface morphology as evident from their reduced root mean square (*RMS*) and peak to valley (*P-V*) values. The *RMS* and *P-V* values were 50 % lower for the sample grown using thicker T_{buff}. A smoother surface is always desirable for AlGaN/GaN HEMT in order to obtain good Ohmic contact with low contact resistance (R_C).

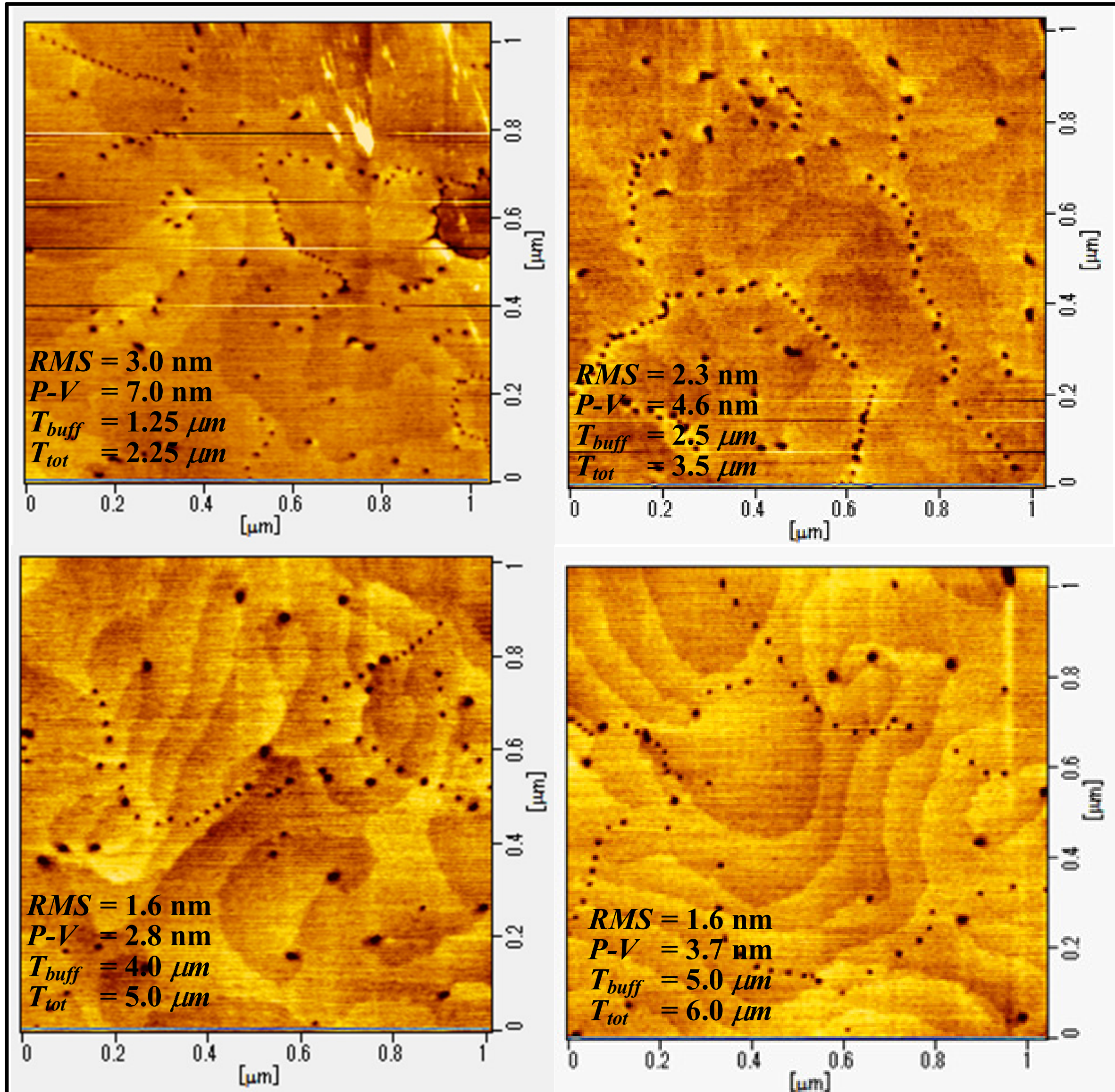

FIG. 3.2. AFM images along with the *RMS* and *P-V* values of AlGaN/GaN HEMT heterostructures grown with increasing buffer thickness (T_{buff}).

3.2.3. Van-der Pauw-Hall measurements

The MOCVD grown AlGaN/GaN heterostructures were subjected to hall measurements at room temperature (300 K) and low temperature (77 K) respectively. By employing Hall method, the intrinsic properties of the heterostructures such as the sheet carrier densities, 2-DEG mobilities and sheet resistances can be measured.

Principle

The Hall effect can be measured by inducing a magnetic field perpendicular to the current flow direction in a semiconductor [6-10]. Under such conditions, a voltage is developed perpendicular to both the current and magnetic field. This voltage is known as the Hall voltage. The origin of the Hall voltage can be seen by considering the forces on a charged carrier in the presence of a magnetic field (see fig. 3.3).

$$\vec{F} = q\vec{E} + q\vec{v} \times \vec{B} \quad (3.3)$$

The first term in the equation 3.3 is due to the total electric field driving the current through the sample. The second term is due to the Lorentz force on the charged carriers, and tends to deflect the carrier toward the side of the sample. The direction of the deflection depends on the sign of the carrier's charge. Therefore the advantage of the Hall effect is identification of the majority carriers and their type by using the direction of current flow in the semiconductor.

In this case of AlGaN/GaN heterostructures, a sample square of area 7 x 7 mm^2 was used for the Hall measurements. Ohmic contacts were made on these samples on four corners by using Ti/Al metal alloy and annealing the contacts. A metallic wire bonding was made to these contacts and was subjected to high magnetic field. The parameters and current density were monitored by use of Kiethley Picometers.

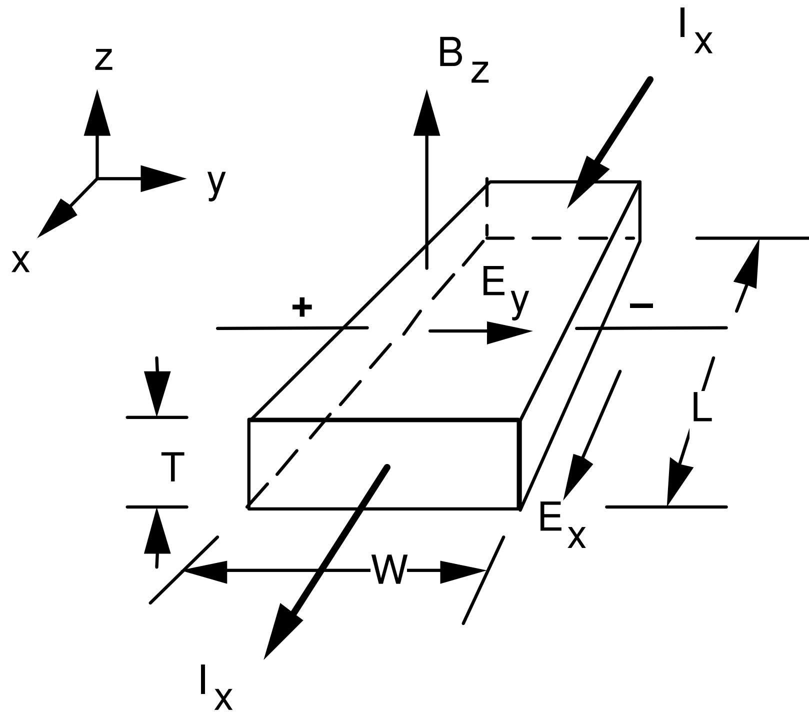

FIG. 3.3. Schematic representation of Hall measurement set up. Current flows in the positive x-direction. The applied magnetic field is in the positive z-direction. For n-type carriers an internal electric field develops in the negative y-direction.

3.2.4. Applications of Hall measurements

a) Carrier concentration

The Hall voltage, magnetic field, current, and sample thickness can be used to determine the Hall coefficient for any semiconductor according to the equation 3.4. From the Hall coefficient (R_H) the doping density can be derived as well as carriers type if p or n. This measurement is a diagnostic tool for determining the doping level in the sample.

$$R_H = \frac{E_y}{J_x B} = \frac{(V_y / W)}{(IB / WT)} = \frac{TV_y}{IB} \tag{3.4}$$

b) Carrier mobility

The carrier mobility of any semiconductor sample can be determined from Hall method by using the equation 3.5.

$$R = \frac{\rho L}{A}, \quad \text{so} \quad \rho = \frac{RWT}{L} = \frac{V_x / I_x}{L / WT} \tag{3.5}$$

If the sample resistance R is known, then the resistivity can be calculated. Since the conductivity $\sigma = 1/\rho$ is directly proportional to $q\mu_n n$, the mobility μ_n is just the ratio of the Hall coefficient (R_H) and the resistivity. Measurements of the Hall coefficient and the resistivity over a range of temperatures yield plots of majority carrier concentration and mobility versus temperature, very useful data to have for semiconductors.

The summary of the HR-XRC results and Hall measurements for AlGaN/GaN HEMT heterostructures are presented in the table. 3.1.

Table 3.1. Summary of XRC and Hall measurement results for AlGaN/GaN HEMT heterostructures grown with increasing buffer thickness

Thickness in µm		**XRC results FWHM (arcsec)**		**Hall measurements @ 300 K**			**Hall measurements @ 77 K**		
T_{tot}	T_{buff}	**(004)**	**(100)**	N_s **x 10^{13} (cm^{-2})**	μ_H **(cm^2/Vs)**	R_{sh} **(Ω/)**	N_s **x 10^{13} (cm^{-2})**	μ_H **(cm^2/Vs)**	R_{sh} **(Ω/)**
2.25	1.25	779	**3073.8**	0.83	923	809	0.92	**2950**	230
3.5	2.50	869.8	**2769.9**	0.83	983	769	0.91	**3450**	188
5.0	4.0	921.5	**2289.6**	0.87	1100	649	0.93	**4240**	158
6.0	5.0	868.1	**2163.3**	0.70	980	978	0.78	**4245**	191

It was unambiguously observed that increasing the T_{buff} resulted in considerable decrease in $D_{D\text{-}edge}$ and improved carrier mobilities at (77 K). A plot of $D_{D\text{-}edge}$ and μ_H against T_{tot} is shown in fig. 3.4. As seen, the $D_{D\text{-}edge}$ were found to decrease with increasing T_{tot} and was low (≅ 52 %) for the heterostructures with thicker T_{tot} that is with increasing buffer thickness [11]. The μ_H was enhanced by 50 % for AlGaN/GaN HEMT heterostructures grown on thick T_{buff} ~5 μm, compared to heterostructures grown on thin T_{buff} ~1.25 μm. However, there is very less percent (~5%) of reduction in edge dislocation density between buffer thickness of 4 and 5 μm. Also, the low temperature mobility value saturates for a buffer thickness of 4 μm. Therefore, for AlGaN/GaN/Si heterostructures with i-GaN thickness of 1 μm, the critical buffer thickness can be around 4 μm based on HR-XRC and hall measurements.

The increase in μ_H is also attributed to good quality AlGaN/GaN heterostructures relatively with a smoother hetero-interface resulted by increasing the T_{buff}. A high concentration of dislocations/defects at the hetero-interface can ultimately limit the μ_H due to interface roughness scattering. The increases in carrier mobilities are often expressed in terms of increase in the epilayers thickness, reduced dislocations, defects and interface roughness [12-16]. Moreover, Jena *et al.* [17] have also showed the dependence of mobility and dislocation density with an extremely good approximation by the expression $\mu^{2D} \propto n_s^{3/2}/N_{dis}$. In this expression, μ^{2D} is the two dimensional electron gas (2-DEG) mobility, n_s and N_{dis} are 2-DEG concentration and dislocation densities respectively.

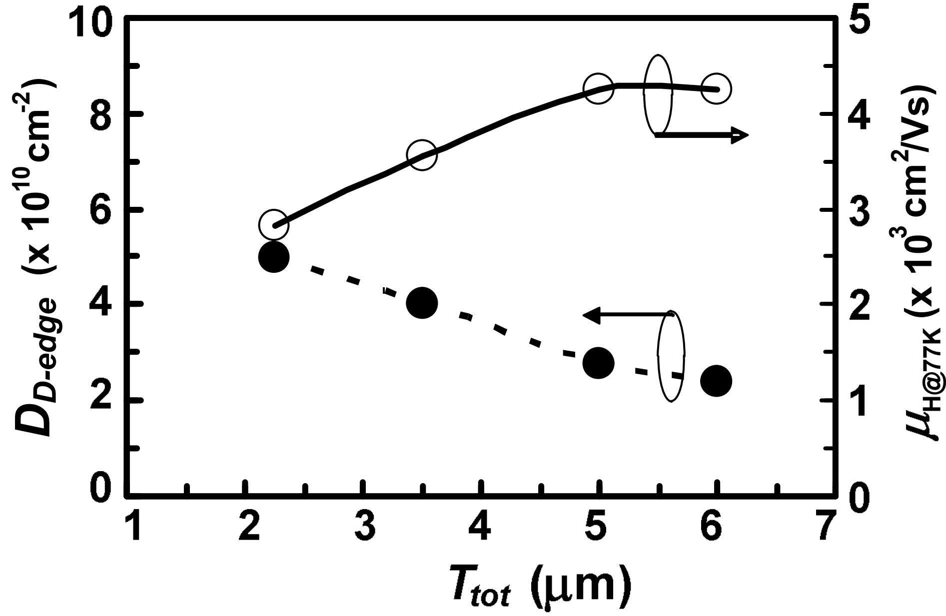

FIG. 3.4. Plot of calculated edge dislocation densites from XRC results and measured carrier moblities versus total epilayer thickness for AlGaN/GaN HEMT heterostructures grown with increasing buffer layers thickness.

3.3. AlGaN/GaN HEMT fabrication

The HEMT device fabrication can be classified into five major steps namely, (i) the structure design, (ii) the mesa isolation, (iii) device passivation, (iv) Ohmic contact and finally (v) the Schottky gate contact. Each step involved is very important for the fabrication of HEMT to attain flawless operation. The sequence of AlGaN/GaN HEMT process from mesa isolation onward is given as,

3.3.1. Mesa-isolation etching

The as grown AlGaN/GaN wafers are cut into 14 x 7 mm^2 for HEMT device fabrication. Prior to performing the isolation pattern using conventional UV-photolithography, the sample surface was thoroughly cleaned using organic solvents like acetone and iso-proponal and then cleaned with de-ionized water. This makes sure that

the AlGaN surface is free from impurities. The sample is then covered with primer and positive photo resist (PR) and kept in oven at an ambient temperature of 90 °C before exposure to UV using a patterned metallic mask. The UV exposed PR covered sample is developed using a suitable developer. After the isolation patterns were formed on the sample, it is moved to a BCl_3 plasma based Reactive Ion Etching (RIE) chamber. The mesa isolation is done using 10 Watts plasma power and BCl_3 flow rate of 10 sccm for 30 minutes. This etching condition will result in mesa-isolation of devices with approximately 150 nm depth.

3.3.2. Device passivation

After the mesa-isolation, the samples are passivated using electron beam evaporated (EB) SiO_2 with a thickness of 100 nm. The SiO_2 deposition was carried out at an evaporation rate of 0.4 ~ 0.6 A°/sec, a substrate temperature of 150 °C and a base pressure of the order of 6-9 x 10^{-3} Pascal in order to attain uniform passivating film. This passivates the individual HEMT device and ensures that no additional adjacent current leakage paths are created. Other commonly used passivating films are SiN_x, $SiON_x$, Al_2O_3, HfO_x etc. Generally high ~ κ dielectric films are preferred for device passivation.

3.3.3. Ohmic contact & alloying

The next step in the HEMT process is the formation of Ohmic patterns using conventional photolithographic technique aforementioned. Prior to Ohmic metallization the SiO_2 in the source and drain access region were completely etched using a HF based buffer based oxide etchant (BOE). Typical Ohmic metals Ti/Al/Ni/Au (15/72/12/60) were then deposited using electron beam evaporation at a pressure of the order of ~10^{-4} Pascal with an evaporation rate as minimum as 0.4 ~ 0.6 A°/sec. Lift-off procedures were

carried out to remove the metal stacks outside the source/drain contact regions. Ohmic alloying for AlGaN/GaN/Si was performed at an elevated temperature of 850 °C/30 sec at nitrogen gas ambient. The annealing temperature may vary depending on the nature of substrate used for AlGaN/GaN HEMT heterostructure growth.

3.3.4. Schottky gate formation

For the effective function of transistor operation, rectifying contacts are essential. The rectifying contacts are also termed as Schottky gate contacts. The Schottky gate contact for AlGaN/GaN HEMT is patterned using the UV based photolithographic unit. The Schottky metal (Pd) in this case was deposited with a thickness of 40 nm. Typical Schottky gate metals Pd, Pt, Ni are widely used for the AlGaN/GaN HEMTs. Contact metals such as Ti and Au (20/80) are finally deposited over the gate metal followed by lift-off procedures. Thus, the above four steps in HEMT process are essential for basic operation and sequences of these steps may vary according to the specifications and desires. Schematic representation of a fabricated AlGaN/GaN HEMT is shown in fig.3.5. (a). The optical microscopic image of the HEMT is also shown in fig. 3.5 (b).

In our cases, Schottky barrier diodes (SBD) of diameter 300 μm are also available in the same HEMT pattern as shown in fig. 3.5 (b), in order to evaluate the Capacitance/Conductance - Voltage (*C-V*, *G-V*) and Schottky gate leakage (I_g-V_g) characteristics respectively. Furthermore, in order to measure the quality of source and drain Ohmic contact's resistance a Transmission Line Model (TLM) is also available with various gaps spacing as shown in the fig 3.5. (b).

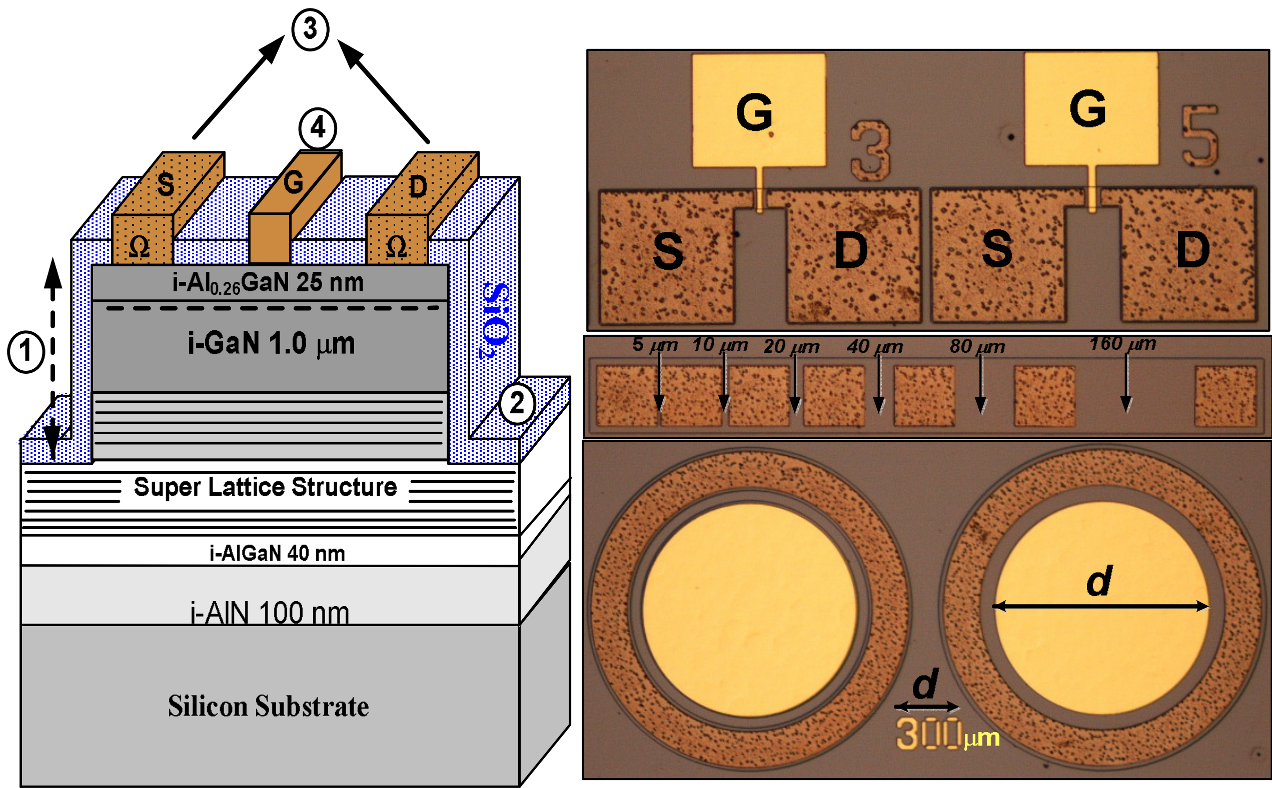

FIG. 3.5. (a) Schematic cross-sectional representation of a fabricated AlGaN/GaN HEMT. Step 1 to 4 represents mesa isolation, passivation, Ohmic contact and Schottky gate contact formation respectively. (b) Optical microscopic view of processed AlGaN/GaN HEMT, TLM pattern and Schottky barrier diode.

3.4. Basics and principle of GaN based HEMTs

The AlGaN/GaN HEMT is a class of field-effect transistors (FET) and is named mainly due to high mobility and high concentration of channel carriers especially in the case of AlGaN/GaN heterostructures. Therefore they are also termed as herterojunction FET (HFETs). The HEMT is formed mainly in group III-V family of heterostructure semiconductors such as GaAs, GaN, InP etc,. When pseudomorphic thin ternary layers of

AlGaAs or AlGaN are grown over binary GaAs or GaN layers, it results in a small lattice mismatch (~2.2 %).

In the case of AlGaN/GaN heterostructures a large *in-built* piezoelectric [18-21] and spontaneous polarizations [21-22] results in high concentration of charge carriers also called as 2-Dimensional Electron Gas (2-DEG) at the heterointerface as discussed in chapter 1. This makes them favorable candidates for high frequency characteristics. The 2-DEG concentration can be modulated by varying the composition of Al in the barrier layer [23-26] and hence sometimes termed as modulation-doped FET (MOD-FETs). The wide band gap of GaN (3.4 eV), makes AlGaN/GaN hetero-system more special, as they can be utilized for high power applications as well. However, when the Al composition exits about 30 % it is accompanied by high surface roughness, sheet resistances and cracks. Therefore, it is difficult to grow high quality and smooth AlN layer with low sheet resistances.

For basic function of HEMT, three contacts are essential namely source, drain and gate (see figs. 3.5. a and b). Out of these three contacts, the source and drain are Ohmic contacts while the gate contact is a rectifying contact. The rectifying contact is also called as Schottky contact named after Walter H. Schottky.

The detailed functions of the Schottky and Ohmic contacts are presented as follows.

3.4.1. Metal-Semiconductor (MS) contacts

a) Ohmic contacts

The Ohmic contacts are otherwise called as source/drain (S/D) electrodes in HEMTs. An ideal Ohmic contact is defined as a metal-semiconductor contact that has negligible contact resistance relative to the bulk or spreading resistance of the

semiconductor. In other words, the assumptions of an ideal metal-semiconductor contact is that metal and semiconductor are at intimate contact at atomic scale and there is no oxides or interface states. This implies that interface or surface states do not play a role and even when there is a barrier at the junction, the strong doping of the semiconductor can minimize the barrier effect. So, even a small applied potential (V_A) results in large current.

The Ohmic contact formation for MS (n-type semiconductor) contact when $\Phi_M < \Phi_S$ is shown in fig. 3.6. (a). Here Φ_M and Φ_S are the metal and semiconductor work functions respectively and χ is electron affinity. As shown in fig. 3.6. (b), a small barrier exists for electron flow from metal to semiconductor, but vanishes when $V_A > 0$ and large current flows when V_A is large as represented in fig. 3.6 (c). In this case, the MS contact behaves as an Ohmic contact for n-type semiconductor. A figure of merit of Ohmic contacts is the contact resistance, R_c. This parameter is defined as the reciprocal of the derivative of current density (J) with respect to voltage (V) evaluated at zero bias. This can be written by equation 3.6 as,

$$R_c = \left| (\partial J/\partial V)^{-1} \right|_{V=0} \ \Omega\text{-cm}^{-2} \qquad (3.6)$$

In realistic conditions, contact metals may react with semiconductor surfaces to form alloys that form new electronic properties. Therefore, for device applications a low contact resistance of the Ohmic contacts is desirable and this is achieved by Ohmic alloying of metal stacks. The R_c values for the S/D in HEMTs can be evaluated by Transmission Line Model (TLM) as shown in fig. 3.6. (d). Hence, the minimum value of R_c corresponds to good Ohmic contact formation.

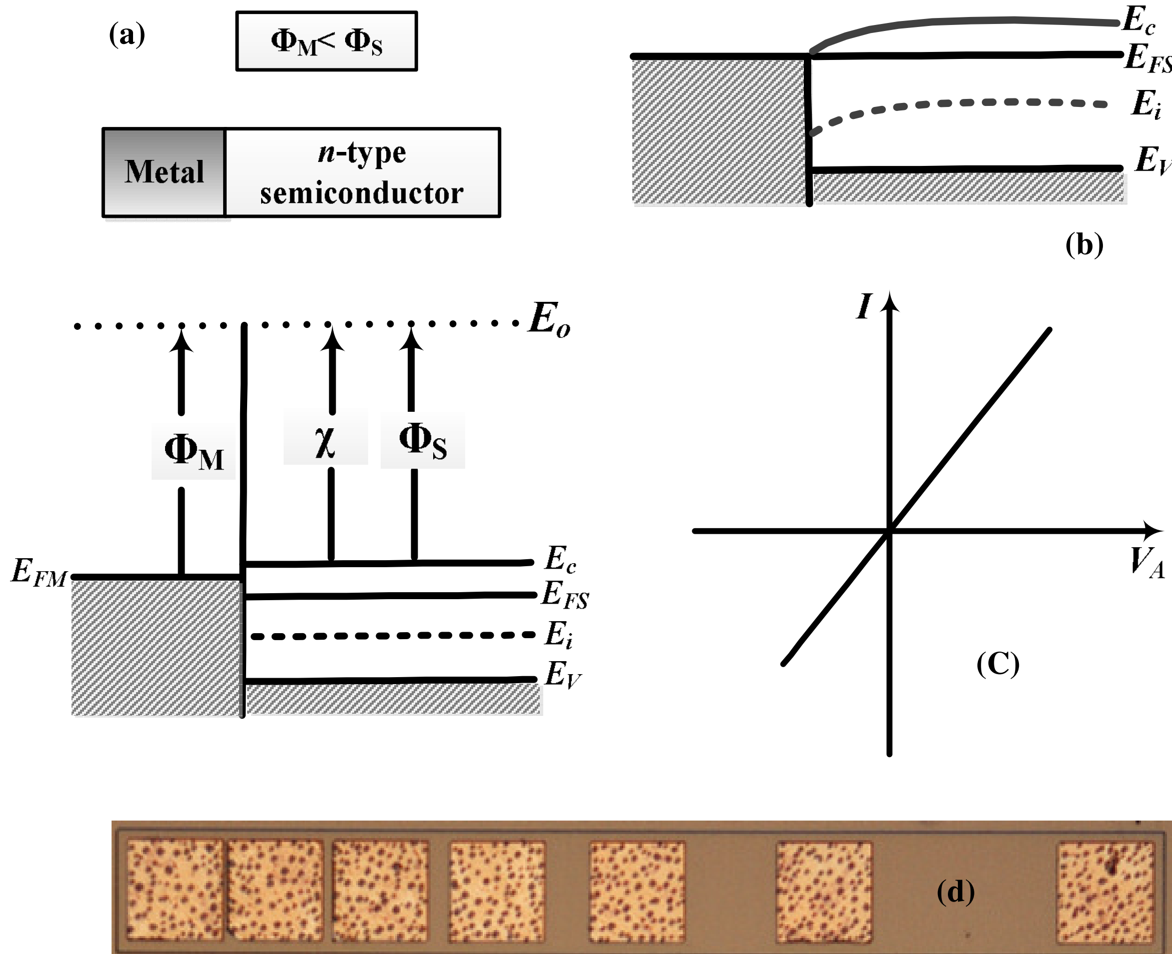

FIG. 3.6. (a) and (b) Schematic representation of MS (Ohmic) contacts in n-type semiconductor (c) Ohmic current as function of applied bias (d) Optical microscopic view of TLM pattern for contact resistance measurements.

b) TLM measurements: (Ohmic contact characterization)

TLM is the technique that is widely used to access the electrical properties and the quality of Ohmic contacts by employing four probes method [27]. The TLM test structures consist of Ohmic metal pads separated by increasing gaps. Adjacent metal pads were used to measure the voltage drop by supplying constant current. Using this method

the specific contact resistance and sheet resistance can be evaluated using the equation 3.7 as,

$$R_{Tot} = 2R_C + R_{sh}\,(L/W) \tag{3.7}$$

In this equation W and L are width of the pad and gap length respectively. The plot of total resistance (R_{tot}) measured as a function of various gap lengths is shown in fig. 3.7. The contact resistance R_c is evaluated from the Y-axis intercept wherein the sheet resistance is deduced from the slope of the line. By knowing the R_c the specific contact resistance, the specific contact resistivity ρ_C is calculated using the expression, $\rho_C = R_C.W.L_T$, where L_T is the transfer length.

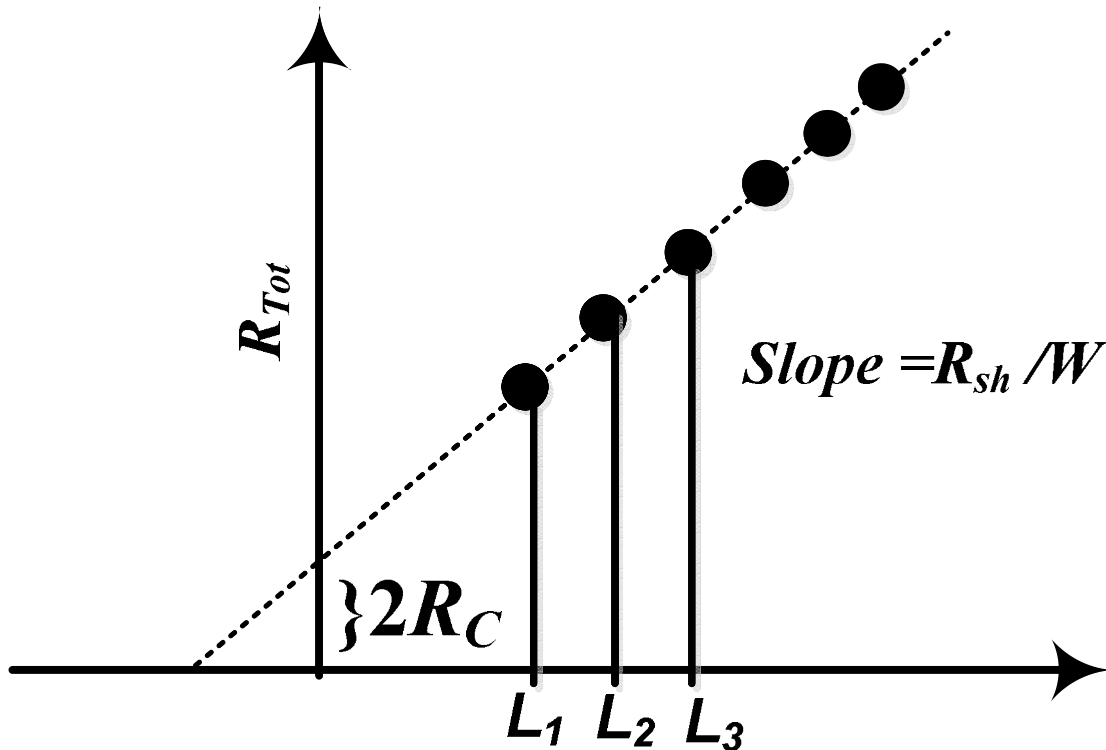

FIG. 3.7. Transmission line model to determine contact resistance of an Ohmic contact.

c) Shottky contacts/ Barrier Diodes (SBD)

The Shottky barrier diode also called as the gate electrode in HEMT is formed as soon as the gate metal with work function greater than the semiconductor ($\Phi_M > \Phi_S$) comes in contact with the respective semiconductor as shown in fig. 3.8. (a). Unlike the case of Ohmic metals, the gate metals are not annealed in order to form the barrier. Under equilibrium, net flow of carriers will be zero, and the Fermi-level will be constant as shown in fig. 3.8. (b). A barrier (Φ_B) forms for electrons to flow from metal to semiconductor. Here (Φ_B) is called the barrier height and is given by ($\Phi_B = \Phi_M - \chi$). Hence the barrier height depends both on the metal work function as well as on the electron affinity of the semiconductor considered.

The typical Schottky gate current measured as a function of applied bias is shown in fig. 3.8 (c). As shown, at positive bias the barrier is lowered and hence the electrons can freely flow from semiconductor to metal where in the current flows from the metal to the semiconductor. On the other hand, applying negative bias with respect to the metal will raise the barrier height and very less current flows and saturates at higher negative bias. Hence, the Schottky diode acts as a rectifying contact and allows only when the diode is forward biased. A rectifying contact for an n-type semiconductor ($\boldsymbol{\Phi_M > \Phi_S}$) can be Ohmic contact for p-type semiconductor and vice-versa (see table 3.2).

Table. 3.2. Electrical nature of Metal-Semiconductor contacts

Condition/Type	**n-type**	**p-type**
$\boldsymbol{\Phi_M > \Phi_S}$	Rectifying	Ohmic
$\boldsymbol{\Phi_M < \Phi_S}$	Ohmic	rectifying

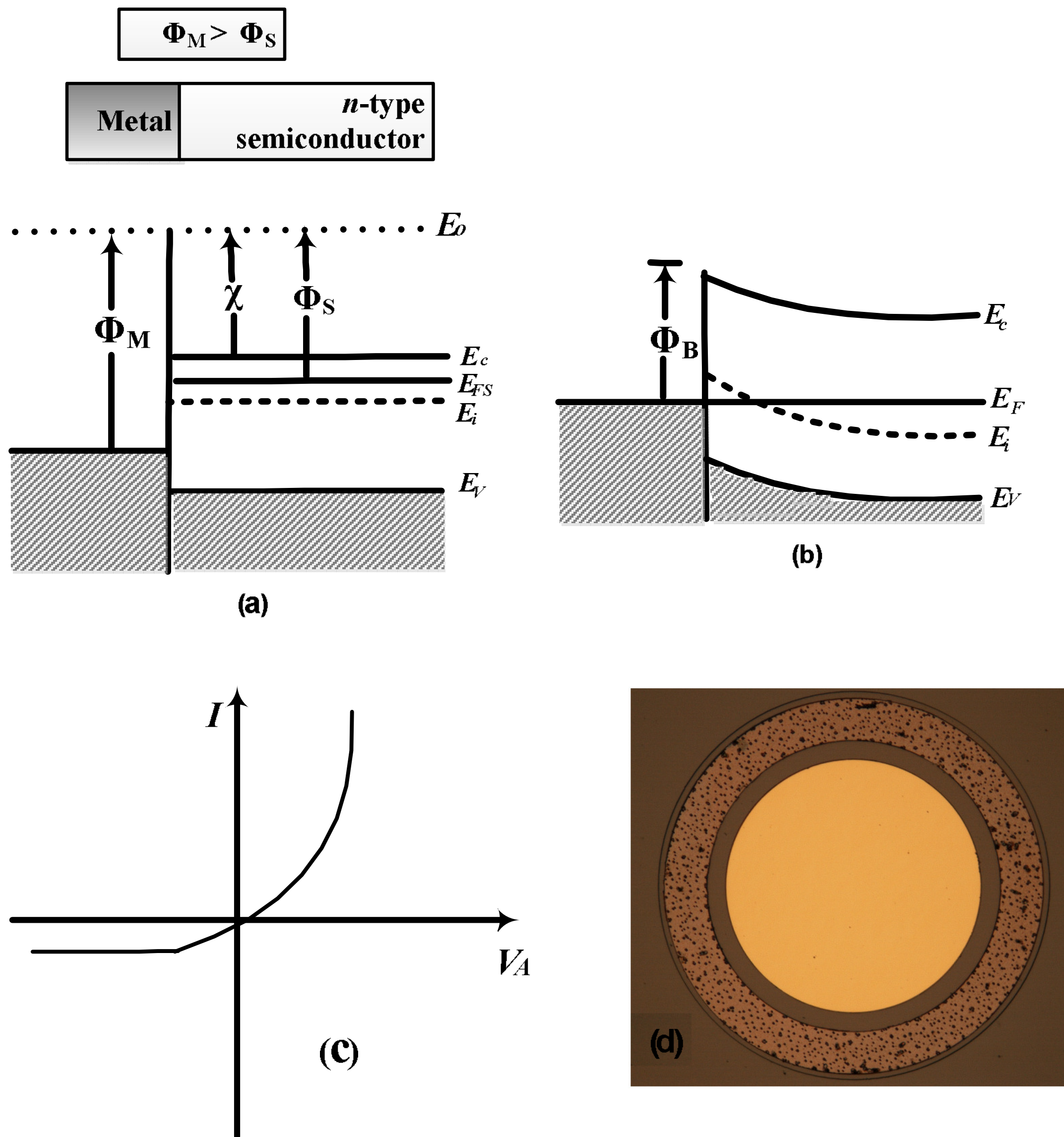

FIG. 3.8. (a) and (b) Schematic representation of MS (Schottky) contact and energy band diagram in n-type semiconductor.(c) Schottky gate current as function of applied bias (d) Optical microscopic view of SBD (dot) of diameter 300 μm and ring Ohmic.

3.4.2. Current transport processes in Metal-Semiconductor contacts

There are several ways that the carriers can be transported across a metal-semiconductor rectifying contact. They are Thermionic emission (TE), Field emission (FE) and Thermionic Field emission (TFE). In a practical rectifying Schottky contact, the dominant current transport process is the Thermionic emission of carriers [28]. The general current equations for Thermionic process (V> 3 $K_B T$) in the diode are given by,

$$I = I_s .\, exp\, (qV/nK_B T) \quad (3.7)$$

$$I_s = AA^* T^2 exp\, (-q\Phi_B/K_B T) \quad (3.8)$$

In the above equations I_s is the saturation current density, n is ideality factor, K_B is the Boltzman constant, T is absolute temperature, A is effective diode area, q is electronic charge and A* is effective Richardson's constant respectively. For heavily doped semiconductors, the probability of tunneling becomes higher and hence field emission process becomes dominant. In this case the barrier height is much larger than the KT, the corresponding current density equation of the diodes are given by,

$$I= Is.[exp.[(qV/kT)^{-1}] \quad (3.9)$$

3.5. Theory and operations of GaN HEMT

In normal open channel condition, that is when the gate is forward biased (V_{GS}) and any potential applied at drain electrode (V_{DS}) will result in 2-DEG flow from source to drain, while the current flow is just in opposite direction denoted by I_{DS}. Under drain bias, the source acts as a base where the carriers flow towards the drain. Here the drain acts as sink or the collector and the drain current is the resultant. The current flowing between the source and the drain electrode when the gate voltage is forward biased can be written as,

$$I_{DS} = q.n_s.v_{eff}.W_G \tag{3.10}$$

In this equation n_s is the sheet carrier concentration (2-DEG) and v_{eff} is the effective velocity of electrons in the channel and W_G is the gate width respectively. For maximum drain current the sheet carrier concentration and the v_{eff} must be high.

3.5.1. Capacitance – Voltage (*C-V*) characteristics

Considering that the Schottky gate metal and the 2-DEG acts as a capacitor, the n_s value can be derived as a function of applied gate bias (V_G) from capacitance voltage (*C-V*) curve and is given by,

$$n_s = \frac{\varepsilon_{AlGaN}}{q(d_{AlGaN} + \Delta d)}(V_G\text{-}V_{th}) \tag{3.11}$$

In this equation, the ε and *d* represents the dielectric constant and thickness of the AlGaN barrier layer respectively, while Δd is the effective distance of 2-DEG from the hetero-interface. The V_{th} is the threshold voltage or the *pinch-off* potential of the channel. Theoretically, when the V_g equals to V_{th} there is no current flow in the channel as n_s tends to zero. Therefore, for effective flow of current in the channel, the condition that must be satisfied is $V_g > V_{th}$. In the case of AlGaN/GaN HEMTs, as n_s and V_{th} are directly related, they both depend on the Al composition as well as the barrier layer thickness.

In practical case, the slight difference in n_s from Hall and *C-V* measurements arise due to the additional parasitic resistance in the later. Figures 3.9 (a) and (b) shows the *C-V* curves and corresponding derived carrier concentration in cm^{-3} ($N_{D\text{-}2DEG}$) as a function of depth profile. The $N_{D\text{-}max}$ is the maximum carrier density that exists in the channel. In the case of *C-V* measurements, the capacitance is sweeped by biasing the Shottky gate electrode while the Ohmic electrode is grounded.

During *C-V* sweep, an ac modulation of small amplitude (20 mV) and a step voltage of 30 or 50 mV is applied to the test structure. A typical *C-V* curve can be divided into three major regions namely, accumulation, depletion, and inversion. The accumulation regime is the region where the ($V_G > V_{th}$) where in the charges get accumulated and saturates as a function of gate bias. The depletion is the region where the charges get depleted due the gate bias approaches towards the *pinch-off* conditions ($V_G \cong V_{th}$). And the deep depletion is the condition where the charges in the channel are completely depleted and depletion zone extends towards the GaN layer. In other words the applied gate bias is much larger than the threshold voltage ($V_G > V_{th}$).

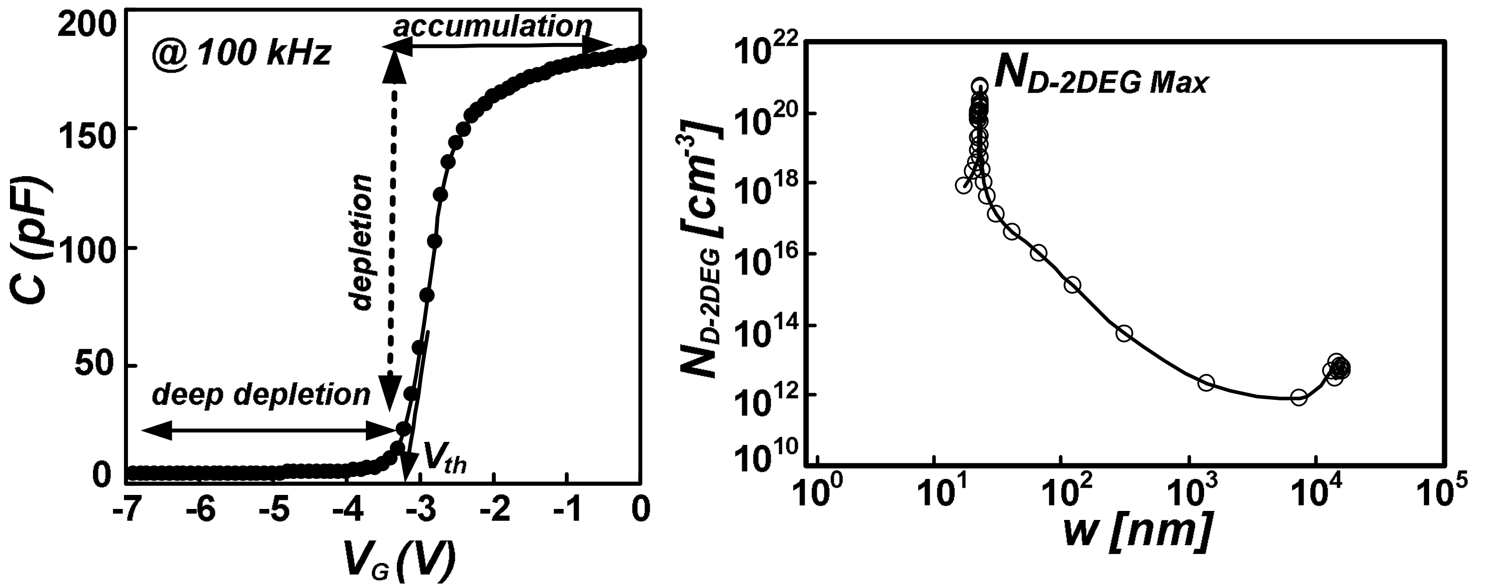

FIG. 3.9. (a) Measured capacitance as a function of applied gate bias in AlGaN/GaN SBD, (b) extracted $N_{D\text{-}2DEG}$ as a function of depletion width (W). The $N_{D\text{-}2DEG\ max}$ is the maximum carriers near the AlGaN/GaN hetero-interface.

3.5.2. Current – Voltage (I_{ds}-V_{ds}) characteristics

As mentioned above, in an open channel condition and at low drain bias ($V_{DS} < V_G - V_{th}$) when the device is said to be operating in linear regime (shown in fig. 3.10), as the electron velocity is linearly related to electric field strength. But at high drain bias ($V_{DS} > V_G - V_{th}$), the effective electron velocity saturates (υ_{sat}) and is independent of the applied drain bias or electric field strength. This region of device operation is called saturation region and for all practical purposes the device is preferably operated in saturated region. The υ_{sat} occurs due to various reasons such as scattering of carriers near the hetero-interface due to interface roughness and charged dislocations.

The interface roughness scattering can be minimized by raising the conduction band discontinuity near the hetero-interface using a thin AlN inter-layer, while the dislocation related scattering can be effectively minimized by growing less defect HEMT structures. The onset drain voltage near the saturation region is called the knee voltage (V_{knee}) and the corresponding drain current density is maximum ($I_{ds\text{-}max}$). A larger V_{knee} can also signify a higher specific on-state resistance (R_{on}). For high-power applications of AlGaN/GaN HEMT, a lower R_{on} and higher $I_{ds\text{-}max}$ are generally required. This can be achieved by obtaining a good Ohmic contact. The drain current density in the saturation region is given by,

$$I_{ds} = \frac{\varepsilon_{AlGaN} . v_{sat} . W}{q(d_{AlGaN} + \Delta d)} (V_G - V_{th}) \tag{3.12}$$

In this equation I_{ds} is independent of applied drain bias V_{ds} based on the assumption that the electron has saturated velocity. However, in reality at higher V_{ds}, some of the carriers may be trapped at various trap centers. Additionally, there may be a conduction path between the source and gate due to the high electric field. Furthermore,

there can be drop in the I_{ds} at higher V_{ds}, which are due to the self-heating effects that are characteristics of AlGaN/GaN HEMTs.

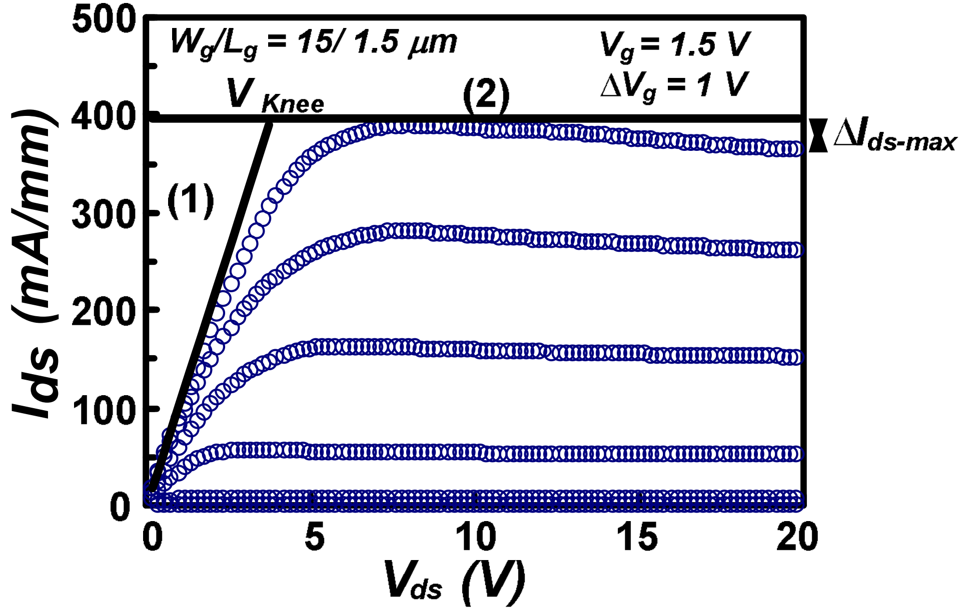

FIG. 3.10. I_{ds}-V_{ds} characteristics of AlGaN/GaN HEMTs. The linear and saturation regimes are indicated by (1) and (2) respectively. $\Delta I_{ds\text{-}max}$ is due to the self-heating effects at high drain bias.

3.5.3. Transfer ($I_{ds}/g_m - V_{gs}$) characteristics

The transconductance (g_m) is the figure of merit value in the ability of a gate electrode to modulate the drain current I_{ds} and is expressed as,

$$g_m = \left(\frac{\partial I_{ds}}{\partial V_{gs}}\right)[V_{ds\,=\,const}] \tag{3.13}$$

The conductance in the channel varies sheet carrier concentration, which is modulated by the gate bias (V_{gs}). When the gate bias is positive, more 2-DEG accumulates in the channel and as a result I_{ds} of HEMT will be higher. The I_{ds} will decrease with the decrease in the gate bias. In other words, the 2-DEG will be completely depleted and the I_{ds} will

drop to zero when the V_{gs} reaches a negative threshold value, which is otherwise called the threshold voltage (V_{th}). Theoretically, V_{th} is determined from the linear extrapolation of $\sqrt{I_{ds}}$ against V_{gs}. The transconductance measured is called extrinsic transconductance since it includes parasitic resistances of the source and drain contacts. In practical operations, this series source and drain resistances limit the current-capabilities of HEMT as a result leading to lower values of I_{ds} and higher values of V_{knee} at which the current saturates. The extrinsic transconductance is related to the intrinsic transconductance by the equation given as,

$$g_{m,ext} = \frac{g_{m,int}}{1 + g_{m,int}.R_s} \tag{3.14}$$

where R_s is the source-channel resistance including contact resistance. The typical transfer characteristics of AlGaN/GaN HEMT are shown in fig. 3.11.

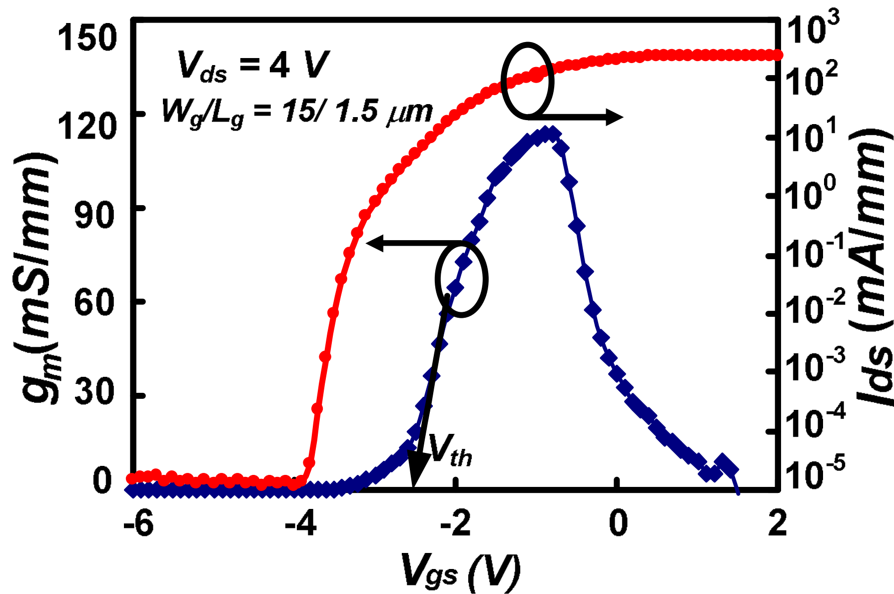

FIG. 3.11. Typical transfer characteristics of AlGaN/GaN HEMTs grown on Si substrate. The threshold voltage is indicated by an arrow.

3.6. Analyses of trapping characteristics in AlGaN/GaN HEMT structures on Si

3.6.1. Traps in AlGaN/GaN HEMT structures

In semiconductors, any defect which disrupts the periodicity of the crystal lattice will also result in the semiconductor band structure. A localized defect existing in the semiconductor can act as a "trapping center" for mobile charges in the region of defect. The occupancy of the trap centers is governed by the capture and emission process for both electrons and holes. In the case of hole-capture and emission processes, the trap levels behave as generation and recombination centers. However, the samples used in this study all are n-type so the analyses are focused mainly on electron-capture and emission processes. Moreover, trapping centers in AlGaN/GaN HEMTs are very much responsible for current collapse [29]. The presence of these traps limits the HEMT performance in high-speed power switching devices depending on the location, concentration, cross-section and energy. On comprehensive literature survey, possible locations of the traps are,

a) the interface between the substrate (Si or SiC or sapphire)

b) the buffer layers

c) the GaN channel layer

d) the AlGaN/GaN hetero-interface and

e) the free AlGaN surface.

3.6.2. Frequency dependent conductance technique for AlGaN/GaN structures

The trap centers existing in the interface between substrate-nucleation layers and buffer layers are regarded as deep traps and are identified vastly by deep-level transient spectroscopy technique [30-32]. In addition, there are considerable amount of traps located in the AlGaN/GaN active device structure. These traps could not be successfully

characterized by the conventional high-low frequency *C-V* and Terman techniques due to limitations and associated errors in case of hetero-structures. This made frequency dependent conductance method to be extended for hetero-structures, which was initially developed for Si/SiO_2 MOS-devices by Nicollian and Goetzberger (also called *NG* method [33-34]). Later, conductance technique was proved to be an effective tool to diagnose the trapping effects in AlGaN/GaN HEMT structures on the consideration that the AlGaN barrier acting as a loosy-dielectric layer [35-36]. In addition, two kinds of traps, namely fast and slow traps were identified based on their time constants by this method [37-39]. The slower traps are mainly surface related and are present along the access region between the gate and drain electrode. Further, they can be minimized by using a passivating material. Recently, a variety of such materials like Al_2O_3, HfO_2 SiN, AlN, etc. and their post deposition annealing conditions have considerably reduced the slow surface related traps [37-40].

However, these passivating films had no effects on the fast traps. This shows that the location of the fast traps can be in close proximity to the AlGaN/GaN hetero-interface near the channel. The AlGaN/GaN hetero-interface traps usually have shorter time constant (~μs) for trapping/detrapping process. Apparently, location of these fast traps in the hetero-interface near channel has also been confirmed by techniques like backgating current deep level transient spectroscopy (DLTS) [41], frequency dependent conductance analyses [42] and noise spectral studies [43]. Unfortunately, not many reports are available for minimizing these AlGaN/GaN hetero-interface traps and/or interface roughness in AlGaN/GaN/Si HEMT heterostructures by improving the hetero-epitaxial growth conditions.

3.6.3. Trapping characteristics of AlGaN/GaN HEMT structures grown with thick buffer layers

It is our imperative attention to characterize the AlGaN/GaN HEMTs grown using thick buffer layers (T_{buff}) by conductance method to establish growth standards for GaN on silicon. SBD were fabricated on same AlGaN/GaN HEMT epilayers that were used for the HR-XRC and Hall measurements. The thickness of the undoped AlGaN barrier layer and Al composition were fixed as 25 nm and 26 % respectively. The undoped GaN layer thickness (T_{GaN}) for all the heterostructures was 1 μm. In order to investigate the AlGaN/GaN hetero-interface trapping effects, an increasing sequence (1.25 – 5 μm) of GaN/AlN T_{buff} (20/5 nm) was used. All these layers were grown at high temperature. The total epilayer thickness (T_{tot}) given by ($T_{tot}=T_{GaN} + T_{buff}$) will be used in further discussions. AlGaN/GaN SBDs of uniform area 7.07 x 10^{-4} cm^{-2} were used for the conductance measurements.

Capacitance voltage (C-V) and conductance voltage (G-V) measurements were performed between frequency ranges (1 kHz -5 MHz) by sweeping the gate bias (V_g) using Agilent B1505 power device analyzer. The amplitude of ac signal was fixed as 20 mV and the measurement period was long, so that small signal conditions were maintained. The normalized C-V curves measured at 100 kHz showed a sharp transition from accumulation to depletion region for all devices as shown in fig. 3.12. As seen, a small negative shift in threshold voltage (ΔV_{th} ~ 0.12 V) was observed on increasing the T_{tot}. This can be explained in terms of AlGaN/GaN heterostructures grown on thicker buffer layers can increase the 2-DEG carrier density ($N_{D\text{-}2DEG}$) in the channel. Then a higher voltage would be required to pinch off the channel [44]. This was also confirmed

from the extracted $N_{D\text{-}2DEG}$ versus depth profile (W in nm) with increasing T_{Tot} as shown in fig. 3.13. An increase in $N_{D\text{-}2DEG}$ with respect to the increase in T_{Tot} at a depth of 24 ± 2 nm for these hetero-structures further suggests the improvements in AlGaN/GaN hetero-interface. In other words, the reduced carrier scattering effects can be a major contributing factor for the increase in carrier density with thicker $T_{Tot.}$ About one order difference in $N_{D\text{-}2DEG}$ (i.e. 2.2 x 10^{19}~ 2.0 x 10^{20}) cm^{-3} was observed for AlGaN/GaN HEMT hetero-structures grown with thin and thick buffer layers respectively.

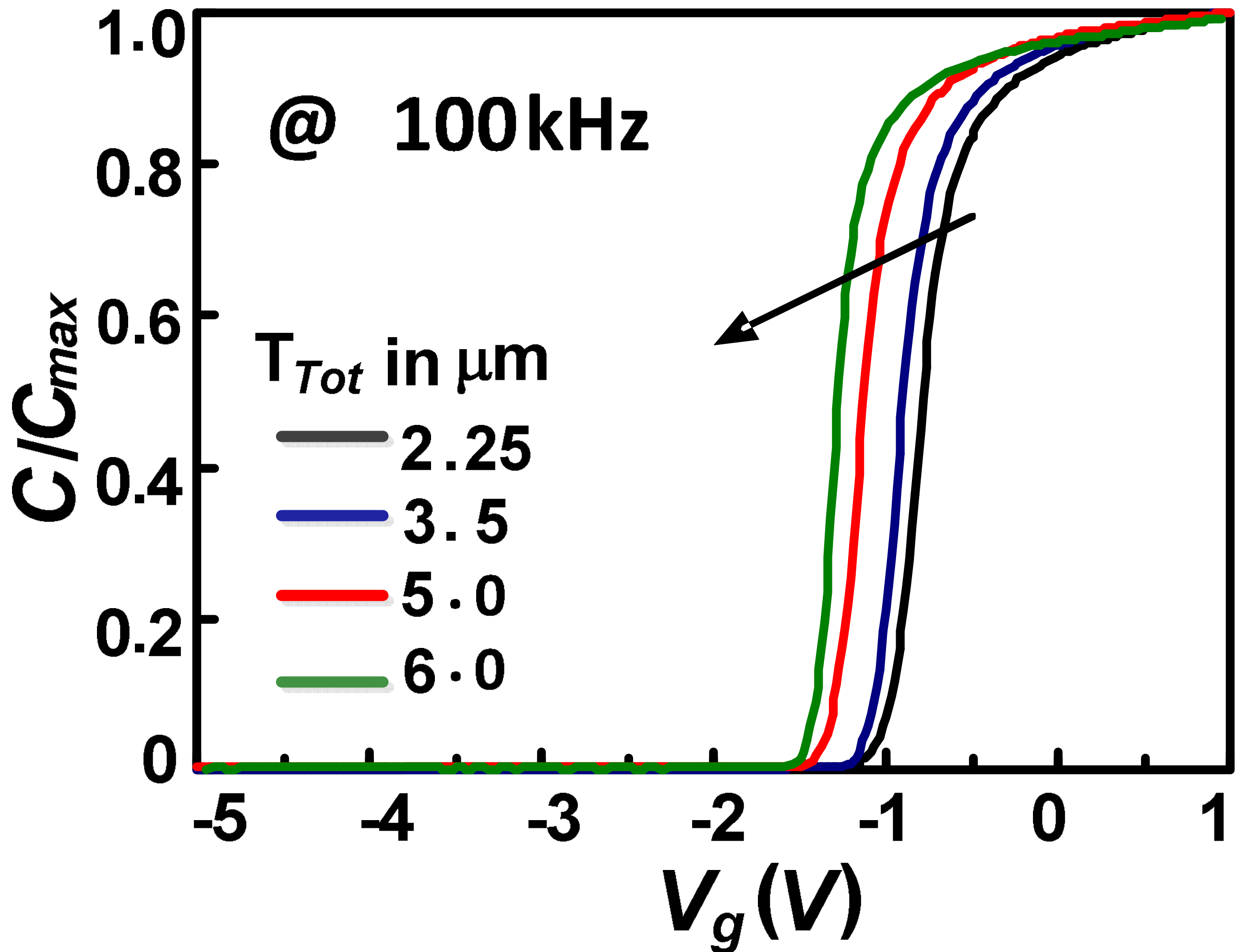

FIG. 3.12. Normalized *C-V* curves of AlGaN/GaN HEMT heterostructures grown with increasing epilayer thickness (T_{tot}).

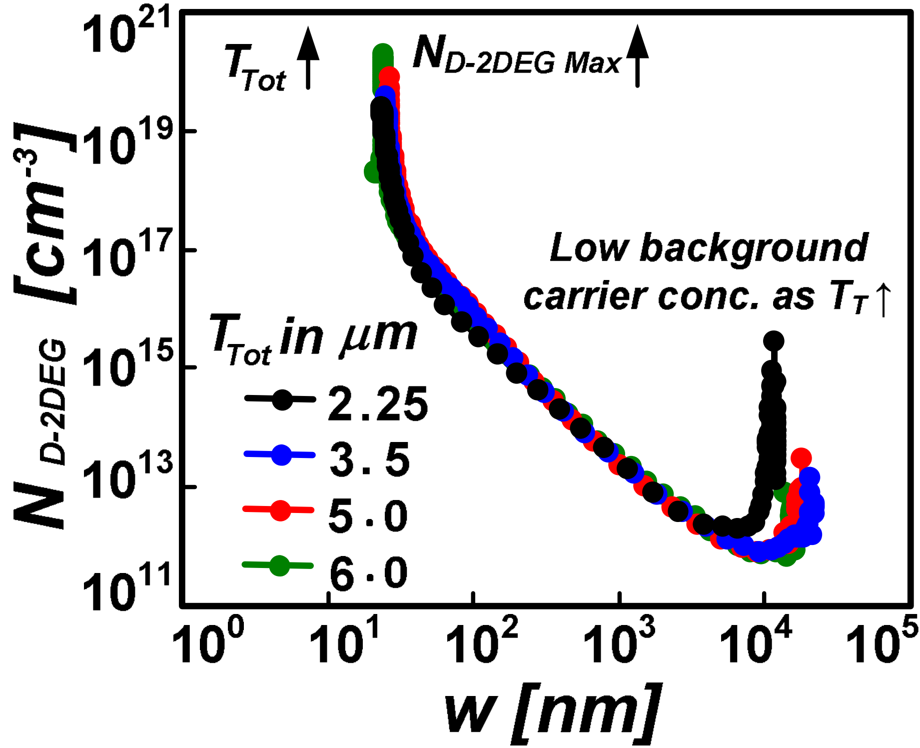

FIG. 3.13. Extracted 2-DEG carrier density versus depth profile for AlGaN/GaN HEMT heterostructures grown with an increasing T_{tot}.

A plot of measured $N_{D\text{-}2DEG}$ and V_{th} as a function of T_{tot} are also shown in fig. 3.14. An exponential function of $N_{D\text{-}2DEG}$ against T_{tot} showed a good fit with maximum accuracy for AlGaN/GaN HEMT heterostructures which also accompanied a V_{th} shift. In addition, the background carrier concentration was found to be low for AlGaN/GaN HEMT heterostructures grown with thicker T_{buff}, which is advantageous because of low buffer leakage. Although, the exact reason for an increase in carrier concentration with increased buffer thickness is not clearly understood, yet the improvements in AlGaN/GaN heterostructures/hetero-interface are consistent with the HR-XRC and hall measurements.

A decrease in trapping effects near the hetero-interface can be one of the possible explanations for both increase in carrier concentration and mobility, because these traps can also act as scattering centers. Furthermore, the trap centers can be associated with charged line defects, since a low V_{th} of (-0.9 V) due to partial depletion of the 2-DEG electrons was observed in the case of AlGaN/GaN HEMT structure grown using thin buffer layers, which obviously showed low carrier density and had maximum edge dislocation densities. It is noteworthy to mention that the charged line defects are known to exist in GaN based devices and may provide acceptor traps and form negatively charged Columbic scattering centers [45-47]. However, conclusive evidence is therefore necessary to quantitatively justify the arguments based on hetero-interface trapping properties.

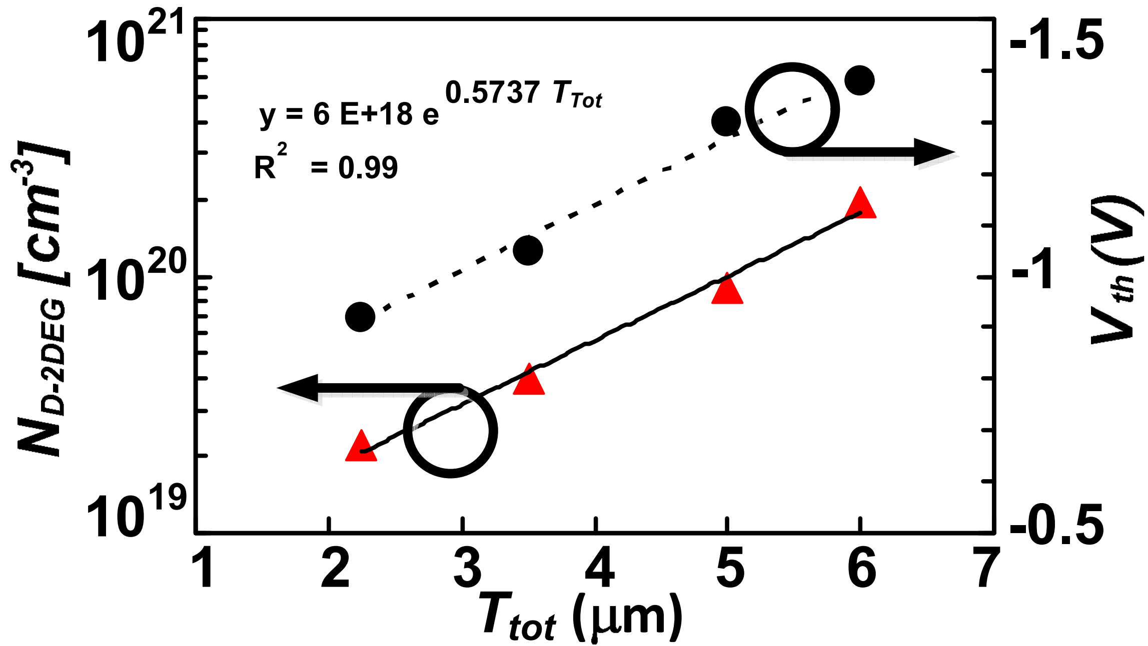

FIG. 3.14. Plot of 2-DEG carrier densities and threshold voltage for AlGaN/GaN HEMT heterostructures grown with an increasing T_{tot}.

In order to evaluate the hetero-interface trapping effects quantitatively, the equivalent parallel conductance/angular frequency (G_p/ω) values near the depletion region were fitted according to the equation [35-38],

$$\frac{Gp}{\omega} = \frac{qD_T}{2\omega\tau_t} \text{ x } \ln\left[1+(\omega\tau_t)^2\right], \quad (3.15)$$

where D_T and τ_t are the trap densities and trap time constants which are parameters evaluated by fitting the experimental G_p/ω values.

As shown in fig. 3.15 (a), typical G_p/ω fitting curves against ω for selected gate voltages near the depletion region ($V_g < V_{th}$) showed an excellent agreement with the experimental G_p/ω results. Both surface related slow traps as well as AlGaN/GaN hetero-interface traps were identified and evaluated. Figure 3.15 (b) shows only the contribution of hetero-interface traps to the G_p/ω fitting curves and were found to be two orders of magnitude lower than the surface traps. The densities of slow traps (D_{st}) were in the order ~ 0.5 x 10^{12} $cm^{-2}eV^{-1}$ with slow trap time constant (τ_{st}) range between (0.3 – 1 ms). Nevertheless, these D_{st} values are lower for AlGaN/GaN HEMTs without a gate insulating layer [37-38].

On the other hand, the evaluated hetero-interface trap time constants (τ_{it}) increased with an increasing T_{tot} and were in the range of (0.6 – 10 μs). Furthermore, the τ_{it} of these devices showed exactly an exponential dependence on the gate bias ($\tau_{it} \propto \exp V_g$) near the depletion region ~$V_g \leq V_{th}$ as shown in fig. 3.16. This confirms the presence of continuum of hetero-interface trap states near the AlGaN/GaN layers. Also, these electrically active traps may represent material imperfections such as impurities or point defects, dislocations, etc. that are capable to capture and emit charge carriers with a

specific time constant. A decrease in hetero-trap state density (D_{it}) probably associated with the edge dislocation densities were eventually reflected in conductance analyses too.

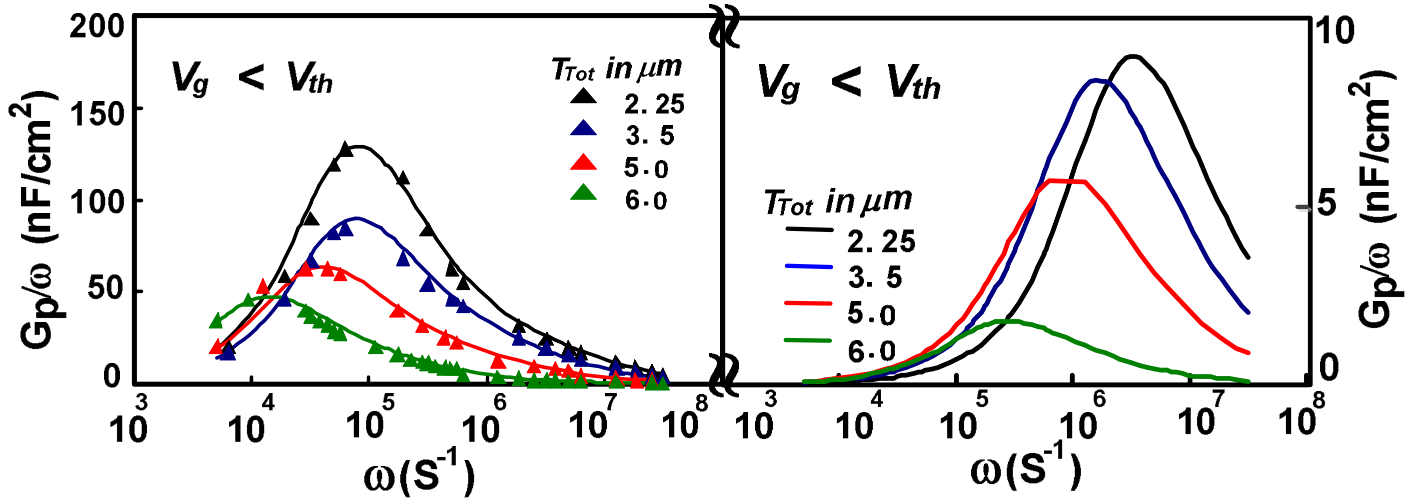

FIG. 3.15. (a) Parallel conductance as a function of angular frequency at selected gate voltages near depletion for AlGaN/GaN HEMT structures grown with an increasing T_{tot}. (b) Contribution of hetero-interface trap states to the measured parallel conductance.

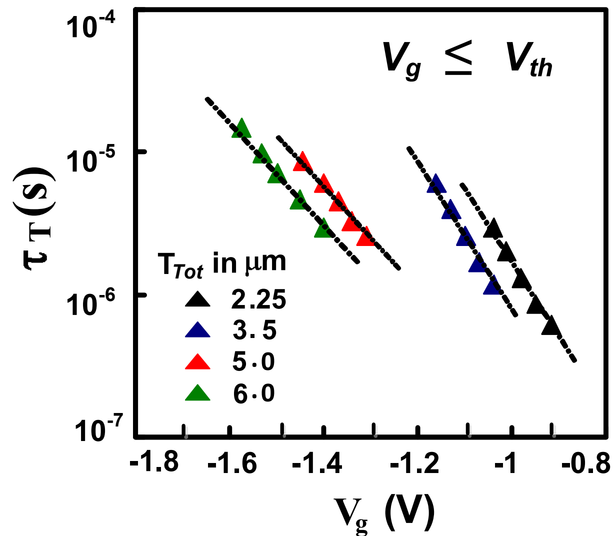

FIG.3.16. Hetero-interface trap time constants as a funciton of gate voltages in the vicinity of depletion region for AlGaN/GaN HEMT heterostructures grown with an increasing T_{tot}.

The hetero-interface traps, otherwise termed as fast traps as a function of epilayer thickness were exclusively studied by conductance technique and are shown in fig. 3.17. The extracted AlGaN/GaN hetero-interface state density (D_{it}) versus the gate voltages ($V_g \leq V_{th}$) normalized to the V_{th} showed a decreasing trend with respect to the increase in T_{tot}.

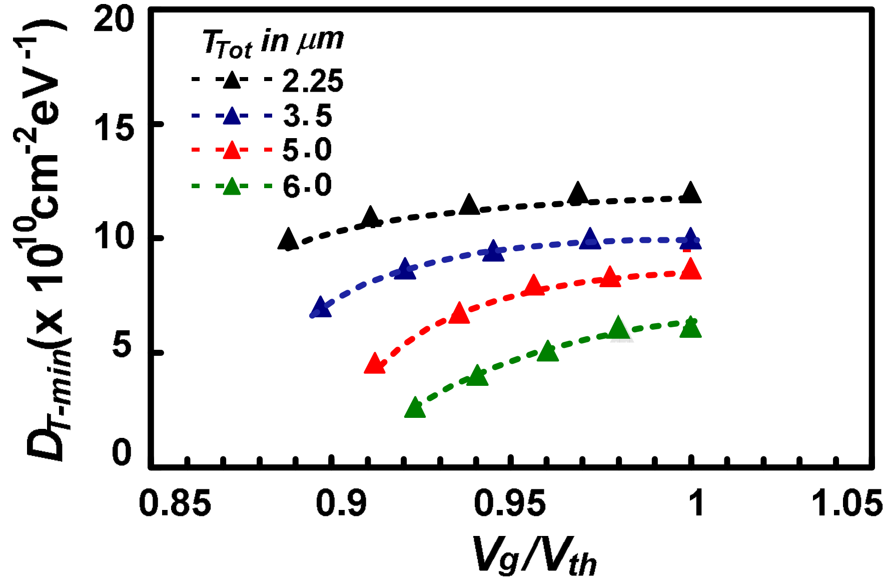

FIG. 3.17. Hetero-interface state density versus the gate voltages normalized to the threshold voltage for AlGaN/GaN HEMT heterostrucutures grown with an increasing T_{tot}.

Furthermore, the comparison chart of previous and present $D_{it\text{-}min}$ results versus T_{tot} exclusively with similar kind of traps evaluated from conductance analyses is also shown in fig. 3.18. The $D_{it\text{-}min}$ is the minimum value of hetero-interface state density that can be extracted near the depletion region. The τ_{it} in this study and in the references was well within the comparable range between (0.1 -10 μs). In addition, the composition in Al_xGaN layer was x ≥ 20 % and the barrier layer thickness considered was also reasonable. A $D_{it\text{-}min}$ value of 2.5 x 10^{10} cm^{-2}eV^{-1} was observed for AlGaN/GaN heterostructures grown with T_{tot} ~6 μm. In contrast, the $D_{it\text{-}min}$ value for similar

AlGaN/GaN heterostructures with thin T_{tot} ~2.25 μm was 1 x 10^{11} $cm^{-2}eV^{-1}$. However, this value is low when compared to heterostructures ($T_{tot} \leq 3$ μm) grown without the multipairs of AlN/GaN buffer layers [37].

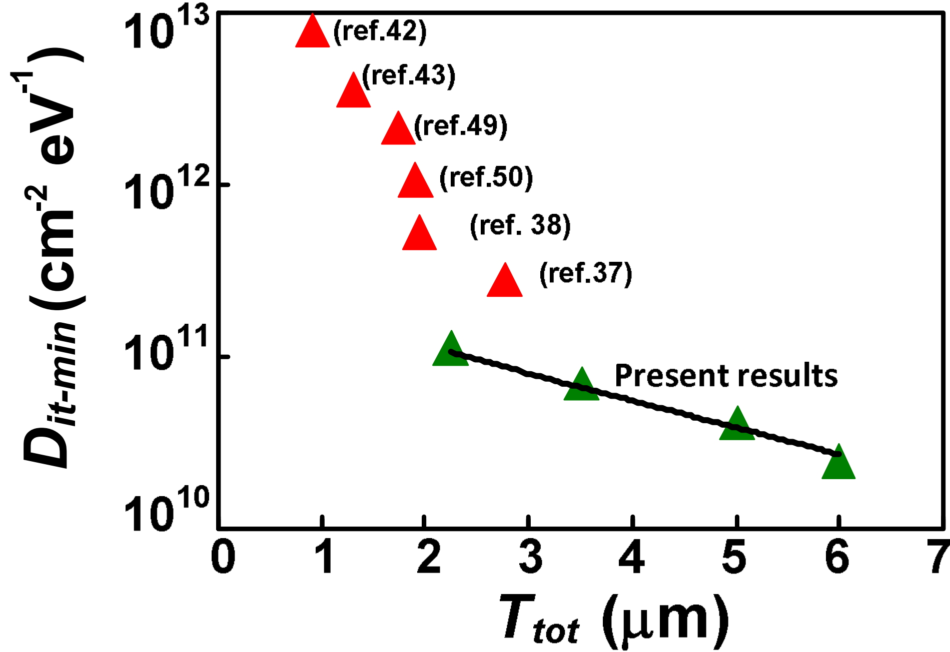

FIG. 3.18. A comparision chart of $D_{it\text{-}min}$ for AlGaN/GaN HEMT heterostructures from conductance analyses versus T_{tot}. The AlGaN/GaN HEMT heterostructures in this work were all grown using thick AlN/GaN multilayers. The solid line represents the exponential fitting for $D_{it\text{-}min}$ versus T_{tot}.

A significant decrease in $D_{it\text{-}min}$ by nearly an order was evident with an exponential dependence on T_{tot}. From the slope of $D_{it\text{-}min}$ against T_{tot}, it was found that the interface traps concentration decreased by a factor of ≅ 2 x 10^{10} $cm^{-2}eV^{-1}$ per unit increase in T_{tot} (in μm). Ultimately, the reduced $D_{D\text{-}edge}$ and $D_{it\text{-}min}$ with an increasing T_{tot} further suggests that dislocations or extended line defects can be a factor that influences the AlGaN/GaN hetero-interface traps. The presence of extended defects due to

dislocations mostly located at the AlGaN/GaN hetero-interface was also confirmed by Fourier Transform (FT-DLTS) technique [48]. A decrease in 2-DEG density for AlGaN/GaN HEMT structures with respect to thin T_{buff} confirms that the hetero-interface traps are acceptor like.

3.7. Summary

In summary, the hetero-interface trapping characteristics of MOCVD grown AlGaN/GaN HEMT heterostructures on silicon substrate with increasing buffer thickness were extensively studied. The frequency dependent conductance analyses revealed an exact exponential dependence of interface trap time constants on applied gate bias near the threshold voltage. A low D_{it-min} value of 2.5 x 10^{10} $cm^{-2}eV^{-1}$ was observed for AlGaN/GaN heterostructure grown using thick buffer layers, T_{buff} ~5 μm. On contrast, similar heterostructures grown using thin T_{buff} ~1.25 μm showed a D_{it-min} value of 1.0 x 10^{11} cm^{-2} eV^{-1}. The HR-XRC and Van der Pauw-Hall measurements also confirms that increasing the T_{buff} improves the AlGaN/GaN HEMT heterostructures and its interface properties as evident from reduced edge dislocations and enhanced N_{D-2DEG} and carrier mobilities respectively. Therefore, good quality MOCVD AlGaN/GaN HEMT heterostructures were grown using thick T_{buff} with reduced D_{D-edge} as observed from the XRC results as well as smoother interface with low D_{it-min} values as evident from increased N_{D-2DEG} and carrier transport properties.

However, considerable amount of surface related slow traps that were present in the AlGaN/GaN hetero-structures has to be minimized by using a passivating material.

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Chapter 4

AlGaN/GaN based metal - oxide - semiconductor high-electron-mobility transistors (MOS-HEMTs)

4.1. Introduction

Although, Schottky gate for GaN HEMTs finds tremendous attention towards high-frequency device applications, it is difficult to utilize them for high-power applications. The drawbacks of Schottky gate invariably of the metal used (Ni or Pt or Pd); include a high gate leakage current, small gate voltage swing (GVS) accompanied by a very low breakdown voltage. An introduction of a thin insulator/oxide (dielectric) layer between the barrier layer and the metal gate would in-turn overcome the drawbacks aforementioned. For better performance of the GaN MOS-devices the quality of the dielectric layer also plays a significant role. Since good quality dielectric layer can passivate the undesirable surface defects that are present in the barrier layer, hence the gate leakage can be considerably reduced in MOS-devices. On the other hand, poor quality of the dielectric layer can lead to additional interface defects which can cause current collapse. Therefore, the deposition condition of the dielectric layer also determines the device characteristics in MOS-devices.

In general, a native oxide can offer a good interface quality with the semiconductor as in the case of SiO_2/Si MOS-devices. However, in the case of compound semiconductors like GaAs and GaN, the unavailability of native oxide (Ga_2O_3) or the suitable deposition condition make it hard to develop a high quality GaN based MOS-devices. This prompts the use of other dielectric materials such as SiO_2, Si_3N_4, SiO_xN, Al_2O_3, Sc_2O_3, ZrO_2, NiO and HfO_2 for GaN MOS-devices [1-8]. Nevertheless,

researchers are keen in developing new dielectric materials as well as improving the quality of existing dielectrics for GaN MOS-devices.

4.2. Oxide, insulator deposition methods

As mentioned earlier, the quality of the oxide layer mainly affects the GaN MOS-devices. Therefore, the deposition condition of the dielectric layer is the key and deciding factor of the effective functioning of an insulated gate transistor. Considerable amount of interface charges if present in the semiconductor/oxide interface, can adversely affect the device characteristics. As the interface charges can act as both virtual gate and parallel conduction path for gate leakage. In addition the interface charges can partially deplete the channel electrons and cause current collapse when operated under rf conditions. Hence, precautions and proper surface cleaning has to be taken care while depositing dielectric layer for AlGaN/GaN MOS-HEMT structures. There are many deposition techniques available for the deposition of dielectric layer depending upon the nature of the dielectric films to be deposited. Although, each technique has invariably its own advantages as well disadvantages. Some of the conventional methods for the deposition of dielectric layers are

(i) Electron Beam (EB) evaporation,

(ii) Sputtering,

(iii) Chemical Vapor Deposition (CVD),

(iv) Metal Organic Chemical Vapor Deposition (MOCVD),

(v) Atomic Layer Deposition (ALD),

(vi) Liquid Phase Deposition (LPD) and other techniques.

Besides these techniques, unconventional methods such as plasma oxidation of AlGaN layer are also available to introduce dielectric layer. Of all the dielectrics/oxides available high~κ dielectric such as Al_2O_3 is highly preferred because of its large band gap (~9 eV), high dielectric constant (~9) and high breakdown field (upto 30 $MVcm^{-1}$), high thermal stability, and a good interface quality with GaN. Furthermore, the use of high- κ Al_2O_3 based AlGaN/GaN MIS transistors can result in superior performance such as low gate leakage current, large GVS, and improved input-output linearity compared to the Schottky gate transistors. On the other hand, materials like SiO_2, SiN, SiON have relatively low band gap and small dielectric constant value.

Following are dielectric deposition methods used for the GaN MOS-devices,

4.2.1. Electron beam evaporation

In this method, the samples are loaded in a high vaccum chamber facing the target anode. Under high voltage, the electron beam bombards the target material and causes the atoms to transform into gaseous phase. This vapor then precipitates into solid form when it comes into contact with the samples or the semiconductor surface. The advantages of the EB evaporation is that, the thickness can be controlled with precision from few angstroms to nanometer with minimum evaporation rate. Substrate temperature can be varied to offer uniform adhesion of the dielectric layer. Prior to loading, the samples are thoroughly cleaned using organic solvents in an ultrasonic bath. Using this technique the dielectrics that can be deposited are SiO_2, SiN, SiON, Al_2O_3, GdO_3 and HfO_x. Oxygen can be used as carrier gas as mostly oxide layers are deposited. The disadvantage of EB evaporation in high vaccum is necessary to create uniform deposition as it is a line of sight deposition method [1, 10-11].

4.2.2. Sputtering

Sputtering is a deposition technique where in atoms or ions are ejected from solid material that acts as source for the dielectric material to be deposited. A high energy radio frequency or direct current (DC) plasma may be used to bombard the target material. Electron cyclotron resonance (ECR) sputtering is also widely used for deposition of insulators. The advantage of sputtering method is the substrate temperature and substrate position can be varied. However the disadvantage includes non-uniformity of the film deposited, difficult to maintain vaccum as it involves plasma source. The secondary ions and atoms that are produced during sputtering can act as defect states including the plasma damage induced on the semiconductor surface. The dielectric materials that are deposited using this technique are the SiO_2, Si_3N_4, SiO_xN, Al_2O_3, Sc_2O_3, ZrO_2, MgO, NiO and HfO_2 depending on the availability of the target material [12-16].

4.2.3. Plasma enhanced chemical vapor deposition (PECVD)

Unlike EB evaporation and sputtering which are physical phenomena, chemical vapor deposition is a material synthesis process which involves highly volatile chemical precursors. Otherwise, PECVD is a transport process of reacting gaseous species to the surface of the substrate where adsorption of the species occurs on the surface. Here the plasma source is used to enhance the thermodynamics of the reactive gaseous species. The advantages of PECVD are the process parameters such as precursors gas ratio, substrate temperature, deposition time, pressure, flow rate can be easily controlled. The dielectric parameters such as deposition rate, microstructure, composition/stiochiometry, thickness, uniformity can also be controlled. The disadvantages includes expensive and involves highly toxic and flammable substances. The precursors can be halides, hydrides,

metal alkyls etc. The dielectric layers that can be deposited are SiO_2, SiN etc., where the precursors are $SiCl_4$, NH_3 and H_2O respectively [17-20].

4.2.4. Metal-organic chemical vapor deposition (MOCVD)

Metal-organic chemical vapor deposition is also a CVD technique where it involves the metal-organic compounds as the primary precursors. Recently, MOCVD has been found to be employed to grow dielectric films for III-V semiconductors because of the advantages of thickness uniformity over large substrate areas, low impurity content and precise thickness control. In MOCVD process, the precursor gas is transported to the deposition chamber by a carrier gas (e.g., NH_3) where it reacts with the reaction gas (e.g., O_2). Using MOCVD method some of the insulators deposited are AlN, SiO_2, SiN, ZrO_2, NiO, $GdScO_3$ and Al_2O_3. In the case of MOCVD grown Al_2O_3, the precursors employed are tri-methyl aluminum (TMA) and oxygen source [21-24].

4.2.5. Atomic Layer Deposition (ALD)

Atomic layer deposition is a chemical gas phase thin film deposition process based on surface reactions. ALD primarily differs from chemical vapor deposition as ALD involves reactant precursors that are separated and pulsed on alternative cycles. Hence by keeping the precursors separated throughout the coating process, atomic layer control of the thin film growth can be attained as fine as 0.1 A° per cycle. The advantageous include film thickness control, accuracy, uniformity and conformality. Using ALD, the commonly deposited dielectrics for III-V based MOS-devices are Al_2O_3, HfO_2 and ZrO_2 where in the precursors used are tri-methyl (aluminum, hafnium or Zirconium) (TMA, TMH and TMZr) and H_2O vapor or ozone. As ALD deposited Al_2O_3 is of high atomic precision and good quality it finds wide application for GaN high-power

MOS-HEMTs. Other oxides that are widely deposited using ALD process are SiO_2, ZnO_2, TiO_2, MgO_2 and Nb_2O_5 [25-28].

4.2.6. Liquid Phase Deposition (LPD) and other techniques

Liquid phase deposition of dielectric films is another way to deposit thin dielectric films on the semiconductor surface. Unlike other sophisticated deposition techniques involving complex machine geometry, LPD offers simple deposition process under water bath with suitable solvents. In most cases LPD is temperature and *pH* controlled process. In LPD the sample to be deposited is immersed in a water bath where in the oxidizing solvents are introduced. By this method the native oxides (GaO or AlO_x) can be grown by partially oxidizing the AlGaN or GaN surface. *S. Basu et. al*, have successfully demonstrated the LPD growth of Al_2O_3 on GaN layer by using aluminum sulfate in crystallized water [$Al_2(SO_4)_3.18\ H_2O$] and sodium bicarbonate [$NaHCO_3$] as the precursors under appropriate pH [29]. Other oxidizing agents include $NH_4OH:H_2O_2:H_2O$ or H_2O_2 or H_3PO_4 solution. Sometimes LPD is performed in presence of the illumination (e.g. He:Cd laser) to enhance the oxidation, it is otherwise termed as photo electrochemical oxidation method (PEC) [30]. The advantageous of LPD is simpler and less time consuming and oxides like SiO_2, TiO_2 and ZnO can be deposited. The disadvantageous include difficult to control the film thickness and stiochiometry [31-35].

Other techniques that are unconventional and less commonly used for the formation of oxide layer are surface treatments such as oxygen and N_2 plasma treatments. These techniques are based on utilizing AlO_x that are prone to exists on the AlGaN surface either during the growth or during the sample exposure to air. These methods found to be useful since converting oxide impurity states to AlO_x results in low gate

leakage and MOS like devices. These techniques are effective for thin oxide layer. The demerits are prolonged plasma exposure of sample can cause plasma damages and additional trapping centers that can lead to current collapse [36-38].

4.3. Basics and principle of GaN based MIS/MOS-HEMTs

The metal-oxide/insulator-semiconductor (MOS/MIS)-device is the most comprehensive device in the study of any semiconductor surfaces. The reliability and stability of any semiconductor material is primarily related to its surface conditions. Therefore, an understanding of the surface physics with the help of MIS-diodes is of great importance to device operations. The schematic representation of a basic MIS/MOS-diode or MOS capacitor is shown in fig. 4.1. As shown, the MOS-diode consists of an oxide layer of considerable thickness between the metal gate and semiconductor, unlike a SBD where the oxide layer is absent. The gate metal and the semiconductor act as two parallel plates of capacitors just separated by an oxide/insulator of definite thickness and dielectric constant respectively. A typical example of a MOS-device is SiO_2/Si where in the oxide layer SiO_2 is sandwiched between the metal gate and the semiconductor surface. An Ohmic electrode is placed on the other side of the semiconductor.

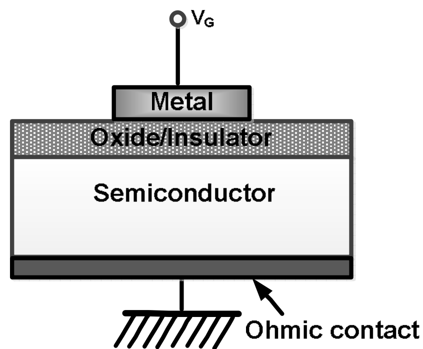

FIG. 4.1. The cross-sectional schematic representation of a conventional MOS-diode.

Three typical situations can be considered occurring on the semiconductor surface depending upon the bias applied between the gate and Ohmic electrodes respectively.

Accumulation:

Considering an n-type semiconductor and a positive gate bias ($V_g > 0\ V$) when applied, the majority carriers that is the free electrons are attracted close to the oxide-semiconductor interface. As a result, the energy bands at the semiconductor surface bend downward and the conduction band become closer to the Fermi energy level with more electrons accumulated near the oxide-semiconductor interface. This condition of the MOS-diode is called accumulation as illustrated in fig. 4.2 (a). The oxide capacitance (C_{ox}) can also be extracted in the accumulation region by knowing the thickness and dielectric permittivity of the material.

Depletion:

A small negative bias ($V_g < 0\ V$) when applied to the MOS-diode, the energy bands are bent upwards and the carrier electrons are started to deplete away from the oxide-semiconductor interface. This is called depletion and the measured capacitance starts to decrease with increasing negative bias. In other words the depletion width extends towards the semiconductor substrate as more negative gate bias is applied. The energy bands in the depletion regime is shown in fig. 4.2 (b)

Inversion:

Considering large negative bias is applied to the MOS-diode, so that the energy bands bend upwards furthermore, so that the intrinsic level at the surface crosses over the Fermi level. As a result, the number of minority carriers (holes) is larger near the semiconductor surface and is called inversion as shown in fig. 4.2 (c). A strong inversion

occurs when the hole concentration near the oxide-semiconductor interface is nearly equal to the semiconductor doping level and this is obtained at large negative gate bias.

The most important characteristics of a MOS-diode/capacitor are the Capacitance-Voltage response as shown in fig. 4.3. For any MOS-capacitor, the capacitance changes with the applied gate bias. The measurement involves the constant DC bias applied at the diode along with a small test ac signal. And the capacitance can be determined by using the parallel plate capacitor equation,

$$C = \frac{\varepsilon_0 \varepsilon_r A}{t} \tag{4.1}$$

In the equation 4.1, ε_0, ε_r are permittivity of free space and the material respectively, A is the diode area and t is the thickness of the oxide layer.

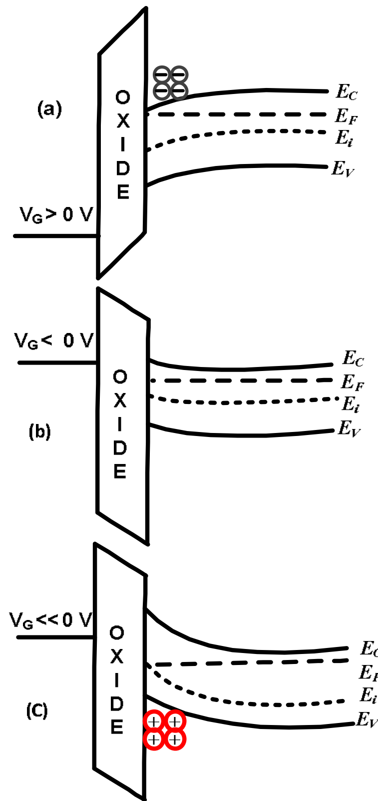

FIG. 4.2. The energy band diagrams of ideal MOS-diode at (a) accumulation (b) depletion and (c) inversion.

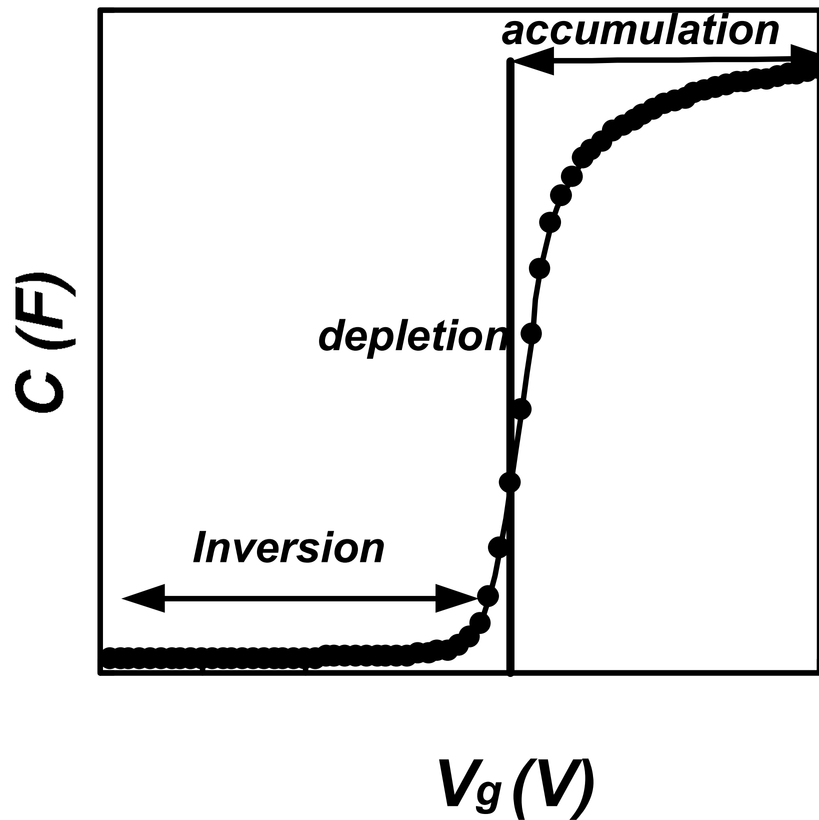

FIG. 4.3. Typical capacitance-voltage curve of an ideal MOS-diode

In the case of wide-band gap semiconductors such as GaN, it is impossible to form the inversion region due to extremely long generation time of the minority carriers. Thus the depletion layer extends further into the GaN channel layer and is termed as deep depletion layer as the capacitance tends to a minimum value with negative gate bias. For GaN based MOS-HEMTs three electrodes form the device structure. The two Ohmic contacts are called the source and drain electrodes respectively. The gate electrode is located on the oxide/insulator and in-between the Ohmic contacts. By varying the gate bias, the effective channel thickness can be modified/modulated by varying the width of the depletion region as described earlier [39-43].

4.4. Fabrication of thermally oxidized Al_2O_3/AlGaN/GaN MOS-HEMTs

In the past decade of years, various insulating materials like Al_2O_3, SiO_2, Si_3N_4, SiO_xN, and HfO_2 have been widely studied and reported for AlGaN/GaN MOS/MIS HEMT. Among the insulators available Al_2O_3 is promising due to its large band gap and high dielectric constant (~9). Several researchers have demonstrated the growth of Al_2O_3 on AlGaN/GaN HEMT structure by conventional techniques like LPD [29], ALD [2] and MOCVD [24] for AlGaN/GaN MOS-HEMT applications. Few studies were made to convert Al layer into its respective oxide before gate metallization for AlGaN/GaN HEMT [36-37]. These approaches were based on diffusion of oxide impurity states that exist in AlGaN surface into the pure Al layer. For effective suppression of charge non-uniformities, gate leakage and enhancement of *B-V,* Al oxidation at elevated temperature is desirable. Therefore, we experimented oxidative coupled annealing of 10 nm pure Al layer which can act as an effective gate dielectric for AlGaN/GaN heterostructures [44].

The AlGaN/GaN heterostructures were grown on 4 in. *p*-Si (111) substrate using Taiyo Nippon Sanso SR-4000 MOCVD system. For the given structure the Al concentration and thickness of AlGaN layer was fixed as 26% and 25 nm respectively. A Hall mobility of 1520 cm^2/Vs, a sheet resistance of 413 Ω/cm^2 and a sheet carrier concentration of $9.94 x 10^{12}$ cm^{-2} were recorded for the sample using Van der Pauw Hall measurements. The device fabrication started with mesa isolation using BCl_3 plasma based Reactive Ion etching (RIE). The devices were passivated using electron beam evaporated SiO_2. Ohmic patterns were performed using photolithography followed by metallization of Ti/Al/Ni/Au (15/80/12/40 nm). The Ohmic contacts were annealed at 850°C using infra-red lamp annealing for 30s in N_2 ambient. Gate lithography was

performed to define Al_2O_3 layer under the Schottky gate. A 10 nm pure Al layer was deposited by filament heating at the patterned gate region. A base pressure of $7x10^{-5}$ Pascal was maintained and the evaporation rate was as minimum as 0.1 nm/sec. The samples were transferred to the oxidative annealing chamber where Al layer was oxidized/annealed at $600^{\circ}C$ for 15 minutes at a constant oxygen flow rate of 4.5 ml/min and at atmospheric pressure. Finally, gate and contact metals Pd/Ti/Au (40/20/60 nm) was deposited followed by lift off. Figure 4.4 shows the cross-sectional schematic representation of a fabricated Al_2O_3/AlGaN/GaN MOS-HEMT. By this method, the oxide impurities especially near the gate electrode can be eliminated and hence can expect lower gate leakage current.

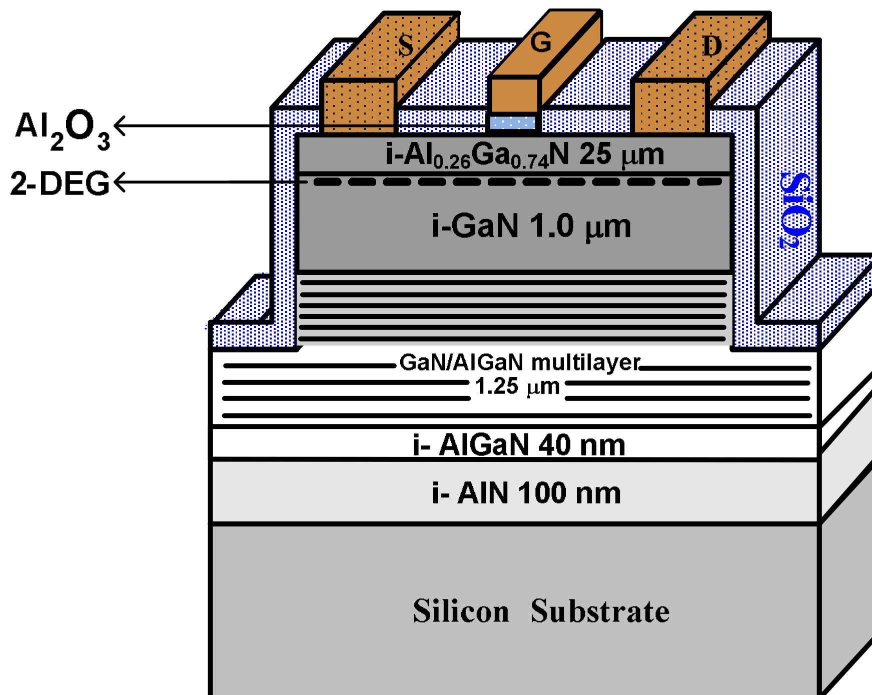

FIG.4.4. Cross-sectional schematic representation of Al_2O_3/AlGaN/GaN MOS-HEMT.

4.5. Surface and compositional analyses of oxidized Al layer

4.5.1. X-ray photoelectron spectroscopy (XPS) analyses

XPS analyses were carried out to confirm that as deposited pure Aluminum layer has been partially or fully converted into the respective oxide layer. XPS measurements were recorded using SSX-100 with AlKα monochromator source. The oxidized Al layer was scanned and it consists of Al2*p* peak at a higher binding energy of 75.7 eV as shown in fig.4.5. The alumina surface was precisely etched up to the AlGaN surface and XPS measurements were carried out. An Al2*p* peak at binding energy of 74.5 eV corresponding to Al-N bond in AlGaN barrier layer was observed. On the other hand, we did not observe any metallic Al2*p* peak at low binding energy between 65 to 73 eV, neither in alumina surface nor in the AlGaN barrier layer. This also confirmed the absence of metallic Al-Al bond under the gate electrode.

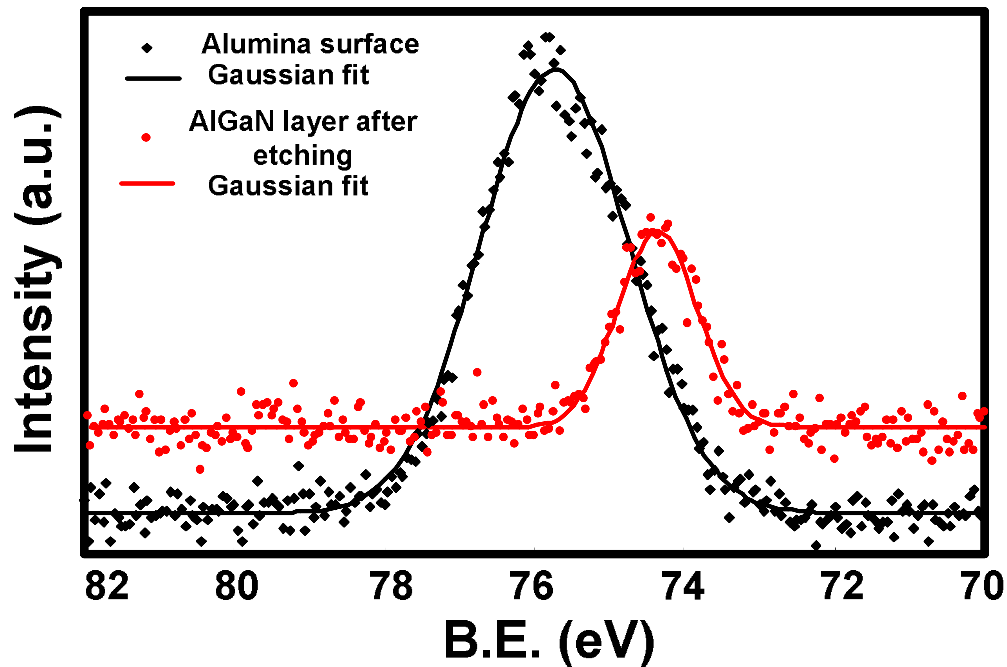

FIG. 4.5. Core level Al2*p* signal from Al_2O_3 surface and AlGaN layer.

The O1*s* peak was observed at a binding energy of 532.8 eV as shown in fig. 4.6. The higher binding energies of Al2*p* and O1*s* indicate nearly stoichiometric alumina layer. Since the alumina exists in several forms, we could not distinguish the exact phase in which it exists. Similar binding energy was also reported in other papers [29, 45].

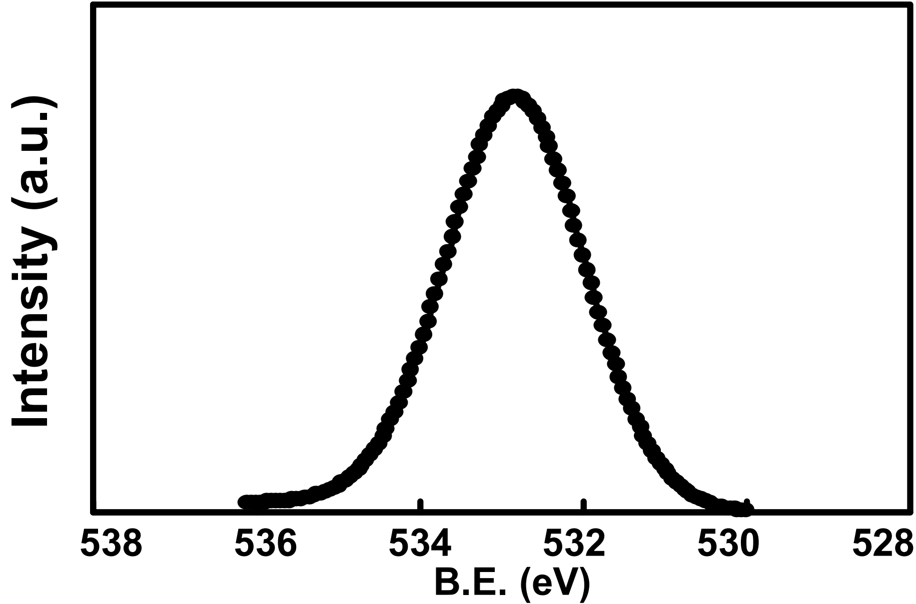

FIG. 4.6. Core level O 1s signal from Al_2O_3 surface.

4.5.2. Atomic force microscopy (AFM) analyses

The morphological investigations of the Al_2O_3 were carried out using Seiko SP 300 Sound Proof Housing AFM system as shown in fig. 4.7. Using AFM, images with very good atomic resolution have been obtained for the oxide layer. Because AFM does not involve the induction of a tunneling current between the probing tip and sample, it can be applied to study oxide systems that have low conductivity such as insulators or wide band-gap semiconductors [46]. The R_{MS} and *P-V* measured from AFM of Al_2O_3 were around 1.5 nm and 1.3 x 10^1 nm respectively.

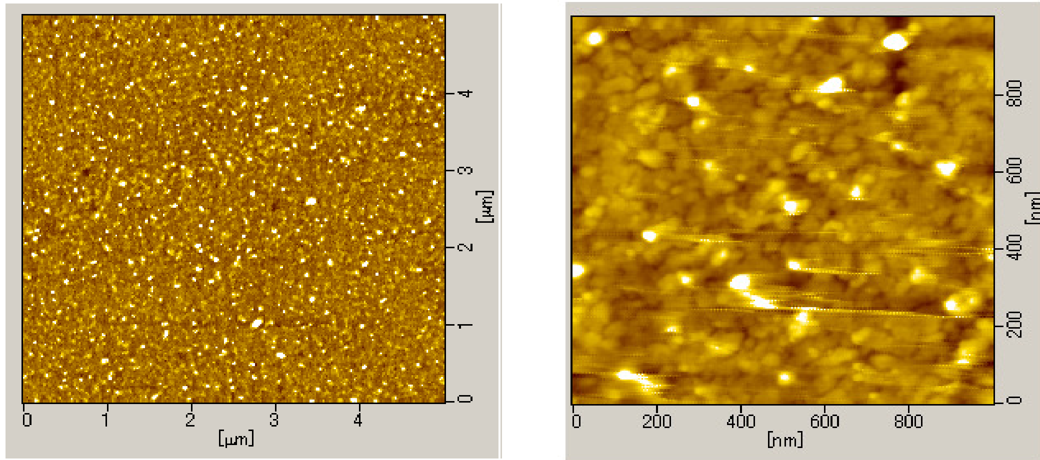

Fig. 4.7. AFM images of Al_2O_3 layer at scan area of 5 x 5 and 1 x 1 μm^2 respectively.

4.5.3. Cross-sectional Transmission electron microscopy (TEM) analyses

Cross-sectional TEM analyses were carried out to evaluate the thickness and the nature of the Al_2O_3 layer on AlGaN surface. From the TEM images (see fig. 4.8), the thickness of the Al_2O_3 layer was found to be little larger (12 ± 2 nm) than the deposited 10 nm pure Al layer. This is consistent as one can expect the volume of pure Al to expand when metal is converted into its oxide. This also indirectly signifies that the deposited Al layer has been transformed fully into oxide and was amorphous.

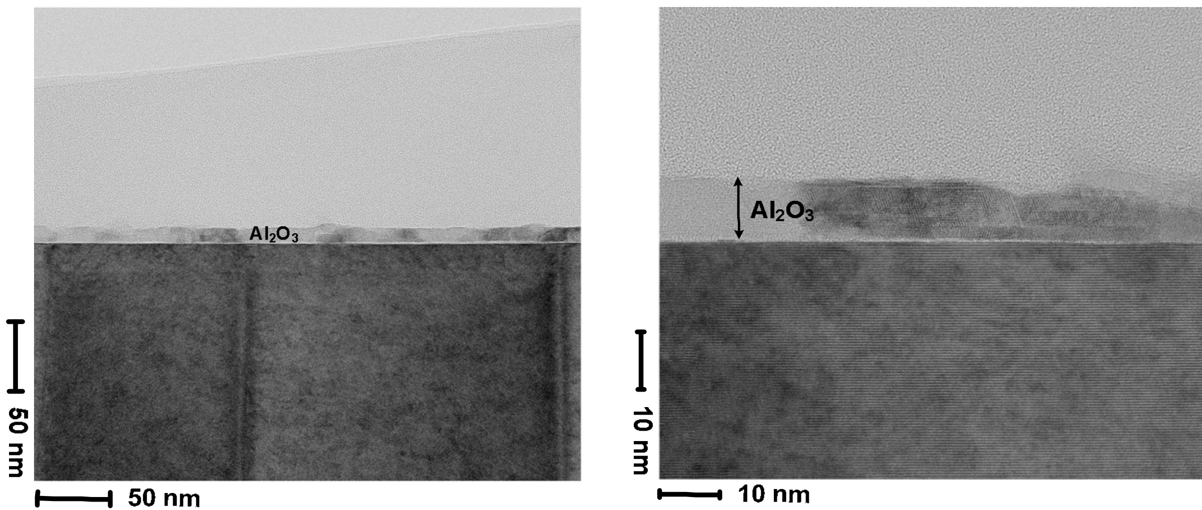

FIG.4.8. Cross-sectional magnified TEM images of Al_2O_3/AlGaN layers.

4.6. Device characterisistics of Al_2O_3/AlGaN/GaN MOS-HEMTs

In order to investigate effect of the Al_2O_3 layer on MOS-HEMT, electrical characterizations were performed. For comparison, conventional HEMT was fabricated without the Al_2O_3 as the dielectric layer. The dc I_{ds}-V_{ds} and transfer characteristics were studied using Agilent 4156C semiconductor parameter analyzer, while *C-V* measurements were carried out using HP 4284A LCR meter. The three terminal (*off-state*) *B-V* measurements were performed using Kiethley Pico-ammeters.

4.6.1. Current-Voltage (I_{ds}-V_{ds}) characteristics

The standard three terminal I_{ds}-V_{ds} for HEMT showed gate leakage at V_g = 2 V, wherein the MOS-HEMT showed no gate leakage current as shown in fig. 4.9 (a) and (b). However, a small decrease in drain current ($I_{ds\text{-}max}$) was also observed for MOS-HEMT. The drain current density ($I_{ds\text{-}max}$) for HEMT and MOS-HEMT were 593 and 425 mA/mm respectively. The observed threshold voltage for HEMT and MOS-HEMT were -2.1 and -2.8 respectively. The increased gate to channel separation due to 10 nm insulating layer is responsible for the V_{th} shift towards negative side.

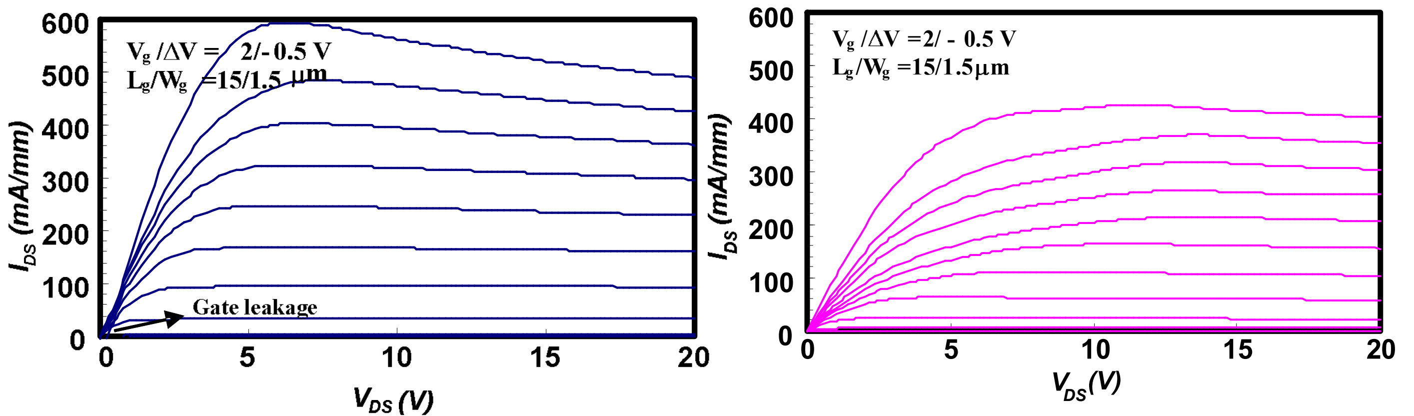

FIG. 4.9. Typical I_{ds}-V_{ds} characteristics of (a) AlGaN/GaN HEMT with gate leakage and (b) Al_2O_3/AlGaN/GaN MOS-HEMT without any gate leakage.

4.6.2. Transfer characteristics

The transfer and logarithmic I_{ds}-V_{ds} characteristics are shown in fig. 4.10. The peak transconductance ($g_{m\,max}$) for conventional HEMT and MOS-HEMT (@ V_{DS} = 4 V) and with similar device dimensions were 124 and 121 mS/mm respectively. This is reasonable because in MOS-HEMT, an additional 10 nm oxide layer can increase the gate to channel separation. As a result, a small decrease in transconductance and a moderate increase in the V_{th} could be expected in MOS-HEMTs with high ~*k* gate dielectrics [47]. The decrease in $I_{DS\,max}$ and g_{mmax} is due to the presence of the Al_2O_3 layer in MOS-HEMT. The MOS-HEMT also exhibited high on/off ratio of the order of 10^4 compared to the normal HEMTs.

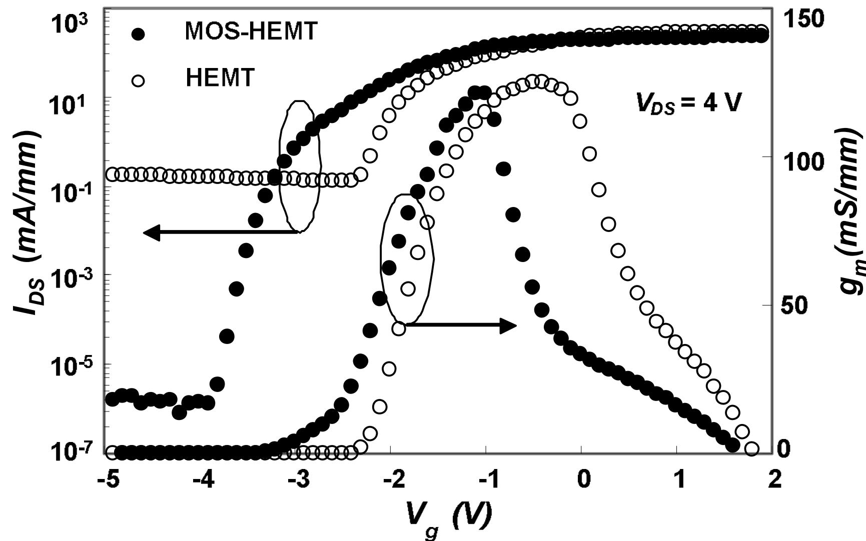

FIG. 4.10. Transfer characteristics of HEMT and Al_2O_3 based MOS-HEMT.

4.6.3. Capacitance-Voltage (*C-V*) measurements and 2-DEG profile

High frequency (1MHz) *C-V* measurements were done in order to evaluate the thickness of the oxide layer. The *C-V* curve (fig.4.11: inset) of both HEMT and MOS-HEMT showed a good transition from depletion mode to accumulation mode suggesting

good interface between the AlGaN layer and the Al_2O_3. The zero bias capacitances of HEMT, MOS-HEMTs were 245 and 175 pF respectively. The dielectric thickness (d_{ox}) was calculated using the equation

$$1/C_{MOS\text{-}HEMT} = 1/\ C_{ox} + 1/C_{HEMT} \tag{4.2}$$

where C_{ox} is the oxide capacitance

$$d_{ox} = \varepsilon_0\ \varepsilon_{oxide}\ A/\ C_{ox} \tag{4.3}$$

In the above equation ε_{oxide} is the dielectric constant of Al_2O_3 ($\varepsilon_{oxide} = 9$) and ε_0 is the vaccum permittivity. A schottky and MOS-diode of uniform area 7.07 $X10^{-4}$ cm^{-2} are available in the same HEMT and MOS-HEMT pattern respectively. The *2DEG* carrier concentration observed for HEMT and MOS-HEMT were 5.1 x 10^{20} cm^{-3} and 2.8 x 10^{20} cm^{-3} respectively as shown in fig. 4.11. The 2DEG for HEMT was observed at 25 nm and the same for MOS-HEMT was observed at 36 nm. This also confirms that the deposited Al has been transformed into respective oxide and do not form part of Schottky gate. The oxide thickness calculated and measured were consistent (10± 2 nm) in MOS-HEMT.

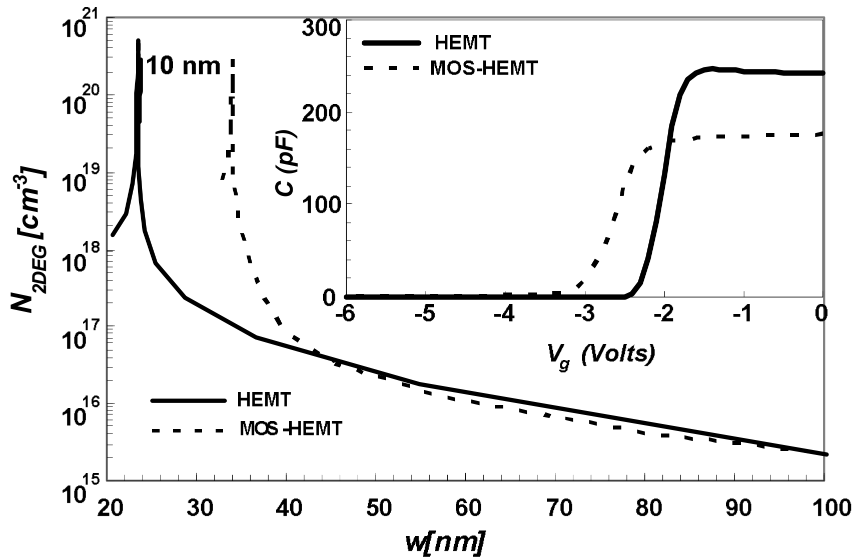

FIG. 4.11. Carrier concentration of HEMT and Al_2O_3 based MOS-HEMT versus depth profile evaluated from *C-V* measurements. (Inset: *C-V* curve measured @ 100 kHz).

4.6.4. Three terminal leakage and breakdown measurements

Three terminal (*off-state*) breakdown measurements were carried out by maintaining a constant V_g of -5 V with increasing V_{DS} voltage. Since the V_g was -5 V the 2DEG channel is closed and the leakage current emanating from the substrate, the buffer and gate of HEMT and MOS-HEMT were sweeped. It is notable from figs. 4.12 (a) and (b) that for HEMT the breakdown voltage (*BV*) was 256 V where as the *B-V* for MOS-HEMT was 431 V. This reflects on the gate leakage (I_g) which contributes to the *BV*.

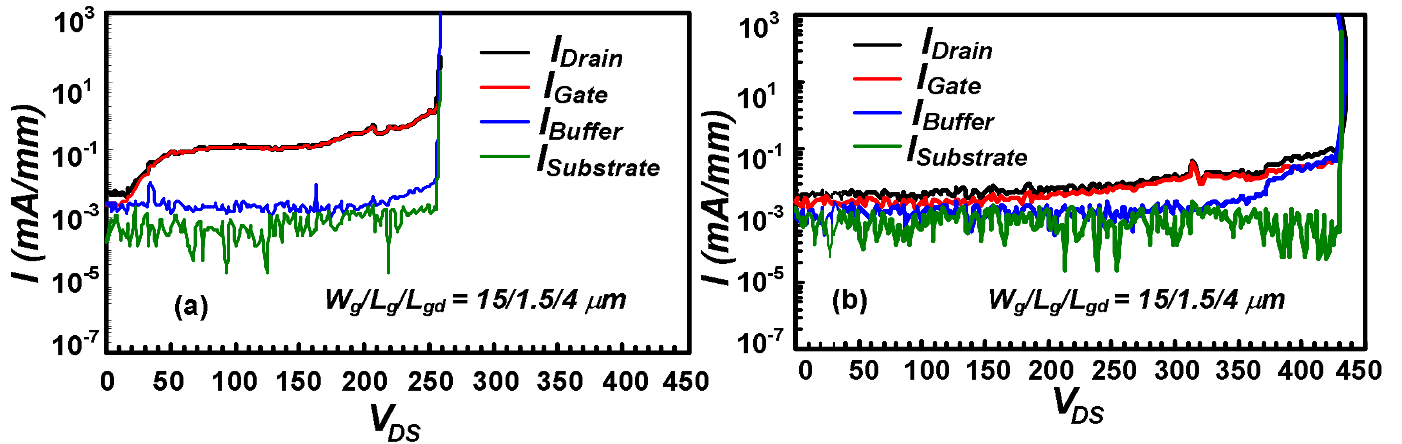

FIG. 4.12. Three-terminal (*off-state*) breakdown measurements for (a) AlGaN/GaN HEMT and (b) Al_2O_3 based MOS-HEMT.

In MOS-HEMT, the gate leakage was suppressed by two orders of magnitude and thereby enhancing the *BV*. The drain breakdown occurs mainly due to the field developed at the drain–gate region. To overcome the electric field, and to increase the *BV*, overlapping gate structures are widely used. On the other hand, one of the effective way to realize high breakdown, for $L_{gd} \leq 4$ μm is, to use oxide layer between the Schottky gate and AlGaN surface. A breakdown of 403 V for L_{gd} of 3 μm has been achieved for AlGaN/GaN HEMT by increasing the buffer thickness to 7 μm and GaN thickness of 2

μm [47]. But in this study, using Al_2O_3 as gate dielectric a *B-V* of 431 V for L_{gd} of 4 μm was achieved by maintaining a very thin buffer as well as GaN layers of 1.0 and 1.25 μm respectively. The results indicate that for the given buffer thickness, the leakage current due to buffer remains almost the same for HEMT and MOS-HEMT but the I_g increases abruptly in the HEMT, which result in premature breakdown. When the voltage approaches breakdown, the leakage current increases rapidly and is therefore destructive for the device [47]. This abrupt increase of I_g has been reduced by using Al_2O_3 in the MOS-HEMT, which results in a high *B-V*. The FOM = $(BV)^2/R_{on}$ was calculated both for HEMT and MOS-HEMT. The specific on-state resistances (R_{on}) of HEMT and MOS-HEMT were 4.28 x 10^{-4} and 9.854 x 10^{-4} Ωcm^2 respectively. The FOM of AlGaN/GaN HEMT with and without Al_2O_3 were 1.53 x 10^8 and 1.89 x 10^8 $V^2\Omega^{-1}cm^{-2}$. The *B-V* and FOM value of MOS-HEMT is the highest reported for any dielectric at $L_{gd} \leq 4$ μm without using any slant fields or overlapping gate insulators.

The suppression of I_g could be described on the basis of surface phenomena of AlGaN as well as on annealing effects performed during oxidation. During the growth of AlGaN/GaN, heterostructures oxygen impurities are incorporated unintentionally. As a result of these oxygen impurities existing on the AlGaN surface tunneling transport occur at the AlGaN and Schottky interface which is responsible for the high gate leakage current. The presence of unintentional oxide impurities on the AlGaN surface is irresistible and the consequent high gate leakage is unavoidable. However, the disadvantageous oxide impurities can be made as an advantageous source for Al_2O_3 synthesis. Thus, in the case of Al_2O_3 MOS-HEMT, it is considered that the initial 2 to 3nm Al_2O_3 is immediately oxidized by absorbing the oxide impurity states present in the

AlGaN surface and the rest of the oxidic layer grows in oxygen ambient at 600 °C. Furthermore, the leakage current density could be reduced considerably by a high-temperature annealing of oxide films [29, 48].

4.7. Analyses of trapping effects in Al_2O_3/AlGaN/GaN MOS-HEMT structures by frequency dependent conductance technique

Frequency dependent conductance measurements of AlGaN/GaN MOS-HEMT were performed to evaluate the interface trap density (D_T) and trap state time (τ_T). Figure 4.13 shows the plot of parallel conductance (G_p/ω) as a function of frequency for selected gate voltages near V_{th}. The G_p/ω values are calculated according to the expression [43, 49],

$$G_p/\omega = \omega G_m C_b^2 / \{G_m^2 + \omega^2 (C_b - C_m)^2\} \quad (4.4)$$

where C_b is the barrier capacitance, G_m and C_m are the conductance and capacitance measured at frequencies between 1 kHz to 1 MHz. The G_p/ω as a function of ω is expressed by the equation

$$G_p/\omega = (qD_T / 2\omega\tau_T) \times \ln [1 + (\omega\tau_T)^2] \quad (4.5)$$

The experimental G_p/ω values agreed well with the theoretical fitting values and only fast traps (~μs) were evaluated in the case of Al_2O_3/AlGaN/GaN MOS-HEMT, unlike the AlGaN/GaN HEMTs which exhibited both surface related slow traps and fast traps as discussed briefly in chapter 3. This also suggests that the surface traps are passivated by the oxidative annealing of pure Al layer at elevated temperature.

The values of D_T and τ_T are extracted by fitting the experimental G_p/ω. We evaluated a maximum D_T of 6.7 x 10^{12} $cm^{-2}eV^{-1}$ with a τ_T of 46 μs and a minimum D_T of

2.2 x 10^{12} $cm^{-2}eV^{-1}$ with a τ_T of 1.3 μs. The τ_T as a function of V_g in the vicinity of V_{th} as shown in fig. 4.14. The τ_T shows an exponential increase versus V_g near threshold voltage.

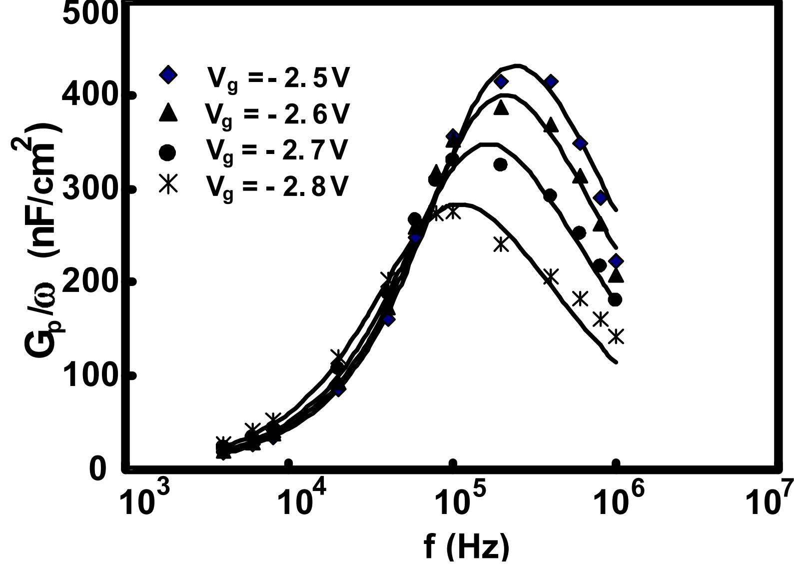

FIG. 4.13. Frequency dependent parallel conductance as a function of radial frequency for selected gate voltages near V_{th}.

The trap state energy can be evaluated using the equation,

$$E_T = \mathrm{kTln}\ (\sigma_T N_c \upsilon_T)\ \tau_T \tag{4.6}$$

where k is the Boltzman constant, T is the absolute temperature, σ_T is the capture cross section. N_c and υ_T are the density of states in conduction band and average thermal velocity. The values of the parameters are considered according to Ref. 3. The D_T as a function of their energy is shown in fig. 4.14 (b: Inset). The τ_T and D_T values are slightly higher than the one reported by *Kordas et. al.* [3], despite high temperature oxidation. Further, the D_T can be improved by choosing optimal preparation conditions such as temperature and thickness of Al layer. Nevertheless, the surface traps are eliminated in the case of Al_2O_3/AlGaN/GaN MOS-HEMT.

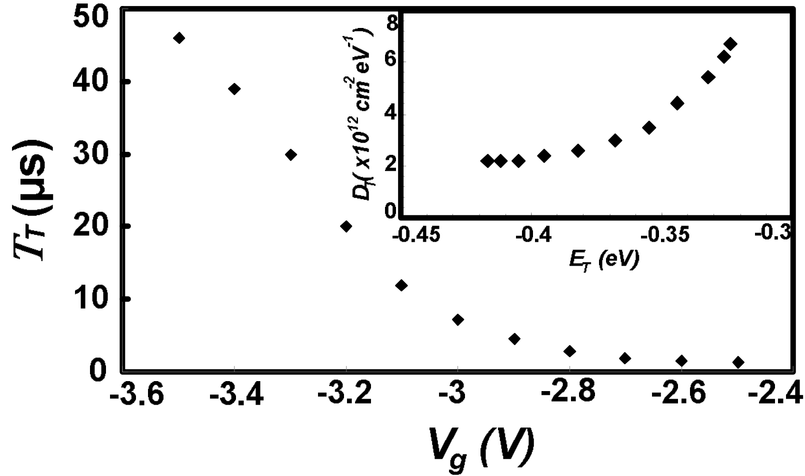

FIG. 4.14. Trap state time as a function of gate voltage of Al_2O_3 based MOS-HEMT. (Inset) Trap state density (D_T) as a function of trap state energy (E_T).

4.8. Summary

A process compatible synthetic route for Al_2O_3 based AlGaN/GaN MOS-HEMT has been developed. The approach is based on oxidative annealing of thin Al layer deposited prior to Schottky gate metallization. The MOS-HEMT exhibits good pinch off features with $I_{ds.\,max}$ and $g_{m\text{-}max}$ of 421 mA/mm and 121 mS/mm. The mechanism of gate leakage has been briefly discussed and has been suppressed by two orders of magnitude using Al_2O_3 layer. A high BV of 431 V and figure of merit (FOM) of 1.89 x 10^8 $V^2\,\Omega^{-1}$ cm^{-2} for ($L_{gd} \leq 4\mu m$) was observed for Al_2O_3 based MOS-HEMT.

Frequency dependent conductance measurements yielded a single continuum of fast trap states. A minimum trap density (D_T) and trap transient time (T_T) of 2.2 x 10^{12} cm^{-2} eV^{-1} and 1.3 μs respectively was observed. The surface traps were absent for the Al_2O_3 based MOS-HEMT due to the effective passivation as well as high temperature annealing.

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Chapter 5

In-situ MOCVD grown AlN/AlGaN/GaN MIS-HEMTs

5.1. Introduction

As discussed in earlier chapters, GaN based HEMTs grown on silicon are attractive for high-power and high- frequency applications. To suppress the gate leakage and to improve breakdown voltage and a larger gate voltage swing, a variety of gate insulators have been used for AlGaN/GaN MIS-HEMTs [1-4]. However, these insulators are deposited *ex-situ* which can introduce additional growth and process related defects. The lack of high quality native oxide (Ga_2O_3) as well as the traps associated in using these foreign/*ex-situ* grown insulators for GaN MIS-devices can adversely hamper the drain current density (I_{ds-max}) under pulsed conditions On the other hand, *in-situ* MOCVD grown thin AlN insulating layer would be advantageous over existing *ex-situ* deposited insulators for its reduced AlN/AlGaN lattice mismatch, high dielectric constant, and large band gap.

Ultra thin AlN layers grown on GaN have also been of great interest recently for a number of applications [5, 6]. High temperature (HT) growth can facilitate the formation of single crystalline AlN insulating layer over AlGaN/GaN heterostructure. On the other hand, for better device performance, lower gate leakage and to prevent tensile strain-induced cracking of AlN layer, low temperature (LT) growth of AlN layer is preferred for MIS-HEMTs [7,8]. Therefore it is worthwhile to study the behavior of trap states existing in AlN/AlGaN/GaN MIS heterostructures (MISHs). Till date, there is lack of adequate information about the *in-situ* MOCVD grown AlN/AlGaN/GaN metal-insulator-semiconductor heterostructures (MISHs) on silicon, for potential applications of AlN MIS devices.

5.2. AlN/AlGaN/GaN MIS-HEMT fabrication

The AlN/AlGaN/GaN MISHs were grown using Taiyo Nippon Sanso, SR 4000 MOCVD system. The MISHs consists of (from the top) 2 nm AlN layer grown at 1030 °C, 25 nm $Al_{0.26}Ga_{0.74}N$ layer, 1 nm AlN spacer interface layer, 1 μm GaN layer, 1.25 μm super lattice structure (SLS) and AlGaN/AlN buffer layer grown over 4 inch p-type Si substrate. The device fabrication started with mesa isolation using BCl_3 plasma based Reactive Ion etching (RIE) [9]. The devices were passivated using electron beam evaporated 100 nm SiO_2. Ohmic patterns were made directly on the AlN layer using conventional photolithography followed by metallization of Ti/Al/Ni/Au (15/80/12/40 nm). The Ohmic contacts were annealed at 850°C using infra-red lamp annealing for 30s in N_2 ambient. Finally, gate metals Pd/Ti/Au (40/20/60 nm) were deposited on the AlN layer followed by lift-off procedure as shown in fig. 5.1.

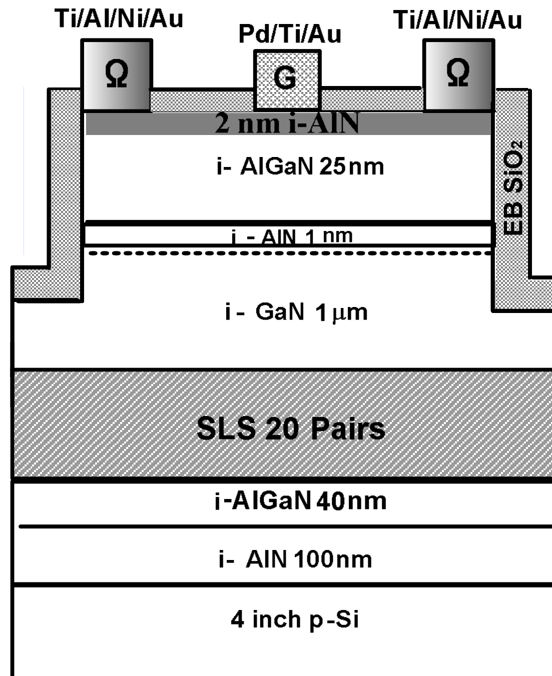

FIG. 5.1. Cross sectional view of MOCVD grown AlN/AlGaN/GaN MIS-HEMT.

5.3. Device characteristics of MOCVD grown AlN/AlGaN/GaN MIS-HEMTs

Electrical characterizations on these MIS-devices were carried out using Agilent B1505 power device analyzer/curve tracer set up connected to a probe station. Circular shaped MIS-diodes of area 7.07 x 10^{-4} cm^2 were used for the *C-V* and *G-V* measurements.

5.3.1. Current -Voltage (I_{ds}-V_{ds}) characteristics

The AlN/AlGaN/GaN MIS-HEMTs exhibited good I_{ds}-V_{ds} characteristics with maximum drain current density (I_{ds-max}) of 235 mA/mm for a gate voltage of +1.5 V as shown in fig. 5.2. The I_{ds-max} is lower than that of the conventional AlGaN/GaN HEMT. The reason for the lower drain current can be due to increased Ohmic resistance, since the Ohmic contacts are placed on the AlN layer than the AlGaN layer [10]. However, low Ohmic contact resistance could be obtained by specific recess etching prior to Ohmic metallization. The *pinch-off* voltage of the MIS-HEMT was -1.7 V. This can vary with the thickness of the AlN insulating layer.

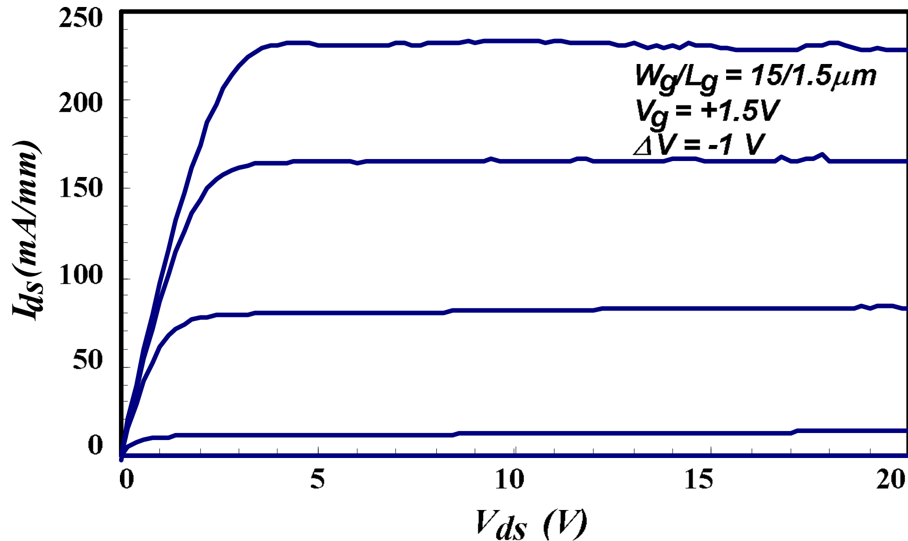

FIG.5 2. Schematic representation of MOCVD grown AlN/AlGaN MIS-HEMT

5.3.2. Transfer characteristics

The AlN/AlGaN/GaN MIS-HEMTs exhibited transfer characteristics with peak transconductance (g_{m-max}) of 76 mS/mm for a drain bias of 4 V as shown in fig. 5.3. The peak transconductance value is also lower than the conventional AlGaN/GaN HEMTs. The exact reason for the low transconductance value is not clearly understood.

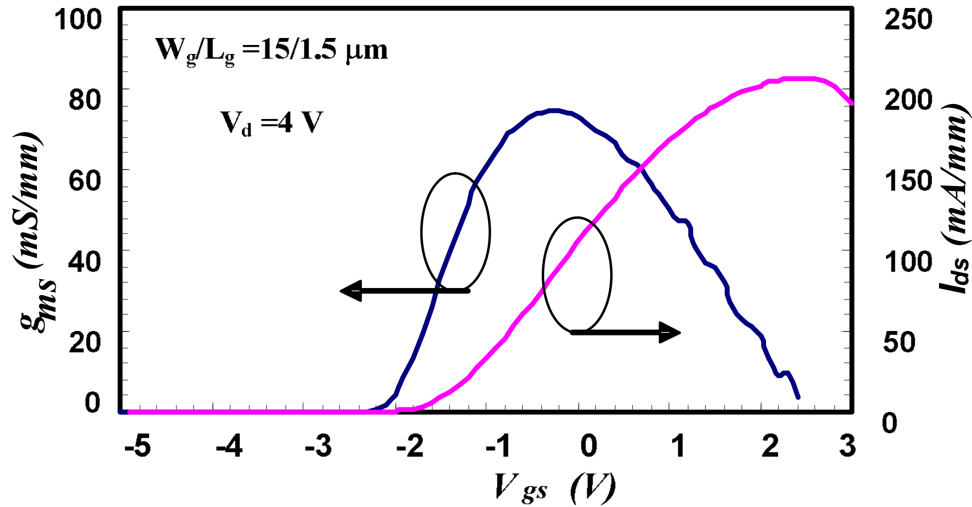

FIG. 5.3. Transfer characteristics of AlN/AlGaN MIS-HEMT

5.3.3. *C-V* measurements and 2-DEG profile

Capacitance voltage measurements performed on MIS-diodes at 100 kHz, showed normal transition from depletion to accumulation regime as shown in the fig.5.4. The V_{th} observed from *C-V* curve was -1.7 V which was in close agreement with the observed V_{th} voltage from *I-V* measurements. Further, the 2-DEG carrier concentration extracted from *C-V* results showed a peak concentration of 10^{19} at a depth of nearly 22 nm (see fig. 5.4: inset). This implies that the 2-DEG exists much closer to the AlGaN/GaN interface [11].

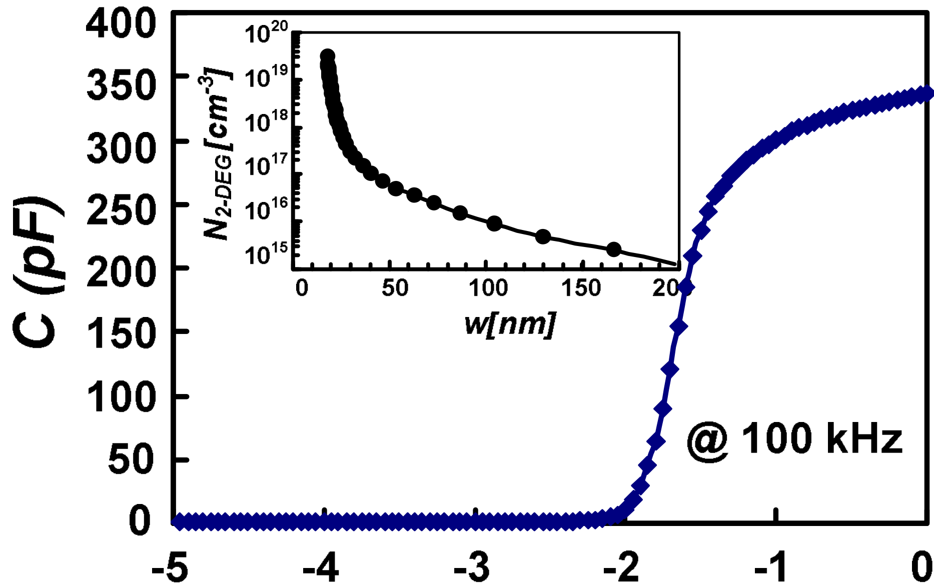

FIG. 5.4. Typical *C-V* curve of AlN/AlGaN/GaN MIS-HEMT. (Inset: 2-DEG concentration versus depth profile evaluated from *C-V* measurements).

5.4. Analyses of trapping effects in *in-situ* MOCVD grown AlN/AlGaN/GaN MIS-HEMT structures on silicon substrate

5.4.1. Traps in AlN/AlGaN/GaN HEMT structures

As discussed briefly in chapter 3, there are various possibilities that a charged carrier can be trapped by the trapping centers present in various epitaxial layers from the substrate to the barrier layer in AlGaN/GaN HEMT. This can be further extended to the case of *in-situ* MOCVD grown AlN/AlGaN/GaN MIS-HEMT structures as an additional AlN insulating layer is present. It is widely accepted that the AlN layer is known to contain defect charges or trapping centers [12, 13]. Further, in the case of MIS-devices the interface between the semiconductor and the insulating layer is a crucial factor for their performance. Therefore, a detailed quantitative and qualitative description on the

trapping properties of the AlN based MIS-devices is necessary for their potential utilization.

5.4.2. Frequency dependent conductance technique for AlN/AlGaN/GaN MIS-HEMT structures

Frequency dependent conductance measurements were performed between the frequency range of 1 KHz to 5 MHz to evaluate the trap state time (τ_T) and trap state density (D_T). Conductance technique for the measurement of trap states in MIS capacitors is generally accepted as the most accurate technique in existence [14-17]. A device V_{th} of -1.7 V was observed for these MIS-diodes from capacitance-voltage (C-V) measurements. Traps due to the insulating and barrier layers in a MIS structure can be explicitly studied by selectively chosen voltages near the V_{th}.

The equivalent parallel conductance (G_p/ω) values are calculated according to the equation,

$$\frac{Gp}{\omega} = \frac{\omega G_m C_b^2}{G_m^2 + \omega^2 (C_b - C_m)^2}, \tag{5.1}$$

where C_b is the barrier capacitance, G_m and C_m are the conductance and capacitance measured at different frequencies and gate bias respectively. The G_p/ω as a function of radial frequency (ω) is given by the equation,

$$\frac{Gp}{\omega} = \frac{qD_T}{2\omega\tau_T} \text{ x } \ln[1+(\omega\tau_T)^2]. \tag{5.2}$$

The D_T and τ_T are parameters that are extracted by fitting the experimental G_p/ω values. The G_p/ω values were plotted against ω for selected gate voltages near the

vicinity of V_{th}. The G_p/ω-ω plot for in-situ MOCVD grown AlN/AlGaN/GaN MIS-diode at V_g = -1.2, -1.6 and -1.8 V are shown in figs. 5.5 to 5.7 respectively.

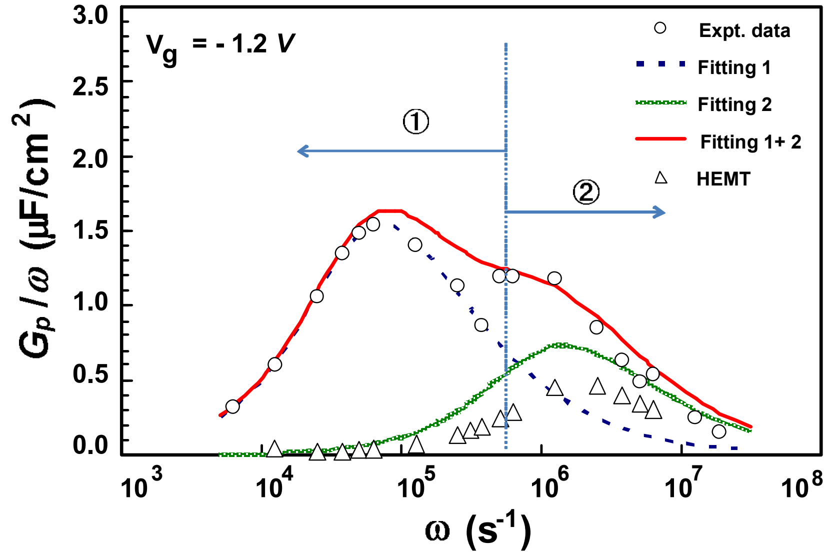

FIG. 5.5. G_p/ω as a function of ω for *in-situ* MOCVD grown AlN/AlGaN/GaN MIS-diode at V_g=-1.2 V. The open triangles represent G_p/ω as a function of ω for AlGaN/GaN HEMT SBD without the insulating AlN layer.

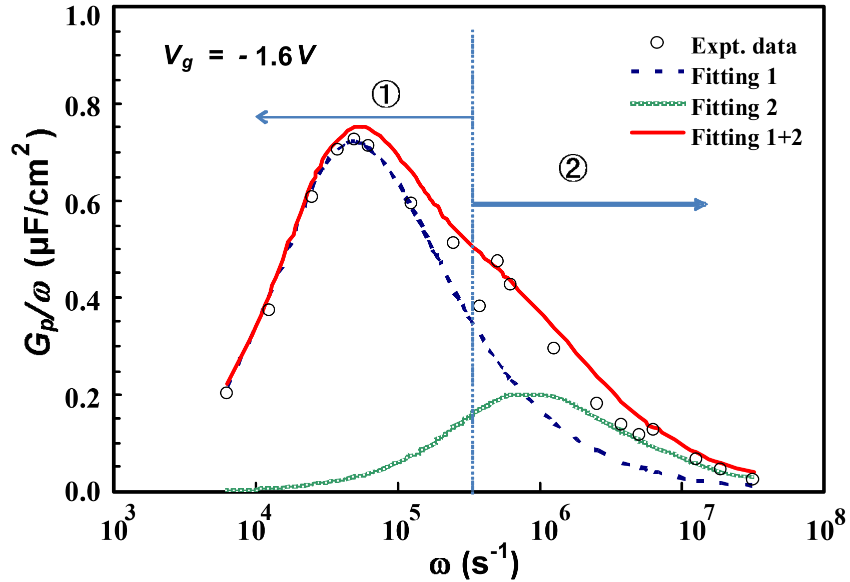

FIG. 5.6. G_p/ω as a function of ω for *in-situ* MOCVD grown AlN/AlGaN/GaN MIS-diode at V_g=-1.6 V.

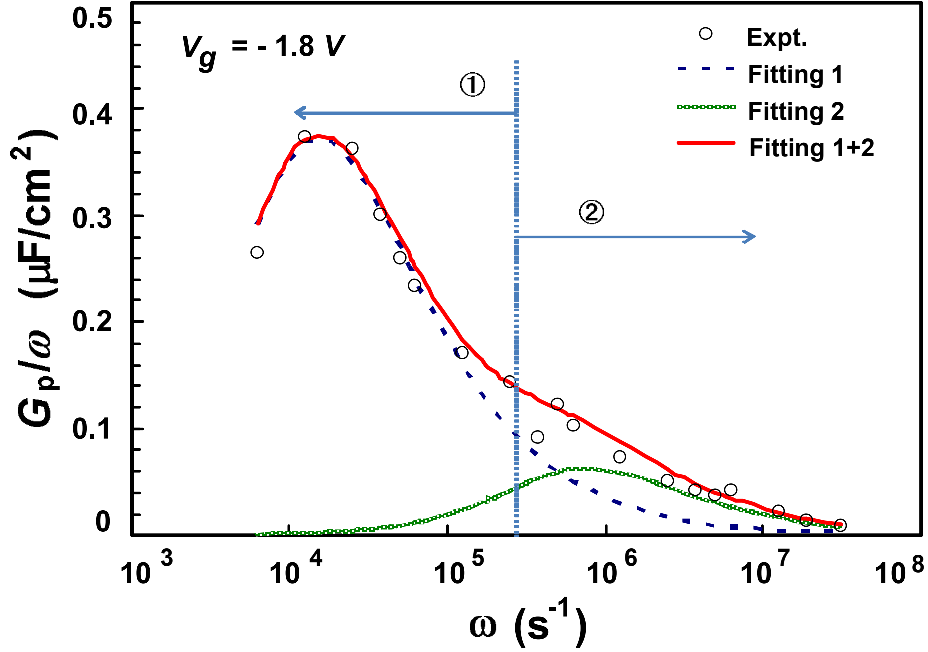

FIG. 5.7. G_p/ω as a function of ω for in-situ MOCVD grown AlN/AlGaN/GaN MIS-diode at V_g =-1.8 V.

Conventional curve fitting method [17] could not explain the experimental G_p/ω dispersions of AlN based MIS-diodes. Alternatively, the experimental G_p/ω values were resolved into two fitting curves for all gate voltages near V_{th} using a curve fitting model. In the low frequency region (≤ 50 kHz) indicated as region ① in figs. 5.5 to 5.7, the experimental G_p/ω values can be fitted into a single G_p/ω curve. On the other hand, in the high frequency region indicated as region ②, two G_p/ω curves were necessary to fit the experimental G_p/ω values. Similar fitting results were observed even at higher bias voltages (as shown in fig. 5.6 and 5.7), while the peak position in region ① moved largely toward low frequency with an increasing τ_T value. This shows the gate voltage dependency on τ_T for the AlN insulated MIS-diode. The fitting model clearly indicates

the existence of two types of trap states and their correlation, as evident from the cross over point between regions ① and ② respectively. The G_p/ω dispersions at the cross over point can be due to the smooth AlN/AlGaN interface caused by in-situ deposition of the insulator. This behavior is quiet unique from the previous reports on conductance analyses of ex-situ grown Al_2O_3 as gate insulator for AlGaN/GaN MISHs [4,18], which showed conventional Gp/ω curve in the high frequency region for gate voltages near the vicinity of V_{th}.

The interpretation is that the main G_p/ω peak exhibited in the lower frequency region could be due to trap states existing in insulating AlN layer which includes the traps at the AlN/AlGaN interface. The smaller G_p/ω peak observed relatively in the high frequency region corresponds to the bulk traps caused by the AlGaN barrier layer and AlGaN/GaN interface (hereinafter referred to as the AlGaN barrier layer). Further, the fitting curve (1+2) of the proposed model represents the combined contribution of trap states due to the insulating AlN and AlGaN barrier layers, which agrees well with the experimental G_p/ω values. To validate this, conductance measurements were performed on reference AlGaN/GaN Schottky barrier diodes (SBD) with similar epilayers except, without the AlN insulating layer. The open triangles in fig. 5.5, represent the G_p/ω values against ω for AlGaN/GaN heterostructures. The AlGaN/GaN SBD showed a single Gp/ω peak in same frequency region, as that of smaller G_p/ω peak exhibited in AlN/AlGaN/GaN MIS-diode (referred as fitting curve 2 in figs. 5.5 to 5.7).

Furthermore, to extend the arguments based on this model, conductance analyses was performed on another in-situ MOCVD grown AlN/AlGaN/GaN MISHs with 5 nm AlN insulating layer. Interestingly, the experimental G_p/ω values were also resolved into

two fitting curves, exactly in the same frequency ranges as obtained for AlN/AlGaN/GaN MISHs with 2 nm AlN as insulating layer. Two G_p/ω peaks in the AlN based MISHs could be the result of smooth interface between the in-situ grown AlN layer and the AlGaN barrier layer as observed from our experimental results and fitting model. In contrast, the conductance analyses of any of the AlGaN/GaN MISHs with ex-situ grown insulators could not be explicitly resolved into two trap states caused due to the insulator and barrier layers respectively.

The trap parameters were also extracted for these AlN based MIS-diodes. The τ_T due to insulating AlN layer in MISHs was between (27-300) μs. On the other hand, the τ_T due to AlGaN barrier layer in the MISHs was in the range of (1~3) μs. The trap state energy level as a function of τ_T were extracted using the equation

$$E_T = kT\ln\,(\sigma_T N_c \upsilon_T)\ \tau_T \tag{5.3}$$

where k is the Boltzman constant, T is the measurement temperature, σ_T is the capture cross section of the traps, N_c is the density of states in the conduction band and υ_T is the average thermal velocity of the carriers. The values of the constants were considered according to Ref. 19.

The plot of trap state density as a function of its energy level is shown in fig. 5.8. A D_T of (4 x 10^{12} ~ 20 x 10^{12}) cm^{-2} eV^{-1} due to the AlN insulating layer was located deeply at E_T (0.4 ~ 0.52 eV). The AlGaN barrier layer exhibited D_T of (1 x 10^{11} ~ 10 x 10^{12}) cm^{-2} eV^{-1} distributed at shallow energy levels E_T (0.32 ~ 0.34 eV). Recently, excess traps at energy levels of 0.22 and 0.38 eV below the conduction band were reported for HfAlO and AlO based AlGaN/GaN MISHs respectively [20, 21].

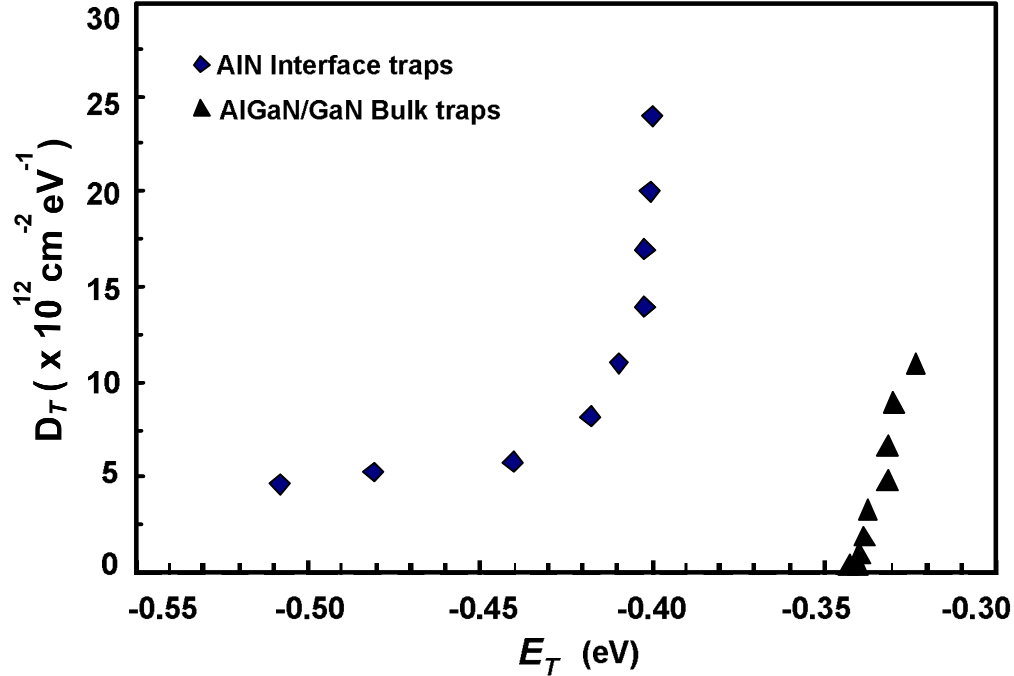

FIG. 5.8. Trap state density as a function of trap state energy of in-situ MOCVD grown AlN/AlGaN/GaN MIS-diode due to AlN insulating and AlGaN barrier layers.

In this study, using thin AlN layer as the gate insulator, these traps is as deep as 0.52 eV. In general, the trap state density and its energy levels can vary with the insulator and the alloy composition of the AlGaN barrier layer due to change in band gap and band-edge energies in the MISHs. Thus, in the case of *in-situ* grown AlN/AlGaN/GaN MISHs, relatively deep traps with higher τ_T due to the AlN insulating layer was observed. On this basis, it might be expected that the E_T and therefore τ_T would increase with increasing Al concentration in the AlGaN barrier, leading to the observation of conductance dispersion at lower frequencies [17]. The $D_{T\text{-}min}$ due to AlN and AlGaN barrier layer was 4 x 10^{12} and 1 x 10^{11} $cm^{-2}eV^{-1}$ located at energy levels of 0.52 and 0.34 eV respectively. However, midgap interface state density cannot be located directly because the trap states located beyond E_c-0.7 eV cannot sufficiently respond during *C-V* and conductance voltage (*G-V*) measurement time, limiting the D_T characterization near

the conduction band edge [8]. Therefore, measurements at higher temperatures and UV assisted (G-V) are necessary to obtain the information of deeper trap states.

5.5. Effect of AlN growth temperature on trap densities of *in-situ* MOCVD grown AlN/AlGaN/GaN MIS-HEMTs on silicon substrate

In order to effectively use AlN layer as an insulating layer for AlGaN/GaN MIS-HEMT hetero-structure, optimization of the growth of AlN is essential. Recently, *in-situ* MOCVD grown AlN/AlGaN/GaN MIS-HFET with the AlN layer growth temperature (T_G) of 600 °C has been demonstrated with better device properties than the conventional HFET [21]. However, detailed studies on trapping and device properties of *in-situ* MOCVD grown AlN/AlGaN/GaN MIS-HFETs as a variation of AlN layer T_G are necessary to understand the potential utilization of AlN layer in GaN based MIS-devices. Therefore, two different growth temperatures 600 and 700 °C were chosen to study the trapping as well as device characteristics of AlN/AlGaN/GaN MIS-HEMTs. By using frequency dependent parallel conductance/angular frequency (G_p/ω) technique reported by us [9], it is feasible to locate the trap states in AlN/AlGaN/GaN MISHs. Further, this technique can also be extended to study traps in AlGaN/GaN based heterostructures with different barrier thickness and alloy compositions. Frequency dependent conductance technique is the most reliable method for investigation of trapping effects, which can effectively locate the traps in $Al_xGa_{1-x}N$/GaN heterostructures [14, 17]. For better understanding the AlN/AlGaN/GaN based MISHs with AlN layer at grown at 600 ^{o}C and 700 ^{o}C are referred as MIS-(diodes/HFETs) A and B respectively.

5.5.1. Trapping characteristics

The capacitance (C-V) and conductance (G-V) measurements were performed by sweeping the gate voltage (V_g) from accumulation to depletion regime, between frequency ranges of 1 kHz to 5 MHz. The amplitude of ac signal was fixed as 30 mV and the measurement period was long, so that small signal conditions were maintained.

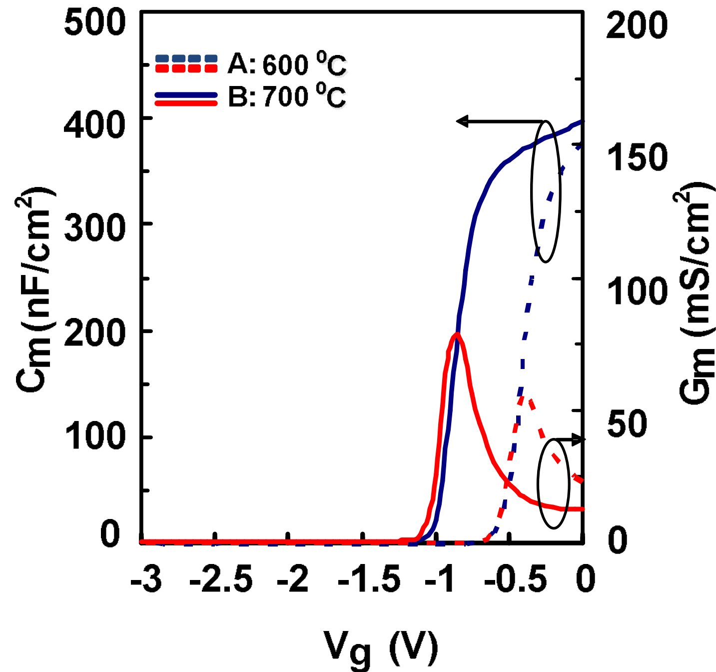

FIG. 5.9. Typical C-V and G-V characteristics measured at 100 kHz for *in-situ* MOCVD grown AlN/AlGaN/GaN MIS-diodes with AlN layer T_G of 600 and 700 °C.

Typical C-V and G-V characteristics measured at 100 kHz for MIS diodes A and B are shown in fig. 5.9. The C-V curves show a sharp transition from depletion to accumulation regime for both MIS diodes. The V_{th} observed for MIS-diodes A and B was -0.65 and -0.95 V respectively. The zero-bias capacitance for MIS-diodes A and B were 394 and 377 nF/cm^2. Nevertheless, a threshold voltage shift of (ΔV_{th} = -0.3 V) and zero bias capacitance as well as conductance differences between the two MIS-diodes indicate

priori information about variations in AlGaN (bulk related) and AlN traps. The frequency dependent capacitance dispersion in *pinch-on* region is due to the surface status while the *pinch-off* capacitance dispersions are due to bulk traps [23]. To evaluate the trap states quantitatively, the (G_p/ω) values near the depletion region were calculated according to the equations 5.1 and 5.2 respectively.

Two curves could be fit to the asymmetric experimental G_p/ω values at V_{th}, for MIS-diodes A and B. For comparison, the fitting results of MIS-diodes are shown in figs. 5.10 (a) and (b) respectively. The fitting curves 1 and 2 correspond to the $D_{T\text{-}AlN}$ and the $D_{T\text{-}AlGaN}$ respectively. Both $D_{T\text{-}AlN}$ and $D_{T\text{-}AlGaN}$ can be quantified from the G_p/ω peak magnitude, while the τ_T can be located from the peak position of G_p/ω. By comparing the fitting results of MIS-diodes, we observed both $D_{T\text{-}AlN}$ and $D_{T\text{-}AlGaN}$ of MIS-diode A is one order lower in magnitude than B.

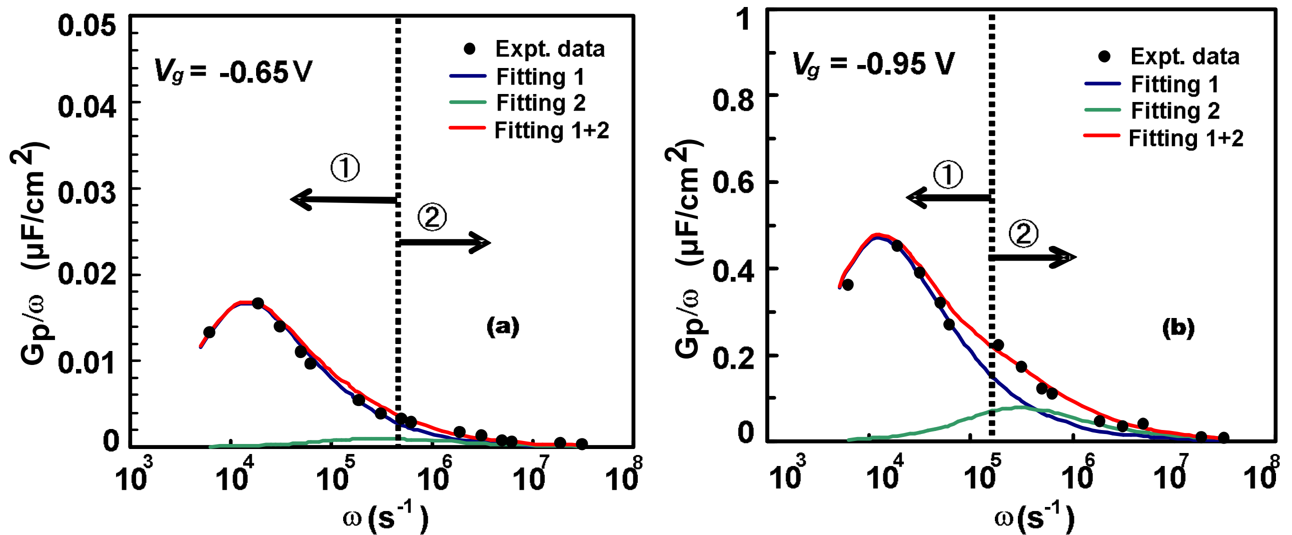

FIG. 5.10. G_p/ω as a function of ω for AlN/AlGaN MIS-HFETs with AlN layer (a) T_G ~ 600 °C and (b) T_G ~700 °C. The dashed line indicates cross over region between AlN and AlGaN traps.

In the fitting process for $V_g \leq V_{th}$, similar trend was observed for both the MIS-diodes. Moreover, the fitting curve (1+2) at the cross over region (denoted by a dashed line in fig 5.10 (a) and (b) was relatively broader than the experimental G_p/ω values in the case of MIS-diode B compared to A. This phenomenon was also observed for AlN/AlGaN/GaN MISHs grown relatively at high temperature $T_G \geq 1000$ °C [9]. This is due to the asymmetric behavior of experimental G_p/ω values caused by a high $D_{T\text{-}AlGaN}$ for MIS-diodes with AlN layers grown at high temperatures. Nevertheless, these *in-situ* AlN/AlGaN/GaN MISHs exhibited two trap states with distinct time constants irrespective of their AlN layer T_G. Therefore, the present G_p/ω studies suggests a good AlN/AlGaN heterointerface due to low temperature *in-situ* grown AlN layer. As evident, this kind of traps response had also been observed in the case of SiO_2/Si MIS-devices using parallel conductance experiments [24, 25].

The AlN trap time constant ($\tau_{T\text{-}AlN}$) and AlGaN trap time constant ($\tau_{T\text{-}AlGaN}$) evaluated are plotted against the V_g for MIS-diodes as shown in figs. 5.11 (a) and (b). In the case of MIS-diode A, both $\tau_{T\text{-}AlN}$ and $\tau_{T\text{-}AlGaN}$ showed better dependencies on V_g than MIS-diode B. An exponential dependency of τ_T on V_g manifests uniformities in the trap states of MIS-diode A than B. A broader conductance curve and a deviation from exponential dependence ($\tau_T \propto V_g$) can be observed if surface potential fluctuation due to some non-uniformity in the oxide (Insulator) and/or interface traps exits [18]. The $\tau_{T\text{-}AlN}$ values for MIS-diodes A and B was in the range of (14 μs – 0.3 ms) and (0.1 – 0.2 ms). On the other hand, $\tau_{T\text{-}AlGaN}$ for MIS-diodes A and B were between (2 – 6 μs) and (5 – 8 μs) respectively. These $\tau_{T\text{-}AlN}$ and $\tau_{T\text{-}AlGaN}$ are consistent with the τ_T ranges generally reported for AlN related traps [26], and AlGaN related bulk traps [20].

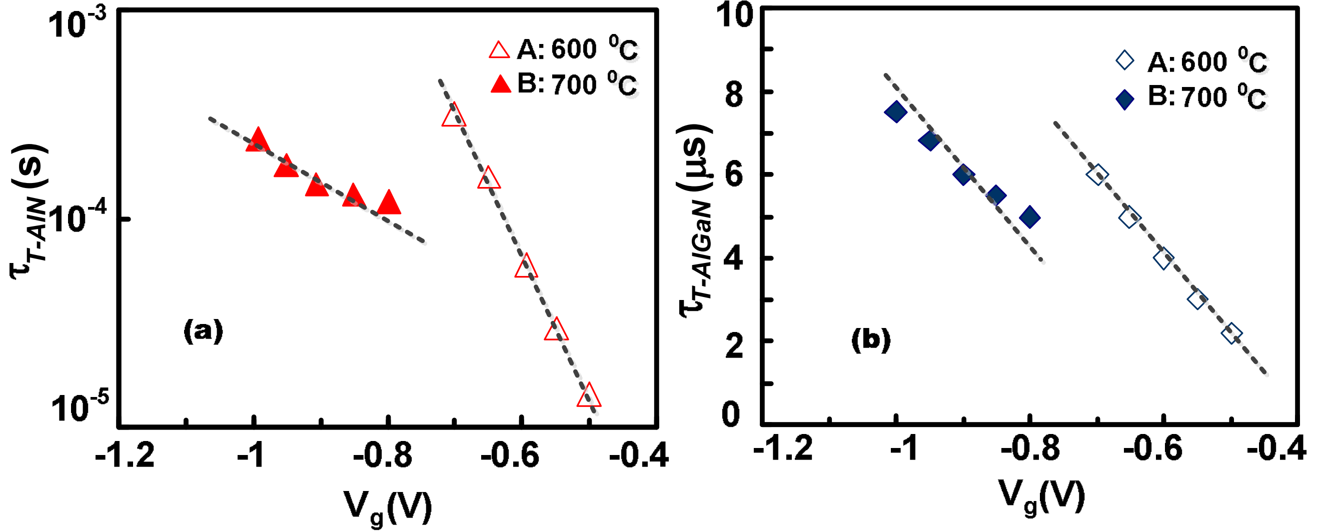

FIG. 5.11. Trap time constants of (a) AlN traps and (b) AlGaN bulk traps in *in-situ* MOCVD grown AlN/AlGaN/GaN MIS-HFETs with AlN layer grown at 600 and 700 °C.

The trap state energy level (E_T) is proportional to the τ_T, and therefore it can be deduced using the equation 5.3. Furthermore, the $D_{T\text{-}AlN}$ and $D_{T\text{-}AlGaN}$ as a function of corresponding E_T for MIS-diodes A and B are shown in figs. 5.12 (a) and (b). The minimum $D_{T\text{-}AlN}$ and $D_{T\text{-}AlGaN}$ values measured for MIS-diode A were 1.1 x 10^{11} and 1.2 x 10^{10} $cm^{-2}eV^{-1}$. Their corresponding energy levels were -0.47 and -0.36 eV below the conduction band. In contrast, the minimum $D_{T\text{-}AlN}$ and $D_{T\text{-}AlGaN}$ values observed for B at similar energy levels were 3.4 x 10^{12} and 5 x 10^{11} $cm^{-2}eV^{-1}$ respectively. By comparing the $D_{T\text{-}AlN}$ and $D_{T\text{-}AlGaN}$ at their respective E_T, it was observed unambiguously that $D_{T\text{-}AlN}$ and $D_{T\text{-}AlGaN}$ of MIS-diode A was one order of magnitude lower than B. This signifies that low T_G can favour a better AlN layer over AlGaN with reduced trap densities.

R. Stoklas et al., [20] have reported two trap densities in the range of (2.5-4) x 10^{11} and (0.3-1.2) x 10^{12} $cm^{-2}eV^{-1}$ for Al_2O_3/AlGaN/GaN/Si non-annealed MOSFETs. We have also recently reported trap densities of 4.5 x 10^{12} and 1 x 10^{11} $cm^{-2}eV^{-1}$ due to

AlN and AlGaN traps in *in-situ* AlN/AlGaN/GaN/Si MISHs grown at 1030 °C (Ref. 9). However, the $D_{T\text{-}AlN}$ and $D_{T\text{-}AlGaN}$ values for AlN/AlGaN/GaN MISHs (T_G ~ 600 °C) in this study are lower than the previous reports. The reason is due to good AlN/AlGaN/GaN MISH with AlN layer grown at low temperature, although the AlN mole fraction (x = 10%) was low in the AlGaN layer. The *in-situ* MOCVD grown AlN layer (T_G~600 °C) can effectively passivate and protect the AlGaN surface. Meanwhile, low growth temperature of AlN is also preferred for preventing tensile strain-induced cracking of AlN layer, low gate leakage and better device performance [5, 7, and 22].

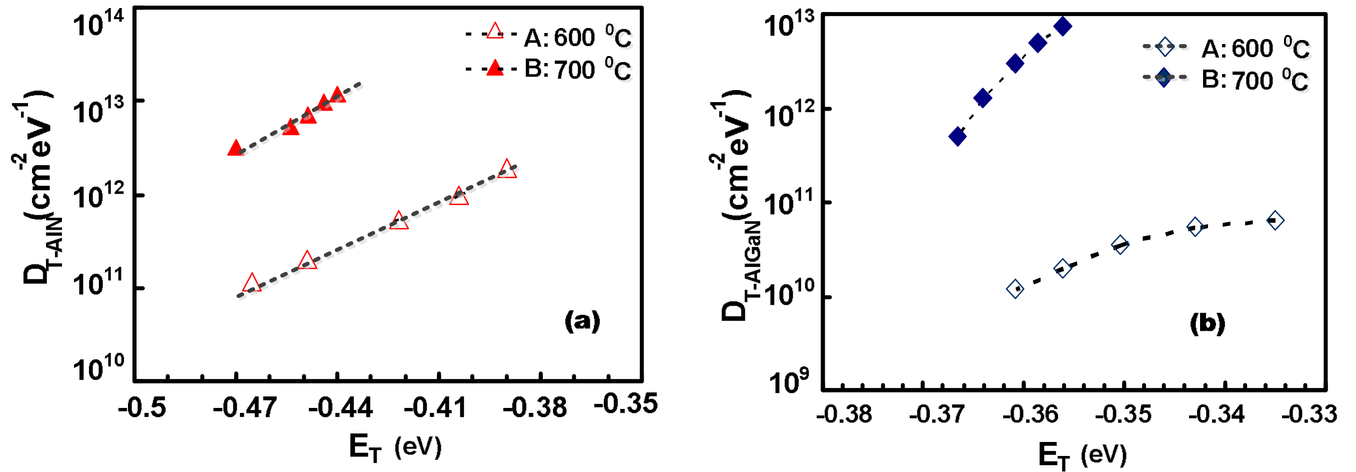

FIG. 5.12. The density of (a) AlN traps and (b) AlGaN bulk traps as a function of their energy levels below the conduction band of *in-situ* MOCVD grown AlN/AlGaN/GaN MIS-HFETs with AlN layer grown at 600 and 700 °C.

5.5.2. Device characteristics: Current collapse

To investigate the influence of these traps on device characteristics, MIS-HFETs were also fabricated simultaneously and subjected to output I_{ds}–V_{ds} characteristics in DC and pulsed conditions. The difference in I_{ds}–V_{ds} characteristics in DC and pulsed mode is referred as gate-lag and are commonly related to surface traps [27, 28]. In this method,

we applied a trap filling short pulses of 500 μs to the AlN insulated gate with duration of 50 ms. Under pulsing condition, the gate was quiescent biased at -5 V ($V_{gs-q} < V_{th}$) and the drain current was measured. Figures 5.13 (a) and (b) shows the current collapse observed on MIS-HFETs A and B respectively. The DC I_{ds-max} of MIS-HFET A was perhaps slightly lower than B, due to increase in Ohmic contact resistance. This can be overcome by recess etching and making Ohmic contacts in the AlGaN layer [29]. However, under gate stress conditions the MIS-HFET A showed less degradation of I_{ds-max} than MIS-HFET B.

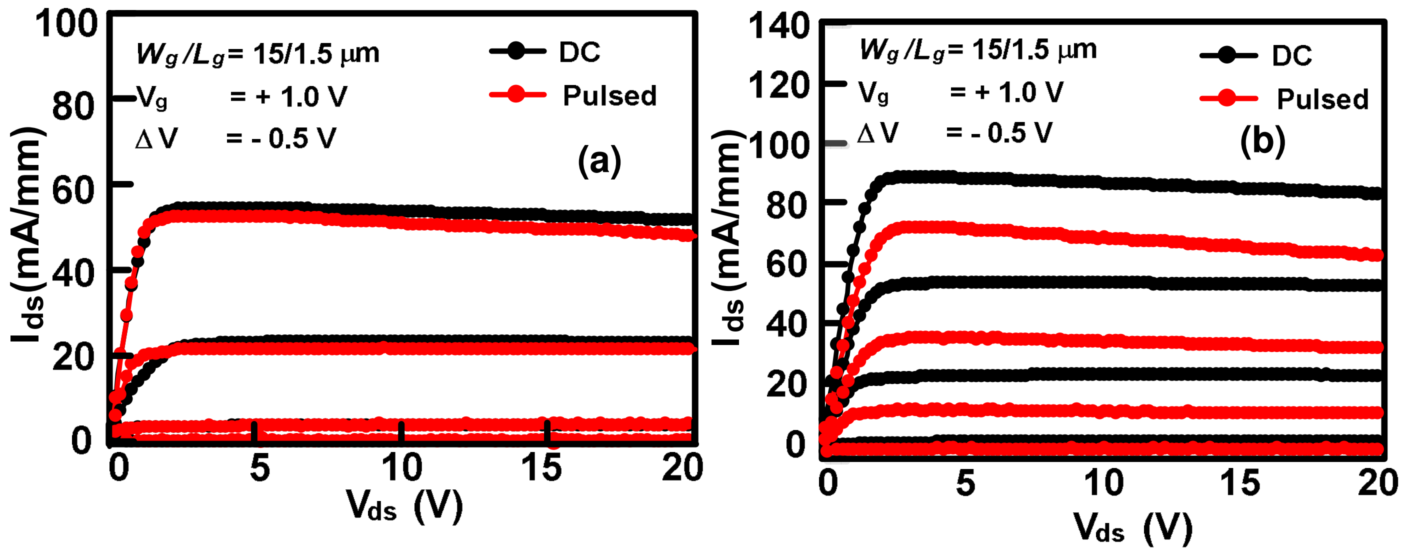

FIG. 5.13. DC and pulsed output I_{ds}-V_{ds} characteristics of AlN/AlGaN MIS-HFETs with AlN layer grown at (a) T_G ~600 °C and (b) T_G ~700 °C. For pulsed measurements a gate pulse of 500 µs was applied with a quiescent gate bias V_{gs-q} of -5 V.

Figure 5.14 shows the I_{ds-max} degradation (in %) as observed from gate-lag measurements for MIS-HFETs A and B respectively. The MIS-HFET B showed a large decline of I_{ds-max} (~26 %) with an increased on state resistance (R_{on}) of 33 % under gate stress conditions. On the other hand, the MIS-HFET A showed less degradation of I_{ds-max}

(≤ 5 %) and R_{on} of 0.75 % under gate stress conditions. This can be attributed to the combination of effective passivation of AlGaN surface states and/or the low $D_{T\text{-}AlN}$ due to the AlN layer grown at low temperature [22, 23 and 28].

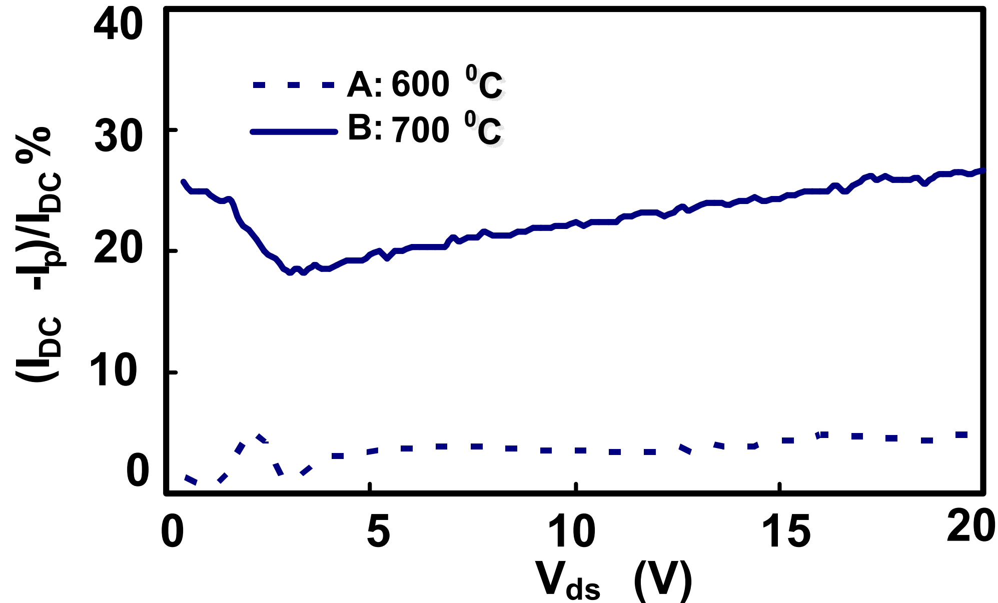

FIG. 5.14. Degradation of $I_{ds\text{-}max}$ (in %) estimated from the measured DC and pulsed output I_{ds}-V_{ds} characteristics of AlN/AlGaN MIS-HFETs with AlN layer T_G of 600 and 700 °C.

5.5.3. Three terminal leakage and breakdown measurements

In addition, the three terminal (*off-state*) *BV* measurements on these devices revealed a high *BV* ~302 V for MIS-HFET A, in contrast to a low *BV* ~ 274 V for MIS-HFET B as shown figs.5.15 (a)and (b). This can be explained on the basis that high trap state density in MIS-HFET B was accompanied by high electric field and a low *BV*. The breakdown voltage decreases with increase in defect states [30]. These results shows that low temperature (T_G ~ 600 °C) *in-situ* MOCVD grown AlN layer offers better device

characteristics under gate-stress conditions and high BV due to less defect states as observed from the conductance measurements.

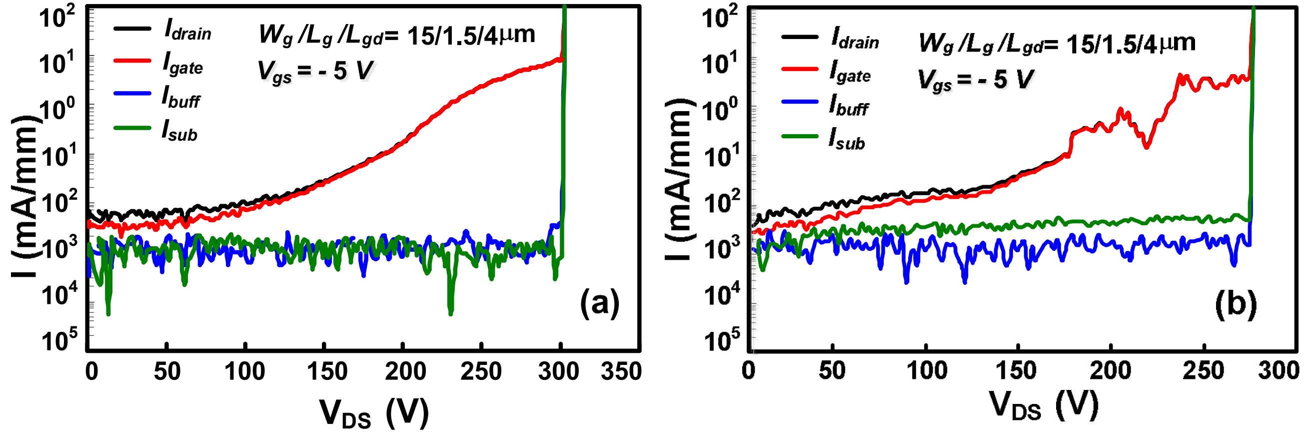

FIG. 5.15. Three terminal (*off-state*) breakdown voltage measurements of AlN/AlGaN MIS-HFETs with AlN layer (a) T_G ~600 °C and (a) T_G ~700 °C respectively. The gate terminal was biased at (V_g =-5 V) well below the *pinch-off* voltage.

5.6. Summary

In summary, the experimental and the fitting results from extensive conductance studies on *in-situ* MOCVD grown AlN/AlGaN/GaN MISHs significantly shows the existence of two types of trap states and their correlation. Frequency dependent conductance analyses were performed on three different AlN based MIS-heterostructures with AlN growth temperatures. We observed the conductance dispersions in the cross over region can be caused by the AlN/AlGaN interface due to *in-situ* deposition of AlN insulating layer compared to the other existing *ex-situ* grown insulators. A $D_{T\text{-}mins}$ of 4.5 x10^{12} and 1 x 10^{11} cm^{-2} eV^{-1} at energy positions E_T (0.52 and 0.33 eV) below the conduction band were observed corresponding to the trap states of AlN insulating and AlGaN barrier layers respectively for AlN MISHs grown at 1030 °C.

Further, the trapping properties of *in-situ* MOCVD grown AlN/AlGaN/GaN MIS-HFETs with AlN layers grown at 600 and 700 °C has been quantitatively analyzed by frequency dependent conductance technique in order to identify the suitable growth condition for AlN layer. The AlN and AlGaN related traps were identified for both the devices and were one order of magnitude lower for MIS-FET with AlN layer grown at 600 °C. They exhibited a lower $D_{T\text{-}AlN}$ and $D_{T\text{-}AlGaN}$ values of 1.1 x 10^{11} and 1.2 x 10^{10} $cm^{-2}eV^{-1}$ with characteristic energy levels at -0.47 and -0.36 eV below the conduction band. Moreover, the gate-lag results revealed less (≤ 5 %) degradation of $I_{ds\text{-}max}$ compared to the MIS-FET grown at 700 °C which exhibited (~26 %) degradation of $I_{ds\text{-}max}$ due high $D_{T\text{-}AlN}$ and $D_{T\text{-}AlGaN}$ of 3.4 x 10^{12} and 5 x 10^{11} $cm^{-2}eV^{-1}$ located around similar energy levels. A high *BV* of 302 V was also observed for MIS-HFET with AlN layer grown at 600 °C. These studies indicate that (i) frequency dependent conductance analyses is a beneficial technique for the trap state characterization of AlN/AlGaN/GaN based MISHs. (ii) In addition to that it was found that low temperature growth of AlN layer can favour lesser defect prone AlN based AlGaN/GaN MIS-HFETs.

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Chapter 6

Conclusions and future work

6.1. Conclusions

The results discussed in this dissertation were mainly focused on the importance of realizing high quality AlGaN/GaN based devices MIS-type on less expensive and large diameter silicon substrate. The results of the works lead to the location and reduction of hetero-interface and surface traps existing in the AlGaN/GaN based MIS-type devices on Si which were comprehensively and conclusively discussed with in each chapter. The conclusions drawn are mainly on the basis of extensive investigations performed within the scope of the work that lead to this dissertation. The summary of the results according to individual chapters are as follows,

In **chapter 1**, a realistic review of the existing *state-of-the-art GaN* technology was presented. The extensive advantages of the GaN based devices based on their wide band gap, high saturation velocity, polarization effects and high breakdown field has been discussed. The key role of this GaN technology in near future high power and high frequency devices was briefed along with some of their prevailing limitations. A detailed background for the motivation of the work leading to this dissertation was also stated.

In **chapter 2**, reports mainly on the current challenges and critical issues that exist in the epitaxial growth technology of AlGaN/GaN HEMTs on Si and improvements needed for the high quality growth of AlGaN/GaN heterostructures on Si. The concept of a thicker super lattice structure (SLS) to overcome those challenges in order to attain high quality heteroepitaxial AlGaN/GaN layers were also briefly discussed.

In **chapter 3**, the MOCVD growth of AlGaN/GaN heterostructures on Si using thick buffer layers or the super lattice structures (SLS) and consequent improvements in crystal quality and current transport properties were presented. A detailed XRC characterization of the AlGaN/GaN HEMT heterostructures grown using thicker SLS showed lower dislocation densities. The carrier mobilities measured using the Hall set up confirmed higher mobilities for the AlGaN/GaN HEMT heterostructures grown using thicker SLS. The reason for the increase in carrier mobilities is attributed to the reduction of dislocation related carrier scattering.

The concept and theory of AlGaN/GaN HEMT was introduced in this section. The device characterizations and trapping effects of AlGaN/GaN HEMTs fabricated on the heterostructures grown using super lattice structure (SLS) are also discussed in detail. The trapping characteristics showed a remarkable decrease in fast traps related to the AlGaN/GaN heterostructure confirming improvements in the crystal quality using thicker SLS.

In **Chapter 4** discussions were mainly about the work related to minimizing the surface traps using a potential oxide layer. The concept of metal-insulator/oxide-semiconductor (MIS/MOS) HEMTs was presented with the principles of device characteristics. A detailed description about preparation of process compatible Al_2O_3 by oxidative annealing technique was also elaborated. The device characteristics of thermally oxidized Al_2O_3 based AlGaN/GaN MOS-HEMT was compared with the normal HEMT characteristics. Furthermore, the trapping characteristics by frequency dependent conductance analyses on the MOS-HEMT showed fast traps corresponding to the AlGaN/GaN heterostructure. The distinct surface related slow traps were not

observed in the case of MOS-HEMT revealing the passivation effects due to the Al_2O_3 as well as due to surface annealing conditions.

Chapter 5 described about the potential importance of using a thin *in-situ* MOCVD grown AlN as a passivating layer for AlGaN/GaN MIS-HEMTs on Si substrates. The influence of AlN layer's growth temperature on surface traps and their role in device characteristics were also briefly discussed. The AlN/AlGaN/GaN MIS-heterostructures were analyzed by frequency dependent conductance method. The results revealed that low growth temperature of AlN layer favor less defect AlN/AlGaN/GaN MIS-HEMT structures. The device characteristics also support the results of the conductance analyses.

From this study, its was concluded that AlGaN/GaN hetero-interface states and (i) hetero-interface traps do exist near the AlGaN/GaN heterostructure interface and it was minimized my growing thicker buffer layers for AlGaN/GaN on Si, (ii) Further, a high~κ Al_2O_3 layer effectively passivates the surface traps existing in the AlGaN layer, and (iii) for using AlN as insulator for AlGaN/GaN MIS-type devices low temperature growth of AlN layer results in lower trap density due to AlN layer.

6.2. Future Work

It is well established that current collapse is a serious trap related phenomena that adversely affects the effective functioning of any GaN based high-power and high-frequency devices. The location and magnitude of these traps can be evaluated using existing techniques. Therefore the development of high quality *state-of-the-art* AlGaN/GaN devices on large size Si wafers (8 ~16 ") relies on the fact to minimize the

traps. This can be achieved by AlGaN/GaN MOS-HEMTs that can meet the requirements of near-future high-power, high-frequency and high-speed switching devices.

Therefore the vision and mission of future work is the to use AlGaN/GaN/Si HEMT heterostructure grown using thick buffer layers and to fabricate high quality high~κ material based AlGaN/GaN MOS-HEMT with negligible traps and associated current collapse for high-power and high-frequency potential applications.

I believe that the results discussed in this dissertation are essential and will obviously contribute to the development of futuristic high quality AlGaN/GaN MOS-devices on Si.

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AUTHOR'S ACCOMPLISHMENTS

A. Peer reviewed publications in international journals

1. "Suppression of gate leakage and enhancement of breakdown voltage using thermally oxidized Al layer as gate dielectric for metal-oxide-semiconductor high-electron-mobility transistors"

   Joseph J. Freedsman, Toshiharu Kubo, S. Lawrence Selvaraj Takashi Egawa,

   Japanese Journal of *Applied Physics*, **50** (2011) pp.04DF03-1-04DF03-3**.**

2. "Trap characterization of In-situ MOCVD grown AlN/AlGaN heterostructures by frequency dependent conductance technique",

   Joseph J. Freedsman, Toshiharu Kubo, Takashi Egawa,

   Applied Physics Letters, **99** (2011) pp.033504-1-033504-3.

3. "Effect of AlN growth temperature on trap densities of *in-situ* metal-organic chemical vapor deposition grown AlN/AlGaN/GaN metal-insulator-semiconductor heterostructure field-effect transistors",

   Joseph J. Freedsman, Toshiharu Kubo, Takashi Egawa,

   Aip Advances **2**, pp. 022134-1-013506-9.

4. "Analyses of hetero-interface trapping properties in AlGaN/GaN high electron mobility transistor heterostructure grown on silicon with thick buffer layers",

   Joseph J. Freedsman, Toshiharu Kubo, Takashi Egawa,

   Applied Physics Letters, **101** (2012) pp. 013506-1-013506-4.

B. International conferences:

1. "Comparative study of AlGaN/GaN HEMT and MIS-HEMT with Al_2O_3 as gate dielectrics",

   Joseph J. Freedsman, Toshiharu Kubo, S. Lawrence Selvaraj and Takashi Egawa,

   Asia Pacific Workshop on Advanced Semiconductors, (***AWAD*)**, 2nd July 2010, Tokyo Institute of Technology, Japan.

2. "Suppression of gate leakage and enhancement of breakdown voltage using Al_2O_3 nano particles as gate dielectrics for MIS-HEMTs",

   Joseph J. Freedsman, Toshiharu Kubo, S. Lawrence Selvaraj and Takashi Egawa,

   International Conference on Solid State Devices and Materials (***SSDM***), 22nd September 2010, University of Tokyo, Japan.

3. "Characterization of trapping effects in MOCVD grown AlN/AlGaN MIS-HEMT Structures grown on Si",

   Joseph J. Freedsman, Toshiharu Kubo, and Takashi Egawa,

   3rd *International Symposium on Plasma and Nitride Semiconductors* (***IS Plasma*)**, 3rd March 2011, Nagoya Institute of Technology, Nagoya, Japan.

4. "Investigation of trap state density in AlN/AlGaN/Si Metal-Insulator-Semiconductor High-Electron-Mobility Transistors",

   Joseph J. Freedsman, Toshiharu Kubo, and Takashi Egawa,

   9th International Conference on Nitride Semiconductors (***ICNS 2011***), 12th July, 2011, Scottish Exhibition and Conference Centre, Glasgow, U.K.

5. "Investigation of trap states in *in-situ* MOCVD grown AlN/AlGaN/GaN MIS-HEMTs grown on Sapphire substrates",

   Joseph J. Freedsman, Toshiharu Kubo, and Takashi Egawa,

   4th ***IS Plasma*****,** 7th March 2012, Chubu University, Japan

6. "Investigation of trapping properties in AlGaN/GaN HEMT heterostructures grown on silicon with thick buffer layers",

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   SSDM, 26th September 2012, Kyoto International Conference Center, Kyoto, Japan.

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