

# Low etch pit density GaAs on Si grown by metalorganic chemical vapor deposition

Tetsuo Soga, Takashi Jimbo, and Masayoshi Umeno

Department of Electrical and Computer Engineering, Nagoya Institute of Technology, Gokiso-cho, Showa-ku, Nagoya 466, Japan

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GaAs was grown on a Si substrate by metalorganic chemical vapor deposition using GaAs/GaAsP strained-layer superlattice (SLS) intermediate layers. The dislocation density decreases at the interface between GaAs and the SLS, but does not decrease in the SLS. When a GaAs/GaAsP SLS is used as the intermediate layer, part of the threading dislocation propagates into the top GaAs layer because of the lattice mismatch of GaAs and SLS. The low etch pit density of  $(3-5) \times 10^5 \text{ cm}^{-2}$  was obtained by using the intermediate layer of a GaAs/GaAsP SLS and an AlAs/GaAs superlattice with thermal cycle annealing.

The heteroepitaxy of GaAs on Si is an important technology which enables the combination of GaAs optical and Si electronic devices. However, high dislocation density caused by the lattice mismatch (about 4%) is a large problem to be solved. Much effort has been made and a dislocation density of the order of  $10^6 \text{ cm}^{-2}$  has been obtained using the strained-layer superlattice (SLS) intermediate layer and thermal cycle annealing.<sup>1,2</sup> However, a dislocation density less than  $10^6 \text{ cm}^{-2}$  has not been obtained yet. This is due to the lack of information on how the threading dislocations generate at the GaAs/Si interface and the dislocation density reduces by the strained-layer superlattice or by thermal cycle annealing. If the reduction mechanism of the dislocation becomes clear, it is then possible to design the effective intermediate layer to reduce the dislocation density. In this letter, GaAs is grown on Si with several kinds of SLS intermediate layers and an intermediate layer structure to obtain a low etch pit density GaAs on Si is presented.

GaAs was grown on a Si substrate by conventional metalorganic chemical vapor deposition (MOCVD). The growth apparatus is almost the same as that reported previously.<sup>3</sup> The source materials are trimethylgallium (TMG), trimethylaluminum (TMA), AsH<sub>3</sub>, and PH<sub>3</sub>. The orientation of the Si substrate is (100) 2° off toward [011]. GaAs was grown on Si by the conventional two-step growth method.<sup>4</sup> 12.5-nm-thick GaAs was deposited on the high-temperature annealed Si substrate, followed by the growth of the GaAs layer at 750 °C. A GaAs/GaAsP SLS for various P compositions and layer thicknesses and an AlAs/GaAs superlattice (SL) were grown as the intermediate layers. The total GaAs thickness is 3 μm. The growth temperature of these intermediate layers is 750 °C. Thermal cycle annealing was performed by interrupting the growth. The sequence of the thermal cycle annealing is as follows. The temperature of the sample is lowered to 200 °C from the growth temperature, and then it is raised to 900 °C. The temperature is kept at this scale for 10 min. After this annealing process, the sample is cooled to 200 °C and the temperature of the sample is raised to 750 °C again. The samples are evaluated by etch pit density (EPD) using molten KOH and transmission electron microscopy (TEM).

First, the effects of the GaAs/GaAsP SLS on the overgrown GaAs layer were studied. A 0.5-μm-thick GaAs, three kinds of GaAs/GaAsP SLSs [structures (A), (B), and (C)] and a 2.5-μm-thick GaAs were grown on Si sequentially. The structures of (A), (B), (C) (the composition of P in the GaAsP layer, each layer thickness, the period of the SLS) and the corresponding EPD are summarized in Table I. As shown in this table, structure (A) is not effective in reducing the dislocation density since the EPD is almost the same as that without the intermediate layer:  $4.8 \times 10^7 \text{ cm}^{-2}$ . However, structures (B) and (C) effectively reduce the EPD. The layer thickness in structure (A) is thinner than the critical thickness of the multilayer,  $h_c$ , which is derived by Matthews and Blakeslee<sup>5</sup> and the layer thickness of samples (B) and (C) is thicker than the critical thickness. So, it is shown that the layer thickness in the SLS which is thicker than the critical thickness is effective in reducing the dislocation density when the dislocation density is on the order of  $10^7 \text{ cm}^{-2}$ .

Structure (C), which is the most effective in reducing dislocations in this study, was analyzed by cross-sectional TEM. The TEM micrograph is shown in Fig. 1. Many threading dislocations originate at the GaAs/Si interface. One interesting point is that most dislocations are bent at the interface between GaAs and SLS and that there is no dislocation reduction in the SLS. Even if an effective SLS is used, part of the threading dislocations propagates into the top GaAs layer because of the lattice mismatch between the top GaAs layer and the GaAs<sub>0.72</sub>P<sub>0.28</sub>.

TABLE I. Correlation between the SLS structure and the etch pit density.

Sample	SLS		( $\times 10^7 \text{ cm}^{-2}$ ) EPD
(A)	GaAs <sub>0.5</sub> P <sub>0.5</sub> /GaAs (20 nm) (20 nm)	$\times 5$	4.5
(B)	GaAs <sub>0.5</sub> P <sub>0.5</sub> /GaAs (50 nm) (50 nm)	$\times 5$	2.0
(C)	GaAs <sub>0.72</sub> P <sub>0.28</sub> /GaAs (100 nm) (100 nm)	$\times 3$	1.5
(D)	...		4.8

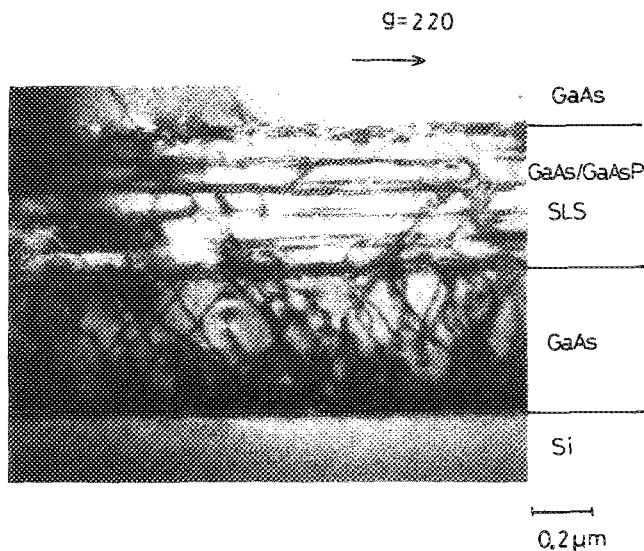


FIG. 1. Cross-sectional TEM micrograph of GaAs on Si with a three-period GaAs/GaAs<sub>0.72</sub>P<sub>0.28</sub> SLS. The etch layer thickness is 0.1 μm.

To reduce the dislocation density further, two or more superlattice intermediate layers should be grown separately on the top GaAs layer. The increase of the number of layers in the SLS is not effective because the dislocation density does not decrease in the SLS. The structure and the cross-sectional TEM micrograph of GaAs on Si with two stages of SLS are shown in Fig. 2. In this structure, after a 0.5-μm-thick GaAs (GaAs1) and a three-period GaAs<sub>0.72</sub>P<sub>0.28</sub>/GaAs SLS (SLS1) (each layer thickness is 0.1 μm) were grown, a 1-μm-thick GaAs layer (GaAs2), a

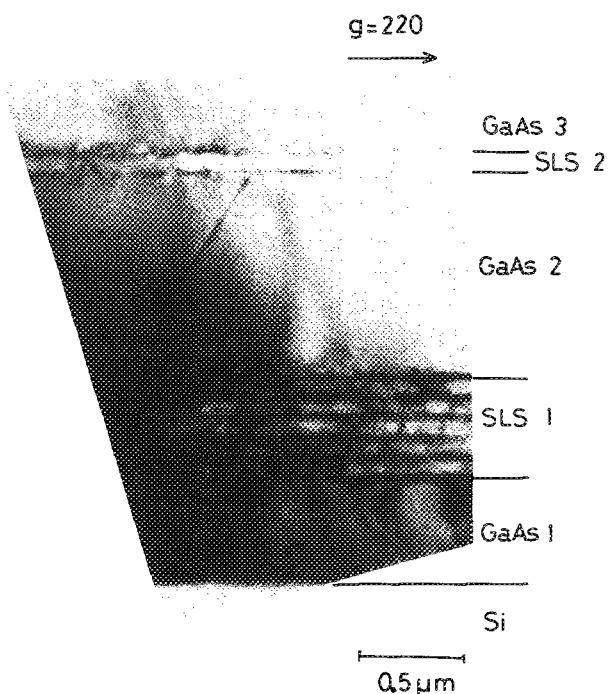
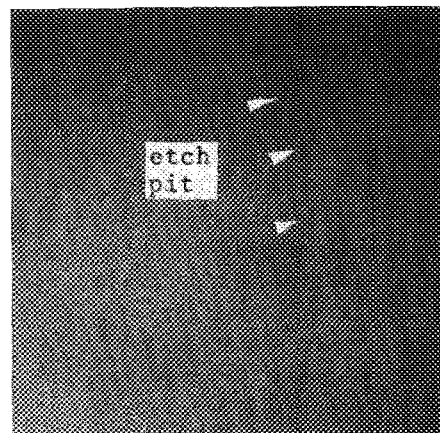
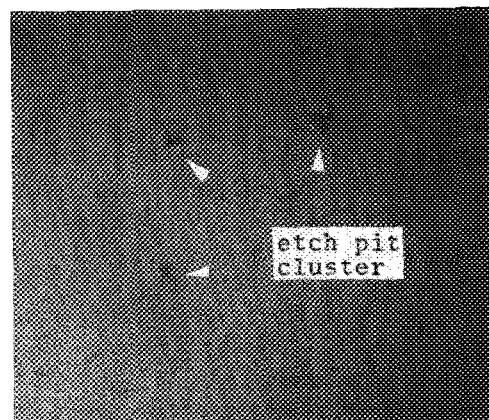


FIG. 2. Structure and cross-sectional TEM micrograph of GaAs on Si with SLS1 and SLS2. SLS1 is the same as in Fig. 1. The each layer thickness and the period of SLS2 are 10 nm and 5, respectively.

five-period GaAs<sub>0.8</sub>P<sub>0.2</sub>/GaAs SLS (SLS2) (each layer thickness is 10 nm), and a 1.5-μm-thick GaAs top layer (GaAs3) were grown. The thickness and the lattice mismatch of the SLS2 are almost the same as that used in Ref. 6 and are shown to be effective in reducing the etch pit density by about one order. Thermal cycle annealing was performed between GaAs2 and SLS2. As shown in Fig. 2, some dislocations which are observed in GaAs2 by TEM are bent at the interface of GaAs2 and SLS2. As a result, the dislocation density of GaAs3 is lower than that of GaAs2 and there is no dislocation in this photograph in GaAs3. The dislocation density of the GaAs layer is summarized to be GaAs1 > GaAs2 > GaAs3. The etch pit density of this sample is about  $1 \times 10^7 \text{ cm}^{-2}$ , which is lower than the EPD of GaAs on Si with only SLS1  $1.5 \times 10^7 \text{ cm}^{-2}$ , as shown in Table I. However, the etch pit density of  $1 \times 10^7 \text{ cm}^{-2}$  is not so low compared with the value of  $1.5 \times 10^7 \text{ cm}^{-2}$ . This indicates that the dislocations originate at the interface of SLS2 and GaAs3. Therefore an almost lattice-matched superlattice such as AlGaAs/GaAs or AlAs/GaAs is preferred not to generate new dislocations at the interface of SLS2 and



(a)



(b)

FIG. 3. Typical etch pit pattern of GaAs on Si with a GaAs/GaAsP SLS and an AlAs/GaAs SL (a) and the cluster of etch pit (b). (a) and (b) are the same sample.

GaAs<sup>3</sup> if these superlattices can bend the dislocation at the interface.

It is recently reported that the AlAs/GaAs SL is effective in reducing the dislocation density of homoepitaxial GaAs on GaAs substrate and the dislocation density is suppressed almost perfectly by the AlAs/GaAs SL.<sup>7</sup> So GaAs was grown on Si with SLS1 and a five-period AlAs/GaAs SL, where the AlAs/GaAs SL (each layer thickness is 0.1  $\mu\text{m}$ ) is replaced by SLS2 in Fig. 2. The typical etch pit pattern of this sample is shown in Fig. 3(a). The etch pit density is about  $(3-5) \times 10^5 \text{ cm}^{-2}$ , which is the lowest EPD ever reported. In some parts of the wafer, the EPD is almost zero. However, in some part of the wafer, the cluster of the etch pit was observed as shown in Fig. 3(b).

GaAs was grown on Si using the AlAs/GaAs SL intermediate layer alone. However, the EPD of this sample is only a little lower than that without the intermediate layer, and is on the order of  $10^7 \text{ cm}^{-2}$ . This indicates that almost lattice-matched SLs such as AlAs/GaAs SL are effective in reducing the dislocation density when the dislocation density is less than about  $10^7 \text{ cm}^{-2}$ , but are not effective when the dislocation density is more than about  $10^7 \text{ cm}^{-2}$ .

The mechanism of the dislocation bending by the AlAs(Si)/GaAs SL is thought to be the interaction between dislocation and electric charge.<sup>7</sup> It is not clear yet whether the reduction mechanism of the dislocation in GaAs on Si with the AlAs/GaAs intermediate layer is the same or not, but it is not due to the strain in the AlAs/GaAs interface because the lattice mismatch of GaAs and AlAs is very small, 0.13%, and the built-in strain in the AlAs/GaAs SL is not large enough to bend the threading dislocations. The mechanism of the dislocation reduction by the AlAs/GaAs

SL is now under consideration. Hopefully the EPD of GaAs on Si can be reduced to levels comparable to that of commercial GaAs substrates by the optimization of SLS, SL, and thermal-cycle annealing, especially in the AlAs/GaAs SL layers.

In summary, low etch pit density GaAs could be grown on Si with a GaAs/GaAsP SLS and an AlAs/GaAs SL. In the GaAs/GaAsP SLS, the dislocation decreases at the interface between GaAs and SLS, but does not decrease in the SLS. Even if the effective GaAs/GaAsP SLS is used as the intermediate layer, part of the threading dislocations propagates into the top GaAs layer because of the lattice mismatch between SLS and GaAs. To reduce the dislocation density further, both the GaAs/GaAsP SLS and the almost lattice-matched AlAs/GaAs SL are grown as the intermediate layers. The etch pit density of this sample is as low as  $(3-5) \times 10^5 \text{ cm}^{-2}$ .

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