

# Crystallinity and Schottky diode characteristics of GaAs grown on Si by metalorganic chemical vapor deposition

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The crystallinity of GaAs grown on Si with various intermediate layers by metalorganic chemical vapor deposition and characteristics of Schottky diodes fabricated on the grown GaAs/Si have been studied. The GaAs/Si with an  $\text{Al}_{0.55}\text{Ga}_{0.45}\text{P}$  intermediate layer has both good crystallinity, x-ray full width at half maximum of 188 arcsec, and a smooth surface. The Schottky diode fabricated on the GaAs/Si with an  $\text{Al}_{0.55}\text{Ga}_{0.45}\text{P}$  intermediate layer also shows good forward and reverse current-voltage characteristics with an ideality factor of 1.06, as good as for an *n*-type GaAs substrate. However, a relatively large leakage current is observed under reverse and small forward bias. This leakage current is caused by generation and recombination through the centers related to dislocations in the GaAs/Si.

## I. INTRODUCTION

In recent years many attempts have been made to obtain high-quality GaAs/Si grown by metalorganic chemical vapor deposition (MOCVD) or molecular-beam epitaxy (MBE) techniques. However, serious heteroepitaxial problems with growth of GaAs/Si still remain: polar/nonpolar interface and differences in thermal expansion and lattice constants between GaAs and Si. Many dislocations originating at the GaAs/Si interface propagate through the GaAs epitaxial layer. A high density of dislocations may degrade device performance for GaAs/Si. In spite of these problems, a GaAs epitaxial layer was successfully grown on Si by the two-step growth technique<sup>1</sup> and by using the intermediate layer consisting of GaP/GaAs<sub>0.5</sub>P<sub>0.5</sub> and GaAs<sub>0.5</sub>P<sub>0.5</sub>/GaAs strained layer superlattices on GaP(SLSs/GaP)<sup>2</sup> in a MOCVD reactor. Although many electronic and optical devices were fabricated on GaAs/Si by MOCVD or MBE techniques,<sup>3-8</sup> degradation of electrical characteristics of the devices on GaAs/Si due to the dislocations have not been reported in detail.

In this paper, we discuss crystallinity and Schottky diode characteristics of MOCVD-grown GaAs/Si by the two-step growth technique and by using the intermediate layers consisting of SLSs/GaP and  $\text{Al}_x\text{Ga}_{1-x}\text{P}$ . Crystallinity and Schottky diode characteristics of GaAs/Si were found to be sensitive to an intermediate layer grown directly on Si. The 50-nm-thick  $\text{Al}_{0.55}\text{Ga}_{0.45}\text{P}$  intermediate layer provides good crystallinity and Schottky diode characteristics. We also studied dislocation formation at the interfaces between intermediate layers and GaAs and intermediate layers and Si by cross-sectional transmission electron microscopy (TEM).

## II. EXPERIMENT

GaAs epitaxial layers were grown on Si substrates oriented 2° off (100) towards [011] in an rf-heated horizontal MOCVD reactor at atmospheric pressure by the two-step growth technique and by using the  $\text{Al}_x\text{Ga}_{1-x}\text{P}$  and SLSs/GaP intermediate layers. The source materials were trimethylgallium (TMG), trimethylaluminum (TMA), pure  $\text{AsH}_3$ , and  $\text{PH}_3$ . The substrates were decreased in organic solutions and cleaned using  $\text{H}_2\text{O}_2 + 4\text{H}_2\text{SO}_4$  and  $\text{HF} + \text{H}_2\text{O}$  solution. Then the substrates were heated at 1000 °C in an  $\text{AsH}_3 + \text{H}_2$  ambient in order to remove the oxide. In the two-step growth technique, a GaAs layer with a thickness of 12.5 nm was first deposited at 400 °C with a V/III ratio of 80, followed by a GaAs epitaxial layer doped with Se. In the structure with the  $\text{Al}_x\text{Ga}_{1-x}\text{P}$  intermediate layer, a 50-nm-thick  $\text{Al}_x\text{Ga}_{1-x}\text{P}$  layer was grown on Si at 900 °C with a V/III ratio of 100, followed by growth of a GaAs epitaxial layer doped with Se. In the structure with the SLSs/GaP intermediate layer, a 0.1-μm-thick GaP film was grown on a Si substrate at 900 °C, followed by five periods of 20-nm GaP/20-nm GaAs<sub>0.5</sub>P<sub>0.5</sub> SLS and five periods of 20-nm GaAs<sub>0.5</sub>P<sub>0.5</sub>/20-nm GaAs SLS at 750 °C. Then, a GaAs epitaxial layer doped with Se was grown. In all cases, 3-μm-thick GaAs epitaxial layers doped with Se to  $5 \times 10^{16} \text{ cm}^{-3}$  were grown at 650, 700, and 750 °C with the growth rate of 50 nm/min and a V/III ratio of 40.

Surface morphology was examined under a Nomarski microscope and the crystallinity of the GaAs top layers was characterized by double-crystal x-ray diffraction, the etch pit density (EPD) revealed by molten KOH etch and electron-beam-induced current (EBIC) measurements. The EBIC images were obtained using a scanning electron microscope with an electron beam current of  $2.0 \times 10^{-9} \text{ A}$ .

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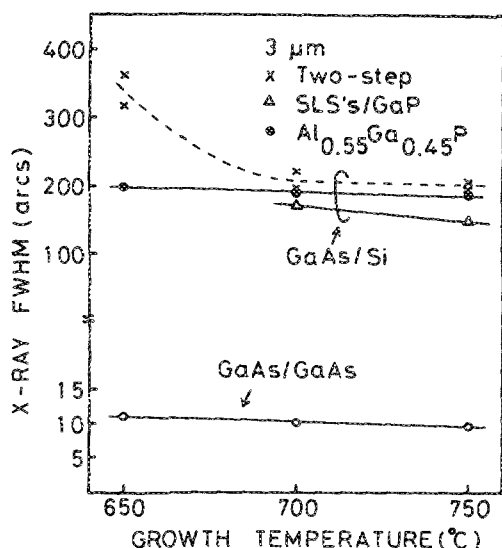


FIG. 1. Growth-temperature dependence of x-ray FWHM of GaAs/GaAs and GaAs/Si grown by two-step growth, SLSs/GaP, and  $\text{Al}_{0.55}\text{Ga}_{0.45}\text{P}$  techniques.

and an accelerating voltage of 12 kV. The formation of dislocations and structures of intermediate layers were studied by cross-sectional TEM. The solid compositions ( $x$ ) of  $\text{Al}_x\text{Ga}_{1-x}\text{P}$  ternary alloys were determined by Auger electron microscopy (AES).

AuGe/Ni/Au ohmic electrodes were formed by vacuum evaporation and alloyed at 380 °C for 1 min in a  $\text{N}_2$  ambient. After the contacts were etched by chemical solution, Schottky contacts to Se-doped GaAs were then made by the lift-off technique using Au as the Schottky contact metal. The area of the Schottky diodes in the study was  $7.85 \times 10^{-3} \text{ cm}^2$ . Forward and reverse current-voltage ( $I$ - $V$ ) and capacitance-voltage ( $C$ - $V$ ) characteristics of the Schottky diodes were measured. The ideality factor and the  $I$ - $V$  barrier height ( $\phi_b^{I-V}$ ) were calculated from the forward  $I$ - $V$  at various temperatures from 150 to 313 K. The capacitance was measured at 1 MHz, and the  $C$ - $V$  barrier height ( $\phi_b^{C-V}$ ) was also calculated.

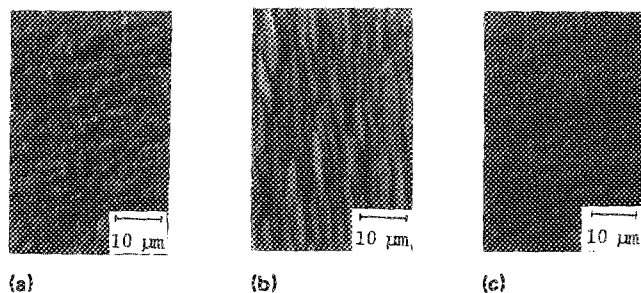


FIG. 2. Surface morphology of GaAs/Si grown by (a) two-step growth, (b) SLSs/GaP, and (c)  $\text{Al}_{0.55}\text{Ga}_{0.45}\text{P}$  techniques.

### III. RESULTS AND DISCUSSIONS

#### A. Crystallinity of GaAs/Si

Figure 1 shows the full width at half maximum (FWHM) of the (400) reflection peak in the x-ray double-crystal rocking curve as a function of growth temperature. For all samples except the GaAs/Si with the  $\text{Al}_{0.55}\text{Ga}_{0.45}\text{P}$  intermediate layer, the FWHM decreases with increasing growth temperature of the GaAs top layer, which suggests that crystallinity of GaAs/Si improves at higher growth temperatures. Particularly for the two-step-grown GaAs/Si, improvement of crystallinity with increasing temperature from 650 °C to 700 °C is significant. At 750 °C, the FWHMs of the GaAs/Si grown by the two-step growth

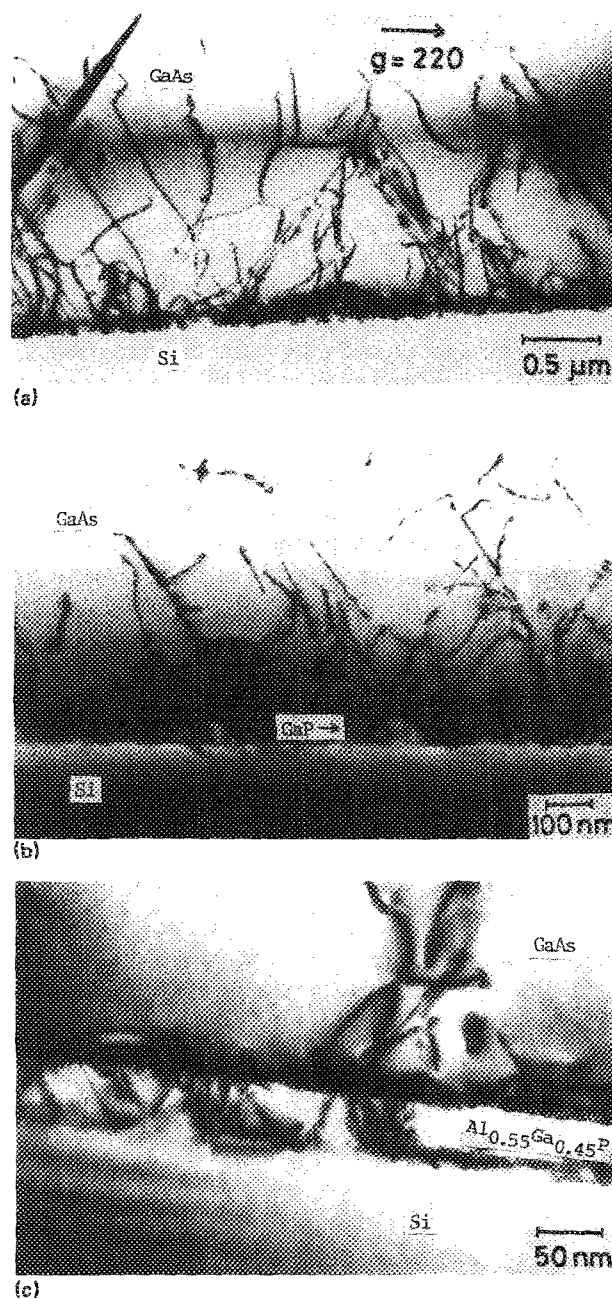


FIG. 3. Cross-sectional TEM micrographs of GaAs/Si grown by (a) two-step growth, (b) GaP, and (c) with  $\text{Al}_{0.55}\text{Ga}_{0.45}\text{P}$  intermediate layers.

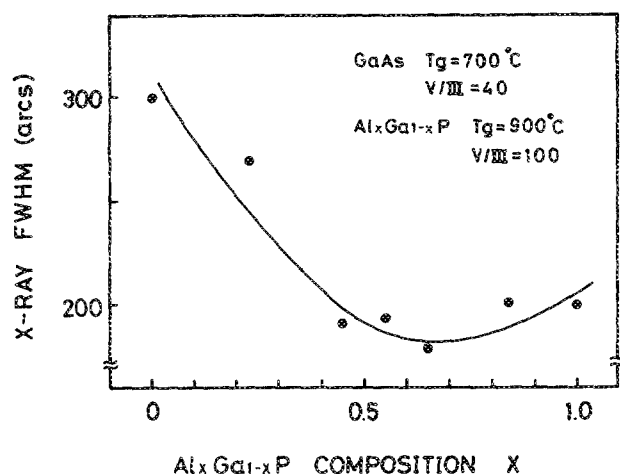


FIG. 4. Al composition dependence of x-ray FWHM of GaAs/Si grown with  $\text{Al}_x\text{Ga}_{1-x}\text{P}$  intermediate layer.

technique and by using  $\text{Al}_{0.55}\text{Ga}_{0.45}\text{P}$  and SLSSs/GaP intermediate layers are 210, 188, and 152 arcsec, respectively.

As shown in Fig. 2, the surface morphology of the GaAs/Si grown at  $750^\circ\text{C}$  with the  $\text{Al}_{0.55}\text{Ga}_{0.45}\text{P}$  intermediate layer is smoother than that of the GaAs/Si grown by the two-step growth technique and by using the SLSSs/GaP intermediate layer. To understand the improvement of surface morphology and crystallinity with the  $\text{Al}_{0.55}\text{Ga}_{0.45}\text{P}$  intermediate layer, cross-sectional TEM was performed. Figure 3 shows cross-sectional TEM micrographs of the GaAs/Si grown by the two-step growth technique and with the GaP and  $\text{Al}_{0.55}\text{Ga}_{0.45}\text{P}$  intermediate layers. In the GaAs/Si grown by the two-step growth technique, threading dislocations originating from the GaAs/Si interface decrease as the surface is approached. The EPD revealed by molten KOH etch is  $3.0 \times 10^7 \text{ cm}^{-2}$ . At the initial stage of GaAs growth, the GaAs grows three-dimensionally, and GaAs islands are formed. In the GaAs/Si grown with the GaP intermediate layer, the GaP grows three-dimensionally and GaP islands are formed on Si. Dislocations originate at the GaAs/Si and GaAs/GaP interface and decrease as the surface is approached. On the other hand, the  $\text{Al}_{0.55}\text{Ga}_{0.45}\text{P}$  intermediate layer grown on Si is planar, which indicates that the  $\text{Al}_{0.55}\text{Ga}_{0.45}\text{P}$  intermediate layer grows quasi-two-dimensionally. Most dislocations originate at the GaAs/ $\text{Al}_{0.55}\text{Ga}_{0.45}\text{P}$  interface. However, the majority of the dislocations are confined near the GaAs/ $\text{Al}_{0.55}\text{Ga}_{0.45}\text{P}$  interface and do not reach the surface

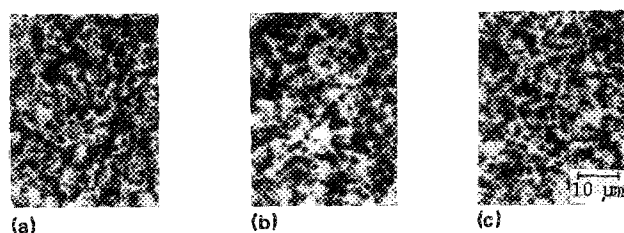


FIG. 5. EBIC images of GaAs/Si grown by (a) two-step growth, (b) SLSSs/GaP, and (c)  $\text{Al}_{0.55}\text{Ga}_{0.45}\text{P}$  techniques.

TABLE I. Crystallinity of GaAs/Si grown by two-step growth, SLSSs/GaP, and  $\text{Al}_{0.55}\text{Ga}_{0.45}\text{P}$  techniques.

GaAs/Si	FWHM (arc s)	EPD ( $\times 10^7 \text{ cm}^{-2}$ )	DSD ( $\times 10^7 \text{ cm}^{-2}$ )	Surface morphology
Two-step growth	210	3.0	3.6	mirror
SLSSs/GaP	152	2.0	3.4	mirrorlike
$\text{Al}_{0.55}\text{Ga}_{0.45}\text{P}$	188	2.5	3.1	mirror

of the GaAs layer. The EPD of the GaAs/Si grown with the  $\text{Al}_{0.55}\text{Ga}_{0.45}\text{P}$  intermediate layer is  $2.5 \times 10^7 \text{ cm}^{-2}$ . The planar growth of  $\text{Al}_{0.55}\text{Ga}_{0.45}\text{P}$  on Si is a main factor for improvement of surface morphology and crystallinity in the wide range of growth temperatures.

Figure 4 shows the x-ray FWHMs of the GaAs/Si grown with the  $\text{Al}_x\text{Ga}_{1-x}\text{P}$  intermediate layers with various compositions ( $x$ ) from 0 to 1. The x-ray FWHM depends on the composition ( $x$ ), and the minimum FWHM is obtained near 0.55. The dependence of the x-ray FWHM on the composition ( $x$ ) is similar to the dependence of the etch pit density and surface morphology.<sup>9</sup>

The EBIC measurement was performed to study an electrical influence of the dislocations. Figure 5 shows the EBIC images of the GaAs/Si grown by the two-step growth technique and by using the SLSSs/GaP and  $\text{Al}_{0.55}\text{Ga}_{0.45}\text{P}$  intermediate layers. The dark spot densities (DSD) of the GaAs/Si grown by the two-step growth technique and by using the SLSSs/GaP and  $\text{Al}_{0.55}\text{Ga}_{0.45}\text{P}$  intermediate layers are  $3.6 \times 10^7$ ,  $3.4 \times 10^7$ , and  $3.1 \times 10^7 \text{ cm}^{-2}$ , respectively. Table I summarizes the results of the x-ray FWHM, EPD, DSD and surface morphology. (We will later point out that Schottky diode characteristics are degraded by a high density of the dark spots in the GaAs/Si.)

## B. Schottky diode characteristics of GaAs/Si

Figure 6 shows the ideality factor calculated from the forward  $I$ - $V$  characteristics of Schottky diodes on GaAs/Si as a function of the growth temperature of the GaAs top layer. For comparison, the ideality factor of a Schottky diode fabricated on an  $n$ -type GaAs substrate is also shown

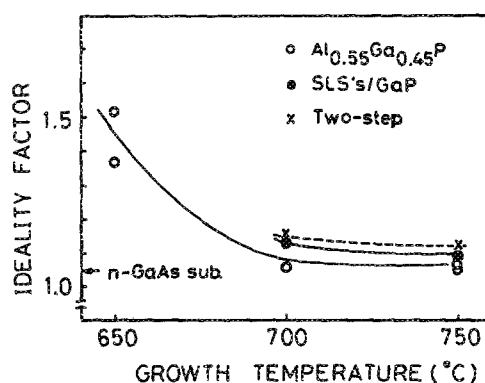


FIG. 6. Growth-temperature dependence of ideality factor of Au-GaAs/Si Schottky diode. The area of Schottky diode is  $7.85 \times 10^{-3} \text{ cm}^2$ .

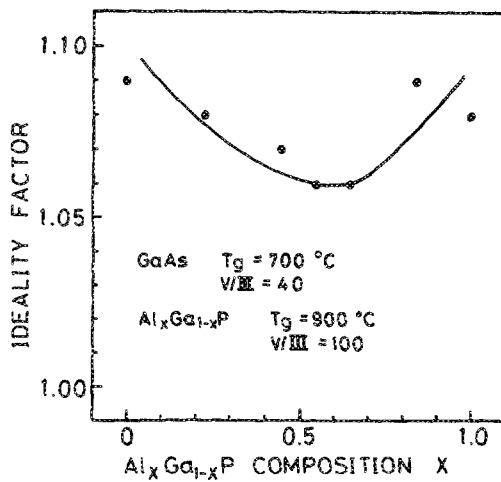


FIG. 7. Al composition dependence of ideality factor of Schottky diode on GaAs/Si grown with  $\text{Al}_x\text{Ga}_{1-x}\text{P}$  intermediate layer. The area of Schottky diode is  $7.85 \times 10^{-3} \text{ cm}^2$ .

in the figure. For the  $\text{Al}_{0.55}\text{Ga}_{0.45}\text{P}$  intermediate layer with increasing growth temperature, the ideality factor approaches 1. The ideality factors for the GaAs/Si grown at  $750^\circ\text{C}$  by the two-step growth technique and by using the SLs/GaP and  $\text{Al}_{0.55}\text{Ga}_{0.45}\text{P}$  intermediate layers are 1.11, 1.09, and 1.06, respectively. The Schottky diode characteristic for the GaAs/Si with the  $\text{Al}_{0.55}\text{Ga}_{0.45}\text{P}$  intermediate layer is as good as that for the *n*-type GaAs substrate.

Figure 7 shows the dependence of the ideality factor for the GaAs/Si with the  $\text{Al}_x\text{Ga}_{1-x}\text{P}$  intermediate layer on the composition (*x*). The diode ideality factors were averaged over 10 samples for each composition. The ideality factor depends on the composition (*x*), and the ideality factor of 1.06 is obtained at a composition of 0.55. This dependence of the ideality factor on the composition (*x*) is similar to that of x-ray FWHMs and the surface morphology discussed earlier.

Assuming the Richardson constant  $A^{**}$  is  $8.6 \text{ A cm}^{-2} \text{ K}^{-2}$  and that the *I-V* characteristic follows the thermionic emission model,<sup>10</sup> the *I-V* barrier height ( $\phi_b^{I-V}$ ) was calculated from the extrapolated current at 0 V in the forward *I-V* characteristic, and they are all between 0.86 and 0.87 eV.

Figure 8 shows plots of  $C^{-2}$  vs *V*. A linear dependence of  $C^{-2}$  on *V* was found for all samples in the reverse bias voltages from 0 to 4 V. The diffusion potential ( $V_f$ ) of the Schottky diodes was obtained from the intercept of the horizontal axis in the plots of  $C^{-2}$  vs *V*. The *C-V* barrier height ( $\phi_b^{C-V}$ ) from the *C-V* measurement is calculated from<sup>10</sup>

$$\phi_b^{C-V} = V_f + \xi + kT/q, \quad (1)$$

where  $\xi$  is the energy difference between the Fermi level and the bottom of the conduction band in the bulk semiconductor. The ideality factor, the carrier concentration (*N*) and the barrier heights,  $\phi_b^{I-V}$  and  $\phi_b^{C-V}$ , are tabulated in Table II. The ideality factor,  $\phi_b^{I-V}$ , and  $\phi_b^{C-V}$ , of a Schottky diode on lightly doped ( $7 \times 10^{16} \text{ cm}^{-3}$ ) *n*-type GaAs substrate are 1.05, 0.90, and 0.96 eV, respectively, which in-

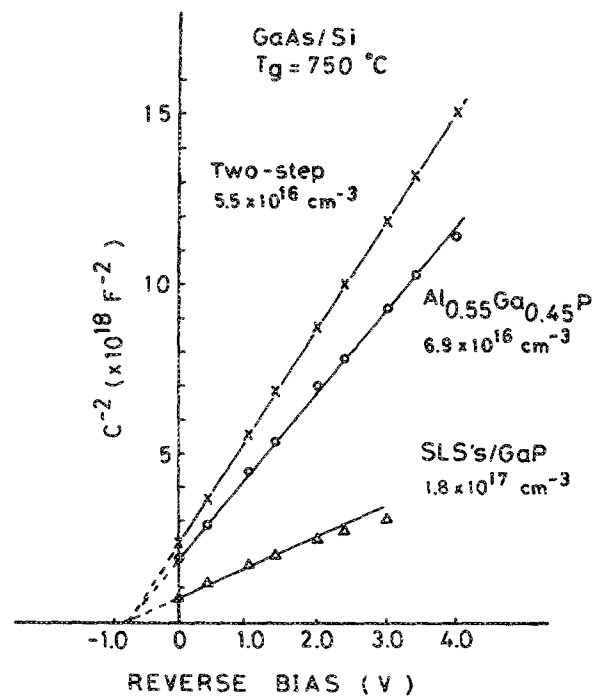


FIG. 8. *C-V* data of Au-GaAs/Si Schottky diode. The area of Schottky diode is  $7.85 \times 10^{-3} \text{ cm}^2$ .

dicates that affects of the thin GaAs native oxide or variation of the fabrication process on Schottky diode characteristics are negligible.

Assuming that the *I-V* characteristics of a Schottky diode is determined by the thermionic emission current ( $I_{te}$ ) and the recombination current ( $I_r$ ), the total current is now given by<sup>10,11</sup>

$$I = I_{te} + I_r = I_0 [\exp(qV/kT) - 1] + I_{r0} [\exp(qV/2kT) - 1], \quad (2)$$

where  $I_0 = AA^{**}T^2 \exp(-\phi_b/kT)$  and  $I_{r0} = Aqn_iw/2\tau_r$ . Here *A* is the area of a diode,  $A^{**}$  is the Richardson constant, *T* is the device temperature, *V* is the applied voltage, *k* is the Boltzmann constant,  $\phi_b$  is the effective barrier height,  $n_i$  is the intrinsic carrier concentration proportional to  $\exp(-qE_g/2kT)$ , *w* is the thickness of the depletion region,  $E_g$  is the band-gap energy, and  $\tau_r$  is the lifetime within the depletion region. By measuring the forward current as a function of temperature it is possible to determine

TABLE II. Ideality factor, carrier concentration, and Schottky barrier heights calculated from forward *I-V* and *C-V* characteristics for GaAs/Si grown by two-step growth, SLs/GaP, and  $\text{Al}_{0.55}\text{Ga}_{0.45}\text{P}$  techniques. The area of the Schottky diode is  $7.85 \times 10^{-3} \text{ cm}^2$ .

GaAs/Si	Ideality factor	Carrier concentration ( $\times 10^{16} \text{ cm}^{-3}$ )	$\phi_b^{I-V}$ (eV)	$\phi_b^{C-V}$ (eV)
Two-step growth	1.11	5.5	0.87	0.90
SLs/GaP	1.09	18.0	0.86	0.89
$\text{Al}_{0.55}\text{Ga}_{0.45}\text{P}$	1.06	6.9	0.87	0.92

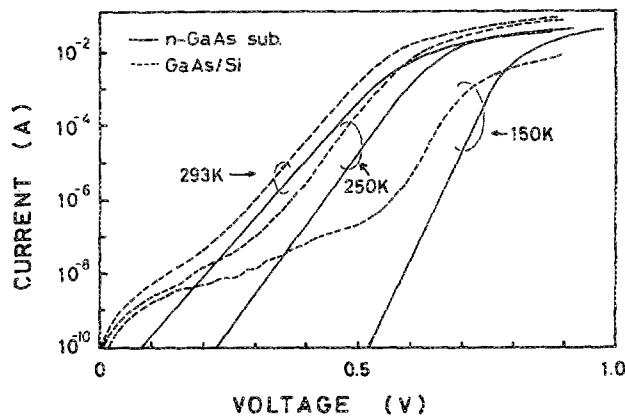


FIG. 9. Forward  $I$ - $V$  characteristics of Schottky diode on  $n$ -type GaAs substrate and GaAs/Si grown with  $\text{Al}_{0.55}\text{Ga}_{0.45}\text{P}$  intermediate layer as a function of temperature. The area of Schottky diode is  $7.85 \times 10^{-3} \text{ cm}^2$ .

which is dominant, the thermionic emission or the recombination current. When the thermionic emission current is dominant, a plot of  $\ln(I_{\text{te}}/T^2)$  as a function of  $1/T$  should yield a straight line with a slope of  $-q(\phi_b - V)$ , which gives the activation energy. When the recombination current is dominant, on the other hand, the temperature dependence of the forward current shows two activation energies, and the reverse current ( $I_{r0}$ ) becomes proportional to the square root of the reverse bias ( $V_r^{1/2}$ ) if the concentration of the recombination centers is uniform across the thickness.

The typical forward  $I$ - $V$  characteristics of Schottky diodes on an  $n$ -type GaAs substrate and on GaAs/Si with the  $\text{Al}_{0.55}\text{Ga}_{0.45}\text{P}$  intermediate layer as a function of temperature are shown in Fig. 9. The nonlinearities in the curves under large forward bias are caused by series resistance. Note much larger current under small forward bias for the GaAs/Si. Similar temperature dependencies of  $I$ - $V$  characteristics are observed in the GaAs/Si grown by the two-step growth technique and by using the SLSs/GaP intermediate layer. This leakage current cannot be explained by the thermionic emission current. The ideality factor in this region is about 2, which suggests that this leakage current is due to the recombination current. To further verify that this leakage current is the recombination current, the value of  $\ln(I/T^2)$  from the current at the forward voltage of 0.4 V is plotted as a function of  $1000/T$  in Fig. 10. The plot for an  $n$ -type GaAs substrate shows a single activation energy, while the plots for the GaAs/Si show two activation energies. The activation energy for the  $n$ -type GaAs substrate is 0.508 eV, while the activation energy for the GaAs/Si grown with the  $\text{Al}_{0.55}\text{Ga}_{0.45}\text{P}$  intermediate layer is 0.407 eV above 180 K and 0.221 eV below 180 K. This indicates that the leakage current of GaAs/Si increases at lower temperatures.

Figure 11 shows a plot of  $\ln I_{r0}$  vs  $\ln V_r$ . In the GaAs/Si, a sharp increase of current at near 4 V is due to avalanche breakdown. The value is rather small compared with that for the  $n$ -type GaAs substrate, which may be related to the higher dislocation density in the GaAs/Si. The slope of the plot indicates that the reverse current

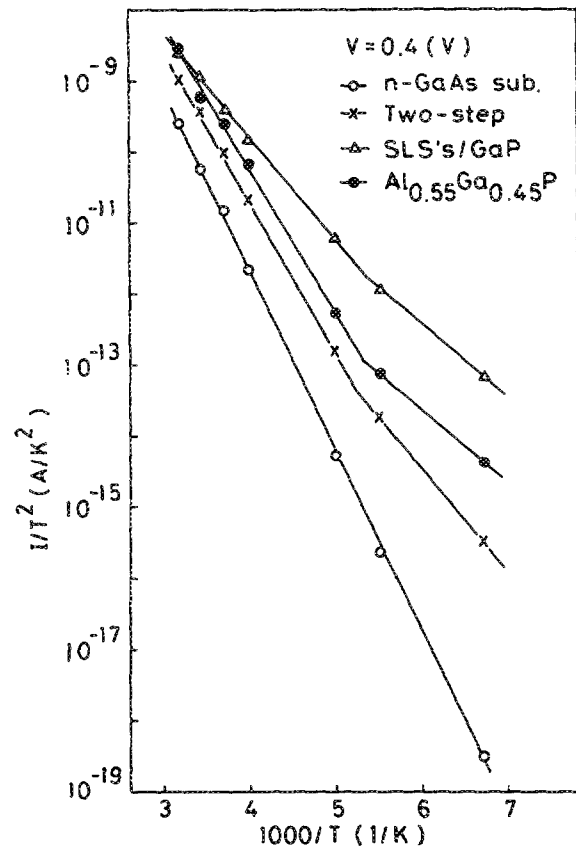


FIG. 10. Temperature dependence of  $I/T^2$  obtained from the current at the forward bias of 0.4 V for  $n$ -type GaAs substrate and GaAs/Si grown by two-step growth, SLSs/GaP, and  $\text{Al}_{0.55}\text{Ga}_{0.45}\text{P}$  techniques. The area of Schottky diode is  $7.85 \times 10^{-3} \text{ cm}^2$ .

( $I_{r0}$ ) is proportional to  $V_r^{1.8}$ , which suggests that the reverse current is caused by the generation current due to the recombination centers. The generation current density ( $J_{\text{gen}}$ ) due to the recombination centers in the depletion region is given by

$$J_{\text{gen}} = \int_0^w \frac{qn_i}{\tau_e} dx, \quad (3)$$

where  $\tau_e = 1/N_r$ . Here  $\tau_e$  is the effective lifetime and  $N_r$  is the trap density. The depth profile of  $N_r$  to satisfy

$$I_{r0} \propto V_r^{1.8}, \quad (4)$$

is expected that

$$N_r \propto x^{2.6}. \quad (5)$$

Figure 12 shows the dependence of the ideality factor and the  $\phi_b^{I-V}$  on temperature. The  $\phi_b^{I-V}$  is reportedly a decreasing function of temperature.<sup>12</sup> The ideality factor and  $\phi_b^{I-V}$  for the  $n$ -type GaAs substrate are unchanged. For the GaAs/Si, however, the ideality factor and the  $\phi_b^{I-V}$  are decreasing and increasing functions of temperature, respectively. The ideality factor approaches 1 at high temperature where the thermionic emission process becomes dominant compared with the recombination process. The observation that the  $\phi_b^{I-V}$  for the GaAs/Si is an increasing

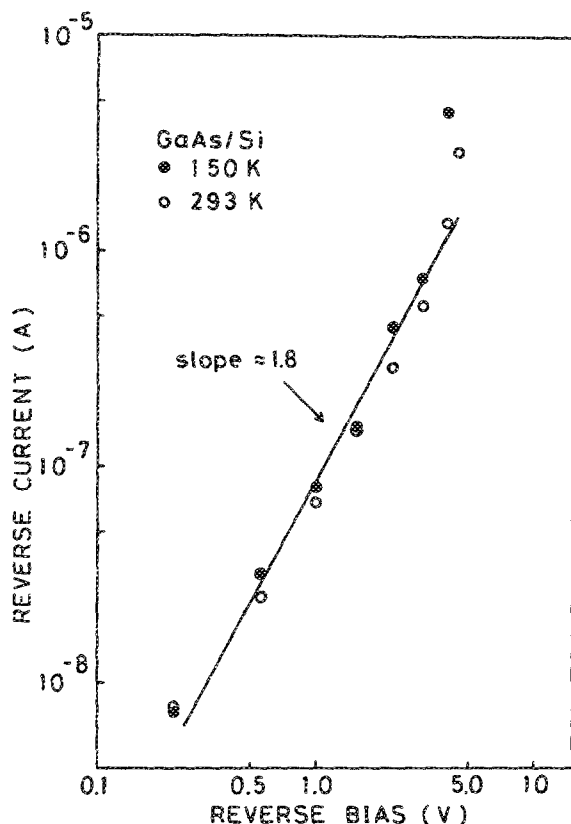


FIG. 11. Relationship between reverse current and reverse bias for GaAs/Si grown with  $\text{Al}_{0.55}\text{Ga}_{0.45}\text{P}$  intermediate layer at 150 and 293 K. The area of Schottky diode is  $7.85 \times 10^{-3} \text{ cm}^2$ .

function of temperature may be related to material and electrical properties unique to the GaAs/Si.

#### IV. CONCLUSIONS

We have studied the crystallinity of MOCVD-grown GaAs/Si with various intermediate layers and the characteristics of Schottky diodes fabricated on the grown GaAs/Si. The  $\text{Al}_{0.55}\text{Ga}_{0.45}\text{P}$  intermediate layer overall optimizes crystallinity, morphology, and Schottky diode characteristics. The cross-sectional TEM study shows that the improvements with the  $\text{Al}_{0.55}\text{Ga}_{0.45}\text{P}$  intermediate layer are due to quasi-two-dimensional growth of  $\text{Al}_{0.55}\text{Ga}_{0.45}\text{P}$  on Si. Although the forward and reverse  $I$ - $V$  characteristics of the Schottky diodes fabricated on the GaAs/Si with the  $\text{Al}_{0.55}\text{Ga}_{0.45}\text{P}$  intermediate layer are good, a significant leakage current is observed under reverse and small forward bias, in contrast to the  $n$ -type GaAs substrate. The leakage current is caused by recombination and generation centers associated with the high density of dislocations in the GaAs/Si.

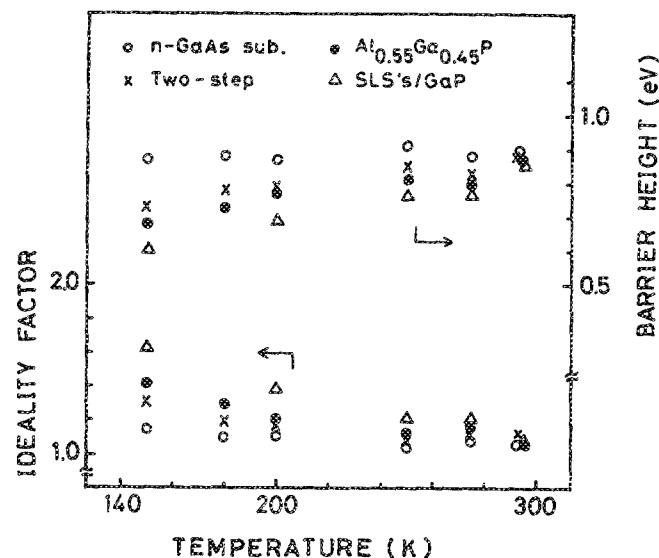


FIG. 12. Temperature dependence of ideality factor and  $I$ - $V$  barrier height for  $n$ -type GaAs substrate and GaAs/Si grown by two-step growth, SLSs/GaP and  $\text{Al}_{0.55}\text{Ga}_{0.45}\text{P}$  techniques. The area of Schottky diode is  $7.85 \times 10^{-3} \text{ cm}^2$ .

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