

Improved characteristics of GaAs metal-semiconductor field-effect transistors on Si substrates back-coated with SiO₂ by metalorganic chemical vapor deposition

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(Received 21 August 1990; accepted for publication 24 December 1990)

GaAs metal-semiconductor field-effect transistors (MESFETs) on Si substrates back-coated with SiO₂ grown at high temperature by metalorganic chemical vapor deposition have shown good pinch-off and suppressed sidegating. The SiO₂ back-coating suppresses Si incorporation into an undoped GaAs layer during growth, and use of such an undoped layer with a low electron concentration beneath the channel layer improves a pinch-off characteristic. Higher growth temperature also improves crystallinity of GaAs layers grown on Si and helps to suppress the sidegating effect of GaAs MESFETs. The maximum transconductance of 160 mS/mm and the K value of 46.8 mA/V² mm have been obtained for a MESFET with 2.5 μ m gate length.

Laser diodes, solar cells, metal-semiconductor field-effect transistors (MESFETs), and high electron mobility transistors (HEMTs) have been fabricated on Si using the molecular beam epitaxy (MBE) and the metalorganic chemical vapor deposition (MOCVD) techniques.¹⁻⁵ However, mismatches of lattice parameters and thermal expansion coefficients, and unintentional Si autodoping in a grown GaAs layer affect the device characteristics. In particular, it is necessary for realization of high-performance GaAs integrated circuits (ICs) on Si to improve the pinch-off characteristic and suppress the sidegating effect of a GaAs MESFET on Si. The pinch-off characteristics of GaAs MESFETs and HEMTs grown on Si by MOCVD are often degraded by unintentional Si autodoping in undoped layers. To ease this problem some workers doped GaAs layers with vanadium,³ and others lowered growth temperature to increase resistivity of undoped GaAs layers.⁴

One of major problems limiting an integration level of GaAs ICs is the sidegating effect, and susceptibility to the sidegating effect is expected to depend on the crystallinity of GaAs layers grown on Si. In general, higher growth temperature improves the crystallinity of GaAs on Si and may reduce the sidegating effect. However, an undoped GaAs layer grown on Si at high temperature by MOCVD has a high electron concentration due to enhanced Si incorporation,⁶ which degrades the pinch-off characteristic of a MESFET on Si. In this letter, we propose the use of Si substrate back-coated with SiO₂ to improve pinch-off and suppress sidegating of a GaAs MESFET on Si.

All epitaxial layers were grown on (100) p -Si substrates oriented 2° off toward [011] in a rf-heated horizontal MOCVD reactor at atmospheric pressure using the two-step growth technique. The back of some substrates were coated with a 720-nm-thick sputtered SiO₂ film.¹ The source materials were trimethylgallium (TMG), trimethylaluminum (TMA), arsine (AsH₃). A detailed growth

procedure for GaAs on Si is described elsewhere.^{1,7} For MESFETs, the following layers were successively grown on p -Si substrates with and without SiO₂ back-coating: a 12.5-nm-thick GaAs nucleation layer at 400 °C, a 0.8- μ m-thick undoped GaAs buffer layer at 700 °C, a 1- μ m-thick p -Al_{0.3}Ga_{0.7}As layer at 700 °C, a 1- μ m-thick undoped GaAs layer at 650, 700, and 750 °C, a 0.3- μ m-thick channel layer doped with Se to 3×10^{17} cm⁻³ at 750 °C, and a 60-nm-thick ohmic contact layer doped with Se to 1×10^{18} cm⁻³ at 750 °C. The p -Al_{0.3}Ga_{0.7}As layer was not inserted for some MESFETs characterized by the transmission line model (TLM). Then, MESFETs were fabricated using the recessed gate technique. A 0.1- μ m-thick SiO₂ film was sputtered on the top n^+ -GaAs layer, and a 0.8- μ m-deep mesa isolation was performed by chemical etching. AuGe/Ni/Au source and drain ohmic contacts were formed by evaporation/liftoff and alloyed at 380 °C for 1 min in flowing N₂ gas. The gate region was recessed to a depth of about 0.2 μ m by chemical etching, and the gate contact was made by evaporation/liftoff of Ti/Au. The test pattern for the device isolation consists of two 80- μ m-long ohmic contacts to the n^+ -GaAs layer regions separated by 8 μ m with the etched isolation. The test pattern of the TLM, which consists of 80 μ m \times 80 μ m ohmic contacts to the n^+ -GaAs layer with various spacings from 10 to 160 μ m, was used to study the laterally spreading current flow.

Figure 1 shows the electron concentration profiles of MESFETs grown at 750 °C on the "passivated" and "unpassivated" Si substrates. In the "passivated" Si substrate, the back and side edges of the Si substrate were covered with a Si₃N₄/SiO₂ stacked layer to suppress the gas phase transport of Si from Si substrate during the growth.⁶ As seen in the figure, the electron concentration of the undoped GaAs layer beneath the channel layer for the "passivated" Si is 3×10^{14} cm⁻³, as low as that of the undoped the GaAs layer grown on GaAs substrate. However, for simplicity of experiments MESFETs discussed below were fabricated on Si substrates, only the back of which were covered with a sputtered SiO₂ film. These Si

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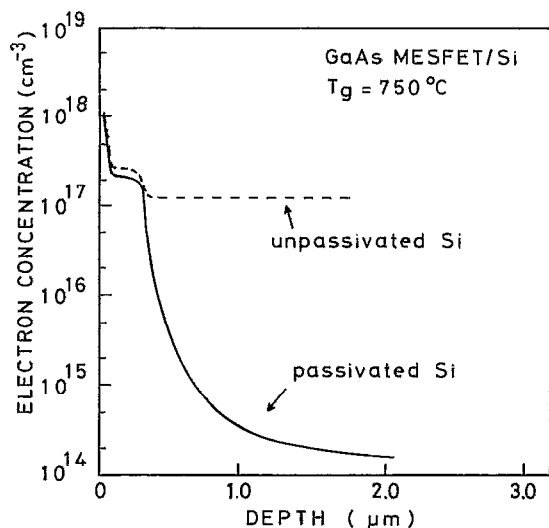


FIG. 1. Electron concentration profiles of MESFET structures grown at 750 °C on the "passivated" and the "unpassivated" Si substrates. In the "passivated" Si, the back and side edges were covered with a $\text{Si}_3\text{N}_4/\text{SiO}_2$ stacked layer.

substrates, back-coated with a sputtered SiO_2 film, have side edges still exposed to the ambient and are less effective in suppressing the gas phase transport of Si during growth. Nevertheless, the electron concentration of an undoped GaAs layer grown at 750 °C has been reduced to $1 \times 10^{15} \text{ cm}^{-3}$ from $1 \times 10^{17} \text{ cm}^{-3}$ by using the Si substrates back-coated with a 720-nm-thick sputtered SiO_2 film.^{1,6}

The isolation leakage current in the undoped GaAs layers measured at 0.1 V is shown in Fig. 2. The undoped GaAs layers were grown at 650, 700, and 750 °C on Si substrates without and with 720-nm-thick SiO_2 back-coating. The isolation leakage is determined by conduction paths in the undoped layer beneath the channel and near

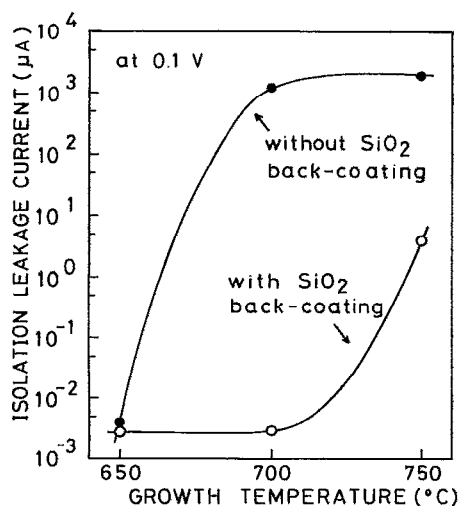


FIG. 2. Isolation leakage currents in the undoped GaAs layers beneath the channel layers grown at 650, 700, and 750 °C on Si substrates with and without 720-nm-thick SiO_2 back-coatings. The samples have MESFET structure with a $p\text{-Al}_{0.3}\text{Ga}_{0.7}\text{As}$ layer.

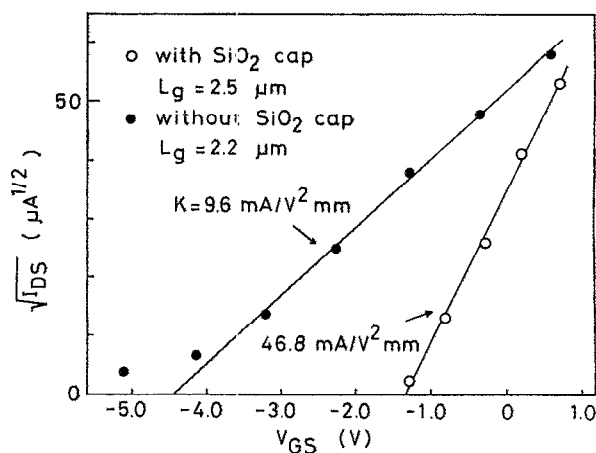


FIG. 3. Relationship between the gate bias and the square root of the source-drain current of MESFETs with 15 μm gate width on Si substrates with and without SiO_2 back-coating.

the GaAs/Si interface. The inserted $p\text{-Al}_{0.3}\text{Ga}_{0.7}\text{As}$ prevents the current reaching the GaAs/Si interface, as will be discussed in detail later. If the undoped layer beneath the channel is of high resistivity, the isolation leakage current should be negligibly small. This measurement tests whether the resistance of the undoped layer is high enough to isolate two MESFETs. Without SiO_2 back-coating, the isolation leakage current greatly increases from 4 nA to 1.9 mA with increasing growth temperature from 650 to 750 °C. An increase of the leakage current reflects an increase of electron concentration in the undoped GaAs layer with increasing growth temperature.⁷ With SiO_2 back-coating, however, it remains less than 4 μA even when growth temperature is as high as 750 °C. The larger leakage observed for a growth temperature of 750 °C suggests that Si incorporation into a GaAs layer by the gas phase transport of Si from the side edges exposed to the ambient seems more significant than at lower temperature.

By using the TLM pattern, we studied the lateral current flow in the MESFETs with and without a $p\text{-Al}_{0.3}\text{Ga}_{0.7}\text{As}$ buffer layer on Si. A linear dependence of the resistance on the spacing between the ohmic metal pads was found for a Si substrate back-coated with SiO_2 when a $p\text{-Al}_{0.3}\text{Ga}_{0.7}\text{As}$ buffer layer was grown beneath the undoped GaAs layer. The conductivity near the GaAs/Si interface is comparable to that of the n^+ -GaAs layer because there is a high electron concentration near the GaAs/Si. The current reaching the GaAs/Si interface can flow laterally to the ohmic metal pad and create a parallel conduction path. Use of Si substrate back-coated with SiO_2 cannot prevent such current. Creating a barrier by inserting a $p\text{-Al}_{0.3}\text{Ga}_{0.7}\text{As}$ layer prevents the current reaching the interface.

Figure 3 shows the relationship between the gate bias and the square root of the source-drain current of MESFETs on Si substrates with and without SiO_2 back-coating. The MESFET structures were grown on the $p\text{-Al}_{0.3}\text{Ga}_{0.7}\text{As}$ buffer layer discussed above. The undoped GaAs layers beneath the channel layers were grown at 700 °C. The

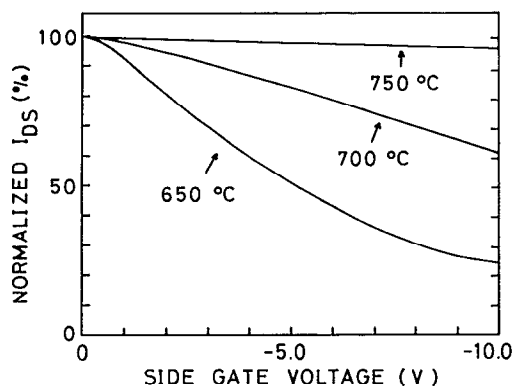


FIG. 4. Comparison of the drain saturation currents at $V_{GS} = 0$ V for MESFETs on SiO_2 back-coated Si substrates. The undoped GaAs layers beneath the channel layers were grown at 650, 700, and 750 °C. The current is normalized to their respective values at $V_{sg} = 0$ V.

MESFET on the Si substrate without SiO_2 back-coating has a serious problem with pinch-off because of lateral current flow in the undoped GaAs layer beneath the channel layer. The threshold voltage (V_{th}), the maximum transconductance (g_{mmax}), and the K value in a “square law” drain current-to-gate voltage relationship are -4.4 V, 74 mS/mm, and 9.6 mA/V² mm, respectively, for a MESFET with a 2.2×15 μm gate on Si substrate without the back-coating. However, a MESFET on a Si substrate with the back-coating shows better pinch-off and a higher K value. For a MESFET with a 2.5×15 μm gate on a Si substrate back-coated with SiO_2 , the V_{th} , the g_{mmax} , and the K value are -1.3 V, 160 mS/mm and 46.8 mA/V² mm, respectively. A reason for the higher g_{mmax} and K value is that the current flow in the undoped GaAs layer beneath the channel layer is suppressed because of its higher resistance.

Figure 4 is the normalized drain saturation current at

the gate bias (V_{GS}) of 0 V as a function of the side gate bias (V_{sg}) for the MESFETs on SiO_2 back-coated Si substrates. The undoped GaAs layers beneath the channel layers were grown at 650, 700, and 750 °C. The current is normalized to their values at $V_{sg} = 0$ V. The sidegating pad is located 30 μm away from the source of the device. Higher growth temperature of the undoped GaAs layer beneath the channel layer reduces the sidegating effect. For a growth temperature of 750 °C, reduction of the drain current is less than 4% even when -10 V is applied to the sidegating pad. The sidegating effect is strongly affected by crystallinity of the undoped GaAs layer. Higher growth temperature improves crystallinity⁷ and reduces the sidegating effect.

In summary, GaAs MESFETs with good pinch-off and suppressed sidegating were fabricated on Si substrates back-coated with a sputtered SiO_2 film. The back-coating suppresses the gas phase transport of Si from substrate and reduces Si incorporation into an undoped GaAs layer during MOCVD growth even at high temperature. The undoped GaAs layer grown at high temperature is of good crystallinity and suppresses the sidegating effect. Since the undoped GaAs layer beneath the channel grown even at high temperature has a low electron concentration, the pinch-off characteristic of the MESFET has been improved by the back-coating of Si substrates with SiO_2 .

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