Radical assisted metalorganic chemical vapor deposition of CdTe on GaAs and carrier transport mechanism in CdTe/*n*-GaAs heterojunction

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The growth and carrier transport mechanism in CdTe on the GaAs substrate is reported. Epitaxial layers of CdTe were grown on *n*- and semi-insulating GaAs substrates by the hydrogen radical assisted metalorganic chemical vapor deposition technique at a low pressure. Dimethylcadmium and diethyltelluride were used as the source materials. The growth was carried out in the substrate temperature range of 150–300 °C. The grown films have high resistivity in the order of 10^7 Ω cm for the entire growth range. Applicability of this heteroepitaxial CdTe layer on *n*-GaAs as an x-ray detector was then investigated. The carrier transport mechanism of the CdTe/*n*-GaAs heterojunction was studied by means of current–voltage measurements at different temperatures. The forward current was characterized by multitunneling capture-emission current and space charge limited current. The reverse current was considered as the generation current from the heterojunction interface states through the analysis of capacitance–voltage measurement. It is found that for devices using minority carriers, this heterojunction alone is not useful because of the high concentration of interface states. A suitable modification, like an isotype heterojunction between GaAs and CdTe before forming the *p*-*n* junction, seems to be necessary. © *1998 American Institute of Physics.* [S0021-8979(98)03405-7]

I. INTRODUCTION

The growth of high quality CdTe films is essential because of the technological importance of CdTe and related compounds for high energy flux (x ray, γ ray) detectors. In comparison to other materials which have been popularly used, such as PbO, Si, Se, etc., CdTe has a high absorption coefficient because of its high atomic number (Cd=48, Te =52) and an appropriate band gap ($\approx$1.5 eV), making it the most promising detector material. There are many reports on the fabrication of detectors using polycrystalline CdTe grown by metalorganic chemical vapor deposition (MOCVD)[1,2] or sputter deposition.[3,4] Polycrystalline CdTe has the advantages of large-area coverage and low-cost fabrication. However, it has drawbacks of slow temporal response and low energy resolution characteristics because of its low carrier mobility. Single crystal CdTe and related compound semiconductors may solve these problems.

Many researchers have been investigating the growth of CdTe on GaAs and other substrates because of the lack of availability of high quality, large-area single crystal CdTe.[5–7] Heteroepitaxial layers of this type can then be used as an active medium for device applications or as buffer layers for subsequent growth of related compounds. There are also reports on the growth of single crystal CdTe by molecular beam epitaxy (MBE)[6–9] and atmospheric pressure MOCVD.[10–16] Since MOCVD growth is usually carried out at atmospheric or near atmospheric pressure, there are many unwanted reactions in the gas phase which yield dusty powder. Moreover, nitrogen doping using plasma source, which is now recognized as a promising way for impurity doping in MBE, cannot be applied in MOCVD due to rapid recombination of atomic radicals at high pressure. We have used a low pressure MOCVD method to suppress unwanted powder formation and to improve radical-surface reactions on the substrate. However, when the pressure is low, the deposition rate is too slow for practical applications. So, atomic hydrogen radicals produced in a remote plasma source have been introduced into the reaction chamber in order to accelerate the decomposition rate of source monomer and hence to increase the deposition rate. Moreover, *p*-type doping of CdTe can be achieved by introducing nitrogen as a plasma gas source.

In the present work, the hydrogen radical assisted MOCVD method working at low pressure[17,18] and low substrate temperature has been studied for the growth of single crystal CdTe. Then, the heterointerface between CdTe and *n*-GaAs is also studied through the measurement and analysis of current–voltage (I–V) characteristics. Although there are numerous reports on the growth of CdTe on GaAs, to our knowledge, the electrical characteristics of this heterojunction have not yet been clearly understood. Hence study of this heterojunction seems appropriate for understanding the performance of detectors based on this material.

II. EXPERIMENT

Figure 1 shows the schematic diagram of the MOCVD system used in this study. The vacuum chamber is made of stainless steel and inner gas flow tubes are made from quartz. Hydrogen plasma was produced by applying inductively coupled rf (13.56 MHz) power to the branched quartz tube.

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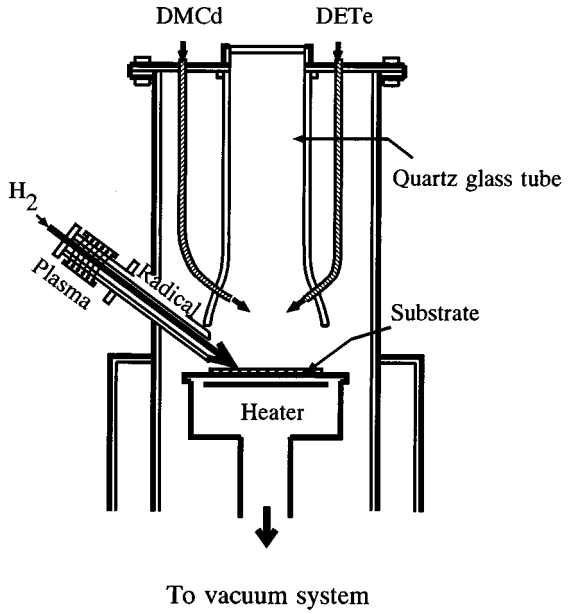


FIG. 1. Schematic diagram of RAMOCVD reactor.

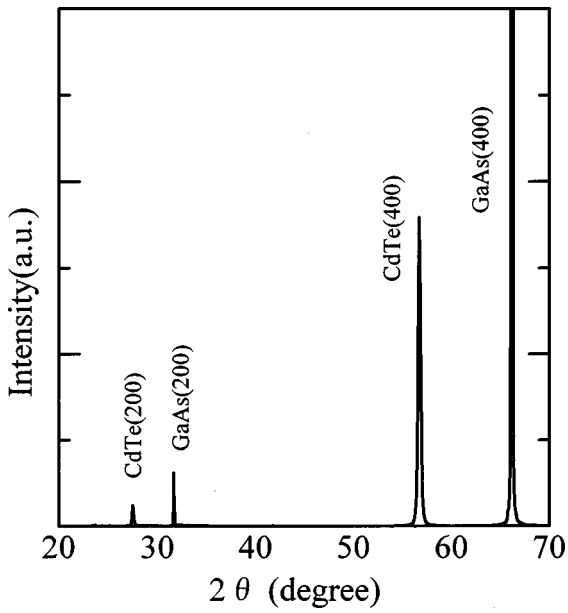


FIG. 2. X-ray diffraction patterns of CdTe layer.

The rf coils were 20 cm from the reaction region and hydrogen radicals were transported through the quartz tube into the chamber. In this experiment, 50 W rf power was applied. Dimethylcadmium (DMCd) and diethyltelluride (DETe) were used as the source materials. Typical growth conditions are shown in Table I. The substrates were (100) oriented *n*- and semi-insulating (SI)-GaAs, polished on one side and having a dimension of 11 mm×12 mm. They were first cleaned in organic solvents and chemically etched in a solution of H_2SO_4, H_2O_2, and H_2O in the ratio of 10:1:1, then thoroughly rinsed in deionized water and dried thoroughly. Before the growth, the substrates were heated at 400 °C in hydrogen atmosphere at a pressure of 0.01 Torr for 5 min and after adjusting the substrate temperature to an appropriate point, epitaxial growth was carried out. A typical film 500 nm thick was used for the electrical measurements. Ohmic contacts were produced by vacuum evaporation of gold electrodes of 1.5 mm diameter onto the CdTe surface and Ge–Au on the *n*-GaAs backside. The current–voltage ($I-V$) characteristics of this heterojunction were investigated by measuring the direct current through the electrodes, using an electronic picoammeter (ADVANTEST, TR-8641), as a function of temperature in the range between 294 and 355 K in a vacuum chamber. The capacitance–voltage ($C-V$) characteristics were measured at 100 kHz, using a capacitance-conductance meter (MEGABYTEK, MI-490).

TABLE I. Typical growth condition of CdTe films.

DMCd flow rate	12 μmol/min
DETe flow rate	12 μmol/min
Hydrogen flow rate for plasma radicals	10 sccm
rf (13.56 MHz) power	50 W
Deposition pressure	0.2 Torr
Substrate temperature	150–300 °C
Substrates	*n*-GaAs and SI-GaAs, (100) orientation

The electrical resistivity of the CdTe layers was determined by the van der Pauw method using layers grown on the SI-GaAs substrate and having gold electrodes at the four corners.

The crystallinity of the epitaxial films was measured by x-ray diffraction (XRD) and reflection high energy electron diffraction (RHEED).

III. RESULTS AND DISCUSSION

A. Epitaxial growth of CdTe

Figure 2 shows the XRD pattern of the CdTe film grown at the substrate temperature (ST) of 200 °C. XRD was carried out on a Rigaku x-ray diffractometer using Cu $K_{\alpha 1 \text{ and } 2}$ radiation with step angle 2θ which varied from 20° to 70°. The structure of this film was assigned as cubic with a preferential orientation of the (100) plane parallel to the substrate. The CdTe (400) peak was used to calculate the full width at half-maximum (FWHM) value which corresponds to the $\delta 2\theta$ and was estimated as 400 arcsec. Other CdTe epitaxial layers grown at various ST as specified in Table I showed FWHM value ranging from 400 to 700 arcsec. These values are rather higher in comparison to other MOCVD grown CdTe layers,[11,12] because the FWHM value was not calculated from the rocking curve but corresponds to $\delta 2\theta$. Moreover, the film thickness used in our measurements were small (typically 500 nm) which may be a cause for the larger FWHM value, as may the poor resolution of the diffractometer. It was found that layers grown at low ST had good crystallinity. However, polycrystalline growth was observed for ST smaller than 100 °C.

The growth rate is higher at low ST and decreases with increasing temperature in Fig. 3. The slope of the log growth rate scale versus the reciprocal ST has two different values at temperatures below and above 250 °C. The activation energies obtained for low and high temperature regions were -0.045 and -0.577 eV, respectively. The growth mecha-

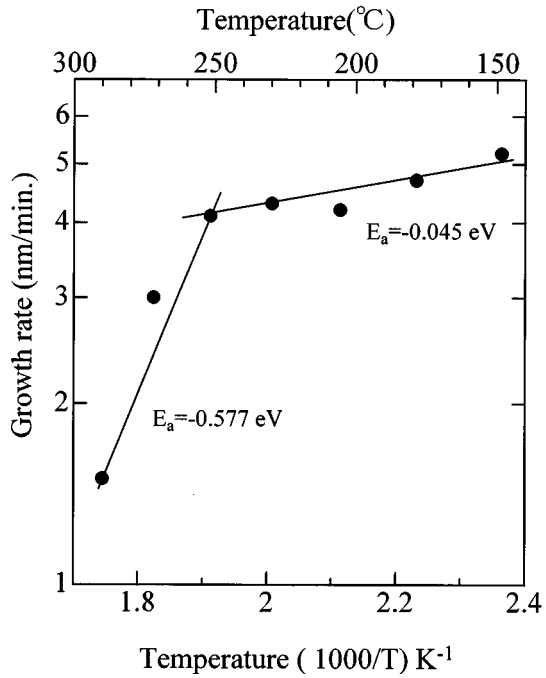


FIG. 3. Dependence of growth rate on substrate temperatures for CdTe films.

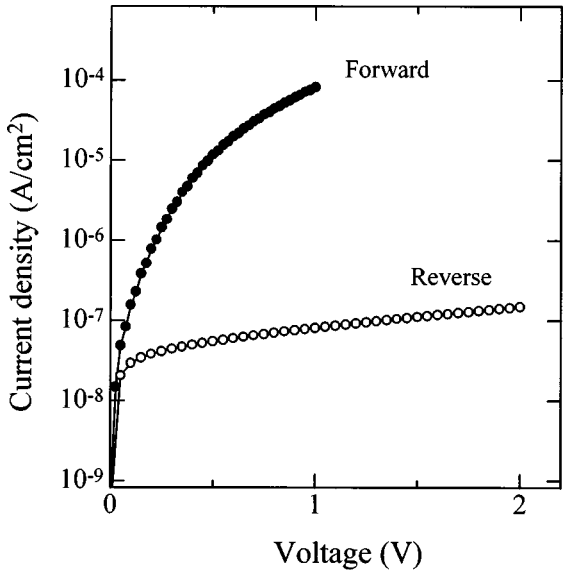


FIG. 4. $I-V$ characteristics of CdTe/n-GaAs heterojunction.

nism in this case is quite different than that of conventional MOCVD found in the literature.[12,19,20] However, in our system a similar growth mechanism has also been found in the case of ZnSe.[17,18,21] The detailed reason for this difference is still under investigation, but we consider that the application of plasma energy in addition to thermal energy for the film formation plays a role. Pai *et al.*[22] and Chin *et al.*[23] have also reported a negative activation energy for the film growth employing plasma in the CVD system. Although their investigations were not for the MOCVD system, the same mechanism should be applicable for the MOCVD employing plasma. In this aspect, the growth mechanism can be described by a surface adsorption and desorption controlled reaction. At low ST, the growth rate is high because of the high surface adsorption of the precursor. As the temperature increases, evaporation of weakly bonded species occur, which can be accounted for by the effect of hydrogen radicals. Hydrogen radicals, which help in film formation by the decomposition of the precursors, also have another effect: etching the growing film. As reported in the case of ZnSe for the same system,[21] the etching effect of hydrogen radicals increases with ST. Hence, the low growth rate at high temperature region can be ascribed by the predominant etching effect of hydrogen radicals.

B. Electrical characteristics

After studying the growth of CdTe in a wide range of ST, an appropriate growth temperature to obtain layers having mirrorlike surface and small FWHM value was determined. It was found that layers grown at a ST of 200 °C and a DMCd and DETe flow rate of 12 μmol/min each, exhibited better quality. Hence these epitaxial layers were used for the measurement of electrical properties.

The current–voltage ($I-V$) measurements were carried out by varying the temperature in the range from 294 to 355 K in a cryostat in which the sample was kept in vacuum in the dark condition. The electrical resistivity of CdTe layers was 9.2×10^6 Ω cm at room temperature, calculated by the van der Pauw method and the activation energy of the dark current was 0.64 eV. The conductivity of these films was confirmed to be p type from the potential profiling using four aluminum dots (Schottky contact) which were deposited collinearly on the sample.[24,25] Hence, the activation energy is considered to be the energy difference between the Fermi level and the top of the valence band.

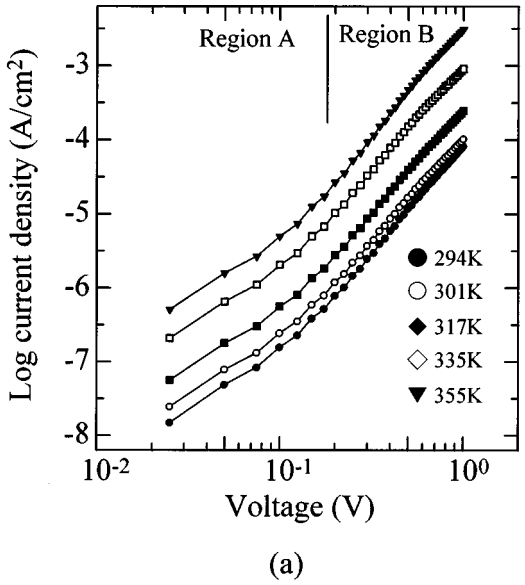
The forward and reverse dark current densities versus voltage ($I-V$) characteristics at room temperature for CdTe/n-GaAs heterojunction show good rectification property as depicted in Fig. 4. The reverse current characteristic somewhat saturates, whereas the forward characteristic deviates from simple exponential behavior. The temperature dependence of the forward current was measured and plotted in logarithmic scale as in Fig. 5(a). The forward current can be classified into two regions corresponding to the applied voltage (V). It was found that current increases exponentially in region A but nonexponentially in region B. In region A (less than 0.2 V), the gradient of the forward currents on a semilogarithmic plot is almost independent of temperature which has been redrawn as in Fig. 5(b). The forward current in this region (A) can be expressed by

$$I=I_0\ \exp(KV), \tag{1}$$

where K is a constant independent of temperature. This result shows that current in this region is dominated by a tunneling mechanism. The temperature dependence of the preexponential factor I_0 can be obtained by extrapolating the forward current curves to zero voltage, and the relation

$$I_0 \propto \exp(-E_a/kT) \tag{2}$$

holds between I_0 and temperature (T), where E_a is the activation energy of carrier conduction and found to be 0.55 eV



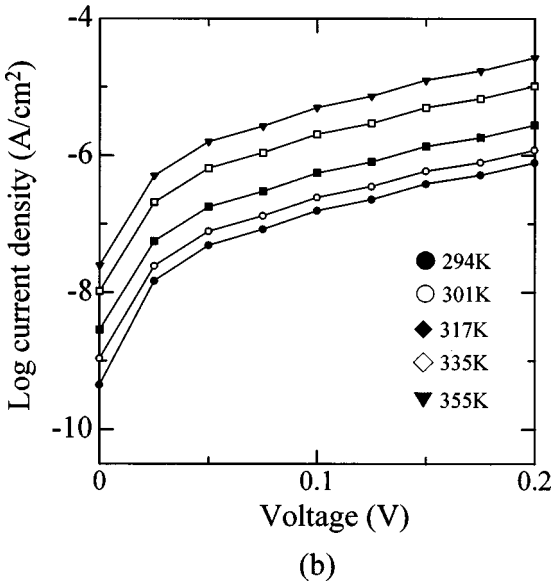


FIG. 5. (a) Forward $I-V$ characteristics at different temperatures, (b) characteristics in region A (redrawn).

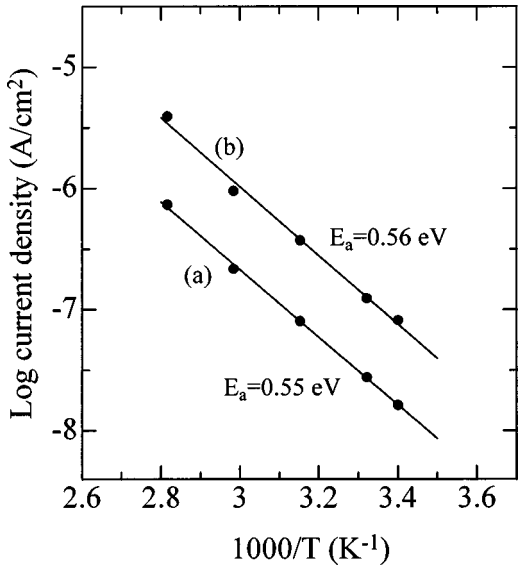


FIG. 6. Temperature dependence of (a) extrapolated values of I_0, (b) reverse currents at 1 V bias.

from Fig. 6. From this figure, I_0 does not change exponentially with T, but varies exponentially with $-1/T$ indicating that I_0-T characteristics are described by a multitunneling capture-emission (MTCE) model, but not by a multitunnel model.[4,26,27] This activation energy almost agreed with the energy difference between the Fermi level and the top of the valence band of CdTe. This confirms that in this region of low applied voltage, the hole capture process dominates the carrier transport mechanism. The forward current in this region can be explained by the MTCE model and can be attributed to the recombination of electrons tunneling from n-GaAs into the gap state in CdTe and holes captured by the gap states in CdTe.

In region B, the forward current is proportional to V^m, where m is an integer equal to 2 for $V \approx 0.2$ V and 3 above this voltage. From this observation it can be concluded that current is limited not by the bulk resistance of CdTe, but by the space charge limited current (SCLC). This SCLC may be due to electrons injected from n-GaAs which are captured by defect states in CdTe and holes injected from the Ohmic contact.

The energy band diagram of this heterojunction can be drawn as in Fig. 7. The following assumptions and values were used to draw this diagram. (a) The abrupt heterojunction model is valid for this heterojunction; (b) the conduction band discontinuity of the CdTe/n-GaAs heterojunction is assumed as 0.21 eV from the electron affinity difference of the two materials; (c) the band gap of GaAs is 1.42 eV and the energy difference Φ_c between the bottom of the conduction band and the Fermi level was theoretically calculated as 0.026 eV from the carrier concentration of GaAs; (d) the optical band gap of CdTe was measured to be 1.5 eV; (e) the energy level difference between the Fermi level and the top of the valence band was obtained as 0.64 eV from the activation energy, deduced from the temperature dependence of conduction current.

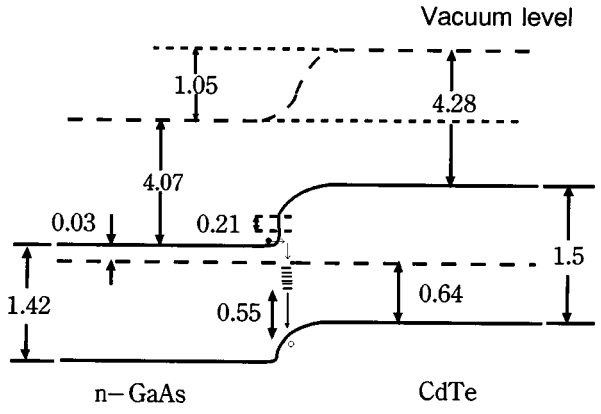


FIG. 7. Energy band diagram of n-GaAs/CdTe heterojunction.

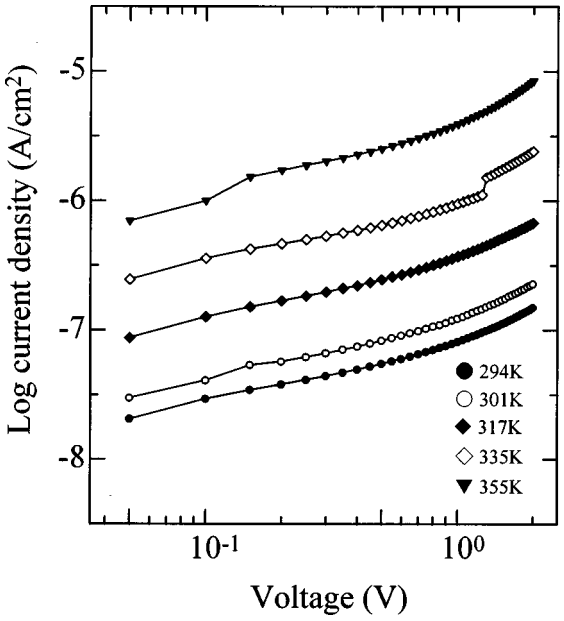


FIG. 8. Reverse $I-V$ characteristics at different temperatures.

Figure 8 gives the reverse current characteristics at various temperatures (the temperature dependence of the reverse current at the bias voltage of 1 V has been shown in Fig. 6, with an activation energy of 0.56 eV). The activation energies for the reverse and forward currents (I_0) were almost equal. The reverse current deviates from the usual saturation tendency (Fig. 8), but follows a nearly exponential dependence in the voltage range investigated (up to 2 V). In order to explain this phenomenon, $C-V$ measurements at 100 kHz have also been made. Figure 9 shows the $C-V$ characteristics in reverse bias condition, where $1/C^2$ is almost constant up to a voltage of 2 V and then increases more or less linearly. Moreover, the value of the depletion capacitance per unit area is almost equal to that of the capacitance per unit area determined only by the film dimension of CdTe, i.e.,

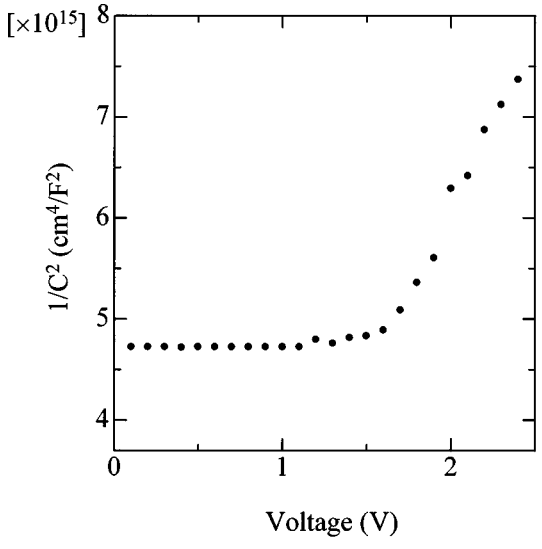


FIG. 9. Depletion capacitance as a function of applied reverse bias.

$$C=\varepsilon_0\varepsilon_s/t, \tag{3}$$

where ε_0 is the free space permittivity, ε_s is the dielectric constant of CdTe, and t is the film thickness. These results suggest that the depletion layer did not spread towards the n-GaAs side but the CdTe side was thoroughly depleted. The defect states existing at the interface of CdTe/n-GaAs as a result of the large lattice mismatch between GaAs and CdTe may be considered to obstruct the depletion layer enhancement in the n-GaAs side. These defect states are assumed to be acceptor type, filled with negative charges from the neutral level below the Fermi level, since n-GaAs has been used on the other side.[28] These negative charges prevented the spread of the depletion layer in n-GaAs as most of the bias applied was used to remove these charges.[29] Hence, the bias voltage was applied only to the CdTe layer. Therefore the reverse current is considered to be generated from the defect states in CdTe. This is consistent with the forward current model because of the same activation energies of the reverse and forward currents. For bias voltage greater than 2 V, these negative charges became sufficiently small and the depletion layer begins to spread in the n-GaAs side, hence the value of depletion capacitance changed. The effective impurity concentration deduced from the gradient of $1/C^2$ in the linear portion in Fig. 9 (around the region of 2 V and beyond) was 2.49×10^{16} cm^{-3} which is in close approximation with that of n-GaAs which is used here. This indicates that bias voltage in this region is mainly applied to n-GaAs. Therefore, it can be said that when increasing the bias voltage, the depletion region shifts from the CdTe side to the CdTe/n-GaAs interface and finally to the n-GaAs side.

For the device application, this heterojunction diode showed good rectification properties. However, it also had a large and nonsaturated reverse dark current generated from the defect states at the junction. These defect states are not only localized at the interface but might also be propagated towards CdTe layers. Photogenerated carriers can easily be lost in such states and it will be difficult to improve the heterojunction properties. Hence, for a device which works on minority carriers, the spread of the depletion region in between GaAs and CdTe should be avoided. This can be achieved by forming isotype heterojunction between GaAs and CdTe and then forming a p-n homojunction so that the structure will be n-GaAs/n-CdTe/p-CdTe. Presently, there will be no barrier potential between the GaAs and CdTe interface and hence the carriers can travel there without being affected.

IV. CONCLUSION

CdTe films were grown on n- and semi-insulating GaAs substrates over the temperature range of 150–300 °C by the radical assisted metalorganic chemical vapor deposition method. All the films grown were epitaxial and p type as confirmed from potential profiling. The growth rate was found to be high at low temperatures but decreased rapidly as the substrate temperature was increased. The carrier transport mechanism of the CdTe/n-GaAs heterojunction was studied in the low voltage range (<1 V). The forward current was characterized by multitunneling capture-emission

current in the low voltage region (≈ 0.2 V) and then by space charge limited current for voltages greater than 0.2 V. The reverse current was due to generation of current from interface defect states and was not a saturation current due to the diffusion of minority carriers. This heterojunction diode showed good rectification properties. However, it also had a large and nonsaturated reverse dark current generated from the defect states at the junction. This heterojunction alone is not suitable because of the high concentration of interface states. A suitable modification, like an isotype heterojunction between GaAs and CdTe before forming the *p*-*n* junction, is necessary to use this heterojunction as a minority carrier device.

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