Investigations of SiO_2/*n*-GaN and Si_3N_4/*n*-GaN insulator–semiconductor interfaces with low interface state density

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(Received 30 March 1998; accepted for publication 10 June 1998)

The electrical properties of electron beam (EB) evaporated silicon dioxide (SiO_2)/n-GaN, plasma enhanced chemical vapor deposited (PECVD) SiO_2/n-GaN, and PECVD silicon nitride (Si_3N_4)/n-GaN interfaces were investigated using high frequency capacitance–voltage measurements. Compositions of the deposited insulating layers (SiO_2 and Si_3N_4) were analyzed using x-ray photoelectron spectroscopy. Metal-insulator-semiconductor structures were fabricated on the metalorganic chemical vapor deposition grown n-type GaN layers using EB, PECVD grown SiO_2 and PECVD grown Si_3N_4 layers. Minimum interface state density (2.5×10^{11} eV^{-1} cm^{-2}) has been observed in the PECVD grown SiO_2/n-GaN interface when it was compared with EB evaporated SiO_2/n-GaN interface (5.3×10^{11} eV^{-1} cm^{-2}) and PECVD Si_3N_4/n-GaN interface (6.5×10^{11} eV^{-1} cm^{-2}). The interface state density (N_f) depends on the composition of deposited insulating layers. © *1998 American Institute of Physics.* [S0003-6951(98)04032-7]

Gallium nitride (GaN) has attracted considerable interest in electronic devices for applications in high temperature environment[1] with high power conditions[2] and in optoelectronic devices[3] for blue light emitting diodes (LED)[4] and UV Schottky barrier diodes because of its direct wide band gap and chemical stability. For the fabrication of high temperature electronic devices, it is necessary to realize metal-semiconductor (MS) and metal-insulator-semiconductor (MIS) contacts in a fundamental point of view. For many applications an MIS technology is desirable since it could provide very high dc input impedance, large gate voltage swings, normally off operation with high source-drain blocking voltages and higher temperature operation as a result of reduced gate leakage. Recently, Pd/GaN Schottky barrier diode has been fabricated and realized by Ishikawa *et al.*[5] using metal organic chemical vapor deposition (MOCVD) grown n-type GaN epilayers. Insulating layer SiO_2 were used for the fabrication of n-GaN MIS structure using plasma enhanced chemical vapor deposition (PECVD) system.[6,7] Casey *et al.*[6] have not observed measurable hysteresis in PECVD grown SiO_2/n-GaN MIS structure. The minimum interface state density (N_f) value 8.9×10^{11} eV^{-1} cm^{-2} has been observed by Casey *et al.*[6] Sawada *et al.*[7] have observed minimum N_f value 3×10^{11} eV^{-1} cm^{-2}. There is no report available for PECVD Si_3N_4/n-GaN and EB SiO_2/n-GaN MIS structures. In this letter, we have investigated the fabrication of MIS structure on MOCVD grown n-GaN layer using PECVD grown SiO_2, Si_3N_4 and EB deposited SiO_2.

A GaN epilayer was grown on sapphire (0001) substrate using the horizontal atmospheric pressure MOCVD method. Trimethylgallium (TMG) and NH_3 were used as source materials, and SiH_4 diluted in H_2 (10 ppm) was used as the n-type dopant. The sapphire substrate was heated at 1100 °C for 10 min in a stream of hydrogen. A 30-nm-thick GaN layer was deposited as the buffer at 530 °C. Then, the substrate was heated up to 1050 °C and a 2.4-μm-thick Si-doped GaN layer was grown on the GaN buffer layer with the free carrier concentration 1.1×10^{17} cm^{-3}.

The SiO_2 layer was grown using both EB evaporation at 150 °C and PECVD at 350 °C on silicon doped n-GaN epilayers, respectively. Evaporation rate 0.2 nm/s was maintained for all electron beam evaporation. The Si_3N_4 layer was also grown on n-GaN using PECVD at 300 °C. The sample was cleaned with organic solvents before insulating layer deposition. For all insulating layers, thickness was 100 nm. For the analysis of oxide and nitride composition, x-ray photoelectron spectroscopy (XPS) measurements were carried out on SiO_2 and Si_3N_4/n-GaN structures. XPS measurements were carried out using Alk$_\alpha$ x-ray (1486.6 eV) source with 600 μm spot-size.

MIS structures were fabricated on the SiO_2, Si_3N_4/n-GaN structure with guard-ring configurations. Metallization was performed by vacuum evaporation equipment with a cryopump as the main pump. After cleaning by organic solvents with ultrasonic agitation and lithographic masking, the deposited insulating layers (SiO_2/Si_3N_4) were removed using hydrofluoric acid for ohmic contact formation. Then titanium (50 nm) and aluminum (100 nm) were evaporated on n-GaN layer using the conventional lift-off technique. The sample was annealed at 900 °C for 40 s in nitrogen ambient in order to obtain good ohmic characteristics. Then, titanium (50 nm) and gold (100 nm) was evaporated on the insulating layer using the conventional lift-off technique. This metal layer will be acting as a gate electrode of MIS structure. Prior to the evaporation process, the sample was dipped in H_3PO_4+H_2SO_4 etchant for 1 min and there were no damages observed on the mask using this treatment. MIS structure gate area was 1.71×10^{-4} cm^{-2}. The schematic diagram of fabricated MIS structure is shown in Fig. 1. The fabricated MIS structures were characterized using high frequency (1 MHz) capacitance–voltage (C–V) measurements. All C–V measurements were carried using

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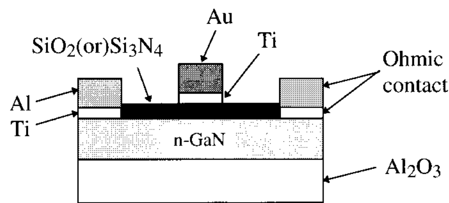

FIG. 1. Schematic diagram of fabricated n-GaN MIS structure.

HP4845A LCR bridge. $C-V$ data was recorded at 100 mV/s bias sweep rate.

Composition of the insulating layers (SiO_2 and Si_3N_4) were analyzed using XPS measurements. XPS spectra of silicon $2p$, oxygen $1s$ core level for both PECVD SiO_2 and Si_3N_4 and EB SiO_2 insulating layers are shown in Figs. 2(a) and 2(b). Reference values of the binding energy for Si $2p$ and O $1s$ core levels are 103.8 and 532.4 eV, respectively, for exact composition of SiO_2.[8] In our case, PECVD SiO_2 insulating layer Si $2p$ core level binding energy is slightly varied from reported binding energy. There were two peaks observed with the binding energy 102.33 and 100.33 eV. The observed binding energy composition of the insulating layer is Si_2O_3 and Si_2O, respectively.[8] For the case of EB-SiO_2, Si $2p$ core level has only one peak with binding energy 100.14 eV (Si_2O). This means silicon-rich oxide layer has been formed from EB evaporation. From the Fig. 2(b), it is clear that the O $1s$ core level binding energy for PECVD SiO_2 has two peaks at 529.04 and 531.43 eV but EB SiO_2 layer has only one peak at 529.58 eV. It is clear that the EB SiO_2 layer composition is silicon-rich. XPS spectra of Si $2p$ and N $1s$ core level for PECVD deposited Si_3N_4 insulating layer is shown in Figs. 2(a) and 2(c). Reference values of the binding energy for Si $2p$ and N $1s$ is 101.5 and 397.4 eV, respectively, for Si_3N_4.[9] In our case, Si $2p$ core level has one peak with binding energy 98.56 eV. N $1s$ core level has two peaks with the binding energies 396.07 and 393.82 eV. From this spectrum, it is clear that the insulating layer is slightly silicon rich. XPS results shows that PECVD grown SiO_2 insulating layer composition is in agreement with reported SiO_2 composition when compared with EB evaporated SiO_2 composition.

Typical C/C_i versus V plot for EB and PECVD deposited SiO_2/n-GaN and Si_3N_4/n-GaN MIS structures are shown in Fig. 3. From Fig. 3, it is clear that the fabricated MIS structures are having good hysteresis behavior with the voltage range -20 to $+20$ V. All the devices typically shows a charge injection-type hysteresis.[10] But Casey *et al.*[6] have not been observed measurable hysteresis. The measured breakdown voltage, hysteresis window width, interface state density (N_f), flat-band voltage shift (ΔV) and C_{FB}/C_i values are shown in Table I. ΔV was determined from the forward C/C_i versus V plot. Width of the hysteresis is small for PECVD grown SiO_2 compared with the other two insulating layer interfaces (Table I). This means, composition of the PECVD SiO_2 is good. Moreover the breakdown voltage of insulating layer is also high for PECVD grown SiO_2 (2.5×10^6 V cm^{-1}) compared with EB deposited SiO_2 (1.8×10^6 V cm^{-1}) which is in agreement with the reported values.[11]

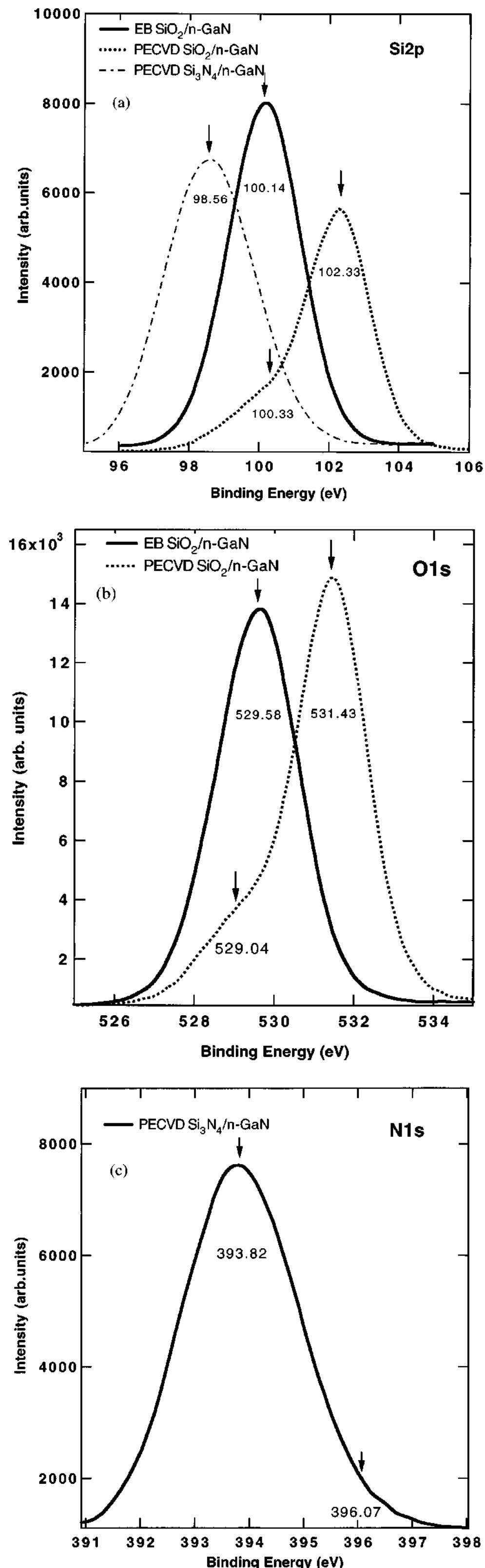

FIG. 2. XPS spectrum for GaN MIS structures. (a) Silicon $2p$ core level for PECVD SiO_2, EB SiO_2 and PECVD Si_3N_4/n-GaN structures, (b) oxygen $1s$ core level for PECVD SiO_2 and EB SiO_2/n-GaN structures, and (c) nitrogen $1s$ core level for PECVD Si_3N_4/n-GaN structures.

Interface state density (N_f) was calculated using Terman method[12] for all MIS structures. The following expression was used for the calculation of flat-band capacitance (C_{FB})

$$C_{FB}=(\epsilon_{GaN}/L_D)A,$$

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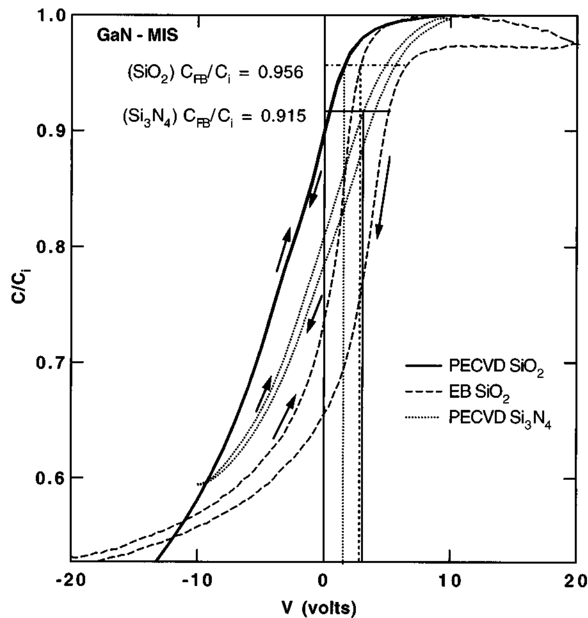

FIG. 3. C/C_i vs V plot for PECVD SiO_2/n-GaN, EB SiO_2/n-GaN, and PECVD Si_3N_4/n-GaN MIS structures. Vertical lines are representing the measured ΔV (see Table I). Horizontal lines are representing the values of C_{FB}/C_i.

where L_D is the Debye length $\sqrt{\epsilon_{GaN}k_BT/q^2N_d^+}$, A is the MIS capacitor cross-sectional area, ϵ_{GaN} is the relative dielectric constant of GaN (9.1), k_B is the Boltzman's constant, T is the absolute temperature (300 K), q is the electronic charge, and N_d^+ is the GaN doping concentration $(1.1 \times 10^{17}\ cm^{-3})$. Insulator capacitance C_i is calculated from $C_i = \epsilon_o \epsilon_i / d$ where ϵ_o and ϵ_i is the dielectric constant of free space and dielectric constant of insulating layer, respectively, and d is the thickness of the deposited insulating layer.

The calculated C_{FB}/C_i values are shown in Table I. From the calculated C_{FB}/C_i value, one can determine the flat band voltage shift (ΔV) from the C/C_i versus V plot (Fig. 3). Once the value ΔV is known, the interface state density (N_f) will be calculated using

$$N_f = \left(\frac{\Delta V - \phi_{MS}}{q} \right) C_i,$$

where

$$\phi_{MS} = \phi_M - \left(\chi + \frac{Eg}{2} + \phi_F \right).$$

ϕ_M is the metal work-function (4.55 eV), Eg is the energy band gap (3.4 eV), ϕ_F is the fermi potential, and χ is the electron affinity of GaN (4.1 eV). The calculated interface state density (N_f) values from C/C_i versus V plot (Fig. 3) are shown in Table I. Minimum interface state density value $(2.5 \times 10^{11}\ eV^{-1}\ cm^{-2})$ has been observed for PECVD grown SiO_2/n-GaN MIS structure when compared with EB-SiO_2/n-GaN and PECVD-Si_3N_4/n-GaN MIS structures. The observed interface state density is less than the reported values.[6,7] This has been correlated with the composition of insulating layer which is confirmed by XPS measurements.

TABLE I. N_f, C_{FB}/C_i, flat band voltage shift (ΔV), breakdown voltage and hysteresis window width values for SiO_2 and Si_3N_4.

Parameters	PECVD-SiO_2	PECVD-Si_3N_4	EB-SiO_2
N_f $(\times 10^{11}\ cm^{-2}\ eV^{-1})$	2.5	6.5	5.3
C_{FB}/C_i	0.956	50.91	0.956
$\Delta V(V)$	1.55	3.07	2.85
Breakdown voltage (V/cm)	2.5×10^6	1.5×10^6	1.8×10^6
Hysteresis window width (V)	0.14	0.89	3.69

In summary, SiO_2/n-GaN and Si_3N_4/n-GaN MIS structures were fabricated using EB and PECVD method. Breakdown voltage is high for PECVD SiO_2 layers when compared with EB deposited SiO_2 layers. Moreover, the interface state density is also small for PECVD grown SiO_2/n-GaN interface. Low interface state density have observed and reported first time in the literature for PECVD SiO_2/n-GaN interfaces. The reduction of interface state density is due to the insulating layer (SiO_2) composition. Very good correlation has been observed between interface state density and the composition of the insulating layer using high frequency $C-V$ and XPS measurements, respectively. MIS structures of EB SiO_2/n-GaN and PECVD Si_3N_4/n-GaN interfaces were investigated and reported first time in the literature. Considerable low interface state density has been observed on Si_3N_4/n-GaN interfaces.

The authors would like to acknowledge H. Takaki for XPS measurements. This work was partially supported by a Grant-in-Aid Scientific Research (c) (Grant No. 09650049) from The Ministry of Education, Science, Sports, and Culture.

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