Interface properties of SiO_2/n-GaN metal–insulator–semiconductor structures

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Electrical characterization of SiO_2/n-GaN metal–insulator–semiconductor structures fabricated on sapphire substrates was performed by using high-frequency pulsed capacitance–voltage and capacitance-transient techniques. Fast and slow capacitance transients are clearly seen after applying reverse voltages, reflecting thermal emissions of carriers from the SiO_2/GaN interface. The temperature dependence of the capacitance–voltage characteristics shows capacitance saturation in deep depletion (>15 V), which is probably associated with the slow capacitance transient. Deep-level transient spectroscopic measurements reveal two interface traps with activation energies of 0.71 and ~0.76 eV from the conduction band, corresponding to the fast and slow capacitance transients, respectively. Therefore, the observed capacitance saturation may be due to Fermi-level pinning induced by the latter interface trap.
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Gallium nitride (GaN) has been widely used in optoelectronic devices such as blue light-emitting diodes and laser diodes.[1,2] In addition, the electronic and structural properties of GaN also make it suitable for high-power and high-temperature electronic device applications. Recently, a number of GaN field-effect transistors (FETs) such as heterobipolar transistors, metal–oxide–semiconductor heterostructure FETs, and metal–insulator–semiconductor (MIS) FETs have been reported.[3–6] In particular, the GaN MIS structure equipped with an inversion mode as a minority-carrier channel is important for high-power switching devices since it would provide for lower leakage currents and reduce power consumption, enabling normally off operation with high blocking voltage even at high temperatures. A GaN MIS structure using a gate insulator comprised of deposited Ga_2O_3 (Gd_2O_3) has been reported by Ren *et al.*[5] Since then, various GaN MIS structures have been intensively investigated.[6–14] Their main purpose was to study gate insulator materials such as Ga_2O_3 (Gd_2O_3), AlN, SiO_2, Si_3N_4, $Pb(Zr,Ti)O_3$, and *p*-phenylenebenzobisthiazole. Inversion behavior in these structures has not yet been reported regardless of inversion being one of the key issues in view of power switching applications. Therefore, it is required to examine whether or not the GaN MIS structure has an inversion mode. In this letter, we report on an electrical investigation of interface properties of SiO_2/n-GaN MIS structures.

Epitaxial GaN films were grown by atmospheric-pressure metal–organic chemical-vapor deposition on *a*-plane sapphire substrates. First, a 20 nm AlN buffer layer was deposited at 400 °C, and then an undoped 3-μm-thick GaN layer was grown at 1050 °C, and sequentially, a Si-doped 1-μm-thick GaN layer was regrown at 1050 °C as an active layer. The GaN active layer had free-electron concentrations of $\sim 5\times 10^{17}$ cm^{-3}, mobilities of ~400 cm^2/V s, and threading dislocation densities of $2-5\times 10^9$ cm^{-2} as determined by room-temperature Hall-effect measurements and transmission electron microscopic observations. The Si concentration was also confirmed to be $\sim 4.5\times 10^{17}$ cm^{-3} by secondary ion mass spectrometry measurements. After growth, lateral dot-and-ring GaN MIS structures were fabricated as follows. First, a 100-nm-thick SiO_2 layer was deposited on the top surface of the GaN samples as a gate insulator by radio-frequency sputtering at nominal room temperature. The SiO_2 layer was selectively removed by wet etching using a photolithographic technique for Ohmic contact directly on the GaN active layer, and then Al metal was evaporated through a shadow mask to provide gate and Ohmic electrodes. The dot gate electrode was 500 μm in diameter, and was surrounded by the ring Ohmic electrode with a 10 μm gap. After metallization, the MIS samples were annealed at 450 °C for 30 min in nitrogen atmosphere.

The MIS structures were characterized by using a high-frequency pulsed capacitance–voltage ($C-V$) technique[15] instead of the conventional $C-V$ method to evaluate the time dependence of charging and discharging at the SiO_2/GaN interface. The measurements were performed in the dark at a frequency of 1 MHz with an ac modulation of 30 mV. On the pulsed $C-V$ measurements, one unit of the pulse pattern consists of two stages. After applying a 1 ms pulsed voltage of +15 V to approach an accumulation region temporarily, the bias voltage is sequentially applied and the capacitance is measured after a delay time t_d. The bias voltage and t_d are independently varied.

Figure 1(a) shows typical room-temperature $C-V$ curves for the fabricated MIS structures at t_d of 1×10^{-5}, 1, 5, and 30 s, respectively. Ideal $C-V$ curves with and without inversion mode are also shown. The bias voltage was swept

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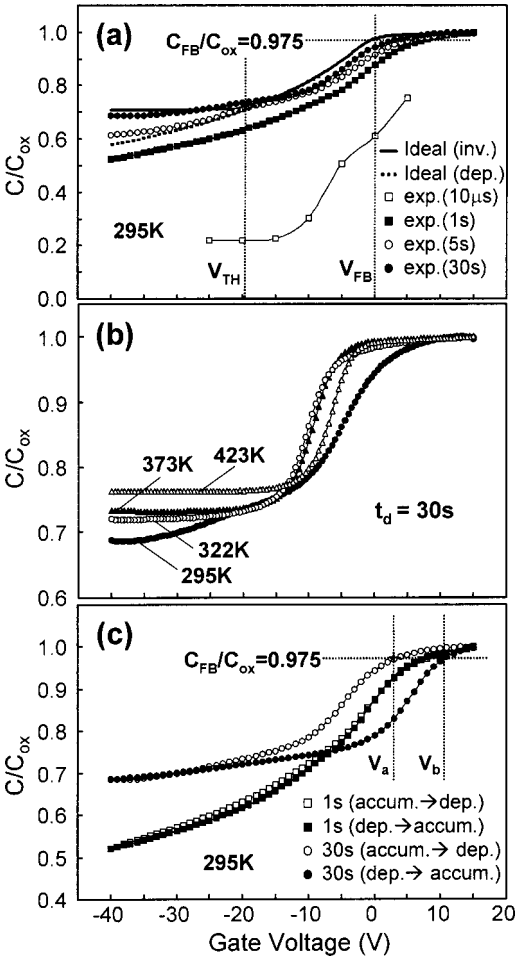

FIG. 1. (a) High-frequency pulsed $C-V$ curves at room temperature for the fabricated SiO_2/n-GaN MIS structures as the bias voltage is swept from +15 to −40 V at t_d of 1×10^{-5}, 1, 5, and 30 s, together with ideal $C-V$ data. (b) Temperature dependence of high-frequency pulsed $C-V$ curves at t_d of 30 s as the bias voltage is swept from +15 to −40 V. (c) High-frequency pulsed $C-V$ hysteresis curves at room temperature as the bias voltage is swept from +15 to −40 V and then back to +15 V at t_d of 1 and 30 s.

from +15 (accumulation) to −40 V (depletion). The t_d dependence of the measured $C-V$ curves is clearly seen; the capacitance in depletion significantly increases toward the ideal one with an increase of t_d. This capacitance transient is caused by thermal emission of carriers from the SiO_2/GaN interface in accordance with applying the bias voltage. In particular, the capacitance in deep depletion seems to be saturated for the long t_d. In addition, this capacitance saturation becomes clear with the rising of temperature for the long t_d, as shown in Fig. 1(b). In the room-temperature measured $C-V$ curve at t_d of 30 s [Fig. 1(a)], the threshold voltage is about −15 V. In the ideal $C-V$ curve, the flatband capacitance (C_{FB}/C_{ox}) is calculated to be 0.975. The flatband voltage (V_{FB}), which is the corresponding voltage of the C_{FB}/C_{ox}, gives a value of 3.85 V from the measured $C-V$ curve at t_d of 30 s. Thus, the flatband voltage shift (ΔV_{FB}) gives a fixed oxide charge density (N_f) of $\sim 9.4\times10^{11}$ $eV^{-1}\,cm^{-2}$. Figure 1(c) shows typical room-temperature $C-V$ hysteresis curves for the fabricated MIS structures at t_d of 1 and 30 s, respectively. Bias voltage was scanned back and forth between +15 and −40 V. No hysteresis is observed in the $C-V$ curve at t_d of 1 s, while a much

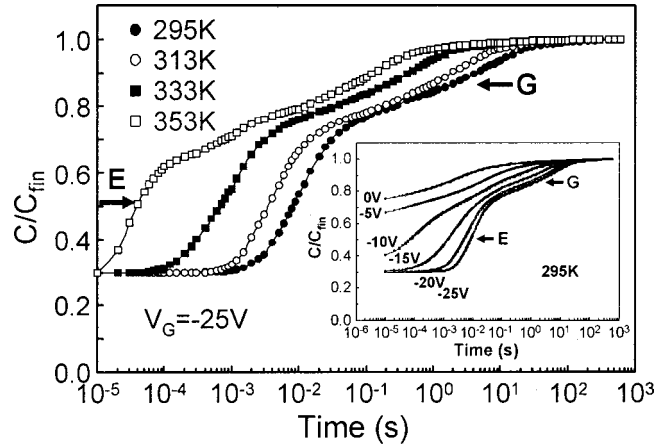

FIG. 2. Temperature dependence of capacitance transient for the fabricated SiO_2/n-GaN MIS structures after applying the bias voltage of −25 V. Inset shows the bias voltage dependence of the capacitance transient at room temperature.

larger increase of hysteresis windows is seen in the $C-V$ data at t_d of 30 s. This indicates charge exchange between the deep interface states and the bulk GaN. Here, V_a is V_{FB} when the bias voltage goes from accumulation to deep depletion and V_b is that when the voltage sweeps from deep depletion to accumulation. Compared with the $C-V$ data at t_d of 1 s, V_a and V_b shift toward negative and positive voltages, respectively, in the $C-V$ curve at t_d of 30 s. This implies the presence of numerous residual negative charges at the SiO_2/GaN interface. These interface states can be attributed to acceptor-like interface electron traps. $|V_a-V_b|$ is the total hysteresis window at flatband. The large window at t_d of 30 s is ~7.0 V, which corresponds to a total interface state density of at least $\sim 1.7\times10^{12}$ $eV^{-1}\,cm^{-2}$. Thus, upon applying reverse voltages toward strong inversion, a large number of interface traps may induce Fermi-level pinning at the SiO_2/GaN interface instead of actual hole inversion, which results in the observed capacitance saturation.[16,17]

To examine the capacitance transient in deep depletion, conventional capacitance–time ($C-t$) measurements were performed in the dark by using the pulsed $C-V$ technique as mentioned above. Figure 2 shows typical $C-t$ curves after applying the bias voltage of −25 V for the fabricated MIS structures at 295 (room temperature), 313, 333, and 353 K, respectively. C_{fin} means final capacitance. Fast and slow capacitance transients are clearly seen, which are labeled E and G, respectively. By combining with the measured $C-V$ characteristics in Fig. 1(a), both capacitance transients correspond to thermal emissions of carriers from the SiO_2/GaN interface states. As shown in the inset of Fig. 2, the capacitance significantly increases with an increase of reverse voltage for the fast capacitance transient E, whereas the capacitance variation remains small, independent of reverse voltage for the slow capacitance transient G. The relaxation time for both capacitance transients E and G becomes longer with increasing the reverse voltage, which is a typical characteristic of interface states. In particular, the capacitance transient G with a long relaxation time seems to be associated with the capacitance saturation in the $C-V$ characteristics, as mentioned in Figs. 1(a) and 2(b). Furthermore, the relaxation time for both capacitance transients E and G becomes shorter

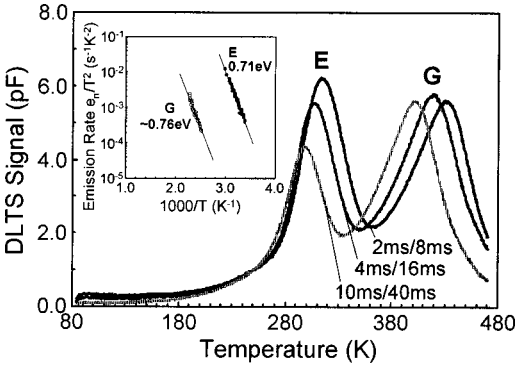

FIG. 3. Typical DLTS spectra at various rate windows t_1/t_2 for the fabricated SiO_2/n-GaN MIS structures after applying the bias voltage of -25 V. Inset shows the Arrhenius plots of the electron-emission rate.

in accordance with the rising of the temperature, which is in reasonable agreement with the theory of thermal carrier emission based on Shockley–Read–Hall statistics.

To estimate the activation energies for the carrier emissions of capacitance transients E and G, deep-level transient spectroscopy (DLTS) measurements were performed at temperatures between 85 and 475 K under the same condition of the $C-t$ measurements as mentioned above. Figure 3 shows typical DLTS spectra measured on the fabricated MIS structures at various rate windows t_1/t_2. The DLTS signal, $|C(t_1)-C(t_2)|$, is displayed for rate windows t_1 (ms)/t_2 (ms)$=2/8$, 4/16, and 10/40; the carrier emission rates are 231, 115.5, and 46.2 s^{-1}, respectively. The spectra reveal two dominant peaks at around 300 and 420 K, which correspond to capacitance transients E and G in Fig. 2, respectively. These peaks shift toward higher temperatures with an increase of the carrier-emission rate, which indicates that both peaks are assigned to deep centers at the SiO_2/GaN interface. In the measured temperature range, no other deep center could be detected. The thermal activation energies for these carrier emissions from deep centers E and G, were determined by an Arrhenius analysis of the emission rates, as shown in the inset of Fig. 3. The activation energies are estimated to be 0.71 and ~0.76 eV for the E and G centers, respectively, from the slopes of the lines fitted to these plots. Both energies are substantial for electron emission into the conduction band. Considering that the slow capacitance transient G is related to the capacitance saturation in the measured $C-V$ characteristics as mentioned above, the latter interface trap may dominantly induce the Fermi-level pinning effect at the SiO_2/GaN interface upon applying reverse voltages. Therefore, the interfacial trap density should be reduced in order to achieve the inversion mode in SiO_2/GaN MIS structures.

In summary, the interface properties of the SiO_2/n-GaN MIS structures have been investigated by using high-frequency pulsed $C-V$ and capacitance-transient techniques. The $C-V$ characteristics in deep depletion are found to be significantly subject to the thermal emission of carriers from two deep interface traps with activation energies of 0.71 and ~0.76 eV from the conduction band.

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