Interface properties of thermally oxidized *n*-GaN metal–oxide–semiconductor capacitors

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We report on the interface properties of thermally oxidized *n*-GaN metal–oxide–semiconductor capacitors fabricated on sapphire substrates. 100-nm-thick β-Ga_2O_3 was grown by dry oxidation at 880 °C for 5 h. From secondary ion mass spectrometry measurements, an intermediate Ga oxynitride layer with graded compositions is clearly observed at the β-Ga_2O_3/GaN interface. Capacitance–voltage measurements show a deep depletion feature and a low interface state density of $\sim 5.5\times 10^{10}$ eV^{-1} cm^{-2}. Additionally, no discrete interface traps can be detected by deep-level transient spectroscopic measurements. These results indicate that the surface Fermi level is unpinned at the β-Ga_2O_3/GaN interface, which may be associated with the presence of the interfacial Ga oxynitride layer. © *2003 American Institute of Physics.* [DOI: 10.1063/1.1536029]

GaN-based metal–oxide–semiconductor (MOS) devices are promising candidates for high-power and high-temperature electronic device applications.[1–4] In particular, the GaN MOS structure equipped with a surface inversion mode as a minority carrier channel is important for high-power switching devices since it would provide for lower leakage currents and reduce power consumption, enabling normally off operation with high blocking voltage even at high temperatures. However, the potential of these devices has been hard to garner because of inferior insulators and insulator/GaN interfaces. The first GaN MOS structure using a gate insulator comprised of deposited Ga_2O_3 (Gd_2O_3) was reported by Ren *et al.*[3] Since then, a number of approaches have been employed to develop an insulator/GaN system using either a GaN native oxide (β-Ga_2O_3) or a deposited insulator using Ga_2O_3 (Gd_2O_3), AlN, SiO_2, Si_3N_4, Pb(Zr,Ti)O_3, p-phenylenebenzobisthiazole, MgO, and Sc_2O_3.[5–17] In these studies, the bottleneck in developing GaN-based MOS field-effect transistors (FETs) using an insulator may be the large interface trap density on the order of 10^{12} eV^{-1} cm^{-2} which leads to the Fermi-level pinning at the GaN surface. Among them, a thermal dry-oxidation technique used for β-Ga_2O_3 formation has only limited success on GaN and has been proven to reduce the interface trap by more than one order of magnitude compared to the other deposition methods in addition to its simple and easy way.[6] β-Ga_2O_3 is generally known to have a wide band gap of 4.7 eV at room temperature.[18] Depending on growth conditions, β-Ga_2O_3 can be an insulator or a semiconductor; growing under oxidizing conditions results in insulating β-Ga_2O_3, while that grown under reducing conditions is conductive. Thus, the β-Ga_2O_3 layer grown by thermal dry oxidation might be expected to exhibit intrinsic properties with applications in dielectrics especially important for the MOS characteristics. However, indepth data on the electrical properties of the thermally oxidized GaN MOS structures have not yet been reported. The issue as to whether or not the GaN MOS structure easily has a surface inversion mode should depend significantly on interface properties of the MOS structures. Therefore, in this study, the interface properties of the thermally oxidized *n*-GaN MOS structures have been investigated electrically, and the results are compared to those of sputtered SiO_2/*n*-GaN MOS structures.

The epitaxial GaN films used in the experiments were grown by atmospheric pressure metalorganic chemical-vapor deposition on *a*-plane sapphire substrates. First, a 20 nm AlN buffer layer was deposited at 400 °C, and then Si-doped 3-μm-thick GaN layer was grown at 1050 °C as an active layer. The GaN active layer had free electron concentrations of $\sim 7.6\times 10^{17}$ cm^{-3} and mobilities of ~ 440 $cm^2/V\,s$ as determined by room-temperature Hall-effect measurements. The Si concentration was also confirmed to be $\sim 6.8\times 10^{17}$ cm^{-3} by secondary ion mass spectrometry (SIMS) measurements. After growth, lateral dot-and-ring β-Ga_2O_3/GaN MOS capacitors were fabricated by a thermal oxidation technique as follows. First, a 500-nm-thick Si layer was deposited on the top surface of the GaN sample as a mask material for thermal oxidation by rf sputtering at nominal room temperature. The GaN-samples were then thermally oxidized at 880 °C for 5 h in a dry oxygen ambient. The formation of monoclinic β-Ga_2O_3 was confirmed by x-ray diffraction (XRD). After removing the Si mask by a HF–HNO_3 solution (HF:HNO_3=20:3) for ohmic contact directly on the GaN active layer, Al metal was evaporated through a shadow mask to provide gate and ohmic electrodes. The dot gate electrode was 500 μm in diameter, and was surrounded by the ring ohmic electrode with a 50 μm gap. After metallization, the MOS samples were annealed at 450 °C for 30 min in an nitrogen ambient. As a reference, sputtered SiO_2/*n*-GaN MOS diode samples were also prepared with the SiO_2 thickness of ~ 100 nm by using conventional methodology.[16]

The MOS capacitors that we fabricated were characterized by using high-frequency capacitance–voltage ($C-V$) and capacitance transient ($C-t$) techniques to evaluate the time dependence of charging and discharging at the MOS

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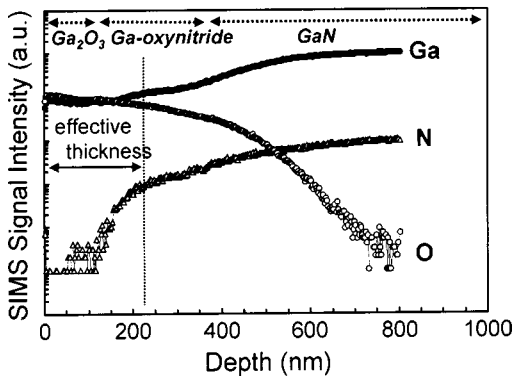

FIG. 1. SIMS profiles of Ga, N, and O atoms in the thermally oxidized β-Ga_2O_3/GaN MOS structure.

interface. The measurements were performed in the dark at a frequency of 1 MHz with an ac modulation of 30 mV. On the $C-V$ measurements, bias voltage is applied and the capacitance is measured after a delay time t_d. The bias voltage and t_d are independently varied. On the $C-t$ measurements, the time dependence of the capacitance under the reverse voltage of 25 V is measured after applying a 1-ms-pulsed voltage of $+10$ V to approach an accumulation region temporarily.

Figure 1 shows SIMS profiles of Ga, N, and O atoms in a thermally oxidized β-Ga_2O_3/GaN sample. A pure Ga oxide containing no N atoms can be clearly seen in the surface region of $\sim$100 nm where the GaN has been completely oxidized. This layer is probably identical with the monoclinic β-Ga_2O_3 layer as confirmed by XRD.[6] In addition, an ambiguous broad β-Ga_2O_3/GaN interface is also observed, that is, an intermediate Ga oxynitride layer with graded compositions is seen in the depth region of 100–400 nm from the surface. This Ga oxynitride layer is found to be formed inevitably under any thermal oxidation conditions. Thus, the thermal oxidation of GaN may be dependent on the combined effect of the interfacial reaction and the diffusion mechanism.

Figure 2(a) shows typical room-temperature $C-V$ curves for a thermally oxidized β-Ga_2O_3/GaN MOS sample at t_d of 1, 5, and 30 s, respectively. An ideal $C-V$ curve with an inversion mode is also shown. Bias voltage was swept from $+20$ (accumulation) to -30 V (depletion). By using a dielectric constant of $\varepsilon_r = 10.2$, an effective thickness of the insulator layer was estimated to be about 220 nm from the capacitance in the accumulation region, whose value is considerably thicker than that of the β-Ga_2O_3 layer. The t_d dependence of the measured $C-V$ curves is hardly ever seen; a small t_d dependence of the capacitance is only observed in the weak depletion region. Additionally, a deep depletion feature can be clearly observed in the depletion region regardless of t_d. In the ideal $C-V$ curve, the flatband capacitance (C_{FB}/C_{ox}) is calculated to be 0.978. The flatband voltage (V_{FB}) which is the corresponding voltage of the C_{FB}/C_{ox}, gives a value of $\sim$6.1 V from the measured $C-V$ curve at t_d of 30 s. Thus, the flatband voltage shift (ΔV_{FB}) gives a fixed oxide charge density (N_f) of $\sim 6.7 \times 10^{11}\ \mathrm{eV^{-1}\,cm^{-2}}$. Figure 2(b) shows typical room-temperature $C-V$ hysteresis curves for thermally oxidized β-Ga_2O_3/GaN MOS and the sputtered SiO_2/GaN MOS samples at t_d of 30 s, respectively. Bias voltage was scanned

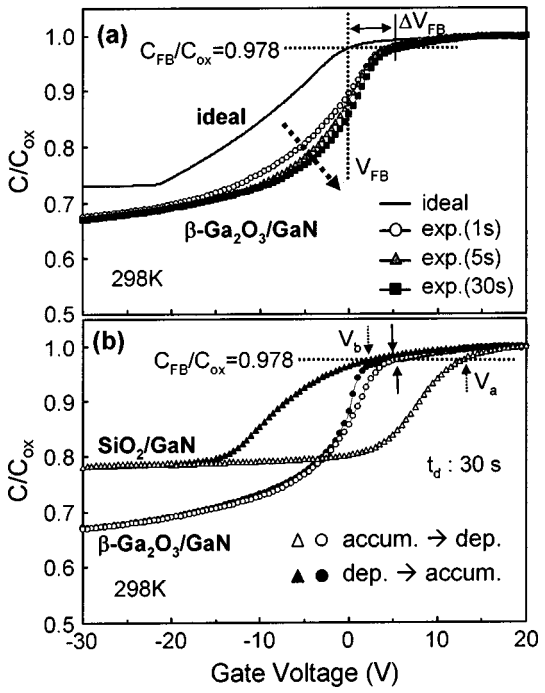

FIG. 2. (a) High-frequency $C-V$ curves at room temperature for the thermally oxidized β-Ga_2O_3/GaN MOS structure as the bias voltage is swept from $+20$ to -30 V at t_d of 1, 5, and 30 s, together with an ideal $C-V$ curve. (b) High-frequency $C-V$ hysteresis curve at room temperature for the thermally oxidized β-Ga_2O_3/GaN MOS and the sputtered SiO_2/n-GaN MOS structures as the bias voltage is swept from $+20$ to -30 V and then back to $+20$ V at t_d of 30 s.

back and forth between $+20$ and -30 V. A large hysteresis is observed for the sputtered MOS sample, while a very small hysteresis window is seen for the thermally oxidized MOS one. This hysteresis reflects charge exchange between the deep interface states and the bulk GaN. Here, V_a is the V_{FB} when the bias voltage goes from accumulation to deep depletion, and V_b is that when the voltage sweeps from deep depletion to accumulation. In the both samples, to a greater or less extent, the V_a and V_b shifted toward negative and positive voltages, respectively, with an increase of t_d. This implies the presence of residual negative charges at the MOS interface. These interface states can be attributed to acceptor-like interface electron traps. $|V_a - V_b|$ is the total hysteresis window at the flatband. The hysteresis windows for the thermally oxidized MOS and the sputtered MOS samples at t_d of 30 s are $\sim$0.5 and $\sim$9.1 V, which correspond to a total interface state density of at least $\sim 5.5\times10^{10}$ and $\sim 2.2 \times 10^{12}\ \mathrm{eV^{-1}\,cm^{-2}}$, respectively. The thermally oxidized MOS sample is found to show an incredibly lower interface state density than the sputtered MOS one. Thus, the deep depletion feature observed in the $C-V$ characteristics is due to this low density of interface states for the thermally oxidized β-Ga_2O_3/GaN MOS sample, which is clearly different from a situation of the sputtered SiO_2/GaN MOS sample where a large number of interface traps may induce the surface Fermi-level pinning at the MOS interface, resulting in the capacitance saturation observed in the deep depletion region of the $C-V$ curve.[16,19,20]

Figure 3 shows typical $C-t$ curves after applying the bias voltage of -25 V for a thermally oxidized β-Ga_2O_3/GaN MOS sample at 298, 323, 373, and 423 K,

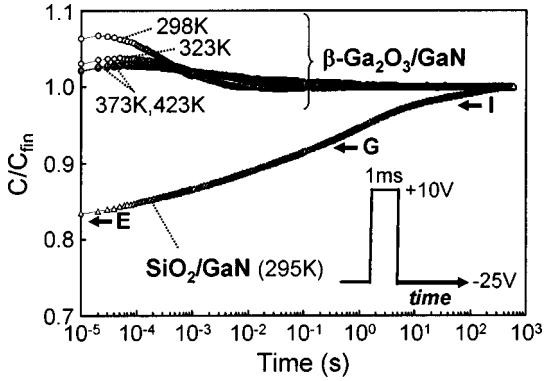

FIG. 3. Temperature dependence of capacitance transient for the thermally oxidized β-Ga_2O_3/GaN MOS structure after applying the bias voltage of -25 V. Room-temperature capacitance transient is also shown for the sputtered SiO_2/n-GaN MOS structure.

respectively. A $C-t$ curve for the sputtered SiO_2/GaN MOS sample at 295 K is also shown. C_{fin} means final capacitance. In the sputtered MOS sample, we can observe some fast and slow capacitance transients (E, G, and I) corresponding to the thermal emissions of carriers from the MOS interface states. On the other hand, in the thermally oxidized MOS sample, a small fast capacitance transient with the opposite code is seen, which seems to reflect the small t_d dependence of the $C-V$ characteristics observed in Fig. 2(a). In addition, the capacitance transient is independent of temperature, which implies that it is not a typical character of interface states. Thus, this small capacitance transient may be related to the presence of the intermediate Ga oxynitride layer with graded compositions at the MOS interface. That is, this phenomenon is considered to be caused by the time delay swelling of the depletion layer in the intermediate layer upon applying reverse voltages.

Figure 4 shows typical deep-level transient spectroscopy (DLTS) spectra measured on the thermally oxidized β-Ga_2O_3/GaN MOS and the sputtered SiO_2/GaN MOS samples under the same condition of the $C-t$ measurements. Here, the DLTS signal, $|C(t_1)-C(t_2)|$, is displayed for the rate window $t_1(\mathrm{ms})/t_2(\mathrm{ms})=10/20$; the carrier emission rate is 69.3 s^{-1}. In the sputtered MOS sample, some DLTS peaks are detected in the temperature range of 300–480 K, which correspond to the capacitance transients E, G, and I in Fig. 3, respectively. In particular, a main interface trap G is found to be discretely located at ~ 0.77 eV below the conduction band, from an Arrhenius analysis of the emission rates for the peak G. This interface trap probably induces the Fermi-level pinning effect at the SiO_2/GaN interface upon applying reverse voltages as just mentioned.[16] On the other hand, in the thermally oxidized MOS sample, no DLTS peaks can be detected. This result implies that there are no discrete interface traps at the thermally oxidized MOS interface. Therefore, the surface Fermi level is considered to be probably unpinned in the thermally oxidized β-Ga_2O_3/GaN MOS structures, which is significantly different from the situation of the sputtered SiO_2/n-GaN MOS structures. These distinguished interface properties of the thermally oxidized MOS structures may be probably associated with the presence of the interfacial Ga oxynitride layer.

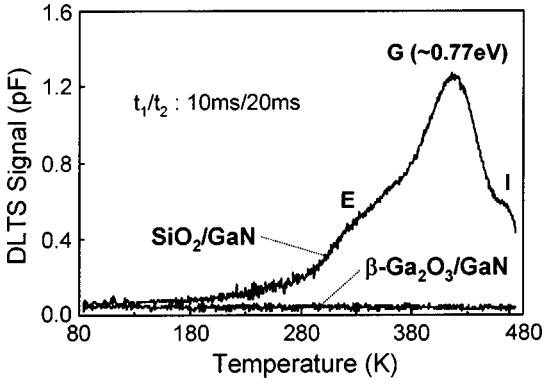

FIG. 4. Typical DLTS spectra at a rate window t_1/t_2 of 10 ms/20 ms for the thermally oxidized β-Ga_2O_3/GaN MOS and the sputtered SiO_2/n-GaN MOS structures after applying the bias voltage of -25 V.

In summary, the interface properties of the thermally oxidized β-Ga_2O_3/GaN MOS capacitors have been investigated electrically by using $C-V$ and capacitance transient techniques. From the $C-t$ and DLTS measurements, no discrete interface traps can be observed, which is in reasonable agreement with the deep depletion feature and the low interface state density of $\sim 5.5\times 10^{10}$ eV^{-1} cm^{-2} displayed by the $C-V$ measurements. Therefore, the surface Fermi level can probably be unpinned at the β-Ga_2O_3/GaN MOS structures fabricated by a thermal oxidation technique.

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