Electrical properties of thermally oxidized *p*-GaN metal–oxide–semiconductor diodes

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We report on the electrical properties of thermally oxidized *p*-GaN metal–oxide–semiconductor (MOS) diodes with n^+ source regions fabricated on sapphire substrates. The n^+ regions were selectively produced in Mg-doped GaN by Si+N coimplantation and subsequent annealing at 1300 °C, and then 100-nm-thick β-Ga_2O_3 was grown by dry oxidation at 880 °C for 5 h. Capacitance–voltage measurements at room temperature display a surface inversion feature with an onset voltage of $\sim$2.5 V and show an extremely low interface trap density less than 1×10^{10} eV^{-1} cm^{-2}. These results suggest that the thermally grown β-Ga_2O_3/*p*-GaN MOS structure is a promising candidate for inversion-mode MOS field-effect transistors. © *2003 American Institute of Physics.* [DOI: 10.1063/1.1567811]

GaN-based metal–oxide–semiconductor (MOS) structures using a number of gate dielectrics such as Ga_2O_3 (Gd_2O_3), AlN, SiO_2, Si_3N_4, and Pb(Zr,Ti)O_3 have been extensively investigated for use in high-power and high-temperature electronic device applications.[1–15] In particular, the MOS structure equipped with a surface inversion mode is important for high-power switching devices because it would provide for lower leakage currents and reduce power consumption, enabling normally off operation with high blocking voltage even at high temperatures. The GaN MOS structure is generally known to show no surface inversion due to the extremely slow thermal generation of minority carriers caused by the wide band gap of 3.4 eV.[6] Recently, Kim *et al.* have reported that MgO/*p*-GaN and Sc_2O_3/*p*-GaN gate-controlled MOS diodes with n^+ source regions show inversion behavior at room temperature.[16,17] In their reports, the selective-area Si-implanted regions play an effective role to provide an external source of minority carriers. However, the bottlenecks in these diodes may be a large interface trap density on the order of 10^{12} eV^{-1} cm^{-2} and poor electrical activation of the Si-implanted regions, resulting in the large onset voltages of surface inversion. Regarding interface states, thermal dry oxidation of GaN is known to be effective in reducing the interface trap at the β-Ga_2O_3/GaN MOS interface.[4,14] In our previous study, the thermally grown β-Ga_2O_3/*n*-GaN MOS structures have been proven to display a low interface trap density on the order of 10^{10} eV^{-1} cm^{-2}.[15] In addition, an improvement of *n*-type implantation-doping characteristics for the n^+ source is needed to form a satisfactory n^+p junction under the gate insulator. From this point of view, we have also reported that coimplantation of Si+N and subsequent annealing at high temperatures enhance electrical *n*-type activation and structural properties of the implanted regions, based on a site-competition effect.[18–20] Thus, the thermally oxidized *p*-GaN MOS structures with n^+ source regions fabricated by using thermal dry oxidation and Si+N coimplantation techniques might be expected to garner their outstanding potential.

β-Ga_2O_3 has a wide band gap of 4.7 eV at room temperature and a dielectric constant of 10.2–14.2.[21] Therefore, thermally grown β-Ga_2O_3 layer is expected to exhibit intrinsic properties with applications in dielectrics especially important for GaN MOS devices. The issue as to whether or not the β-Ga_2O_3/GaN MOS structures easily have a surface inversion mode should depend on their interface properties. However, in-depth data on the electrical properties of the thermally oxidized *p*-GaN MOS structures have not yet been reported. In this study, we have fabricated thermally oxidized *p*-GaN MOS diodes with n^+ source regions by combining Si+N coimplantation and thermal dry oxidation techniques, and have electrically investigated their interface properties.

The epitaxial Mg-doped GaN (GaN:Mg) films used in these experiments were 2.5 μm thick. They were grown on *a*-plane sapphire substrates by atmospheric pressure metalorganic chemical-vapor deposition at 1130 °C, with a predeposited 20 nm AlN buffer layer grown at 420 °C. The Mg concentration of the as-grown GaN:Mg layers was determined to be $\sim5\times10^{18}$ cm^{-3} by secondary ion mass spectrometry (SIMS) measurements. After growth, activation annealing was performed at 700 °C for 10 min in flowing N_2, resulting in the free hole concentration of $\sim2.5\times10^{16}$ cm^{-3} as confirmed by room-temperature Hall-effect measurements. Then, thermally oxidized *p*-GaN MOS diodes with n^+ source regions were fabricated as follows. A schematic of the complete MOS diode is shown in Fig. 1. Prior to Si+N coimplantation, a 1-μm-thick Ni layer was selectively deposited as a mask material for the implantation on the top surface of the samples by electron-beam evaporation. The GaN samples were implanted using pure N_2 and SiF_4 gases as the sources of the $^{14}N^+$ and $^{28}Si^+$ species, respectively, to create the n^+ source regions in GaN:Mg. First, multiple step N implantation was performed; the N

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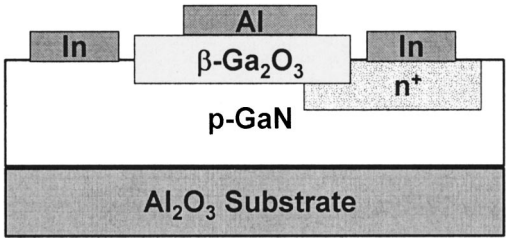

FIG. 1. Schematic cross section of thermally grown β-Ga_2O_3/p-GaN MOS diode with an n^+ source region.

ions were implanted at 240, 180, 120, 60, and 20 keV with dosages of 1.8×10^{14}, 6×10^{13}, 8×10^{13}, 7.5×10^{13}, and 3×10^{13} cm^{-2}, respectively, to produce a mean N concentration of 1×10^{19} cm^{-3} to a depth of ~0.35 μm from the GaN surface. Multiple Si implantation was then performed; the Si ions were implanted at 360, 200, 120, 60, and 30 keV with dosages of 2.5×10^{14}, 9×10^{13}, 5.3×10^{13}, 2.8×10^{13}, and 1.4×10^{13} cm^{-2}, respectively, to produce a mean Si concentration of 1×10^{19} cm^{-3} to a depth of ~0.35 μm. Here, the N/Si ratio was kept ~1 for an optimum doping.[18,19] All the implants were carried out at room temperature, with an incident angle 7° off the surface normal. After implantation, the Ni layer was removed and then a 500-nm-thick SiO_2 capping layer was deposited on the top surface of the implanted samples by rf sputtering at room temperature to provide an encapsulation cap for the subsequent implant activation annealing. All the samples were annealed at 1300 °C for 5 min in flowing N_2 gas. From the room-temperature Hall-effect measurements, the free electron concentration of the n^+ source regions was confirmed to be $\sim4.7\times10^{18}$ cm^{-3}. After removing the SiO_2 capping layer, a 500-nm-thick Si layer was selectively deposited on the top surface of the GaN samples as a mask material for thermal oxidation by rf sputtering at room temperature. The GaN samples were then thermally oxidized at 880 °C for 5 h in flowing dry O_2 gas. The formation of monoclinic β-Ga_2O_3 layer was confirmed by x-ray diffraction and its thickness was ~100 nm from SIMS measurements. After removing the Si mask by a $HF–HNO_3$ solution ($HF:HNO_3=20:3$), Al metal was evaporated through a shadow mask to provide gate electrodes. The dot gate electrode was 500 μm in diameter. After metallization, the MOS samples were annealed at 500 °C for 30 min in flowing N_2 gas. Finally, In metal was deposited at 200 °C directly on the GaN:Mg active layer and the n^+ source for ohmic electrodes. As a reference, thermally oxidized p-GaN MOS structures without any n^+ source regions were also fabricated by using the same methodology as stated earlier.

The MOS structures that we fabricated were characterized by using capacitance–voltage ($C–V$) measurements at room temperature. The $C–V$ measurements were performed under a grounded source contact condition in the dark with an ac modulation level of 30 mV and frequencies ranging from 100 Hz to 10 MHz. On these $C–V$ measurements, gate bias voltage is applied and the capacitance is measured after a delay time t_d.[13,15] The bias voltage and t_d are independently varied.

Figure 2 shows room-temperature $C–V$ curves at a frequency of 1 MHz for a thermally grown β-Ga_2O_3/p-GaN MOS sample with an n^+ source region at t_d of 1 and 30 s, respectively. An ideal $C–V$ curve is also shown. Gate bias voltage was scanned back and forth between -5 and 5 V. In the ideal $C–V$ curve, the flatband capacitance (C_{FB}/C_{ox}) is calculated to be 0.855 by using a dielectric constant of 10.2. The flatband voltage (V_{FB}) which is the corresponding voltage of the (C_{FB}/C_{ox}), gives a value of ~0.56 V from the measured $C–V$ curve at t_d of 30 s. Thus, the flatband voltage shift (ΔV_{FB}) gives a negative fixed oxide charge density (N_f) of 1.3×10^{10} eV^{-1} cm^{-2}. In addition, the t_d dependence of the measured $C–V$ curves is hardly observed in the flatband and depletion regions. That is, the total hysteresis window at the flatband is found to be very small for the measured $C–V$ curves under different sweep directions, regardless of t_d. Even though the frequency dependence of the accumulation capacitance is considered, the total interface trap density is estimated to be less than 1×10^{10} eV^{-1} cm^{-2}.[16,17] Furthermore, the measured $C–V$ curves show capacitance saturation in the depletion region and present a large deviation from the ideal $C–V$ curve. Additionally, the referenced MOS sample without any n^+ source region was found to show a deep depletion feature. These results indicate that the capacitance saturation is probably associated with the surface inversion induced by the injection of minority carriers from the n^+ source region. Thus, we can say that the capacitance saturation observed is a typical feature of the surface inversion in the high-frequency $C–V$ characteristics. A sudden and small capacitance drop is also observed at ~2.5 V in the measured $C–V$ curves when the bias voltage is swept from accumulation to depletion, as shown in Fig. 2. This value may be an onset voltage V_{on} of the surface inversion for this MOS diode. On the other hand, the accumulation capacitance of the measured $C–V$ characteristics seems to depend on the t_d and sweep direction. A large hysteresis is observed in the accumulation region of the measured $C–V$ curves at t_d of 1 s under different sweep directions. This hysteresis dwindles away and the accumulation capacitance becomes slightly smaller than a value expected from the ideal $C–V$ curve with an increase of t_d. These results indicate the observed variation in accumulation capacitance may be related to the presence of defects inside of the β-Ga_2O_3 layer.

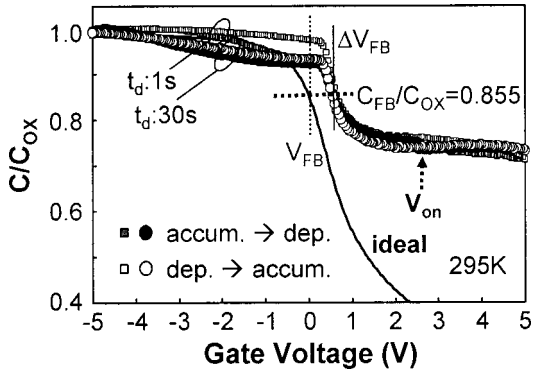

FIG. 2. High-frequency $C–V$ hysteresis curves at room temperature for thermally grown β-Ga_2O_3/p-GaN MOS diode with an n^+ source region as the gate bias voltage is swept from -5 to $+5$ V and then back to -5 V at t_d of 1 and 30 s, together with an ideal $C–V$ curve.

Figure 3(a) shows representative room-temperature $C–V$ curves at frequencies of 1, 2, 3, and 10 kHz for a thermally grown β-Ga_2O_3/p-GaN MOS sample with an n^+

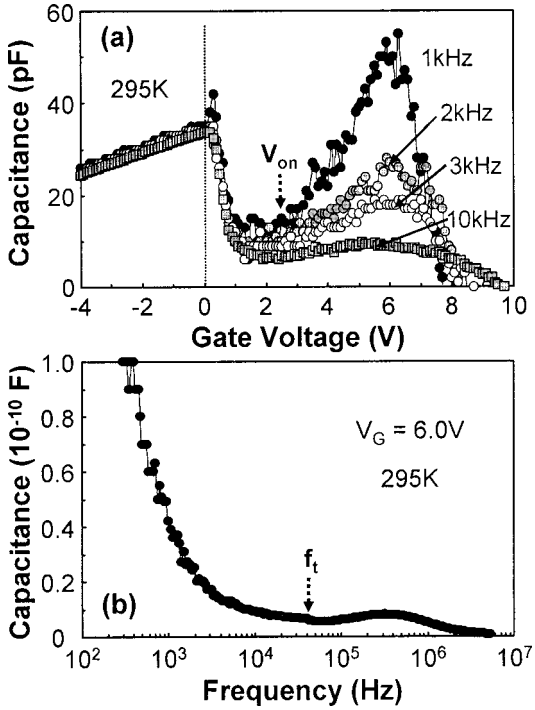

FIG. 3. (a) Room-temperature $C-V$ curves at frequencies of 1, 2, 3, and 10 kHz for thermally grown β-Ga_2O_3/p-GaN MOS diode with an n^+ source region as the gate bias voltage is swept from -4 to $+10$ V at t_d of 30 s. (b) Frequency dependence of inversion capacitance at bias voltage of 6 V at room temperature for thermally grown β-Ga_2O_3/p-GaN MOS diode with an n^+ source region.

source region at t_d of 30 s, respectively. Gate bias voltage was swept from -4 V (accumulation) to $+10$ V (depletion). An increase in capacitance can be clearly seen when the bias voltage is applied towards the depletion region, regardless of measurement frequency. This phenomenon is a typical behavior of the surface inversion in the low-frequency $C-V$ characteristics. As shown in Fig. 3(b), the inversion capacitance is found to increase significantly with decreasing measurement frequency. This is probably caused by the incomplete ionization of Mg dopants in the GaN:Mg active layer.[22–26] That is, as the measurement frequency is decreased, the Mg deep acceptors can follow the frequency voltage modulation, resulting in an improvement of the minority carrier injection from the n^+ source region. This inversion behavior could be seen even at 200 °C. The V_{on} of the surface inversion is $\sim$2.5 V, which value seems to be independent of measurement frequency. The V_{on} of the low-frequency $C-V$ characteristics is also in good agreement with that of the high-frequency characteristics as stated earlier. The $C-V$ characteristics are likely to be classified into low- and high-frequency features at a frequency of $\sim$40 kHz, which characteristic frequency may correspond to the impurity transition frequency f_t of the Mg deep acceptors in the GaN:Mg active layer, as shown in Fig. 3(b).[24–26] In addition, a decrease of capacitance in the accumulation region is due to the poor ohmic contact to the GaN:Mg layer.

The effective V_{on} of the surface inversion is estimated to be $\sim$2 V from the ΔV_{FB}. This V_{on} obtained in this study is apparently much smaller than the values in the previous literature.[16,17] This reduction in V_{on} is considered to be caused by the enhanced implantation-doping characteristics attained by the Si+N coimplantation and subsequent activation annealing at high temperatures in addition to the extremely low interface trap density at the β-Ga_2O_3/p-GaN MOS interface. Here, Si activation efficiency of the n^+ source region is estimated to be $\sim$47% from the implanted Si concentration of 1×10^{19} cm^{-3}, which value is the same level as our previously reported value.[18] As a result, an improvement in characteristics of the n^+p junction under the β-Ga_2O_3 layer gears up for the minority carrier injection from the n^+ source region. Moreover, the results obtained in this study suggest that the thermally grown β-Ga_2O_3/p-GaN MOS structure is a promising candidate for inversion-mode MOS field-effect transistors.

In summary, the thermally grown β-Ga_2O_3/p-GaN MOS structures with the n^+ source regions have been fabricated by combining Si+N coimplantation and thermal dry oxidation techniques. From the frequency dependence of $C-V$ characteristics at room temperature, the surface inversion with the V_{on} of $\sim$2.5 V can be clearly seen. This small V_{on} is considered to be attained by the enhanced implantation-doping characteristics and the extremely low interface trap density less than 1×10^{10} eV^{-1} cm^{-2} at the β-Ga_2O_3/p-GaN MOS interface.

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