

# Interface recombination velocity of silicon-on-insulator wafers measured by microwave reflectance photoconductivity decay method with electric field

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The interface recombination velocity of silicon-on-insulator (SOI) wafers was measured by the microwave-reflectance photoconductivity-decay method. The carrier lifetime was obtained with interface recombination suppressed by applying voltage between the SOI layer and the substrate. The interface recombination velocity was then estimated by comparing two lifetime values with and without voltage application. The velocity is from 500 to 1800 cm/s, relatively large as for thermally oxidized Si/SiO<sub>2</sub> interfaces. © 2003 American Institute of Physics. [DOI: 10.1063/1.1597988]

Thin silicon-on-insulator (SOI) wafers are attracting much attention as high-performance large-scale integrated circuit substrates, because of high speed and low power dissipation due to small parasitic capacitance and ease of device isolation. However, in many cases, characteristics of devices produced on an SOI wafers are greatly sensitive to properties of the SOI/buried-oxide (BOX) interface. For example, the threshold voltage of a metal–oxide–semiconductor field-effect transistor (MOSFET) produced on an SOI is sensitive to the interface state density.<sup>1</sup> Therefore, the interface characterization is very important for fabrication of devices on thin SOI wafers. Until now, many studies of interface characterization have been performed: Yoshida *et al.* obtained a wafer map of interface trap density for SOI wafers by the scanning-charge-pumping method using a contactless gate electrode.<sup>2</sup> Takahashi *et al.* measured the fixed-charge density in the BOX and the interface trap density distribution in the band gap using capacitance–voltage characteristics of the buried MOS diode in SOI wafers.<sup>3</sup> Yang *et al.* measured the interface trap density distribution in the band gap from the measurement of threshold voltage of SOI MOSFETs.<sup>1</sup> However, all these methods are based on the characterization of the devices fabricated on the SOI wafer. As a wafer characterization method, contactless, nondestructive, and high-throughput techniques are desirable.

In this study, in order to characterize interface properties of SOI wafers, we used the microwave-reflectance photoconductivity-decay ( $\mu$ -PCD) method, which is used extensively for the carrier lifetime measurement of silicon. The basic  $\mu$ -PCD measurement can be performed without any contact because the microwave is used as a probe to observe the decay of the carrier. Therefore, it meets the aforementioned requirements. In addition, the  $\mu$ -PCD method also has the advantages of high speed, high sensitivity, and simplicity. In our previous work, using the  $\mu$ -PCD method with voltage applied between the glass electrode and the silicon wafer, we performed the lifetime measurement controlling the surface recombination.<sup>4</sup> In this work, we control the interface recombination of the SOI/BOX interface by applying voltage between the SOI top layer and the substrate, and we evaluate interface recombination velocity for SOI wafers by analyzing

the data of the carrier lifetime with and without voltage application.

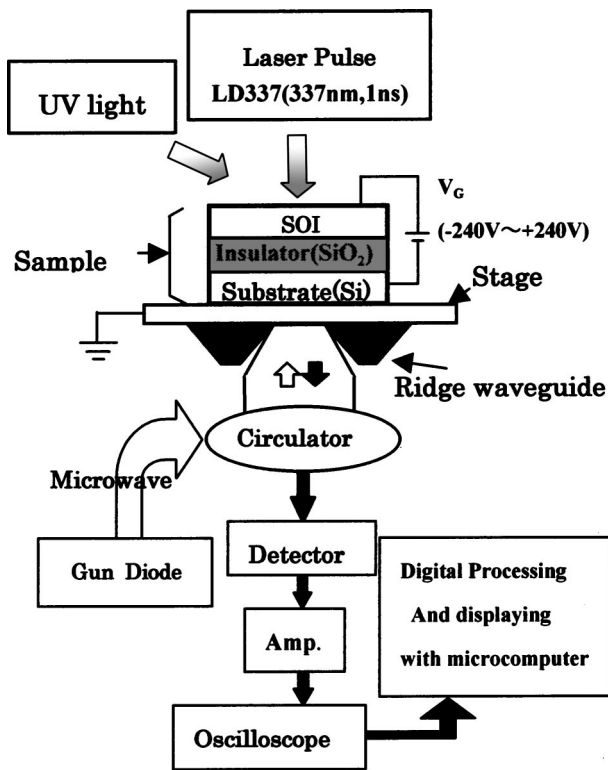
Samples used in this study are three bonded SOI wafers (samples A, B, and C). The wafer properties (conduction type, resistivity, SOI layer thickness, and BOX thickness) are listed in Table I. The system of the  $\mu$ -PCD experiment is schematically shown in Fig. 1. The voltage from  $-300$  to  $300$  V is applied between the SOI top layer and the substrate. The surface of an SOI wafer is irradiated with the pulse laser. The laser light used in this experiment is a nitrogen laser (wavelength 337 nm, pulse width 1 ns, penetration depth into Si 0.03  $\mu$ m). The laser light intensity is modified by optical filters, and the photon density per pulse is in a range from  $7 \times 10^{13}$  cm<sup>-2</sup> (for sample A) to  $2.8 \times 10^{14}$  cm<sup>-2</sup> (for sample B). The excitation density per unit volume is on the order of  $10^{17}$  cm<sup>-3</sup>. The 10-GHz microwave is irradiated simultaneously to the back side. The incident microwave penetrates the wafer, and is partly reflected by excess carriers generated by the irradiation. By measuring reflection intensity, the decay process of the excess carriers is observed.

UV light irradiation has been reported to suppress the surface recombination.<sup>5,6</sup> The nitrogen laser used in the present experiment is a UV laser and is effective to suppress it. The surface recombination velocity needs to be constant during the measurement. To saturate the UV irradiation effect and to prevent the variation of the surface recombination velocity, UV light irradiation is performed for 2 min before the start of a series of the lifetime measurements and for 1 min between the respective measurements. The UV light source used is a deuterium lamp (maximum intensity wavelength 230 nm).

By applying voltage as shown in Fig. 2, the SOI/BOX interface of the sample wafer can be changed between accu-

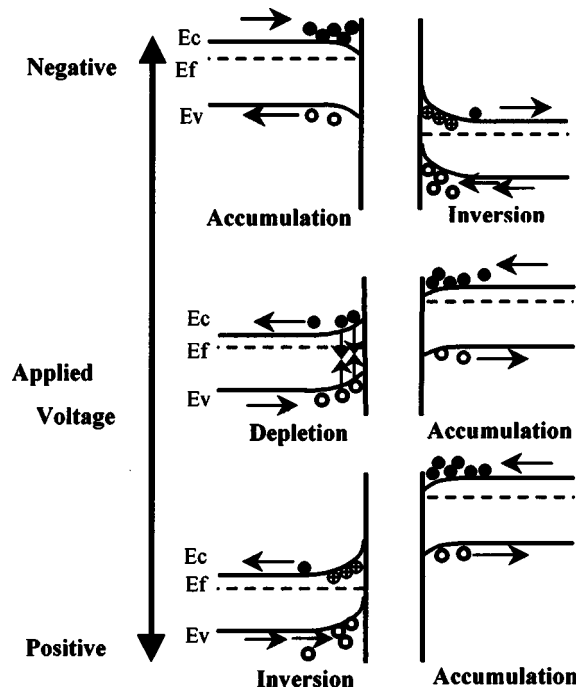
TABLE I. SOI wafers used in the experiment.

Sample	Type	Resistivity ( $\Omega$ cm)	SOI layer thickness ( $\mu$ m)	BOX thickness ( $\mu$ m)
A	<i>n</i>	8–12	1.5	0.5
B	<i>n</i>	2–12	20.5	0.45
C	<i>p</i>	14–22	10.0	0.6

FIG. 1. Schematic illustration of the  $\mu$ -PCD measurement system.

mulation and inversion through depletion. When the interface is in the depletion condition, the interface recombination velocity is the largest because the number of minority and majority carriers become comparable. Under the accumulation and inversion conditions, the interface recombination velocity becomes smaller because of a shortage of minority and majority carriers, respectively. Thus, by applying voltage, we can control the interface recombination.

The lifetime  $\tau$  without voltage application is expressed as

FIG. 2. Relationship between the interface band alignment and the applied voltage ( $n$ -type SOI).

$$\frac{1}{\tau} = \frac{1}{\tau_b} + \frac{S_a}{d} + \frac{S_b}{d}, \quad (1)$$

where  $\tau_b$  is the bulk lifetime and  $S_a$  and  $S_b$  are the recombination velocities at the surface and the interface, respectively, and  $d$  is the SOI thickness. When the interface is changed into accumulation or inversion by the voltage application, the interface recombination is suppressed and the lifetime is increased. If the voltage is high enough, the interface recombination is completely suppressed and  $S_b$  becomes null. The increase in the lifetime stops and the lifetime  $\tau'$  is given by

$$\frac{1}{\tau'} = \frac{1}{\tau_b} + \frac{S_a}{d}, \quad (S_b = 0). \quad (2)$$

From the difference between  $\tau$  and  $\tau'$ ,  $S_b$  is evaluated.

Figure 3(a) shows the normalized decay curves of the excess carrier concentration at various voltages applied to the SOI top layer of sample A, which is  $n$ -type and is the thinnest of the three samples (SOI top layer thickness  $1.5 \mu\text{m}$ ). The carrier lifetime increased with increasing negative voltage applied to the SOI side, and saturated at voltages above  $180 \text{ V}$ , as shown in Fig. 3(a). The tendency is also similar when the positive voltage is applied to the SOI side. Here, we define the  $1/e$  lifetime as the time interval of the decay from the peak of photoconductivity to  $1/e$  of the peak. The reason we use the  $1/e$  lifetime for evaluation of the interface recombination velocity is as follows. The decay curves are initially almost a straight line, and a slow component appears in the later part. This slow component has been reported to be due to the minority carrier traps<sup>7,8</sup> and should be excluded from the analysis. Therefore, the  $1/e$  lifetime was used. The  $1/e$  lifetime was increased from  $0.2$  to  $1.2 \mu\text{s}$  by the voltage application. This clearly shows that the voltage application between the SOI layer and the substrate results in suppression of the interface recombination. Since the lifetime saturated at voltages above  $180 \text{ V}$ , the interface recombination is thought to be completely suppressed. Without the UV light irradiation before the measurement, the lifetime was smaller ( $0.1 \mu\text{s}$ ) and did not change so significantly by applying voltage. The  $1/e$  lifetime without the voltage application increased from  $0.1$  to  $0.2 \mu\text{s}$  with the UV light irradiation. It is considered that by the UV light, the surface recombination was suppressed, so that the information of the interface came to be clearly observed.

Figure 3(b) shows the normalized decay curves of the excess carrier concentration at various applied voltages for sample B ( $n$ -type SOI, top layer thickness  $20.5 \mu\text{m}$ ). The carrier lifetime increases from  $1.0$  to  $8.1 \mu\text{s}$  with increasing negative voltage applied to the SOI side, and saturated at voltages above  $240 \text{ V}$  as shown in Fig. 3(b). The change in the lifetime for sample B is larger than that for sample A. Figure 3(c) shows the normalized decay curves for sample C ( $p$ -type SOI, top layer thickness  $10.0 \mu\text{m}$ ). The carrier lifetime increased from  $0.9$  to  $10.4 \mu\text{s}$  with increasing positive voltage applied to the SOI side. Therefore, the interface recombination was suppressed by the voltage application, as for samples A and B.

We extracted the  $1/e$  lifetime without voltage application  $\tau$ , and the saturated one with voltage application  $\tau'$ , from the measurement results, and calculated interface recombination

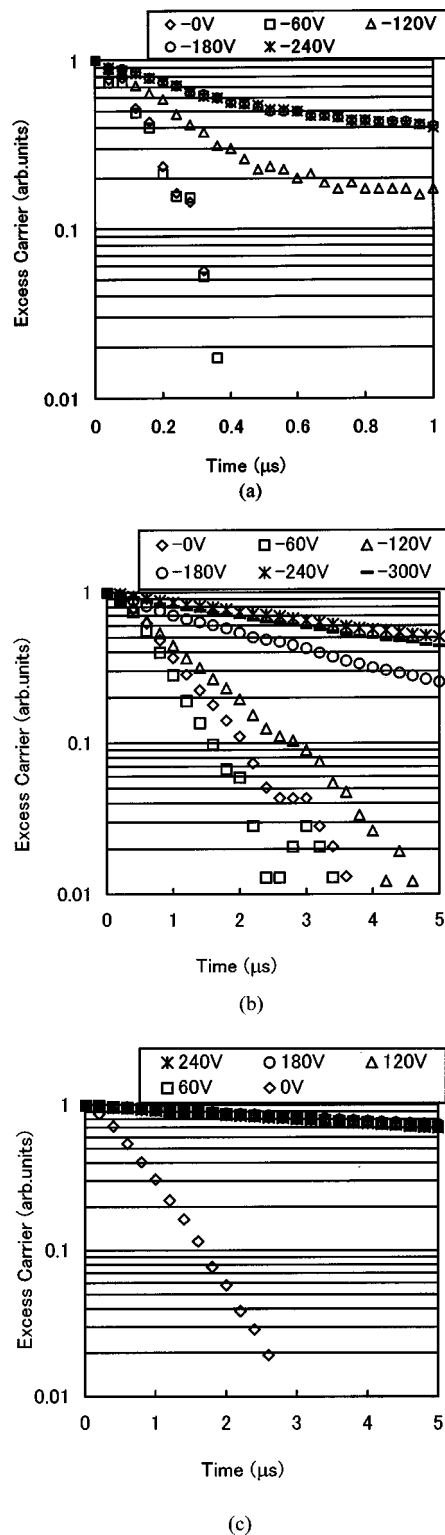


FIG. 3. Normalized decay curves of the excess carriers for various applied voltages. (a) sample A (*n*-type), (b) sample B (*n*-type), and (c) sample C (*p*-type). (a) and (b) are for negative voltage application and (c) is for positive voltage application to the SOI side.

velocity  $S_b$ , as listed in Table II. Under application of a positive voltage for *n*-type SOI and of a negative voltage for *p*-type SOI, the slow component tends to be significant. This is because the excess minority carriers are collected in the inversion layer of the SOI/BOX interface. Therefore, for the analysis, we used results under negative (positive) voltage application for the *n*-type (*p*-type) samples.

TABLE II. Interface recombination velocity  $S_b$  evaluated from the measurement results.

Sample	SOI layer thickness ( $\mu\text{m}$ )	$\tau$ ( $\mu\text{s}$ )	$\tau'$ ( $\mu\text{s}$ )	$S_b$ (cm/s)
A	1.5	0.2	0.7	506
B	20.5	1.0	8.1	1798
C	10.0	0.9	10.4	1040

For sample A, the  $S_b$  was evaluated to be about 500 cm/s. It is the smallest value among the three samples. For sample B, a large value of about 1800 cm/s was obtained. The change in the lifetime with applied voltage for sample B is much larger than that for sample A. This indicates that  $S_b$  of sample B is larger than  $S_b$  of sample A. For sample C,  $S_b$  of about 1000 cm/s was obtained.

In the bonded SOI wafers, the SOI/BOX interface is formed by the thermal oxidation. The surface recombination velocity of the properly thermally oxidized silicon has been reported to be from 1 to 15 cm/s.<sup>9</sup> In comparison with this value, the value evaluated in this study is greatly larger. However, a value of from 1 to 15 cm/s is realized only when the silicon surface is very ideally oxidized, and the actual value of the recombination velocity depends on various factors. The interface recombination velocity increases with increasing interface state density, and its effective value also depends on the fixed-charge density in the oxide. The fabrication process of the bonded SOI wafers includes the multi-step heat treatment for the bonding. It is considered that  $S_b$  was increased because of the introduction of the fixed-charge in the BOX and the increase in the interface state density during the bonding process. From carrier profiles obtained by the spreading-resistance measurement, we estimated the interface state density of bonded SOI wafers to be of the order of  $10^{11} \text{ eV}^{-1} \text{ cm}^{-2}$ .<sup>10</sup> This value roughly corresponds to recombination velocity on the order of 100 cm/s, and thus both results seem consistent. The interface state density was found to be decreased by annealing around 1000 °C.<sup>10</sup> The effects of annealing on  $S_b$  will be reported in a future publication.

We performed the  $\mu$ -PCD measurement applying voltage between SOI and the substrate, and evaluated interface recombination velocity for SOI wafers. For the three bonded SOI wafers, the interface recombination velocity was evaluated. The values are from 500 to 1800 cm/s, relatively large as for thermally oxidized Si/SiO<sub>2</sub> interfaces.

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