Characteristics of SiO_2/n-GaN interfaces with β-Ga_2O_3 interlayers

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We report on the characteristics of SiO_2/n-GaN metal-oxide-semiconductor (MOS) structures with β-Ga_2O_3 interlayers. β-Ga_2O_3 15 nm thick was grown by dry oxidation at 800 °C for 6 h, and 100-nm-thick SiO_2 was then deposited by sputtering. Capacitance–voltage measurements show a low interface trap density of $\sim 3.9\times 10^{10}$ $eV^{-1}\,cm^{-2}$, probably indicating an unpinning of the surface Fermi level. Additionally, current–voltage measurements display a low leakage current of ~ 1.2 $\mu A/cm^2$ at a gate voltage of +20 V, regardless of rough oxide surface, as confirmed by atomic force microscopy observations. Thus, the stacked SiO_2/β-Ga_2O_3 insulator is found to improve both the electrical interface properties and the gate dielectric characteristics of the GaN MOS structures. © *2003 American Institute of Physics.* [DOI: 10.1063/1.1629371]

Recently, a number of GaN metal-oxide-semiconductor (MOS) structures have been investigated from high-temperature and high-power electronics points of view. The first GaN MOS structure using a gate insulator consisting of deposited Ga_2O_3 (Gd_2O_3) has been reported by Ren *et al.*[1] Since then, several approaches have been employed to develop an insulator/GaN system using either a GaN native oxide (β-Ga_2O_3) or a deposited insulator using Ga_2O_3 (Gd_2O_3), AlN, SiO_2, Si_3N_4, $Pb(Zr,Ti)O_3$, MgO, and Sc_2O_3.[2–16] However, none exhibits optimal characteristics. The bottlenecks have been surface Fermi-level pinning at the oxide/GaN interface, which is a well-known problem with most GaN, and poor insulator quality. Thus, both issues need to be overcome for the fabrication of advanced GaN MOS devices. Regarding interface states, thermal dry and photoelectrochemical oxidation of GaN is known to be effective in reducing the interface trap density at the β-Ga_2O_3/GaN interface.[2–8] In our previous study, the thermally grown β-Ga_2O_3/n-GaN MOS structures have been proven to display a low interface trap density on the order of 10^{10} $eV^{-1}\,cm^{-2}$, resulting in an unpinning of the surface Fermi level at the β-Ga_2O_3/n-GaN interface.[6] In a narrow sense, the interfacial Ga-oxynitride layer is considered to play a significant role in improving the electrical interface properties. However, β-Ga_2O_3/n-GaN MOS structures also showed relatively large gate leakage current compared to that of the SiO_2/n-GaN MOS structures, which may be caused by a poor quality of β-Ga_2O_3 layer and a small conduction-band offset of ~ 0.9 eV between GaN and β-Ga_2O_3. Therefore, a stacked gate insulator consisting of β-Ga_2O_3 and well-known dielectric SiO_2 might be expected to improve the gate dielectric characteristics.[17] That is, in the SiO_2/β-Ga_2O_3/n-GaN MOS structures, the β-Ga_2O_3 interlayer can provide good electrical interface properties and the SiO_2 layer should reduce gate leakage currents and enhance oxide breakdown voltages, resulting in overcoming the troublesome issues of GaN-based MOS structures, as stated earlier. In this study, we have fabricated the stacked SiO_2/β-Ga_2O_3/n-GaN MOS structures by using thermal dry oxidation and SiO_2 deposition techniques, and have investigated the characteristics of SiO_2/n-GaN interfaces with β-Ga_2O_3 interlayers, in comparison with those of conventional SiO_2/n-GaN interfaces.

The epitaxial GaN films used in the experiments were grown by atmospheric pressure metalorganic chemical-vapor deposition on *a*-plane sapphire substrates. First, a 20 nm AlN buffer layer was deposited at 420 °C, and then a Si-doped 4-μm-thick GaN layer was grown at 1130 °C as an active layer. The GaN active layer had free electron concentrations of 9.9×10^{17} cm^{-3} and mobilities of 263 $cm^2/V\,s$, as determined by RT Hall-effect measurements. The Si concentration was also confirmed to be $\sim 1\times 10^{18}$ cm^{-3} by secondary ion mass spectrometry (SIMS) measurements. After growth, lateral dot-and-ring SiO_2/β-Ga_2O_3/GaN MOS capacitors were fabricated by thermal oxidation and SiO_2 deposition techniques as follows. First, a 500-nm-thick Si layer was selectively deposited on the top surface of the GaN sample as a mask material for thermal oxidation by rf sputtering at room temperature. The GaN samples were then thermally oxidized at 800 °C for 6 h in dry oxygen ambient. The formation of monoclinic β-Ga_2O_3 was confirmed by x-ray diffraction (XRD). After removing the Si mask by a HF-HNO_3 solution ($HF:HNO_3=20:3$), a 100-nm-thick SiO_2 layer was deposited on the top surface of the GaN samples as a gate dielectric by rf sputtering, using an SiO_2 target. This SiO_2 layer was selectively removed by wet etching using a photolithographic technique, and Al metal was then evaporated through a shadow mask to provide gate and ohmic electrodes. The dot gate electrode was 500 μm in diameter, and was surrounded by the ring ohmic electrode with a 50 μm gap. After metallization, the stacked SiO_2/β-Ga_2O_3/GaN MOS samples were annealed at 400 °C for 20 min in nitrogen ambient. As a reference, conventional SiO_2/n-GaN MOS samples without β-Ga_2O_3 interlayers were also prepared with the SiO_2 thickness of 100 nm by using conventional methodology.[13]

The MOS capacitors that we fabricated were electrically assessed by $I-V$, $C-V$, capacitance–transient ($C-t$), and

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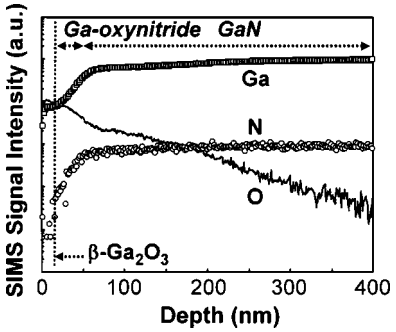

FIG. 1. SIMS profiles of Ga, N, and O atoms in a thermally oxidized *n*-GaN sample before SiO_2 deposition.

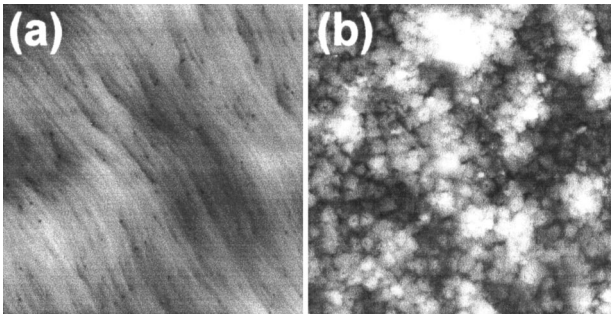

FIG. 2. AFM images of *n*-GaN samples before and after thermal dry oxidation. Both images are $5\times5\ \mu m^2$.

deep-level transient spectroscopy (DLTS) techniques. The $I-V$ measurements were carried out in the dark at a voltage step of 0.1 V under a conventional dc mode. The $C-V$ measurements were also performed in the dark at a frequency of 1 MHz and a voltage step of 0.01 V with various delay times t_d. On the $C-t$ measurements, the time dependence of the capacitance under a reverse voltage was measured after applying a 1 ms pulsed voltage of +10 V to approach an accumulation region temporarily. The DLTS measurements were carried out at temperatures between 80 and 475 K under the same condition as the $C-t$ measurements.

Figure 1 shows SIMS profiles of Ga, N, and O atoms in a thermally oxidized GaN sample before SiO_2 deposition. A pure Ga oxide containing no N atoms is seen in the surface region of ~15 nm, where the GaN has been completely oxidized. This layer probably corresponds to the monoclinic β-Ga_2O_3 layer, as confirmed by XRD. In addition in the deeper lying region of 15–50 nm from the surface, the β-Ga_2O_3 is transformed into the GaN; that is, ~35-nm-thick intermediate Ga-oxynitride layer with composition gradient is seen.

Figures 2(a) and 2(b), respectively, show typical atomic force microscopy (AFM) images of GaN samples before and after thermal dry oxidation. A clear difference can be seen between them. Before thermal dry oxidation, smooth surface morphology with a number of growth steps is clearly observed, where the mean roughness R_{ms} is ~0.35 nm. In addition some dark points that we can see correspond to threading dislocations. In sharp contrast, the surface morphology is seen to become very rough, with R_{ms} of ~13.6 nm by thermal dry oxidation, indicating nonuniform oxidation of GaN. In a narrow sense, polycrystalline shapes with small grain size of ~10 nm can be clearly observed in the oxide surface, which suggests that the oxidation occurs preferentially at dislocation sites. In particular, a higher degree of roughness at the oxide surface can be attributed to the process features of thermal dry oxidation.

RT forward $I-V$ characteristics of SiO_2/GaN MOS samples with and without a β-Ga_2O_3 interlayer are shown in the inset of Fig. 3. The $I-V$ data of the 100-nm-thick β-Ga_2O_3/*n*-GaN MOS sample that we have previously fabricated are also shown.[6] The SiO_2/β-Ga_2O_3/GaN sample shows a relative large leakage current of 1.2 $\mu A/cm^2$ at a gate voltage of +20 V, compared to 4.3 nA/cm^2 of the conventional SiO_2/GaN sample. This increase in forward leakage current by the presence of the β-Ga_2O_3 interlayer is probably caused by a reduction in effective thickness of SiO_2 layer due to the rough oxide surface, as shown in Fig. 2. From the surface roughness R_{ms} of the β-Ga_2O_3 interlayer, the effective thickness of the SiO_2 layer is estimated to be ~73 nm. However, the SiO_2/β-Ga_2O_3/GaN sample displays a leakage current by less than one order of magnitude compared to that of the β-Ga_2O_3/GaN MOS sample. In addition, both samples show high oxide breakdown voltages of ~4 MV/cm regardless of the presence of the β-Ga_2O_3 interlayer.

Figure 3 shows typical RT $C-V$ hysteresis curves for SiO_2/GaN MOS samples with and without β-Ga_2O_3 interlayer at t_d of 30 s, respectively. Their corresponding ideal $C-V$ curves with an inversion mode are also shown, considering the thinning effect of the SiO_2 layer as stated earlier. A deep depletion feature can be clearly observed in the depletion region for the SiO_2/β-Ga_2O_3/GaN sample, whereas capacitance saturation is seen for the SiO_2/GaN sample. In addition, a large hysteresis is observed for the SiO_2/GaN sample, while a very small hysteresis window is seen for the SiO_2/β-Ga_2O_3/GaN sample. These hysteresis windows should reflect charge exchange between the deep interface traps and the bulk GaN. Thus, these results suggest that the SiO_2/β-Ga_2O_3/GaN sample has much lower interface traps than the SiO_2/GaN sample, which probably results in unpin-

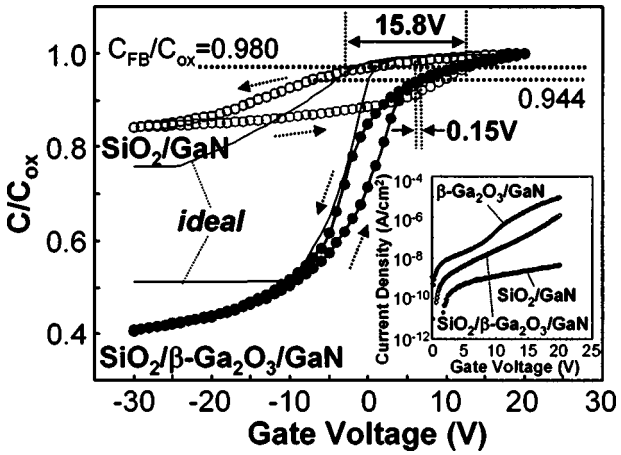

FIG. 3. High-frequency hysteresis $C-V$ curves at RT for SiO_2/β-Ga_2O_3/*n*-GaN and SiO_2/*n*-GaN samples as bias voltage is swept from −30 to +20 V and then back to −30 V at t_d of 30 s, together with respective ideal $C-V$ curves. Inset shows forward $I-V$ characteristics of SiO_2/β-Ga_2O_3/*n*-GaN and SiO_2/*n*-GaN samples, together with those of the 100-nm-thick β-Ga_2O_3/*n*-GaN MOS sample.

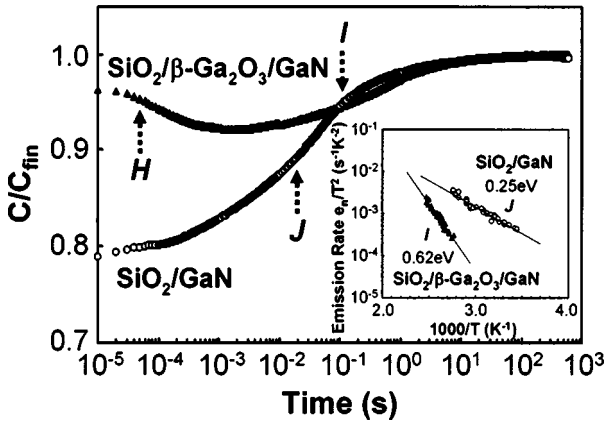

FIG. 4. Capacitance transients for $SiO_2/\beta\text{-}Ga_2O_3/n\text{-GaN}$ and $SiO_2/n\text{-GaN}$ samples after applying bias voltage of -25 V. Inset shows Arrhenius plots of emission rates from DLTS measurements of $SiO_2/\beta\text{-}Ga_2O_3/n\text{-GaN}$ and $SiO_2/n\text{-GaN}$ samples.

ning the surface Fermi-level at the $\beta\text{-}Ga_2O_3/\text{GaN}$ interface. Here, in their ideal $C-V$ curves, the flatband capacitance (C_{FB}/C_{ox}) is calculated to be 0.944 and 0.980 for the SiO_2/GaN MOS samples with and without the $\beta\text{-}Ga_2O_3$ interlayer, respectively. V_{FB}^f is the flatband voltage V_{FB} when the bias voltage goes from deep depletion to accumulation and V_{FB}^b is that when the voltage sweeps from accumulation to deep depletion. $|V_{FB}^f - V_{FB}^b|$ is the total hysteresis window at flatband. The hysteresis windows for the SiO_2/GaN MOS samples with and without the interlayer are ~ 0.15 and ~ 15.8 V, which correspond to a total interface trap density of at least $\sim 3.9\times 10^{10}$ and $\sim 4.5\times 10^{12}\ \text{eV}^{-1}\,\text{cm}^{-2}$, respectively. Thus, the $SiO_2/\beta\text{-}Ga_2O_3/\text{GaN}$ sample is found to show an incredibly lower interface trap density than the SiO_2/GaN sample, which is the same level as that of the $\beta\text{-}Ga_2O_3/\text{GaN}$ MOS sample that we have previously reported.[6]

In addition, to evaluate time dependence of charging and discharging in deep depletion at the oxide/GaN interface, conventional $C-t$ measurements were performed. Figure 4 shows typical RT $C-t$ curves after applying a gate voltage of -25 V for SiO_2/GaN MOS samples with and without $\beta\text{-}Ga_2O_3$ interlayer. C_{fin} means final capacitance. A large capacitance transient J with the time constant τ of ~ 20 ms is seen for the SiO_2/GaN sample, whereas two kinds of small capacitance transients with the opposite codes are seen for the $SiO_2/\beta\text{-}Ga_2O_3/\text{GaN}$ sample; one is a fast capacitance transient H with the τ of ~ 0.1 ms and the other is a slow capacitance transient I with the τ of 0.1 s. The τ for all the capacitance transients tends to become longer with increasing the reverse voltage, which indicates a typical characteristic of the oxide/GaN interface. However, the fast capacitance transient H is independent of temperature, which implies that it is not a typical character of interface traps. This capacitance transient H may be caused by the time delay swelling of the depletion layer in the intermediate Ga-oxynitride layer upon applying reverse voltages.[6] The other capacitance transients I and J with relatively long τ correspond to the thermal emission of carriers from the interface traps at oxide/GaN interface, because they show the strong dependence of τ on temperature. Furthermore, DLTS measurements were carried out under the same condition as the $C-t$ measurements to investigate deep-level centers at the oxide/GaN interface. In both samples, to a greater or less extent, respective DLTS spectra show a dominant peak, which corresponds to the capacitance transients I and J at RT. From Arrhenius plots of the emission rates e_n/T^2, as shown in the inset in Fig. 4, the thermal activation energies for the carrier emission from the dominant interface traps are estimated to be ~ 0.62 and ~ 0.25 eV for the SiO_2/GaN MOS samples with and without the $\beta\text{-}Ga_2O_3$ interlayer, respectively. Thus, the $SiO_2/\beta\text{-}Ga_2O_3/\text{GaN}$ sample has a deep interface trap level at 0.62 eV below the conduction band at the $\beta\text{-}Ga_2O_3/\text{GaN}$ interface. However, the surface Fermi level is considered to be probably unpinned because of the extremely low interface trap density as determined by the $C-V$ measurements. This behavior is significantly different from a situation of the SiO_2/GaN sample without the $\beta\text{-}Ga_2O_3$ interlayer, in which a number of interface traps induce the surface Fermi-level pinning effect at the SiO_2/GaN interface upon applying reverse voltages. These distinguished interface properties of the SiO_2/GaN sample with the $\beta\text{-}Ga_2O_3$ interlayer may be probably associated with the presence of the intermediate Ga-oxynitride layer.

In summary, we have demonstrated that the stacked $SiO_2/\beta\text{-}Ga_2O_3$ insulator improves both the electrical interface properties and the gate dielectric characteristics of the n-GaN MOS structures. The total interface trap density was estimated to be $3.9\times 10^{10}\ \text{eV}^{-1}\,\text{cm}^{-2}$. The forward gate leakage current was $\sim 1.2\ \mu\text{A/cm}^2$ for a gate voltage of $+20$ V.

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