IEICE TRANS. ELECTRON., VOL.E91–C, NO.1 JANUARY 2008

LETTER

Low-Power Switched Current Memory Cell with CMOS-Type Configuration

Masashi KATO[†a)], ***Member***, **Nobuyuki TERADA**[†*], **Hirofumi OHATA**[†**], ***Nonmembers***, ***and*** **Eisuke ARAI**[†***], ***Member***

SUMMARY This letter presents a low-power switched current (SI) memory cell with CMOS-type configuration. By combining nMOS and pMOS in the SI memory cell and using a polarity discrimination circuit, we design a CMOS-type SI memory cell which eliminates the quiescent current in the SI memory cell. The simulation result shows that the CMOS-type SI memory cell consumes less power than the conventional class-AB memory cell.

key words: *switched current, low-power, CMOS-type, memory cell*

1. Introduction

Switched current (SI) circuits have been widely researched in the analog circuit field because they have the advantages of low voltage operation and small chip area [1], [2]. The basic function of the SI circuit is to sample and hold of the input current by the SI memory transistor. The nMOS memory transistor, however, conducts current only from drain to source, while the pMOS memory transistor conducts current from source to drain. In order to accept input current signal with both the positive and negative polarities, current should be supplied from a current source to a memory transistor, or a memory cell should consist of a class-AB configuration shown in Fig. 1 [3], [4]. However, the circuits with the current source and the class-AB configuration usually conduct the quiescent current, which introduces continuous power consumption in the SI circuits during operation. In this letter, to reduce the power consumption of the SI memory cell, we propose a CMOS-type SI circuit configuration which can suppress the quiescent current.

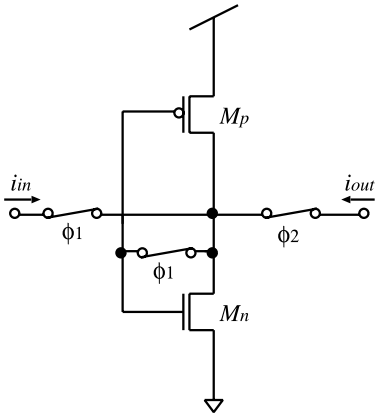

Fig. 1 Class-AB SI memory cell.

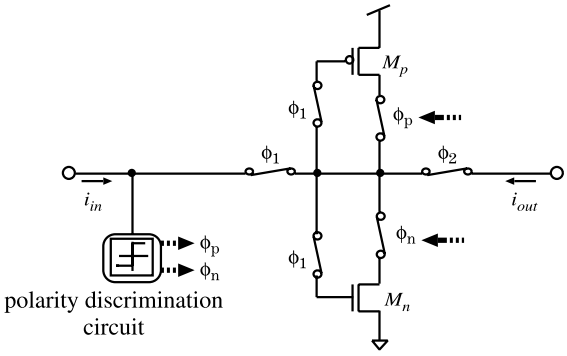

Fig. 2 CMOS-type SI memory cell.

2. Circuit Description

A circuit diagram of the CMOS-type SI memory cell is shown in Fig. 2. *Mn* is an nMOS memory transistor and *Mp* is a pMOS memory transistor. ϕ_1 and ϕ_2 are the same clock as in the conventional SI memory cell [1]. Compared with the conventional SI memory cell, no current source is employed in this circuit, and a polarity discrimination circuit is connected to an input node. The polarity discrimination circuit is the same circuitry as the one-bit current quantizer [5]. When the input current is positive, the polarity discrimination circuit outputs ϕ_n and closes a switch next to *Mn*. The input current flows through *Mn* at clock ϕ_1, and *Mn* samples the input current. Then *Mn* holds the input current at clock ϕ_2, and it outputs the sampled current to the output node. On the contrary, when the input current is negative, the polarity discrimination circuit outputs ϕ_p and closes a switch next to *Mp*. The input current flows through *Mp* at clock ϕ_1, and *Mp* samples the input current. Then *Mp* holds the input current at clock ϕ_2, and it outputs the sampled current to the output node. The polarity discrimination of the input current is performed just before sampling clock ϕ_1. The stationaly current never flows from Vdd to ground through *Mn*

Manuscript received July 18, 2007.
Manuscript revised September 7, 2007.

[†]The authors are with the Graduate School of Engineering, Nagoya Institute of Technology, Nagoya-shi, 466-8555 Japan.
[*]Presently, with the DENSOTECHNO CO., LTD.
[**]Presently, with the OMRON Corporation.
[***]Presently, with the professor emeritus of Nagoya Institute of Technology.
a) E-mail: kato.masashi@nitech.ac.jp

DOI: 10.1093/ietele/e91–c.1.120

and *Mp*, because either ϕ_n or ϕ_p is opened at any time.

3. Simulation Results and Conclusion

We simulate the CMOS-type SI memory cell shown in Fig. 2 by HSPICE with level 49 MOS transistor model for a 0.35 μm CMOS process. A supply voltage is 1.5 V and a clock voltage for switches is 2.0 V. Transistor sizes are 33/10 μm and 100/10 μm for *Mn* and *Mp*, respectively, and the sampling frequency is 500 kHz. Input signals have 10–50 μA amplitude with a 1 kHz frequency. For comparison, we simulate the conventional class-AB SI memory cell shown in Fig. 1 in the same condition.

Figure 3 shows power consumption of the class-AB memory cell and the CMOS-type SI memory cell including the polarity discrimination circuit. The CMOS-type SI memory cell consumes 10–14 μW lower power than class-AB SI memory cell. This means that power consumption due to the quiescent current in the class-AB memory cell can be eliminated in the CMOS-type SI memory cell. In particular, at the small signal amplitude, the difference between them is relatively large. In the class-AB SI memory cell, the potential at gates of *Mn* and *Mp* depends on the signal amplitude. When the signal amplitude is small, the potential there stays around threshold voltages of nMOS and pMOS. Then quiescent current flows through *Mn* and *Mp*, and the class-AB SI memory cell consumes power. Since the CMOS-type SI memory cell does not conduct quiescent current at any signal amplitude, it shows smaller power consumption than the class-AB SI memory cell especially at the small signal amplitude.

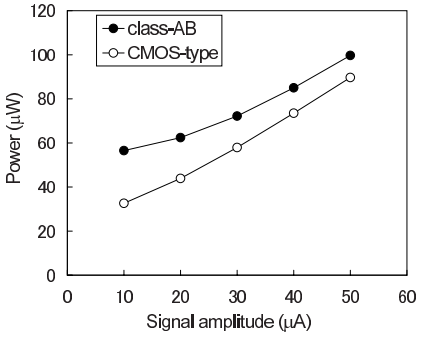

Fig. 3 Power consumption of the class-AB memory cell and the CMOS-type SI memory cell including the polarity discrimination circuit.

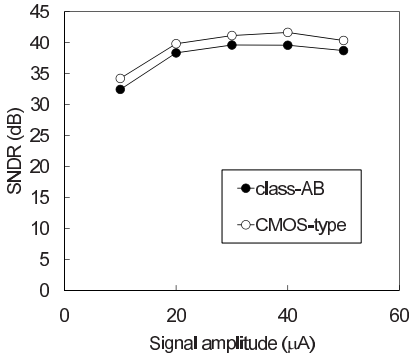

Fig. 4 SNDR of output signals from the class-AB and CMOS-type SI memory cells.

Figure 4 shows SNDR of these memory cells estimated from the FFT analysis of the output signal. These two memory cells show almost the same SNDR (or even slightly better SNDR in the CMOS-type SI memory cell). Therefore, the polarity discrimination circuit in the CMOS-type SI memory cell does not introduce significant noise or distortion to the output signal. We can conclude that the CMOS-type SI memory cell can reduce power consumption without signal degradation compared with the conventional class-AB SI memory cell.

Acknowledgement

This work is supported by VLSI Design and Education Center (VDEC), the University of Tokyo in collaboration with Synopsys, Inc. and Cadence Design Systems, Inc., and it is also supported by the Hori Information Science Promotion Fundation. The authors would like to thank Prof. M. Ichimura and Ms. E. Farida of Nagoya Inst. of Tech. for their fruitful discussion.

References

[1] N. Tan, Switched-Current Design and Implementation of Oversampling A/C Converters, Kluwer Academic Publishers, 1997.
[2] S.-Y. Lee and C.-J. Cheng, "A low-voltage and low-power adaptive switched-current sigma-delta ADC for bio-acquisition microsystems," IEEE Trans. Circuits Syst.-I, vol.53, no.12, p.2628, Dec. 2006.
[3] A. Handkiewicz, P. Sniatala, and M. Lukowiak, "Low-voltage high-performance switched current memory cell," Proc. Ninth IEEE Int. ASIC Conf., ASIC'97, pp.12–16, 1999.
[4] R. Srowik and R. Schüffny, "Low-power class AB current memory cell," Electron. Lett., vol.35, no.23, pp.2014–2015, Nov. 1999.
[5] J.M. dela Rosa, B. Pérez, and A. Rodriguez, Systematic design of CMOS switched-current bandpass sigma-delta modulators for digital communication chips, Kluwer Academic Publishers, 2002.