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Citation: *AIP Advances* **2**, 022134 (2012); doi: 10.1063/1.4722642

View online: <http://dx.doi.org/10.1063/1.4722642>

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# Effect of AlN growth temperature on trap densities of *in-situ* metal-organic chemical vapor deposition grown AlN/AlGaIn/GaN metal-insulator-semiconductor heterostructure field-effect transistors

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(Received 16 March 2012; accepted 2 May 2012; published online 21 May 2012)

The trapping properties of *in-situ* metal-organic chemical vapor deposition (MOCVD) grown AlN/AlGaIn/GaN metal-insulator-semiconductor heterostructure field-effect transistors (MIS-HFETs) with AlN layers grown at 600 and 700 °C has been quantitatively analyzed by frequency dependent parallel conductance technique. Both the devices exhibited two kinds of traps densities, due to AlN ( $D_{T-AlN}$ ) and AlGaIn layers ( $D_{T-AlGaIn}$ ) respectively. The MIS-HFET grown at 600 °C showed a minimum  $D_{T-AlN}$  and  $D_{T-AlGaIn}$  of  $1.1 \times 10^{11}$  and  $1.2 \times 10^{10} \text{ cm}^{-2}\text{eV}^{-1}$  at energy levels ( $E_T$ )-0.47 and -0.36 eV. Further, the gate-lag measurements on these devices revealed less degradation  $\sim \leq 5\%$  in drain current density ( $I_{ds-max}$ ). Meanwhile, MIS-HFET grown at 700 °C had more degradation in  $I_{ds-max} \sim 26\%$ , due to high  $D_{T-AlN}$  and  $D_{T-AlGaIn}$  of  $3.4 \times 10^{12}$  and  $5 \times 10^{11} \text{ cm}^{-2}\text{eV}^{-1}$  positioned around similar  $E_T$ . The results shows MIS-HFET grown at 600 °C had better device characteristics with trap densities one order of magnitude lower than MIS-HFET grown at 700 °C. Copyright 2012 Author(s). This article is distributed under a Creative Commons Attribution 3.0 Unported License. [<http://dx.doi.org/10.1063/1.4722642>]

## I. INTRODUCTION

AlGaIn/GaN metal-insulator-semiconductor heterostructure field-effect transistors (MIS-HFETs) grown on silicon are of immense interest due to its low cost substrate, improved performance in high-power and high-frequency areas.<sup>1-3</sup> The merits of AlGaIn/GaN-MIS technology are that it offers a wider gate voltage swing, reduced gate leakage and enhanced breakdown voltage, which are highly desirable for high power operations. A wide variety of materials have been employed as gate insulators and passivating material to improve the device reliability and performance.<sup>4-7</sup> On the other hand, the lack of high quality native oxide ( $\text{Ga}_2\text{O}_3$ ) as well as the traps associated in using these foreign/*ex-situ* grown insulators for GaN MIS-devices can adversely hamper the drain current density ( $I_{ds-max}$ ) under pulsed conditions. It is difficult to modulate/mitigate the traps associated with AlGaIn/GaN MIS interface,<sup>8-10</sup> that leads to current collapse.<sup>11</sup> On contrast, *in-situ* MOCVD grown AlN layer can be a promising gate insulator for GaN based MIS-HFETs, for its reduced lattice mismatch over AlGaIn/GaN heterostructure and high dielectric constant.

Recently, *in-situ* MOCVD grown AlN/AlGaIn/GaN MIS-HFET with the AlN layer growth temperature ( $T_G$ ) of 600 °C has been demonstrated with better device properties than the conventional HFET.<sup>12</sup> However, detailed studies on trap states of *in-situ* MOCVD grown AlN/AlGaIn/GaN MIS-HFETs as a variation of AlN layer  $T_G$  are necessary to understand the potential utilization of AlN layer in GaN based MIS-devices. By using frequency dependent parallel conductance/angular frequency ( $G_{p/\omega}$ ) technique reported earlier, it is feasible to locate the trap states in AlN/AlGaIn/GaN MISs.<sup>13</sup>

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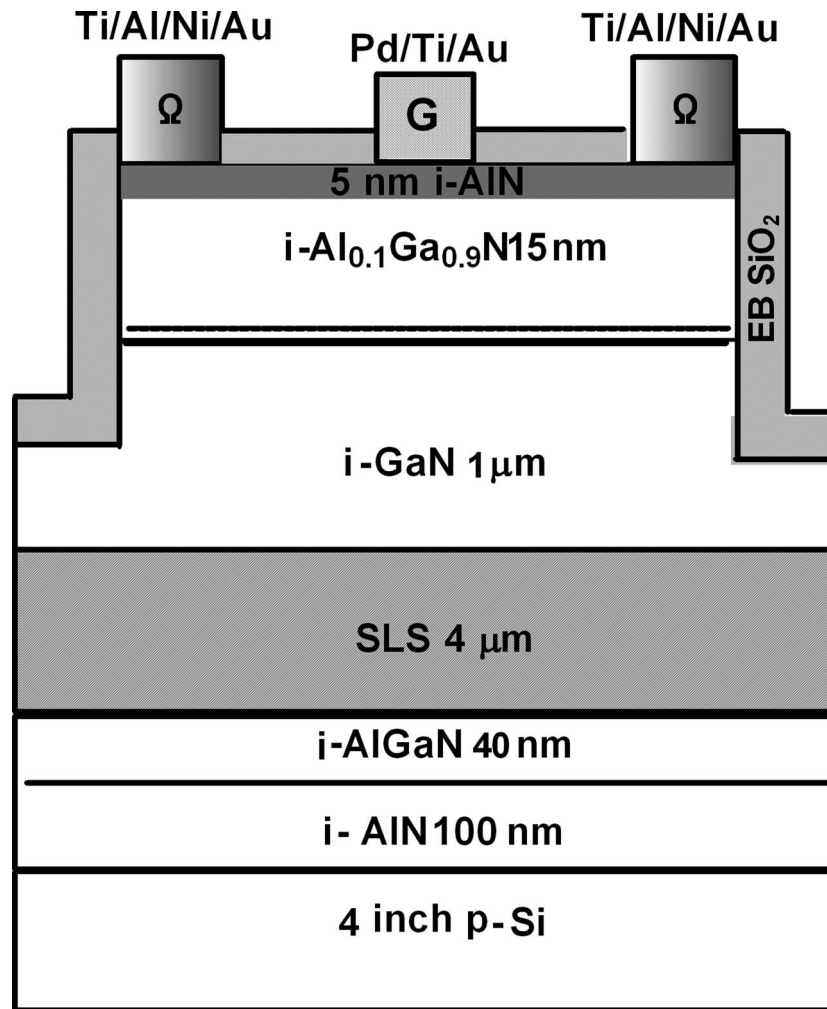


FIG. 1. Schematic representation of *in-situ* MOCVD grown AlN/AlGaN/GaN MIS HFET with the AlN layer  $T_G$  of 600 and 700 °C.

Further, this technique can also be extended to study traps in AlGaN/GaN based heterostructures with different barrier thickness and alloy compositions. Frequency dependent conductance technique is the most reliable method for investigation of trapping effects,<sup>14</sup> which can effectively locate the traps in  $\text{Al}_x\text{Ga}_{1-x}\text{N}/\text{GaN}$  heterostructures.<sup>15-17</sup>

In this study, we have quantitatively analyzed the trap states of *in-situ* MOCVD grown AlN/AlGaN/GaN MIS-HFETs using AlN layers grown at two different temperatures.

## II. EXPERIMENTS

The AlN/AlGaN/GaN MISHs were grown using Taiyo Nippon Sanso, SR 4000 MOCVD system. The MISHs consists of an undoped 5 nm AlN top layer, 15 nm  $\text{Al}_{0.10}\text{Ga}_{0.90}\text{N}$  layer, 1  $\mu\text{m}$  intrinsic GaN layer, a super lattice structure (SLS) of 4  $\mu\text{m}$  grown over 4 inch p-type silicon substrate. To analyze the effect of AlN layer  $T_G$  on trap densities ( $D_T$ ), the active material structure of both the MISHs were same while the  $T_G$  of AlN layer alone was fixed as 600 and 700 °C. The MISHs with AlN grown at 600 and 700 °C will be referred as MIS-diodes/HFETs A and B herein. Van der Pauw-Hall measurement was performed to measure Hall mobilities and sheet carrier densities of these MISHs. The room temperature Hall mobilities of MISHs A and B were 918 and 892  $\text{cm}^2/\text{V}\cdot\text{s}$ , while the carrier densities were 0.65 and 0.48  $\times 10^{13} \text{ cm}^{-2}$  respectively.

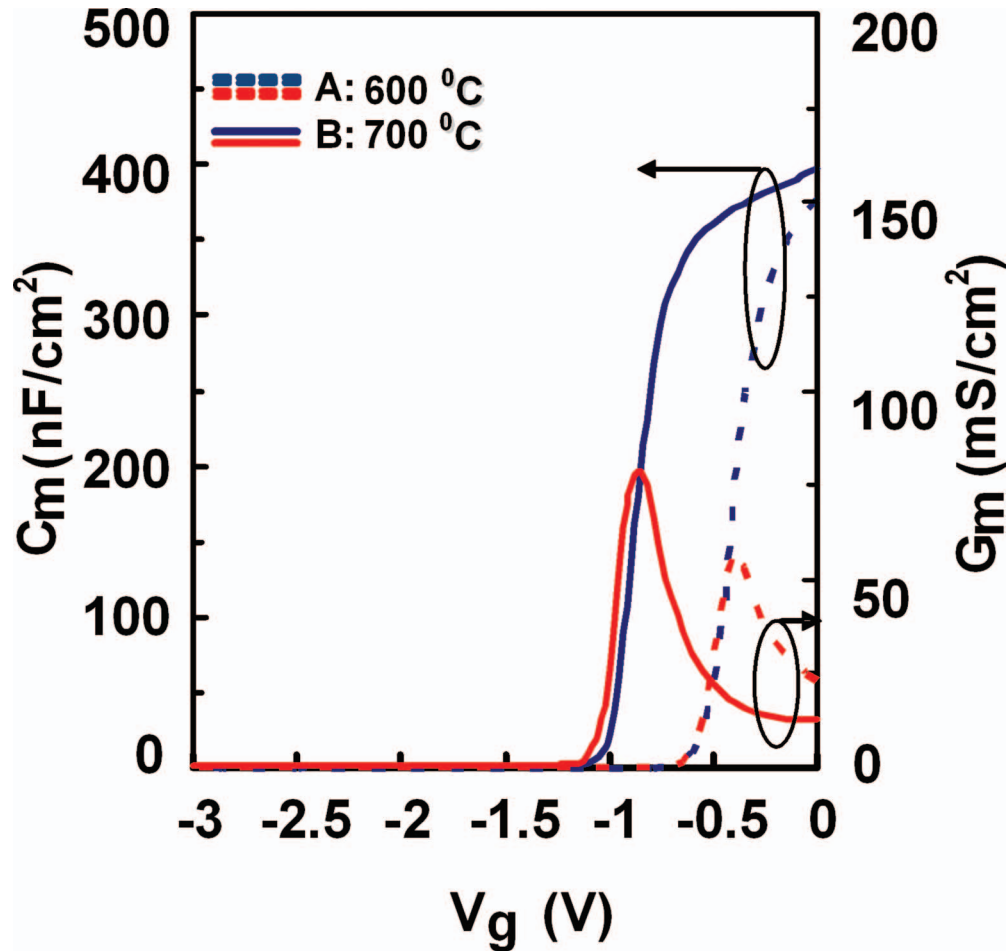


FIG. 2. Typical  $C$ - $V$  and  $G$ - $V$  characteristics measured at 100 kHz for *in-situ* MOCVD grown AlN/AlGaIn/GaN MIS-HFETs with AlN layer  $T_G$  of 600 and 700 °C.

The MIS-devices fabrication started with mesa isolation using  $\text{BCl}_3$  plasma based Reactive Ion etching (RIE). A 100 nm thick electron beam evaporated  $\text{SiO}_2$  was used for device passivation. Ohmic patterns were performed using conventional UV-photolithography followed by metallization of Ti/Al/Ni/Au (15/80/12/40 nm). Prior to ohmic metallization, the  $\text{SiO}_2$  in the ohmic access region was wet etched using HF based buffer and the surface was cleaned by using HCl solution. The Ohmic contacts were annealed at 850 °C using infra-red lamp annealing for 30s in  $\text{N}_2$  ambient. Finally, gate metals Pd/Ti/Au (40/20/60 nm) were deposited directly on the AlN layer followed by conventional lift off procedures. Circular shaped MIS-diodes of uniform area ( $7.07 \times 10^{-4} \text{ cm}^2$ ) were used for the conductance measurements. The schematic representation of the fabricated MIS-HFET/diode is shown in Fig. 1.

Electrical characterizations on these devices were carried out using Agilent B1505 power device analyzer/curve tracer set up interfaced with a shock proof probe station. The capacitance ( $C$ - $V$ ) and conductance ( $G$ - $V$ ) measurements were performed by sweeping the gate voltage ( $V_g$ ) from accumulation to depletion regime, between frequency ranges of 1 kHz to 5 MHz. The amplitude of ac signal was fixed as 30 mV and the measurement period was long, so that small signal conditions were maintained.

### III. RESULTS AND DISCUSSIONS

Typical  $C$ - $V$  and  $G$ - $V$  characteristics measured at 100 kHz for MIS diodes A and B are shown in Fig. 2. The  $C$ - $V$  curves show a sharp transition from depletion to accumulation regime for both

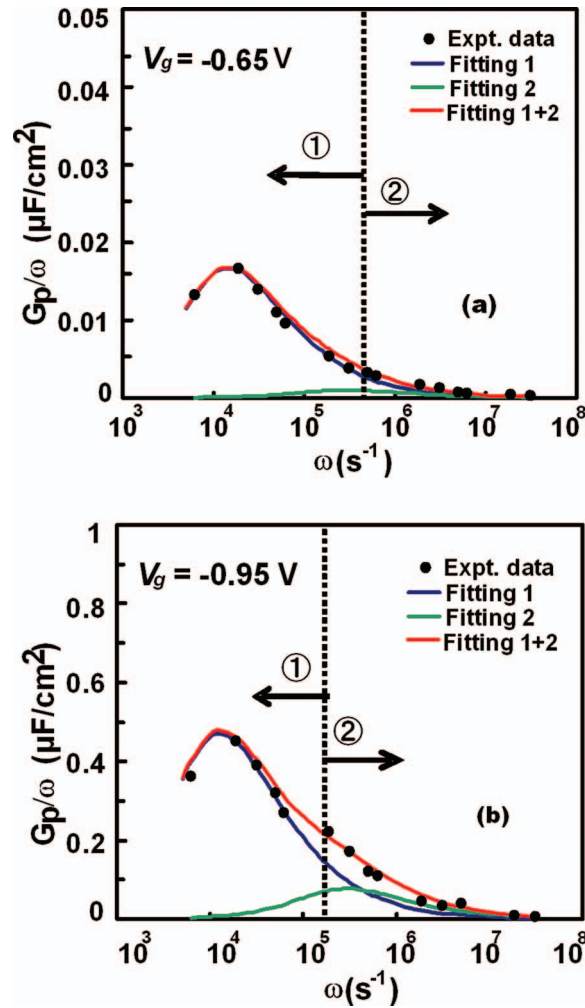


FIG. 3.  $G_p/\omega$  as a function of  $\omega$  for AlN/AlGaIn MIS-HFETs with AlN layer (a)  $T_G \sim 600$  °C and (b)  $T_G \sim 700$  °C. The dashed line indicates cross over region between AlN and AlGaIn traps.

MIS diodes. The threshold voltage ( $V_{th}$ ) observed for MIS-diodes A and B was -0.65 and -0.95 V respectively. The zero-bias capacitance for MIS-diodes A and B were 394 and 377 nF/cm<sup>2</sup>. Nevertheless, a threshold voltage shift of ( $\Delta V_{th} = -0.3$  V) and zero bias capacitance as well as conductance differences between the two MIS-diodes indicate priori information about variations in AlGaIn (bulk related) and AlN traps. The frequency dependent capacitance dispersion in *pinch-on* region is due to the surface status while the *pinch-off* capacitance dispersions are due to bulk traps.<sup>18</sup>

To evaluate the trap states quantitatively, the ( $G_{p(\omega)}$ ) values near the depletion region were calculated according to the expression,<sup>2,14</sup>

$$\frac{G_p}{\omega} = \frac{\omega G_m C_b^2}{G_m^2 + \omega^2 (C_b - C_m)^2}, \quad (1)$$

where  $C_b$  is the barrier capacitance,  $G_m$  and  $C_m$  are the measured conductance and capacitance respectively. The relation between  $G_p/\omega$  and the  $\omega$  is given by the equation,

$$\frac{G_p}{\omega} = \frac{q D_T}{2\omega T_T} \times \ln[1 + (\omega\tau_T)^2], \quad (2)$$

where  $D_T$ ,  $\tau_T$  are the trap densities and trap time constants, that are parameters evaluated theoretically by fitting the experimental  $G_p/\omega$  values.

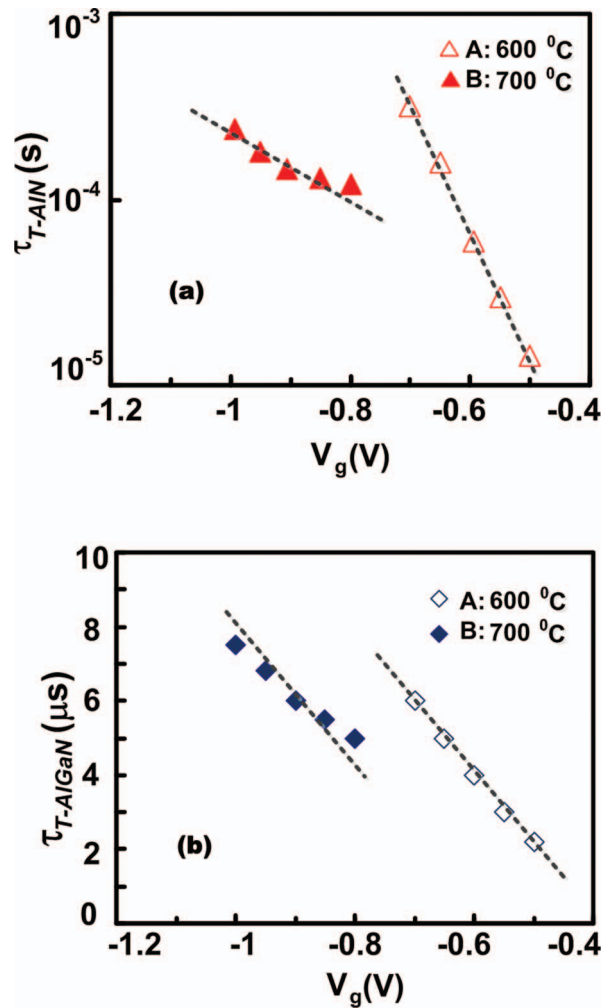


FIG. 4. Trap time constants of (a) AlN traps and (b) AlGaN bulk traps as a function of  $V_g$  for AlN/AlGaN/GaN MIS-HFETs with AlN layer  $T_G$  of 600 and 700 °C.

We could successfully fit two curves 1 and 2 to the asymmetric experimental  $G_p/\omega$  values at threshold voltage ( $V_{th}$ ), for MIS-diodes A and B. For comparison, the fitting results of MIS-diodes are shown in Figs. 3(a) and 3(b) respectively. The fitting curves 1 and 2 correspond to the trap states due to the AlN layer ( $D_{T-AlN}$ ) and bulk traps of the AlGaN layer ( $D_{T-AlGaN}$ ) respectively. Both  $D_{T-AlN}$  and  $D_{T-AlGaN}$  can be quantified from the  $G_p/\omega$  peak magnitude, while the  $\tau_T$  can be located from the peak position of  $G_p/\omega$ . By comparing the fitting results of MIS-diodes, we observed both  $D_{T-AlN}$  and  $D_{T-AlGaN}$  of MIS-diode A is one order lower in magnitude than B. In the fitting process for  $V_g \leq V_{th}$ , similar trend was observed for both the MIS-diodes. Moreover, the fitting curve (1+2) at the cross over region (denoted by a dashed line in Figs. 3(a) and 3(b)) were relatively broader than the experimental  $G_p/\omega$  values in the case of MIS-diode B compared to A. This phenomenon was also observed for AlN/AlGaN/GaN MISHs grown relatively at high temperature  $T_G \geq 1000$  °C.<sup>13</sup> This is due to the asymmetric behavior of experimental  $G_p/\omega$  values caused by a high  $D_{T-AlGaN}$  for MIS-diodes with AlN layers grown at high temperatures. Nevertheless, these *in-situ* AlN/AlGaN/GaN MISHs exhibited two trap states with distinct time constants irrespective of their AlN layer  $T_G$ . Therefore, the present  $G_{p/\omega}$  studies suggests a good AlN/AlGaN heterointerface due to low temperature *in-situ* grown AlN layer. As evident, this kind of traps response had also been observed in the case of SiO<sub>2</sub>/Si MIS-devices using parallel conductance experiments.<sup>19,20</sup>

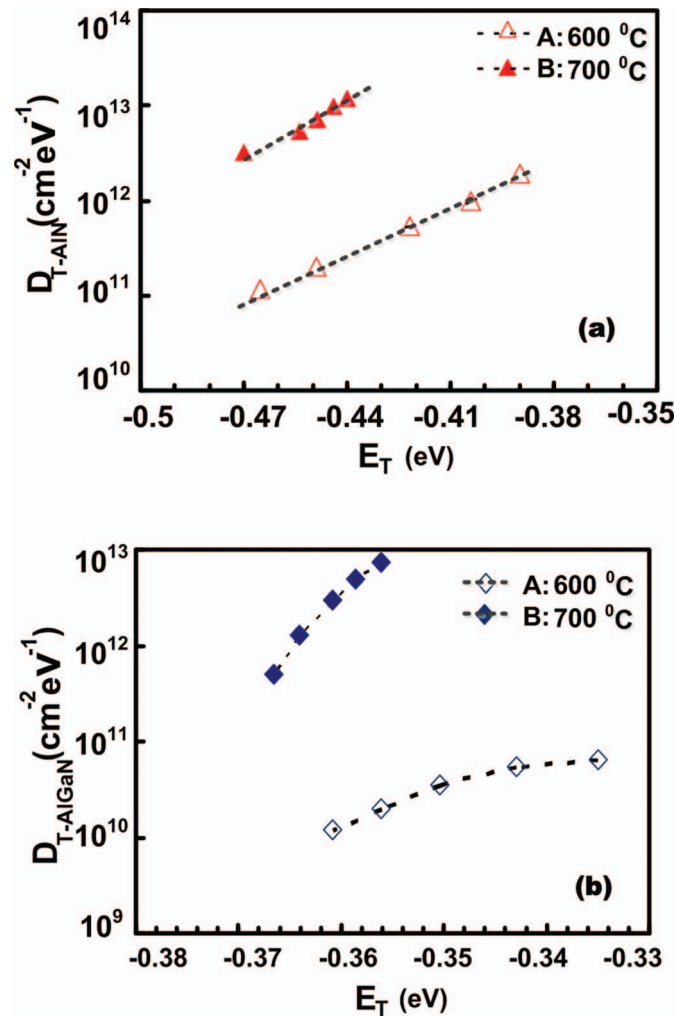


FIG. 5. The density of (a) AlN traps and (b) AlGaN bulk traps as a function of their energy levels of AlN/AlGaN/GaN MIS-HFETs with AlN layer  $T_G$  of 600 and 700 °C.

The AlN trap time constant ( $\tau_{T-AlN}$ ) and AlGaN trap time constant ( $\tau_{T-AlGaN}$ ) evaluated are plotted against the  $V_g$  for MIS-diodes as shown in Figs. 4(a) and 4(b). In the case of MIS-diode A, both  $\tau_{T-AlN}$  and  $\tau_{T-AlGaN}$  showed better exponential dependencies on  $V_g$  than MIS-diode B. An exponential dependency of  $\tau_T$  on  $V_g$  manifests uniformities in the trap states of MIS-diode A than B. A broader conductance curve and a deviation from exponential dependence ( $\tau_T \propto V_g$ ) can be observed if surface potential fluctuation due to some non-uniformity in the oxide (Insulator) and/or interface traps exists.<sup>16</sup> The  $\tau_{T-AlN}$  values for MIS-diodes A and B was in the range of (14  $\mu\text{s}$  – 0.3 ms) and (0.1 – 0.2 ms). On the other hand,  $\tau_{T-AlGaN}$  for MIS-diodes A and B were between (2 – 6  $\mu\text{s}$ ) and (5 – 8  $\mu\text{s}$ ) respectively. These  $\tau_{T-AlN}$  and  $\tau_{T-AlGaN}$  are consistent with the  $\tau_T$  ranges generally reported for AlN related traps,<sup>21</sup> and AlGaN related bulk traps.<sup>3</sup>

The trap state energy level ( $E_T$ ) is proportional to the  $\tau_T$ , and therefore it can be deduced using the expression,

$$E_T = kT \ln(\sigma_T N_c v_T) \tau_T \quad (3)$$

In the above equation,  $k$  is the Boltzman constant,  $T$  is the temperature at which C-V and G-V were measured,  $\sigma_T$  is the capture cross section of the traps,  $N_c$  is the density of states in the conduction band and  $v_T$  is the average thermal velocity of the carriers. The  $E_T$  values were calculated by using

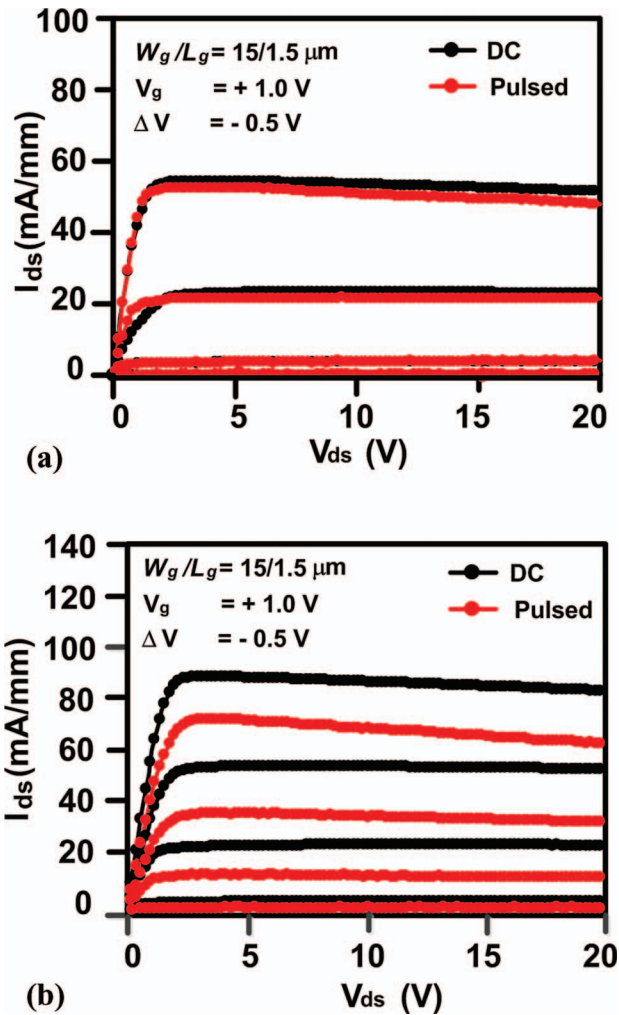


FIG. 6. DC and pulsed output  $I_{ds}$ - $V_{ds}$  characteristics of AlN/AlGaIn MIS-HFETs with AlN layer (a)  $T_G \sim 600$  °C and (b)  $T_G \sim 700$  °C. For pulsed measurements a gate pulse of 500  $\mu$ s was applied with a quiescent gate bias ( $V_{gs-q} = -5$  V).

the evaluated  $\tau_T$  and assuming  $\sigma_T = 3.4 \times 10^{-15}$  cm<sup>-2</sup>,  $N_c = 4.3 \times 10^{14} \times T^{3/2}$  and  $v_T = 2.6 \times 10^7$  cm/s.<sup>16</sup>

Furthermore, the  $D_{T-AlN}$  and  $D_{T-AlGaIn}$  as a function of corresponding  $E_T$  for MIS-diodes A and B are shown in Figs. 5(a) and 5(b). The minimum  $D_{T-AlN}$  and  $D_{T-AlGaIn}$  values measured for MIS-diode A were  $1.1 \times 10^{11}$  and  $1.2 \times 10^{10}$  cm<sup>-2</sup>eV<sup>-1</sup>. Their corresponding energy levels were -0.47 and -0.36 eV below the conduction band. In contrast, minimum  $D_{T-AlN}$  and  $D_{T-AlGaIn}$  values observed for MIS-diode B around similar energy levels were  $3.4 \times 10^{12}$  and  $5 \times 10^{11}$  cm<sup>-2</sup>eV<sup>-1</sup> respectively. By comparing the  $D_{T-AlN}$  and  $D_{T-AlGaIn}$  at their respective  $E_T$ , it was observed unambiguously that  $D_{T-AlN}$  and  $D_{T-AlGaIn}$  of MIS-diode A was one order of magnitude lower than B. This result signifies that low  $T_G$  can favour a better AlN layer over AlGaIn with reduced trap densities. R. Stoklas *et al.*,<sup>3</sup> have reported two trap densities in the range of  $(2.5-4) \times 10^{11}$  and  $(0.3-1.2) \times 10^{12}$  cm<sup>-2</sup>eV<sup>-1</sup> for Al<sub>2</sub>O<sub>3</sub>/AlGaIn/GaN/Si non-annealed MOSFETs. We have also recently reported trap densities of  $4.5 \times 10^{12}$  and  $1 \times 10^{11}$  cm<sup>-2</sup>eV<sup>-1</sup> due to AlN and AlGaIn traps in *in-situ* AlN/AlGaIn/GaN/Si MISHs grown at 1030 °C (Ref. 13). However, the  $D_{T-AlN}$  and  $D_{T-AlGaIn}$  values for AlN/AlGaIn/GaN MISHs ( $T_G \sim 600$  °C) in this present study are lower than the previous reports. This is mainly due to a good *in-situ* AlN layer grown at low temperature, although the AlN mole fraction ( $x = 10\%$ ) was low in the AlGaIn layer. The *in-situ* MOCVD grown AlN layer ( $T_G \sim 600$  °C) can effectively passivate and protect the AlGaIn surface leading to a good AlN/AlGaIn heterointerface. Meanwhile, low growth



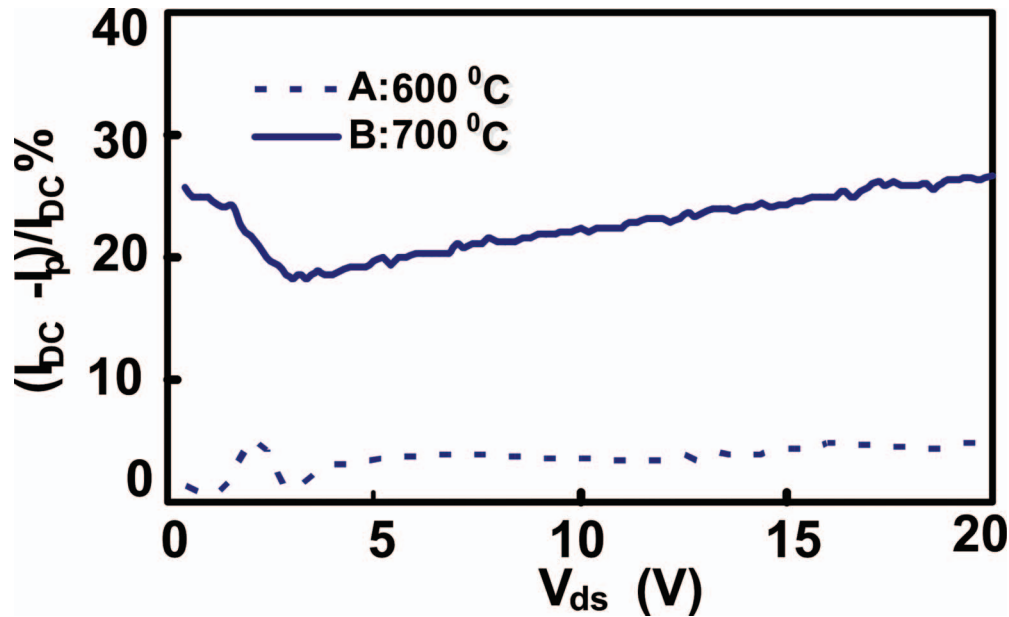


FIG. 7. Degradation of  $I_{ds-max}$  (in %) estimated from the measured DC and pulsed output  $I_{ds}-V_{ds}$  characteristics of AlN/AlGaN MIS-HFETs with AlN layer  $T_G$  of 600 and 700 °C.

temperature of AlN is also preferred for preventing tensile strain-induced cracking of AlN layer, low gate leakage and better device performance with good passivation of AlGaN surface.<sup>12,22,23</sup>

To investigate the influence of these traps on device characteristics, MIS-HFETs were also fabricated simultaneously and subjected to output  $I_{ds}-V_{ds}$  characteristics in DC and pulsed conditions. The difference in  $I_{ds}-V_{ds}$  characteristics in DC and pulsed mode is referred as gate-lag and are commonly related to surface traps.<sup>24,25</sup> In this method, we applied a trap filling short pulses of 500  $\mu$ s to the AlN insulated gate with duration of 50 ms. Under pulsing condition, the gate was quiescent biased at -5 V ( $V_{gs-q} < V_{th}$ ) and the drain current was measured. Figs. 6(a) and 6(b) shows the current collapse observed on MIS-HFETs A and B respectively. The DC  $I_{ds-max}$  of MIS-HFET A was perhaps slightly lower than B, due to increase in ohmic contact resistance. This can be overcome by recess etching and making ohmic contacts in the AlGaN layer.<sup>26</sup> However, under gate stress conditions the MIS-HFET A showed less degradation of  $I_{ds-max}$  than MIS-HFET B.

Figure 7 shows the  $I_{ds-max}$  degradation (in %) as observed from gate-lag measurements for MIS-HFETs A and B respectively. The MIS-HFET B showed a large decline of  $I_{ds-max}$  ( $\sim 26$  %) with an increased on state resistance ( $R_{on}$ ) of 33 % under gate stress conditions. On the other hand, the MIS-HFET A showed a less degradation of  $I_{ds-max}$  ( $\leq 5$  %) and  $R_{on}$  of 0.75 % under gate stress conditions. This can be attributed to the combination of effective passivation of AlGaN surface states and/or the low interface density due to the AlN layer grown at low temperature.<sup>12,18,25,26</sup> In addition, the three terminal *off-state* breakdown voltage ( $BV$ ) measurements on these devices revealed a high  $BV \sim 302$  V for MIS-HFET A in contrast to a low  $BV \sim 274$  V for MIS-HFET B (see supplementary material for three terminal off state  $BV$  characteristics).<sup>27</sup> This can be explained on the basis that high trap state density in MIS-HFET B was accompanied by high electric field and a low  $BV$ . The breakdown voltage decreases with increase in defect states.<sup>28</sup> These results shows that low temperature ( $T_G \sim 600$  °C) *in-situ* MOCVD grown AlN layer offers better device characteristics under gate-stress conditions and high  $BV$  due to less defect states as observed from the conductance measurements.

#### IV. CONCLUSIONS

In summary, the trapping properties of *in-situ* MOCVD grown AlN/AlGaN/GaN MIS-HFETs with AlN layers grown at 600 and 700 °C has been quantitatively analyzed by frequency dependent

conductance technique. The AlN and AlGa<sub>N</sub> related traps were identified for both the devices and were one order of magnitude lower for MIS-FET grown at 600 °C. They exhibited a minimum  $D_{T-AlN}$  and  $D_{T-AlGaN}$  of  $1.1 \times 10^{11}$  and  $1.2 \times 10^{10} \text{ cm}^{-2}\text{eV}^{-1}$  with characteristic energy levels at -0.47 and -0.36 eV below the conduction band. Further, gate-lag results revealed less ( $\leq 5$  %) degradation of  $I_{ds-max}$  compared to the MIS-FET grown at 700 °C which exhibited ( $\sim 26$  %) degradation of  $I_{ds-max}$  due high  $D_{T-AlN}$  and  $D_{T-AlGaN}$  of  $3.4 \times 10^{12}$  and  $5 \times 10^{11} \text{ cm}^{-2}\text{eV}^{-1}$  located around similar energy levels. A high  $BV$  of 302 V was also observed for MIS-HFET with AlN layer grown at 600 °C. These studies indicate that low temperature growth of AlN layer can favour lesser defect prone AlN based AlGa<sub>N</sub>/Ga<sub>N</sub> MIS-HFETs.

## ACKNOWLEDGMENTS

The author (J. J. F) duly acknowledges the Ministry of Education, Culture, Sports, Science and Technology (MEXT), Government of Japan for the award of the doctoral fellowship (Grant No. 090028).

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