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Analyses of hetero-interface trapping properties in AlGaN/GaN high electron mobility transistor heterostructures grown on silicon with thick buffer layers

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We report on the analyses of trapping properties of metal-organic chemical vapor deposition grown AlGaN/GaN high-electron-mobility transistor (HEMT) heterostructures on silicon with increasing buffer thickness (T_{buff}). An exact exponential dependence of AlGaN/GaN hetero-interface trap time constants with gate bias was observed in the vicinity of threshold voltage. A low hetero-interface state density (D_{it}) value of $\sim 2.5 \times 10^{10}\,cm^{-2}\,eV^{-1}$ was achieved for heterostructures grown by using thick $T_{buff} \sim 5\,\mu m$ against a D_{it} value of $\sim 1 \times 10^{11}\,cm^{-2}\,eV^{-1}$ for a similar heterostructures grown with thin $T_{buff} \sim 1.25\,\mu m$. Further, the high resolution x-ray rocking curve and Van der Pauw-Hall measurements also confirmed that increasing the T_{buff} improves the AlGaN/GaN HEMT heterostructures with reduced edge dislocation densities and enhanced carrier transport properties. © *2012 American Institute of Physics*. [http://dx.doi.org/10.1063/1.4733359]

In recent years, there has been tremendous research interest in GaN based high-electron mobility transistors (HEMTs) grown on silicon substrate for its low cost, high power, and high frequency applications.[1–4] However, the growth of high quality AlGaN/GaN/Si HEMTs is still challenging due to large dislocations and defects arising out of large lattice mismatch (~17%) for GaN on silicon. The trap states in these AlGaN/GaN HEMTs that are responsible for current collapse further limit their performance in high-speed power switching devices. These traps can be classified into two kinds, namely, fast and slow traps based on their trap time constants by conductance measurements.[5–7] The slower traps are mainly surface related and are present along the access region between the gate and drain electrodes. Further, they can be minimized by using a passivating material. Recently, a variety of such materials like Al_2O_3, SiN, AlN, etc. and their post deposition annealing conditions have considerably reduced the slow surface related traps.[8–10]

Nevertheless, these passivating films have no effects on the fast traps. This shows that the location of the fast traps can be in close proximity to the AlGaN/GaN hetero-interface near the channel. The AlGaN/GaN hetero-interface traps usually have shorter time constant ($\sim\mu s$) for trapping/detrapping process. Apparently, location of these fast traps in the hetero-interface near channel has also been confirmed by techniques like backgating current deep level transient spectroscopy (DLTS),[10] noise spectral studies,[11] and frequency dependent conductance analyses.[12] Unfortunately, not many reports are available for minimizing these AlGaN/GaN hetero-interface traps and/or interface roughness in AlGaN/GaN/Si HEMT heterostructures by improving the hetero-epitaxial growth conditions.

In this letter, we present a systematic study on the interface trapping properties and consequent improvements in metal-organic chemical vapor deposition (MOCVD) grown AlGaN/GaN HEMT heterostructures on silicon (111) by increasing the buffer layers thickness.

The AlGaN/GaN HEMT heterostructures discussed were all grown using Taiyo Nippon Sanso SR 4000 MOCVD system. The thickness of the undoped AlGaN barrier layer and Al composition were fixed as 25 nm and 26%, respectively. The undoped GaN layer thickness (T_{GaN}) for all the heterostructures was 1 μm. In order to investigate the AlGaN/GaN hetero-interface properties, an increasing sequence (1.25–5 μm) of GaN/AlN (20/5 nm) buffer layers thickness (T_{buff}) was used. All these layers were grown at high temperature. The total epilayer thickness (T_{tot}) given by ($T_{tot} = T_{GaN} + T_{buff}$) will be used in further discussions. Figure 1 shows the schematic representation of MOCVD grown AlGaN/GaN HEMT device.

The crystal quality of GaN layer with increasing T_{buff} were analyzed by measuring (0004) and (10-10)

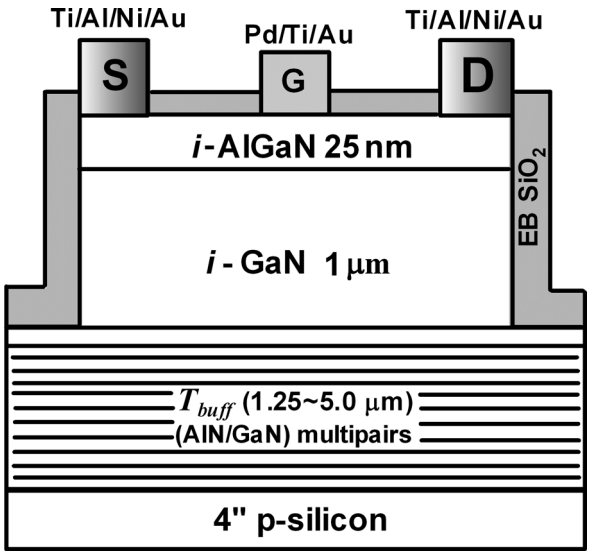

FIG. 1. Schematic representation of AlGaN/GaN HEMT device grown with increasing buffer layers thickness.

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crystallographic reflections by high resolution x-ray rocking curve (HR-XRC) measurements using Philips X′pert x-ray diffractometer. The calculated screw dislocation density for AlGaN/GaN heterostructures with various T_{tot} was around $\sim 1.5 \times 10^9\,cm^{-2}$. Meanwhile, the calculated edge dislocation density ($D_{D\text{-}edge}$) was found to decrease considerably with increasing T_{tot} and was low ($\cong 52\%$) for the heterostructures with thicker T_{tot} as shown in Fig. 2. A thicker T_{buff} can overcome the large lattice mismatch between the silicon substrate and the active device region. This is reasonable because the advantages of thicker buffer layers include smoother growth fronts (smoother interface near the channel) and reduced dislocations and defects.[13,14]

Low temperature (77 K) Hall measurements for these heterostructures yielded high carrier densities in the range of $\sim 0.8 \times 10^{13}\,cm^{-2}$ with an increasing carrier mobility (μ_H) values for thicker T_{tot}. A plot of μ_H measured as a function of T_{tot} is also shown in Fig. 2. As seen in the figure, the μ_H was enhanced by 50% for AlGaN/GaN HEMT heterostructures grown on thick $T_{buff} \sim 5\,\mu m$, compared to heterostructures grown on thin $T_{buff} \sim 1.25\,\mu m$. The increase in μ_H is also attributed to good quality AlGaN/GaN heterostructures relatively with a smoother hetero-interface resulted by increasing the T_{buff}. A high concentration of dislocations/defects at the hetero-interface can ultimately limit the μ_H due to interface roughness scattering. The increases in carrier mobilities are often expressed in terms of increase in the epilayers thickness, reduced dislocations and defects, and interface roughness.[13–17] Moreover, Jena *et al.*[18] have also showed the dependence of mobility and dislocation density with an extremely good approximation by the expression $\mu^{2D} \propto n_s^{3/2}/N_{dis}$. In this equation, μ^{2D} is the two dimensional electron gas (2-DEG) mobility, n_s and N_{dis} are 2-DEG concentration and dislocation densities, respectively.

To characterize the trapping properties especially near the AlGaN/GaN hetero-interface, frequency dependent conductance analyses were employed near the depletion region. Trap detection near the AlGaN/GaN interface or the channel is very much possible by conductance analyses for selected gate bias in the depletion region.[11,12] The device fabrication for the heterostructures started with mesa isolation using BCl_3 plasma based reactive ion etching (RIE). A 100 nm thick electron beam evaporated SiO_2 was used for device passivation. Ohmic patterns were performed using UV-photolithography followed by metallization of Ti/Al/Ni/Au (15/80/12/40 nm). The Ohmic contacts were annealed at 850 °C using infra-red lamp annealing for 30 s in N_2 ambient. The Schottky gate and contact metals Pd/Ti/Au (40/20/60 nm) were finally deposited. Circular shaped Schottky diodes of uniform area ($7.07 \times 10^{-4}\,cm^2$) were used for the conductance measurements.

Capacitance voltage (C-V) and conductance voltage (G-V) measurements were performed between frequency ranges 1 kHz and 5 MHz by sweeping the gate bias (V_g) using Agilent B1505 power device analyzer. The amplitude of ac signal was fixed as 20 mV, and the measurement period was long, so that small signal conditions were maintained. The normalized C-V curves measured at 100 kHz showed a sharp transition from accumulation to depletion region for all devices as shown in Fig. 3. As seen, a small negative shift in threshold voltage ($\Delta V_{th} \sim 0.12$ V) was observed on increasing the T_{tot}. This can be explained in terms of AlGaN/GaN heterostructures grown on thicker buffer layers which can increase the 2-DEG carrier density in the channel. Then a higher voltage would be required to pinch off the channel.[19,20]

To evaluate the trapping parameters quantitatively, the equivalent parallel conductance/angular frequency (G_p/ω) values near the depletion region can be fitted to the equation[1,2,7,8]

$$\frac{Gp}{\omega} = \frac{qD_T}{2\omega\tau_t}\ln[1 + (\omega\tau_t)^2], \tag{1}$$

where D_T and τ_t are the trap densities and trap time constants which are parameters evaluated by fitting the experimental G_p/ω values. As shown in Fig. 4, typical G_p/ω fitting curves against ω for selected gate voltages near the depletion region ($V_g < V_{th}$) showed an excellent agreement with the experimental G_p/ω results. Both slow traps as well as AlGaN/GaN hetero-interface traps were identified and evaluated. The densities of slow traps (D_{st}) were in the order $\sim 0.5 \times 10^{12}\,cm^{-2}\,eV^{-1}$ with slow trap time constant (τ_{st}) range between 0.3 and 1 ms. These D_{st} values are lower for AlGaN/GaN HEMTs without a gate insulating layer.[7,8]

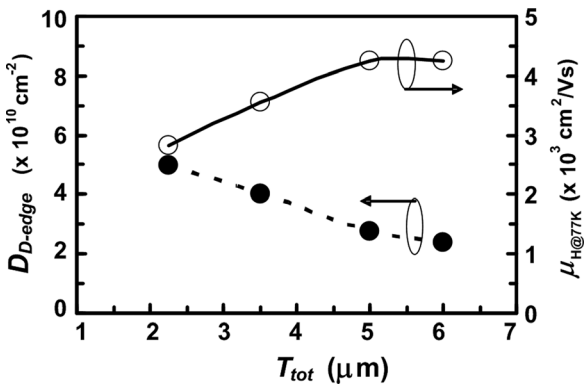

FIG. 2. Plot of calculated edge dislocation densites from XRC results and measured carrier moblities versus total epilayer thickness for AlGaN/GaN HEMT heterostructures grown with increasing buffer layers thickness.

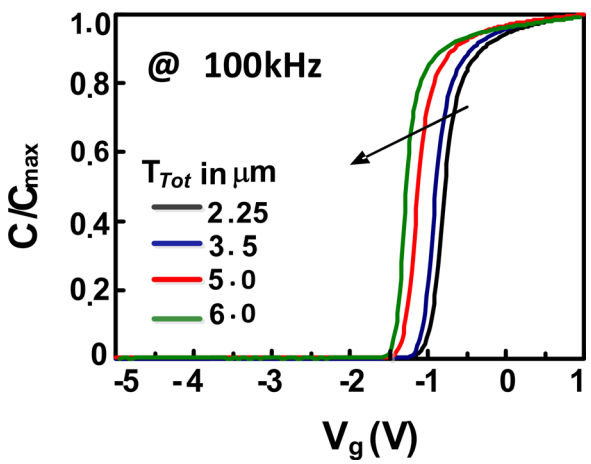

FIG. 3. Normalized C-V curves of AlGaN/GaN HEMT heterostructures grown with increasing buffer layers thickness.

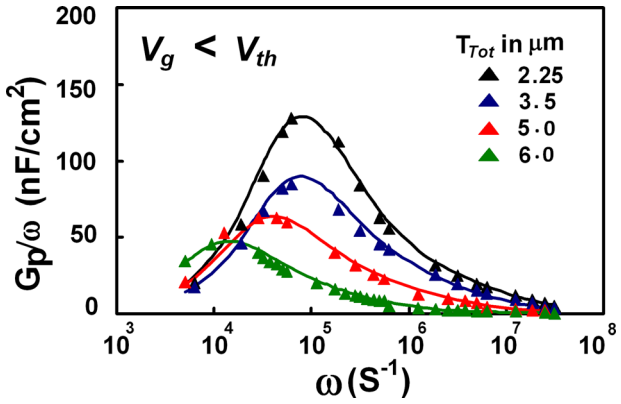

FIG. 4. Parallel conductance as a funciton of radial frequency at selected gate voltages near depletion region for AlGaN/GaN HEMT heterostructures with increasing buffer layers thickness. Solid lines represent the fitting curves of experimental G_p/ω values.

On the other hand, the AlGaN/GaN hetero-interface trap time constants (τ_{it}) of these devices showed exactly an exponential dependence on the gate bias ($\tau_{it} \propto \exp V_g$) near the depletion region $\sim V_g \leq V_{th}$ as shown in Fig. 5. This indicates the presence of continuum of hetero-interface trap states. Also, these electrically active traps may represent material imperfections such as impurities or point defects, dislocations, etc. that are capable to capture and emit charge carriers with a specific time constant. The evaluated τ_{it} increased with an increasing T_{tot} and were in the range of 0.6–10 μs.

Figure 6 shows the comparison chart of previous and present $D_{it\text{-}min}$ results verses T_{tot} exclusively with similar kind of traps evaluated from conductance analyses. $D_{it\text{-}min}$ is the minimum value of hetero-interface state density that can be extracted near the depletion region. The τ_{it} in this study and in the references was well within the comparable range between 0.1 and 10 μs. In addition, the composition in Al_x GaN layer was $x \geq 20\%$ and the barrier layer thickness considered was also reasonable. A $D_{it\text{-}min}$ value of $2.5 \times 10^{10}\,cm^{-2}\,eV^{-1}$ was observed for AlGaN/GaN heterostructures grown with $T_{tot} \sim 6\,\mu m$. In contrast, the $D_{it\text{-}min}$ value for similar heterostructures with thin $T_{tot} \sim 2.25\,\mu m$

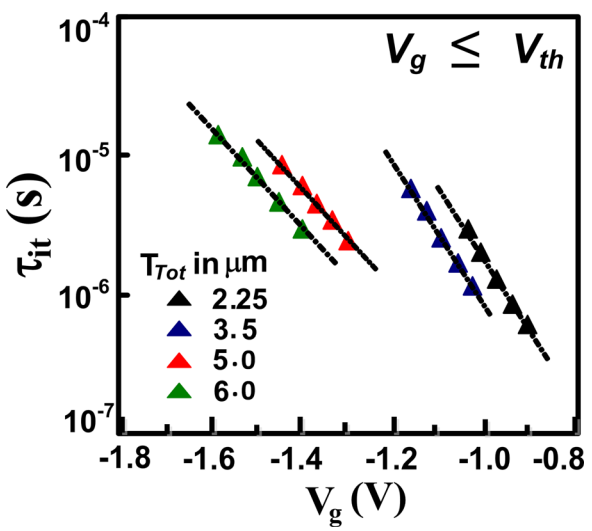

FIG. 5. Interface trap time constants as a funciton of gate voltages in the vicinity of depletion region for AlGaN/GaN HEMT heterostructures grown with increasing buffer layers thickness.

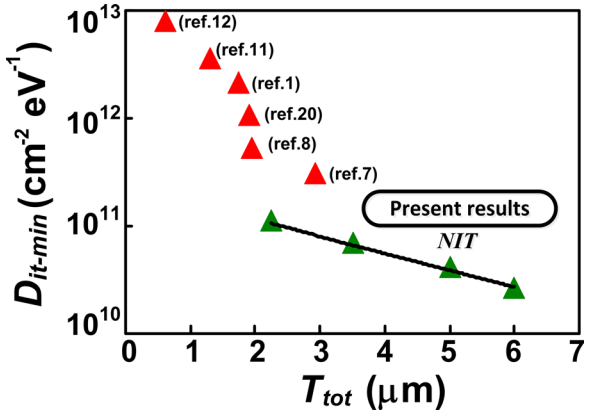

FIG. 6. A comparision chart of hetero-interface state density ($D_{it\text{-}min}$) for AlGaN/GaN HEMT heterostructures from conductance analyses versus total epilayer thickness. The AlGaN/GaN HEMT heterostructures in this work were all grown using thick AlN/GaN multilayers. The solid line represents the exponential fitting for $D_{it\text{-}min}$ versus total epilayer thickness.

was $1 \times 10^{11}\,cm^{-2}\,eV^{-1}$. However, this value is low when compared to heterostructures ($T_{tot} \leq 3\,\mu m$) grown without the multipairs of AlN/GaN buffer layers.[7] A significant decline in $D_{it\text{-}min}$ by nearly an order was evident with an exponential dependence on T_{tot}. From the slope of $D_{it\text{-}min}$ against T_{tot}, it was found that the interface traps concentration decreased by a factor of $\cong 2 \times 10^{10}\,cm^{-2}\,eV^{-1}$ per unit increase in T_{tot} (in μm). Ultimately, the reduced $D_{D\text{-}edge}$ and $D_{it\text{-}min}$ with an increasing T_{tot} further suggests that dislocations or extended line defects can be a factor that influences the AlGaN/GaN hetero-interface traps. The presence of extended defects due to dislocations mostly located at the AlGaN/GaN hetero-interface was also confirmed by Fourier Transform (FT-DLTS) technique.[21] Therefore, good quality MOCVD AlGaN/GaN HEMT heterostructures were grown using thick buffer layers with reduced $D_{D\text{-}edge}$ as observed from the XRC results as well as smoother interface with low $D_{it\text{-}min}$ value as evident from improved carrier transport properties.

In summary, this paper reports on the hetero-interface trapping properties of MOCVD grown AlGaN/GaN HEMT heterostructures on silicon substrate with increasing buffer thickness. The conductance analysis reveals an exact exponential dependence of interface trap time constants on applied gate bias near the threshold voltage. Further, a low $D_{it\text{-}min}$ value of $2.5 \times 10^{10}\,cm^{-2}\,eV^{-1}$ was observed for AlGaN/GaN heterostructure grown using thick buffer layers, $T_{buff} \sim 5\,\mu m$. On contrast, similar heterostructures grown using thin $T_{buff} \sim 1.25\,\mu m$ showed a $D_{it\text{-}min}$ value of $1.0 \times 10^{11}\,cm^{-2}\,eV^{-1}$. The HR-XRC and Van der Pauw-Hall measurements also confirmed that increasing the T_{buff} improves the AlGaN/GaN HEMT heterostructures and its interface properties as evident from reduced edge dislocations and enhanced carrier mobilities, respectively. The present study paves the way for the exploration of GaN devices grown with thick buffer layers on silicon as well as their influence on improvements in the AlGaN/GaN interface and carrier transport properties.

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