Development of Spectroscopic Imaging Arrays Using Epitaxially Grown Thick Single Crystal CdTe Layers on Si Substrates

M. Niraula, *Member, IEEE,* K. Yasuda, *Member, IEEE,* N. Fujimura, T. Tachi, H. Inuzuka, S. Namba, T. Kondo, S. Muramatsu, and Y. Agata

***Abstract*–We present the design and fabrication of a 2D monolithic pixelated detector array using metalorganic vapor-phase epitaxy grown thick CdTe epitaxial layers on Si substrates. Each pixel in the array consists of a p-CdTe/n-CdTe/n^+-Si heterojunction diode structure, and pixels were patterned by cutting deep vertical grooves using a dicing saw. We also developed a low-temperature conductive-epoxy based bonding technique to bond the array to the read out electronic circuit via an interface board. Preliminary evaluation shows that the fabricated array is capable of discriminating energies of the incident radiation and can be applied for the energy discriminating imaging purpose. Moreover, this fabrication technique is useful in developing larger imaging arrays.**

Index Terms- CdTe, epitaxial layers, spectroscopy, x-ray, gamma ray imaging, pixel, array bonding

I. Introduction

CdTe and CdZnTe have emerged as the most promising materials for the development of advanced and high-sensitivity x-ray, gamma ray spectrometers and imaging arrays operable at room temperature. They are in the phase of real applications with a few commercial devices such as x-ray spectrometers as well as photon-counting type imaging sensors based on CdTe/CdZnTe are being developed [1]-[5]. Without any exceptions, these devices are currently developed using melt-grown bulk crystals. Due to the continuous improvement made in the detector-grade bulk crystal growth and the device fabrication technology, performances of these devices have been greatly improved [1]-[5]. However, this improvement has been limited to devices with relatively small dimensions because of the difficulties in the growth of large and uniform single crystals with high-material quality. This hampers the development of large-area imaging arrays tremendously. At present, larger imaging arrays are developed by mounting several carefully-screened small-area independent detectors, or detector modules in mosaic arrays. However, this approach comes at the expense of system cost and the manufacturing complexities. Besides, pixel detectors with very small size and pixel pitches suffer from charge-sharing problem between the adjacent pixels, which leads to the imaging quality degradation [2], [6], [7].

The metalorganic vapor-phase epitaxy (MOVPE) growth of CdTe layers on large-area Si substrates is a promising way to obtain uniform and thick single crystals required for the development of large-area imaging arrays. As the growth is possible at a low substrate temperature compared to the melt-growth temperature, uniform layers with high crystal quality can be obtained. This vapor-phase growth technique further offers flexibilities to control the thickness and the electrical properties of the grown layers because the growth rate as well as the amount of external dopants can be strictly controlled during the growth. Hence, properties of the CdTe layers can be tailored according to the device requirements.

We are studying x-ray, gamma ray detector development using MOVPE grown thick single crystal of CdTe layers on Si substrates for low to medium photon energies up to 100 keV [8]-[11]. We are fabricating spectroscopic detectors in a p-CdTe/n-CdTe/n^+-Si heterojunction diode structure by using 100-260 μm thick single crystal CdTe layers grown directly on the (211) n^+-Si substrates. These detectors are operated in a pulse-mode, with applying a reverse-bias voltage, and they are capable of detecting x-rays, gamma rays and spectrally resolve their energies as already reported [8]- [11].

Currently, we are developing a two-dimensional (2D) monolithic pixelated detector array that possesses spectroscopic and imaging capability using these MOVPE grown thick CdTe layers on Si substrates. We have designed and developed an array fabrication technique that is promising to make larger arrays and offers flexibilities to make pixels with various sizes and pitches, as well as overcomes the charge-sharing problems. Here, we present details on the imaging array fabrication and some preliminary results on the array evaluation.

II. Detector Array Fabrication Details

A. Design and Fabrication of CdTe array

The monolithic pixelated detector array was fabricated using the CdTe epitaxial layers grown directly on the (211) n^+-Si substrates in a custom-designed vertical-type MOVPE reactor. The details about the MOVPE growth of CdTe epitaxial layers, and fabrication and performances of single-element heterojunction diode-type detectors are already reported [8]-[11]. Fig. 1 shows a schematic diagram of the 2D

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Authors are with the Graduate School of Engineering, Nagoya Institute of Technology, Gokiso, Showa, Nagoya 466-8555, Japan (e-mail: m.niraula@nitech.ac.jp).

monolithic pixelated detector array that is being developed. The pixels are patterned by making deep vertical grooves, where each pixel in the array possesses a p-CdTe/n-CdTe/n^+-Si heterojunction diode structure. The detector array is developed by first growing an n-type CdTe buffer layer on the n^+-Si substrate, and then growing a thick undoped p-like CdTe layer. Gold electrodes were then evaporated on the p-CdTe side where the pixels are patterned, as well as on the back side of the n^+-Si substrate which acts as a common electrode. Pixels were patterned on the p-CdTe side as shown schematically in Fig. 1, using a Disco automatic dicing saw that employs a thin diamond blade to groove the crystal surface. Deep vertical grooves were cut in the X-Y directions starting from the gold electrode on the p-CdTe. In order to eliminate the charge sharing problems between the neighboring pixels, the cutting depth of the grooves were extended down to half of the Si substrate. This isolates the pixels by localizing the electric field distribution, and hence prevents the charge movement to the adjacent pixels even for smaller sized pixels where the charge sharing becomes problematic. We fabricated (2x2) and (8x8) arrays, which typically consists of 1.12 mm x 1.12 mm sized pixels in a 1.27 mm pixel pitch. Although, pixels with various sizes and pitches can be developed by using our fabrication technique, however, we choose this pixel size and pitch based on the pitch of the metal pads on the interface board that is used for array bonding.

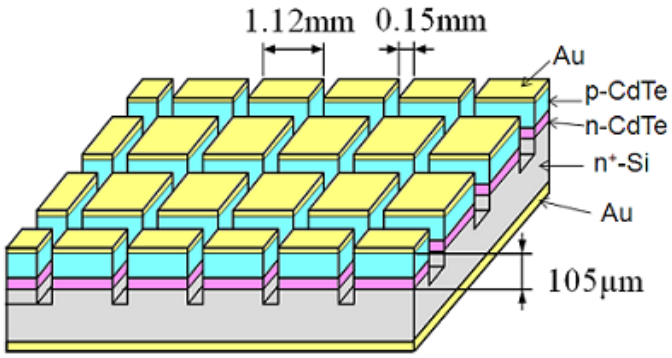

Fig. 1. Schematic diagram of the 2D pixelated detector array. Each pixel consists of a p-CdTe/n-CdTe/n^+-Si heterojunction diode structure. Pixel patterns are formed by cutting deep grooves using a dicing saw. The depth of the vertical grooves has been extended down to half of the Si substrate to isolate the pixels in order to overcome the charge sharing problem.

B. Array Testing System

These detector arrays are operated in a reverse-bias mode by applying a positive voltage on the common electrode. Prior to bonding the arrays to the application specific integrated circuits (ASIC), we measured the reverse biased leakage current from all the pixels in the arrays using probe test system. The system consists of a central movable stage and probe tips, both of them can be moved in the X, Y and Z directions through the micrometer controlled motions. The probes are connected to an Agilent power device analyzer (B1505A) capable of measuring down to the sub-picoampere range. The array is placed on the central stage, and bias voltage in the range of 0 to 250 V was applied to the pixel under test through the probe-tips. The process is then repeated for the entire pixels in the array.

We bonded the (8x8) detector array to the readout ASIC through an interface board. The glass-epoxy interface board has an array of metal pads corresponding to the detector array pixel pitch on the front side. The reverse side of the board has a pin-grid array (PGA) connected through the filled vias. The PGA can be easily plugged into the sockets of the ASIC to make the electrical connection. We used a silver-filled conductive epoxy based low-temperature (~60 ^oC) process to bond the detector array into the interface board. Fig. 2 shows a photograph of the array bonded on the board. This assembly is then plugged into the sockets of the readout ASIC. We used custom-designed 64-channel ASIC from Hamamatsu Photonics Corporation [5]. The (2x2) detector array, on the other hand, was mounted on a TO-8 metal-can package. The detector performance was evaluated at room temperature using ^{241}Am radioisotope as well as white X-rays from a copper target.

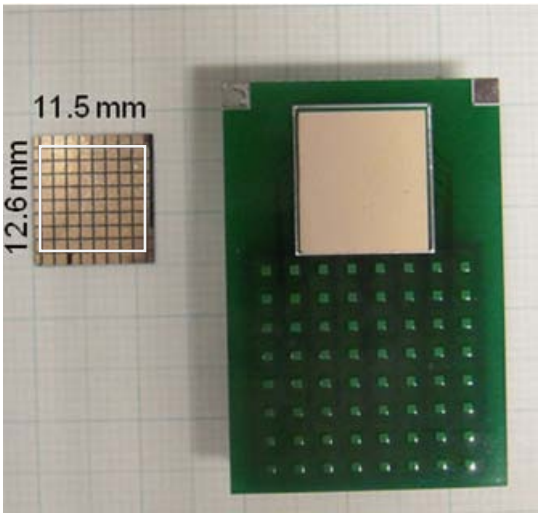

Fig. 2. Photograph of the (8x8) detector array (portion marked) before bonding to the glass-epoxy interface board (left), and after bonding (right). The board has bonding metal pads arranged in a pitch similar to that of the pixel pitch. The detector is bonded upside down position, and the backside full area electrode is visible in the figure. The reverse side of the board (not visible in this figure) has a pin grid array which can be easily plugged into the sockets of the ASIC.

III. Results and Discussion

We measured reverse biased leakage currents at room temperature from the entire pixels in the (2x2) and the (8x8) arrays using the probe test system. Fig. 3(a) shows leakage current density as a function of applied reverse bias measured from three pixels selected randomly from the (8x8) array. All pixels show similar trends of leakage current densities as a function of the applied voltages. The leakage current density shows a square-root dependence with applied reverse bias at

lower voltages (up to 50 V), but the dependence becomes linear and then turns towards higher power dependence at higher voltages. This indicates that generation current from the depletion layer is prominent at lower voltages, while surface leakage current and other current mechanisms becomes prominent at higher voltages [8]. Shown in Fig. 3(b) are the leakage current densities from the entire 64 pixels of the (8x8) array at fixed applied reverse bias of 150 V at room temperature. Most of the pixels in the array exhibit average leakage current density of about 0.3 μA/cm^2. It was observed that the inner pixels had lower values of leakage current density when compared to the outer edge pixels of the array. We found that leakage current exhibited a dependence with the epitaxial layer thickness. The variation of the leakage current and ways to make them uniform is reported in [12]. Likewise, the leakage current density of all four pixels in the (2x2) array was about 0.2 μA/cm^2 at 150 V applied reverse bias at room temperature.

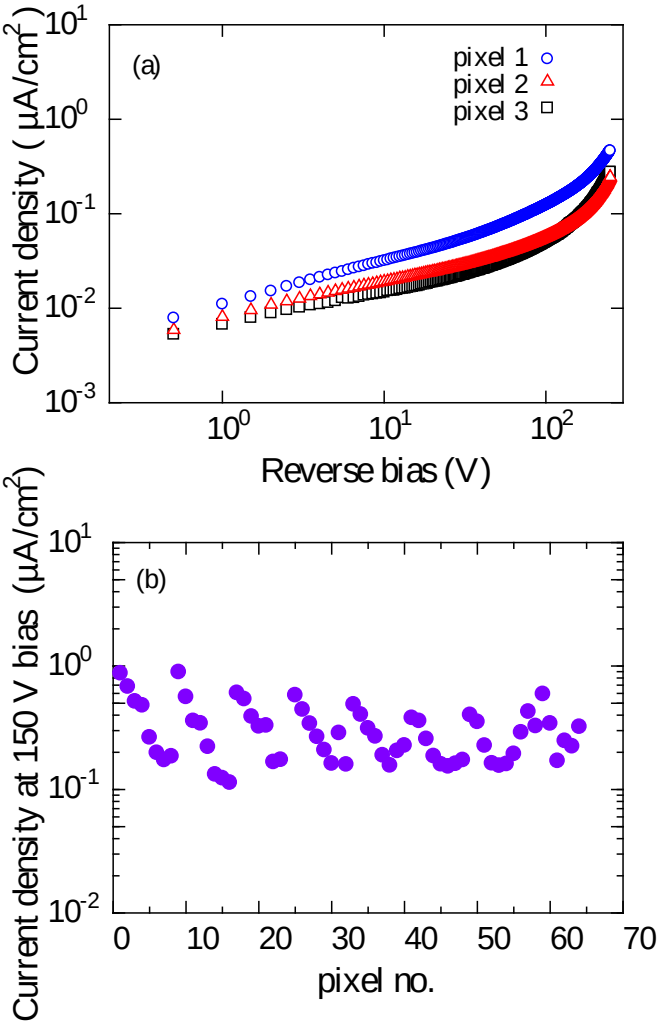

Fig. 3 (a) Reverse dark current (leakage current) density as a function of applied bias for three randomly chosen pixels from the (8x8) array, (b) the leakage current densities measured from all 64 pixels in the array at a fixed bias of 150 V.

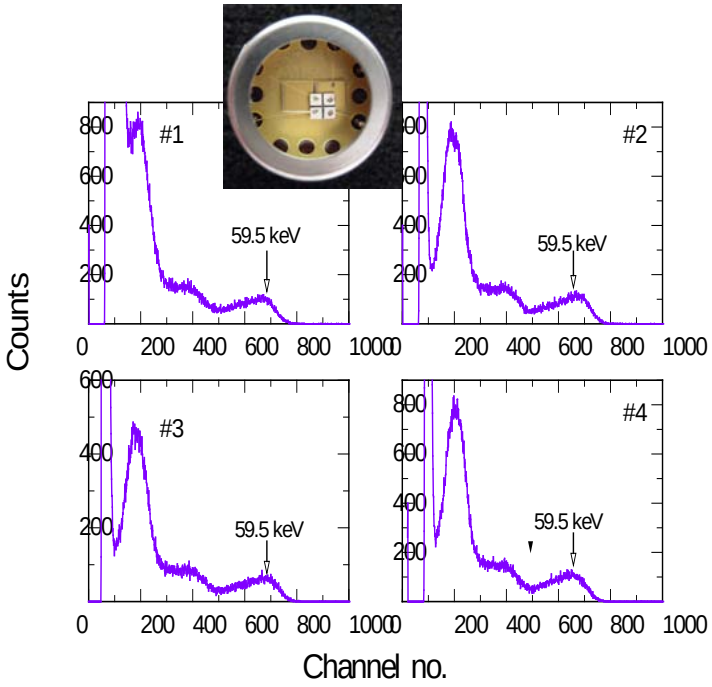

Fig. 4. Spectral performance from all pixels in the (2x2) array measured at room temperature with an ^{241}Am radioactive source. Each pixel was biased at 80 V. The inset shows photograph of the (2x2) detector array mounted on a TO-8 metal-can package

Fig. 4 shows spectral performance of the pixels from the (2x2) array measured at room temperature. The detector array was mounted on a TO-8 metal-can package. The spectra were collected using a standard set of preamplifier, shaping amplifier and multichannel analyzer. A reverse bias of 80 V was applied on the common gold electrode on the n^+-Si side, while the signal from the collecting pixel was fed to the preamplifier, while all other non-collecting pixels remained open. A shaping time of 1 μs was used to collect these spectra. Gamma rays from a 2.81Mbq ^{241}Am radioisotope source were irradiated to the array without using a collimator, where the source to array distance was approximately 2 cm. Similar process was repeated for all 4 pixels to measure their spectral performances individually. Fig. 4 shows that all pixels from the array are capable of resolving peaks from the ^{241}Am radioisotope. The peak located near ch. 700 could be identified as the 59.5 keV peak, however, exact identification of other two peaks located near ch. 200 and 400 is difficult. It is more likely that peak located near ch. 200 is due to Np X-rays (various peaks at 13.9, 17.8, 20.8 keV merged together), while that near ch 400 is due to Cd, and Te escape X-rays peaks merged with ^{241}Am 26.3 keV peak. The initial performance test of the array shows uniformity of the spectral response throughout the pixels, which is one of the important criteria for the imaging array. However, the full energy peaks detected from the array are broad with low counts and high backgrounds because the thickness of the CdTe layer and the applied bias are not sufficient. Cooling the detector and increasing the applied bias should improve their performances as confirmed earlier for single element detectors [8].

The X-ray response from the (8x8) array was evaluated next. The array was bonded to a glass-epoxy interface board and connected to the ASIC as described in Section II. Each channel of the 64-channel ASIC consists of a low-noise amplifier. The output signal from each channel is sent to 5 comparators operating at different threshold levels (energy thresholds). The five levels of the comparators can be easily set externally based on the pulse height of the output signal. Each comparator output is then fed to 16-bit digital counter. The 320 counters are read out sequentially over the data bus. We used white X-ray (generator operated at 50 kVp, 1mA) which was flood irradiated to the array. The distance between the X-ray source and the array was about 20 cm.

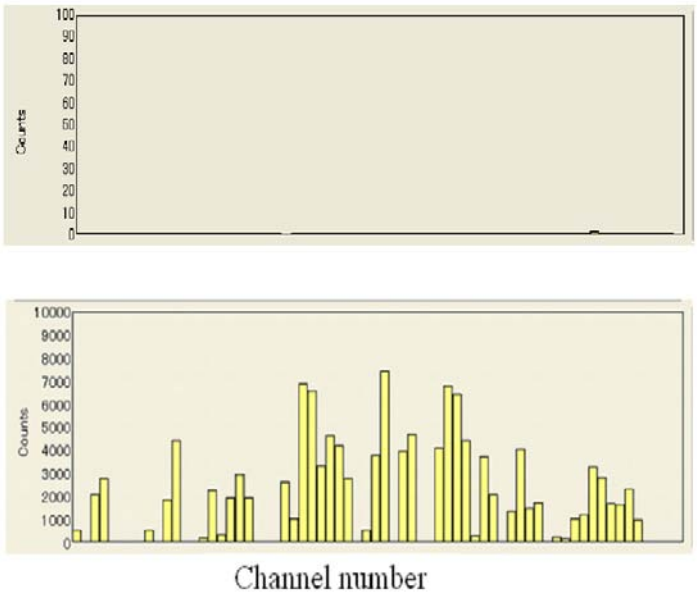

Fig. 5. Output signal obtained from the array without x-ray irradiation (top), and with x-ray irradiation (bottom). The array was biased at 150 V. The x-axis of the bar graph represents channel (pixel) numbers.

Fig. 5 shows the output signal from the array obtained without x-ray irradiation and during x-ray irradiated conditions. The measurement was performed at room temperature and the array was biased at 150 V. We adjusted the threshold voltage level of the comparators in order to eliminate the background and the electronic noise of the system. As a result, there are no signal counts at the dark condition (no x-ray irradiation) at the set threshold level (Fig. 5 (top)). On the other hand, x-ray irradiation results signal counts as in Fig. 5 (bottom). The result, obtained at the same threshold level as that of the dark condition, shows most of the pixels from the array exhibit output signal counts corresponding to the set threshold level. However, there are missing counts from 14 pixels. In order to identify the problem, we re-measured the *I-V* characteristics of the bonded (8x8) array at room temperature. We found that 13 pixels out of 14 had bad electrical connection between the pixels and the bonding pads of the interface board, whereas the problem of the remaining one pixel was due to a problem in the ASIC channel. Moreover, the height of the output signal in Fig. 5 is not uniform as the measurement was performed without adjusting the offset levels of the ASIC channels. At this point, we just wanted to make sure that the system functions well, and can be used for energy discriminating imaging purpose.

Preliminary evaluation revealed that the detector array could clearly discriminate different energies in the incident x-ray spectrum by reading output signals set at different energy thresholds. However, the actual imaging capability of the array was not satisfactory due to the bad pixels in the array resulted from the inefficient electrical connection between the pixels and the metal pads of the interface board. We found that uneven surface of the metal pads was responsible for the poor bonding. The bonding yield could be improved by adjusting the volume of epoxy dispensed and the curing time. Further optimization of the array bonding technique as well as investigation of imaging properties of the array are in progress.

IV. Conclusions

We presented the details about the design and the fabrication of spectroscopic imaging arrays using metalorganic vapor-phase epitaxy grown thick CdTe layers on n^+-Si substrates. The (2x2) and (8x8) arrays consist of a p-CdTe/n-CdTe/n^+-Si heterojunction diode type structure, where pixels are patterned by cutting deep vertical grooves from the CdTe side using a dicing saw. This pixel pattering isolates pixels from the adjacent pixels, and helps to overcome the charge sharing problem between them. We typically made 1.12x1.12 mm^2 pixels in a 1.27 mm pitch. We further developed a low temperature conductive-epoxy based technique to mount the patterned array on to an interface board, which was then plugged in to the ASIC. Preliminary evaluation of the array showed the average dark current from the entire 64 pixels from the (8x8) array was 0.3 $\mu A/cm^2$ at an applied bias of 150 V at room temperature. They were capable of discriminating energies of the incident photons, and can be applied for spectroscopic imaging applications by setting different energy threshold levels. The array fabrication process described here is promising to make larger arrays and offer design flexibilities to make pixels with various sizes and the pitches for spectroscopic imaging applications.

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