Fabrication and Characterization of X-Ray Spectroscopic Imaging Arrays Based on Thick Single Crystal CdTe Epitaxial Layers

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***Abstract*— We present the design and fabrication details of x-ray spectroscopic imaging arrays using metalorganic vapor-phase epitaxy grown thick single crystal CdTe layers on n^+-Si substrate. Each pixel in the array consists of a p-CdTe/n-CdTe/n^+-Si heterojunction diode structure, which was fabricated by subsequently growing n-and p-CdTe layers on the n^+-Si substrate. A mechanical dicing process using a diamond blade was used to make deep cuts on the p-CdTe side to define the pixels in a (8x8) array. We further developed a low-temperature conductive-epoxy based bonding technique to bond the array to the read out electronic circuit via an interface board. Preliminary evaluation shows that the array fabrication technique and the bonding technique work good, and the array is capable of discriminating energies of the incident photon and can be applied for the energy discriminating imaging purpose.**

***Index Terms*— CdTe epitaxy, spectroscopic imaging array, x-ray, gamma ray detector, pixel patterning**

I. Introduction

CdTe and CdZnTe have established themselves as the most preferred material for the development of advanced and high-sensitivity room temperature x-ray and gamma ray detectors. There are several reports on the development of spectroscopic detectors as well as photon-counting type imaging arrays, which demonstrate their excellent energy resolution and spectroscopic imaging capabilities [1-5]. Without any exceptions, these devices are currently developed using melt-grown, either Bridgman or Travelling Heater Method, bulk crystals [1-5]. Due to the continuous improvements made in the crystal growth and device fabrication technology, the performance of these devices has been greatly improved. However, this improvement has been limited to devices with relatively small dimensions because of the difficulties in the growth of large and uniform single crystals with high-materials quality. This limited availability of large single crystals makes the development of large-area imaging arrays a tremendously challenging job. At present, the most common way of constructing a larger imaging detector array is by tiling several carefully-screened small-area independent detectors, or pixelated detectors in mosaic array [4,6,7]. In these approaches, independent detectors are obtained by carefully selecting and dicing out small area detectors having full-area electrodes on both sides from the crystal wafers, whereas pixelated detectors are fabricated by depositing full-area electrode on one surface and segmented electrodes on the opposite face using photolithography. However, this approach comes at the expense of system cost and the manufacturing complexities as CdTe or CdZnTe crystals are very fragile and highly vulnerable to suffer from the manufacturing process-induced damage. Besides, there is yet another problem with pixelated detector. Pixel detectors with small pixel size and pitches, which are required in imaging detector to improve the spatial resolution, suffer from the charge-sharing problem [3, 8-10]. This problem, where the induced charge is shared between multiple pixels, results in a degradation of the imaging performance of the detectors.

The vapor-phase growth of thick single crystal CdTe epitaxial layers on large-area Si substrates by metalorganic vapor-phase epitaxy (MOVPE) technique is a promising way to obtain large and uniform crystals for the imaging array development. As the growth is possible at a low substrate temperature compared to the melt-growth temperature, uniform layers with high crystal quality can be obtained. This vapor-phase growth technique further offers flexibilities to control the thickness and the electrical properties of the grown layers because the growth rate as well as the amount of external dopants can be strictly controlled during the growth. Hence, properties of the CdTe layers can be tailored according to the device requirements.

We have been studying x-ray, gamma ray detector development using MOVPE grown thick single crystal of CdTe layers on Si substrates for low to medium photon energies up to 100 keV [11-14]. Despite a large lattice constant mismatch (about 20%) between the Si and the CdTe, we have succeeded in growing high crystal quality and thick (>260 μm) single crystal CdTe layers directly on (211)Si substrates. The details about the growth are already reported [13-15]. The maximum growth rate

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was about 70 μm/h [13,14]. We further fabricated spectroscopic detectors in a p-CdTe/n-CdTe/n^+-Si heterojunction diode structure by growing a typically 5μm-thick iodine doped n-CdTe layer on the (211) n^+-Si substrates, and then 100-260 μm thick single crystal undoped p-CdTe layers on the top. These detectors are capable of detecting x-rays, gamma rays and spectrally resolve their energies when operated in a pulse-mode, with applying a reverse-bias voltage, as already reported in [11-14].

Currently, we are developing a pixel-type detector array that possesses spectroscopic imaging capability using these MOVPE grown thick CdTe layers on Si substrate and utilizing a mechanical dicing process to define pixels. This approach is promising to make larger arrays and offers flexibilities to make pixels with various sizes and pitches, as well as overcomes the charge-sharing problems. Furthermore, as the CdTe is supported by robust Si substrate, this fabrication technique facilitates the crystal handling and greatly reduces the process-induced damage. Here, we present details on the imaging array fabrication and some results on the array evaluation.

II. Array Fabrication Details

We used single crystal CdTe epitaxial layers grown directly on the (211) n^+-Si substrates in a custom-designed vertical-type MOVPE reactor to fabricate the pixel detector arrays. Our detector possesses a p-CdTe/n-CdTe/n^+-Si heterojunction diode structure as shown schematically in Fig. 1, where an iodine-doped n-CdTe layer and undoped p-CdTe layer were subsequently grown on the highly conductive and typically 300 μm thick n^+-Si substrate. The n-CdTe and the p-CdTe layers were typically 5 μm and 100 μm thick, which were grown at a substrate temperature of 350 ^oC and 560 ^oC, respectively. Finally, gold electrodes were evaporated on the p-CdTe side and on the back side on the n^+-Si substrate. The details about the growth of CdTe epitaxial layers as well our MOVPE growth system are already reported in [11-15].

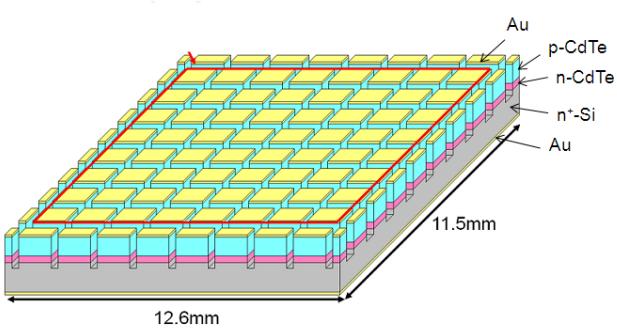

Fig. 1. Schematic diagram of the imaging array. Each pixel in the (8x8) array is 1.12 mm x 1.12 mm, in a 1.27 mm pitch. The pixels are defined using a diamond blade based dicing technique. The square marked portion represents the effective area of the array.

The p-CdTe/n-CdTe/n^+-Si heterojunction diode detector was patterned into pixels array using a mechanical dicing process. We used a diamond blade to pattern pixels on the p-CdTe side. The CdTe crystal dicing or pixel pattering by making cuts on the CdTe surface using a diamond blade is previously reported by our group [11, 16, 17] as well as by others [18, 19]. This technique produces detectors with excellent spectroscopic performance, where detector leakage currents are not affected by the dicing process as confirmed earlier [11, 17]. The pixels are patterned by making deep vertical cuts orthogonally starting from the gold electrode on the p-CdTe side. In order to eliminate the charge sharing problem between the neighboring pixels, we extended the depth of the cuts down to the half of the Si substrate as illustrated in Fig. 1. This isolates the pixels by localizing the electric field distribution, and hence prevents the charge movement to the adjacent pixels to suppress the charge sharing. This concept of making pixels using a diamond blade can be used for making pixels with various sizes and pitches. Currently we are using a 150 μm-thick diamond blade, and we have successfully fabricated array with a pitch as small as 500 μm. However, we are working to reduce it further by using blades of smaller thicknesses and further optimization of the cutting process. In this paper we present results of a (8x8) array, which typically consists of 1.12 mm x 1.12 mm sized pixels in a 1.27 mm pixel pitch. We choose this pixel size and the pitch based on the pitch of the metal pads on the interface board that is used for the array bonding to its photon-counting application specific integrated circuits (ASIC) read-out.

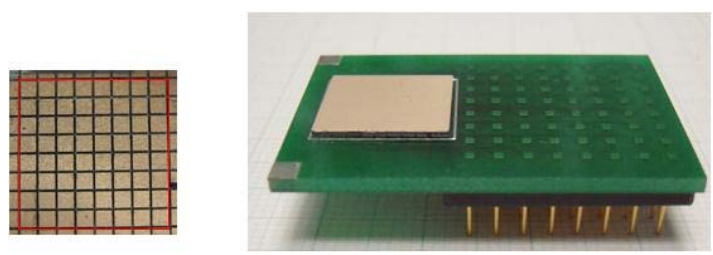

Fig. 2. A photograph showing the (8x8) pixel array before mounting on the interface board (left) and after mounting (right). The array was mounted upside down position, and the backside full electrode is visible on the right photo.

III. Array Bonding and Measurement System

Our detector arrays are operated in a reverse-bias mode by applying a positive voltage on the common electrode. Prior to bonding the arrays to the ASIC read-out, we measured the reverse biased leakage current from all the pixels in the (8x8) arrays using probe test system. The system consists of a central movable stage and probe tips, both of them can be moved in the X, Y and Z directions. The probes are connected to an Agilent power device analyzer capable of measuring down to the sub-picoampere range. Measurement was performed for all

pixels in the array by applying reverse biases from 0 to 200 V, and forward bias from 0 to 30 V at room temperature. We then bonded the (8x8) detector array to the readout ASIC through an interface board. The glass-epoxy interface board has an array of metal pads corresponding to the detector array pixel pitch on the front side. The reverse side of the board has a pin-grid array (PGA) connected through the filled vias. The PGA can be easily plugged into the sockets of the ASIC to make the electrical connection. We used a silver-filled conductive epoxy based low-temperature (~60 ^{o}C) process to bond the detector array into the interface board. A precision-controlled epoxy dispensing unit was used to load small amount of epoxy paste on the metal pads of the mating interface board by placing it inside a custom built mounting jig. The mounting jig helps to align the interface board and the pixel array properly. The pixel array was then aligned onto of the epoxy filled interface board through the mounting jig and pressed gently. Afterward, the assembled array is first kept inside a 60 ^{o}C oven for 2 hr and then at room temperature for curing. We optimized our bonding technique and it gives a good yield. Fig. 2 shows a photograph of the array before and after bonding on the interface board. This assembly is then plugged into the sockets of the readout ASIC. We used custom-designed 64-channel ASIC from Hamamatsu Photonics Corporation [4]. The detector performance was evaluated at room temperature using ^{241}Am radioisotope as well as white x-rays from a tungsten target.

IV. Results and Discussion

Each pixel in the array fabricated possesses a heterojunction diode structure, with a separate gold electrode on the top and a continuous gold electrode on the back side. (see Fig. 1). Fig. 3 shows a typical current-voltage (*I-V*) characteristic which was measured from a single pixel at room temperature. The measurement was performed before bonding the array to its read-out electronics as explained in Section III. It exhibits a good rectification property, where a high current flows when a small positive bias is applied on the CdTe side of the pixel (forward bias), but the current remains low in the opposite case (reverse bias). Shown in the inset is the reverse current plotted in a log-log scale, which shows the current deviates from its square-root dependency (i.e generation current from the depletion region) when the applied bias is increased above 30 V. This suggests surface current and other current mechanisms become dominant. These detectors are operated in the reverse bias mode, as it offers low leakage currents even for higher applied biases. This, in turn, improves the detector charge transport properties. Hence, low reverse bias leakage currents and their pixel-to-pixel uniformity are the important factors for an imaging array. Fig. 4 shows values of the leakage currents from all 64 pixels in the (8x8) array measured at room temperature by applying a reverse bias of 100 V. Most of the pixels exhibit a fairly uniform value of leakage current of about 3 nA, but the value has increased up to 5nA for some pixels mostly locating towards the edge of the array. This could be due to the homogeneity problem of the grown CdTe epilayers as we have discussed previously for the different batch of detector arrays [16] or some problem with mounting and handling the array. Further investigation to make the leakage currents uniform among the pixels is in progress.

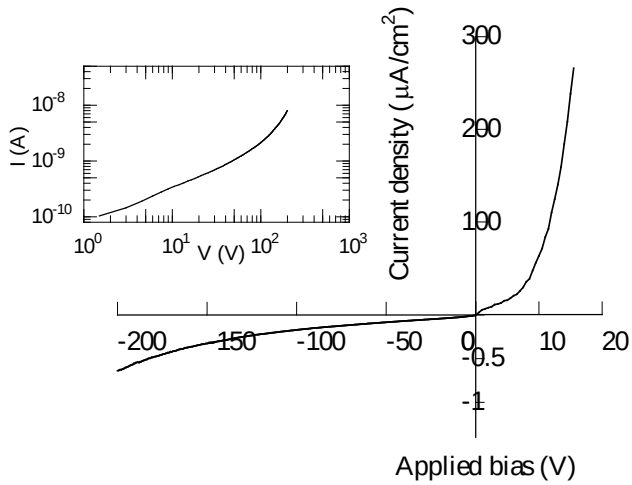

Fig. 3. Typical current-voltage characteristics which was measured from a single pixel in the array at room temperature (please notice the different axis divisions). Shown in the inset is the reverse bias leakage current redrawn in a log-log scale.

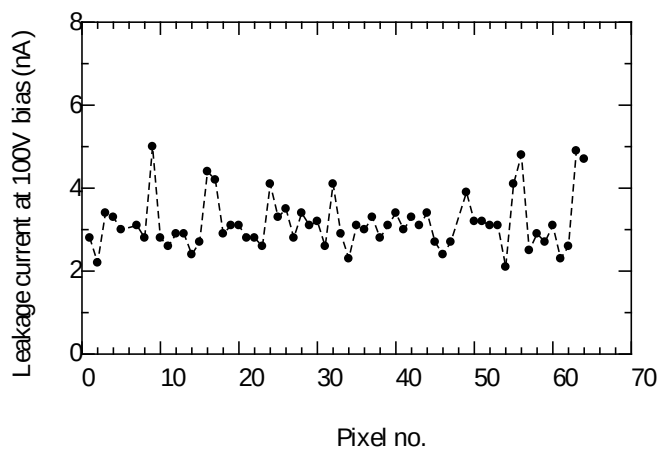

Fig.4. The reverse bias leakage currents from all 64 pixels in the array measured at room temperature for a fixed applied bias of 100V.

We used white x-ray generated from a tungsten target to evaluate the performance of the detector array bonded to the ASIC readout. Each channel of the 64-channel ASIC consists of a low-noise preamplifier. The output signal from each channel is sent to 5 comparators operating at different threshold levels

(energy thresholds). The five levels of the comparators can be set externally based on the pulse height of the output signal. Each comparator output is then fed to 16-bit digital counter. The 320 counters are read out sequentially over the data bus. Fig. 5 shows the pixel-to-pixel counting response of the detector array. It is important that an imaging detector array should have uniform response over the entire area. X-ray was generated by applying a tube current of 1 mA and the tube voltage of 30 kVp. This yields a continuous x-ray spectrum of energies varying from a few keV up to 30 keV. The distance between the x-ray source and the array was about 20 cm, and an aluminum plate was placed between to eliminate soft x-rays. The detector was biased at 100 V. We adjusted the five different threshold voltage levels of the comparators to Th1-Th5, where Th1 corresponds to the background and the electronic noise level of the system. As a result, no counts were detected for this threshold Th1. The count distribution in Fig. 5 shows results for the Th2, which shows satisfactory response uniformity of the array. However, there are missing counts from five pixels (dark black color). It was found that among the five pixels, three had bonding problem, while there was problem with the ASIC channel for the remaining two. On the other hand, increasing the threshold levels to Th3 and above also resulted no counts unless we increased the x-ray flux energies. This result indicates the array can discriminate the energy of the incident photon.

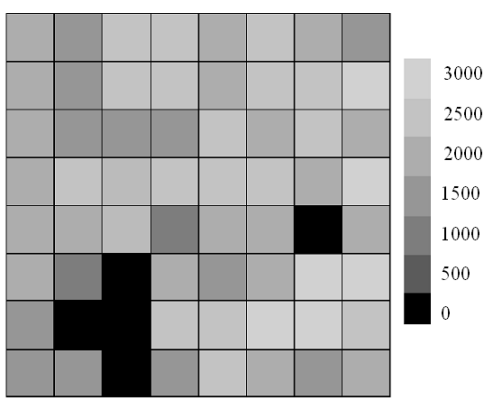

Fig. 5. Counting response of the detector array when irradiated with low energy x-ray (30 kVp, 1mA). The detector was biased at 100V, and counts were recorded form all 64-pixels for a fixed time of 15 s, and mapped. The grey scale value represents the counts recorded per pixel.

The typical pixel counting response of the detector array to increasing x-ray flux is shown in Fig. 6(a). The x-ray flux was varied by changing the x-ray tube current from 1 mA to 4 mA, at a fixed tube voltage of 30 kVp. The detector was biased at 100 V, and all other measurement conditions were similar as in Fig.5. The response shows fairly linear behavior at lower x-ray flux, but it saturates at higher flux. This can be interpreted as a result of the limitation of depletion region growth. At lower x-ray flux, all generated carriers contribute to the response counts. However, increasing the x-ray flux causes excessive charges in the depletion region which could not be removed by the applied field. These accumulated charges then decrease the effective depletion region width. Increasing the detector bias should increase the charge collection efficiency and minimize this effect. This was observed in Fig. 6(b), where varying the detector bias voltage at a fixed x-ray flux (30 kVp, 1 mA) shows a good linear relation between the counts and the detector bias.

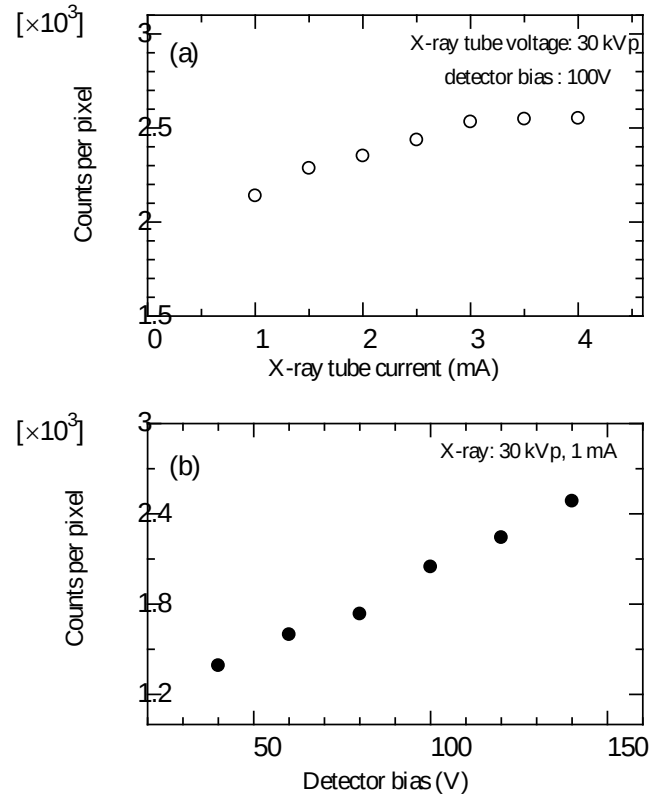

Fig. 6. (a) Typical pixel counting response of the detector array to increasing x-ray flux intensity. The detector was biased at 100V. (b) Dependence of counting response with changing the detector bias. The x-ray flux was fixed (30 kVp, 1mA).

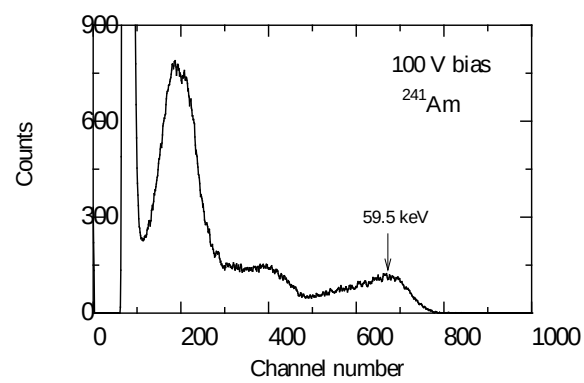

Fig. 7. Typical single-pixel pulse-height spectrum measured with a ^{241}Am radioisotope at room temperature.

Fig. 7 shows a representative ^{241}Am spectrum taken with a single pixel in the detector array at room temperature. The spectrum was collected with a discrete set of preamplifier,

shaping amplifier and the multichannel analyzer. The array was biased at 100 V. The result shows that the detector is capable of detecting gamma rays from the ^{241}Am radioisotope and resolving their energies. Though the full energy peak at 59.5 keV (peak located at Ch 670) could be clearly identified, other peaks associated with lower energy gamma rays as well as the Cd and the Te escape peaks are not individually resolved. Instead they are merged together to produce two group of peaks located at near Ch 200 and 400. Moreover, the full energy peak is broad with low counts, and with high backgrounds. This can be interpreted due to the low detector thickness as well as due to the effect of charge trapping in the detector because of the insufficient applied electric field. Increasing the electric field should improve the charge transport properties, however, the increased detector leakage current limits the further increase of the electric fields in our present detector. Cooling the detector to reduce the leakage current as well as making detector array with higher CdTe thickness to improve the absorption of x-ray, gamma ray in the detector should improve the spectroscopic performance, which are under progress.

Overall, these results confirm that our array fabrication technique and array bonding technique offer a good potential for making larger arrays, and system developed can be used for energy discriminated imaging by setting different energy thresholds. However, to develop imaging arrays for practical applications we need much thicker as well as large-area CdTe epitaxial layers. As explained in section I, we have already achieved more than 260 μm-thick high quality single crystal CdTe epilayers. Currently, we are further optimizing growth temperature and other growth parameters such as flow-rates and flow velocity of metalorganic precursors of cadmium and telluride [16] to increase the growth rate further as well as to obtain large-area uniform crystals to address these challenges for developing working arrays.

V. Conclusion

We presented the details about the design and the fabrication of x-ray spectroscopic imaging array using MOVPE grown thick single crystal CdTe layers on n^+-Si substrate, and some preliminary results on array evaluations. The detector arrays was fabricated in a p-CdTe/n-CdTe/n^+-Si heterojunction diode structure by subsequently growing n-and p-CdTe layers on the n^+-Si substrate. The detector was patterned into pixels array by making deep vertical cuts orthogonally from the p-CdTe side using a diamond blade saw. This pattering process isolates the pixels and thereby helps to overcome the charge sharing problem between the surrounding pixels. We further developed a conductive epoxy based low temperature bonding technique to connect the array to its readout ASIC. Preliminary evaluations of the array in terms of leakage current, bonding efficiency, uniformity of response, as well as energy discriminating properties were encouraging. The array fabrication process described in this paper is very promising to make larger arrays and offer design flexibilities to make pixels with various sizes and pitches for spectroscopic imaging applications.

References

[1] S. Watanabe, S. Ishikawa, H. Aono, S. Takeda, H. Odaka, M. Kokubun, T. Takahashi, K. Nakazawa, H. Tajima, M. Onishi, and Y. Kuroda, "High energy resolution hard x-ray and gamma ray imagers using CdTe diode devices", *IEEE Trans Nucl. Sci.*, vol. 56. pp.777-782, June 2009.

[2] C. Szeles, S. A. Soldber, S. Vydrin, J. Graves, and D. S. Bale, "CdZnTe semiconductor detectors for spectroscopic x-ray imaging", *IEEE Trans. Nucl. Sci.*, vol. 55, pp. 572-582, Feb 2008.

[3] J. S. Iwanczyk, E. Nygard, O. Meirav, J. Arenson, W. C. Barber, N. E. Hartsough, N. Malakhov, and J. C. Wessel, "Photon counting energy dispersive detector arrays for x-ray imaging", *IEEE Trans. Nucl. Sci.*, vol 56, pp. 535-542, June 2009.

[4] Y. Tomita, Y. Shirayanagi, S. Matui, T. Aoki, and Y. Hatanaka, "X-ray color scanner with multiple energy discrimination capability", *Proc. SPIE*, vol. 5922, p. 59220A, Sept 2005.

[5] K. C. Mandal, S. H. Kang, M. Choi, A. Kargar, M. J. Harrison, D. S. McGregor, A. E. Bolotnikov, G. A. Carini, G. C. Camarda, and R. B. James, "Characterization of low defect $Cd_{0.9}Zn_{0.1}Te$ and CdTe crystals for high-performance Frisch collar detectors", *IEEE Trans. Nucl. Sci.*, vol. 54, pp. 802-806, Aug 2007.

[6] I. Mori, T. Takayama, and N. Motomura, "The CdTe detector module and its imaging performance", *Annals Nucl. Med.*, vol. 15, pp. 487-494, 2001.

[7] K. Spartiotis, A. Leppanen, T. Pantsar, J. Pyyhtia, P. Laukka, K. Muukkonen, O. Mannisto, J. Kinnari, T. Schulman, "A photon counting CdTe gamma and x-ray camera", *Nucl. Instr. Meth. A*, vol. 550, pp. 267-277, 2005.

[8] A. E. Bolotnikov, W. R. Cook, F. A. Harrison, A. –S. Wong, S. M. Schindler, and A. C. Eichelberger, "Charge loss between contacts of CdZnTe pixel detectors", *Nucl. Instr. Meth. A*, vol. 432, pp. 326-331, 1999.

[9] G. Pellegrini, M. Chmeissani, M. Maiorino, G. Blanchot, J. Garcia, M. Lozano, R. Martinez, C. Puigdengoles, M. Ullan, and P. Casado, "Performance limits of a 55-μm pixel CdTe detector" *IEEE Trans. Nucl. Sci.*, vol. 53, pp. 361-366, Feb. 2006.

[10] C. Allwork, D. Kitou, S. Chaudhuri, P. J. Sellin, P. Seller, M. C. Veale, N. Tartoni, and P. Veeramani, "X-ray beam studies of charge sharing in small pixel, spectroscopic, CdZnTe detectors", *IEEE Trans. Nucl. Sci.*, early access article (2012) available online 2012DOI:10.1109/TNS.2012.2195678.

[11] M. Niraula, K. Yasuda, K. Noda, K. Nakamura, I. Shingu, M. Yokota, M. Omura, S. Minoura, H. Ohashi, R. Tanaka, and Y. Agata, "Characterization of CdTe/n^+-Si heterojunction diodes for nuclear radiation detectors", *IEEE Trans. Nucl. Sci.*, vol. 54 pp. 817-820, Aug. 2007.

[12] K. Yasuda, M. Niraula, K. Noda, M. Yokota, H. Ohashi, K. Nakamura, M. Omura, I. Shingu, S. Minoura, R. Tanaka, and Y. Agata, "Development of heterojunction diode-type gamma ray detectors based on epitaxially grown thick CdTe on n^+-Si substrates", *IEEE Elect. Dev. Lett.*, vol. 27 pp. 890-892, Nov. 2006.

[13] M. Niraula, K. Yasuda, A. Watanabe, Y. Kai, H. Ichihashi, W. Yamada, H. Oka, T. Yoneyama, H. Nakashima, T. Nakanishi, K. Matsumoto, D. Katou, and Y. Agata, " MOVPE growth of CdTe on Si substrates for gamma ray detector fabrication", *IEEE Trans. Nucl. Sci.*, vol. 56, pp. 836-840, June 2009.

[14] M. Yokota, K. Yasuda, M. Niraula, K. Nakamura, H. Ohashi, R. Tanaka, M. Omura, S. Minoura, I. Shingu, and Y. Agata, "Fabrication and characterization of MOVPE-grown CdTe-on-Si heterojunction diode-type gamma ray detectors", *J. Elect. Mater.*, vol. 37, pp. 1391-1395, Sept. 2008.

[15] M. Niraula, K. Yasuda, H. Ohnishi, K. Eguchi, H. Takahashi, K. Noda, and Y. Agata, "Direct growth of high-quality CdTe epilayers on Si (211) substrates by metalorganic vapor-phase epitaxy", *J. Cryst. Growth*, vol. 284, pp. 15-19, Oct. 2005.

[16] K. Yasuda, M. Niraula, N. Fujimura, T. Tachi, H. Inuzuka, S. Namba, S. Muramatsu, T. Kondo, and Y. Agata, "Dark current characteristics of a radiation detector array developed using MOVPE-grown thick CdTe layers on Si substrate", *J. Elect. Mater.*, (2012) early access available online, DOI: 10.1007/s11664-012-2121-7.

[17] M. Niraula, D. Mochizuki, T. Aoki, Y. Hatanaka, Y. Tomita, and T. Nihashi, "Improved spectroscopic performance of CdTe radiation

detectors in a p-i-n design", Appl. Phys. Lett. , vol. 75, pp. 2322-2324, Oct. 1999.

[18] J. Kalliopuska, S. Nenonen, H. Sipila, H. Andersson, S. Vahanen, S. Eranen, and L. Tlustos, "Patterning thick diffused junctions on CdTe", *Nucl. Instr. Meth. A*, vol. 607, pp. 98-102, 2009.

[19] M. C. Veale, S. J. Bell, L. L. Jones, P. Seller, M. D. Wilson, R. C. Cernik, J. Kalliopuska, H. Pohjonen, H. Andersson, S. Nenonen, and V. Kachkanov, "Characterization of edgeless CdTe detectors for use in hard x-ray imaging applications", *IEEE Trans. Nucl. Sci.*, early access article (2012) available online, DOI 10.1109/TNS.2012.2197025

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