AIP Journal of Applied Physics

Charge transport properties of p-CdTe/n-CdTe/n+-Si diode-type nuclear radiation detectors based on metalorganic vapor-phase epitaxy-grown epilayers

M. Niraula, K. Yasuda, Y. Wajima, H. Yamashita, Y. Tsukamoto, Y. Suzuki, M. Matsumoto, N. Takai, Y. Tsukamoto, and Y. Agata

Citation: Journal of Applied Physics **114**, 164510 (2013); doi: 10.1063/1.4828479
View online: http://dx.doi.org/10.1063/1.4828479
View Table of Contents: http://scitation.aip.org/content/aip/journal/jap/114/16?ver=pdfcov
Published by the AIP Publishing

Articles you may be interested in

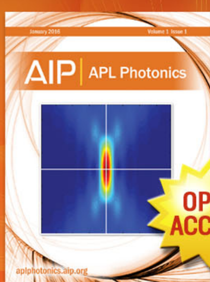
Structural characterization of a -plane Zn 1 − x Cd x O (0 x 0.085) thin films grown by metal-organic vapor phase epitaxy
J. Appl. Phys. **99**, 023514 (2006); 10.1063/1.2163014

High-performance long-wavelength HgCdTe infrared detectors grownon silicon substrates
Appl. Phys. Lett. **85**, 2113 (2004); 10.1063/1.1791740

Optical and structural analysis of ZnCdO layers grown by metalorganic vapor-phase epitaxy
Appl. Phys. Lett. **83**, 3290 (2003); 10.1063/1.1620674

Behavior of hydrogen intentionally introduced by plasma into metalorganic vapor phase epitaxy grown CdTe:As layers
J. Appl. Phys. **88**, 550 (2000); 10.1063/1.373694

Hg 1−x Cd x I 2 /CdTe heterostructures for nuclear radiation detectors: Effect of epitaxial growth on substrate properties
Appl. Phys. Lett. **72**, 2023 (1998); 10.1063/1.121253



Launching in 2016!
The future of applied photonics research is here
AIP APL Photonics

[This article is copyrighted as indicated in the article. Reuse of AIP content is subject to the terms at: http://scitation.aip.org/termsconditions. Downloaded to] IP: 133.68.125.22 On: Fri, 28 Aug 2015 05:45:09

JOURNAL OF APPLIED PHYSICS **114**, 164510 (2013)

Charge transport properties of p-CdTe/n-CdTe/n$^+$-Si diode-type nuclear radiation detectors based on metalorganic vapor-phase epitaxy-grown epilayers

M. Niraula,[a] K. Yasuda, Y. Wajima, H. Yamashita, Y. Tsukamoto, Y. Suzuki, M. Matsumoto, N. Takai, Y. Tsukamoto, and Y. Agata
Graduate School of Engineering, Nagoya Institute of Technology, Gokiso, Showa, Nagoya 466-8555, Japan

(Received 25 July 2013; accepted 16 October 2013; published online 30 October 2013)

Charge transport properties of p-CdTe/n-CdTe/n$^+$-Si diode-type nuclear radiation detectors, fabricated by growing p-and n-type CdTe epilayers on (211) n$^+$-Si substrates using metalorganic vapor-phase epitaxy (MOVPE), were studied by analyzing current-voltage characteristics measured at various temperatures. The diode fabricated shows good rectification properties, however, both forward and reverse biased currents deviate from their ideal behavior. The forward current exhibits typical feature of multi-step tunneling at lower biases; however, becomes space charge limited type when the bias is increased. On the other hand, the reverse current exhibits thermally activated tunneling-type current. It was found that trapping centers at the p-CdTe/n-CdTe junction, which were formed due to the growth induced defects, determine the currents of this diode, and hence limit the performance of the nuclear radiation detectors developed. © *2013 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4828479]

I. INTRODUCTION

Cadmium telluride (CdTe) and cadmium zinc telluride (CZT) have emerged as the materials of choice for nuclear radiation detector development as they offer good energy resolution, high detection efficiency, and room temperature operation. There are several reports on spectroscopic detectors as well as imaging arrays based on these materials which demonstrate excellent performances.[1–7] These devices are presently fabricated using melt-grown single crystal wafers. However, growth of large-area, single crystal CdTe/CZT wafers with uniform material properties is very difficult. As a result, use of these crystals is limited to devices with relatively smaller dimensions. In this regard, vapor phase growth of thick CdTe layers on easily available large-area foreign substrates seems promising.[8–10]

In order to obtain large area crystals with uniform material properties, we have been studying metalorganic vapor-phase epitaxy (MOVPE) growth of thick single-crystal CdTe epitaxial layers on Si substrates.[10] As the growth is possible at lower substrate temperatures compared to the melt-growth temperatures, uniform layers with high crystal quality can be obtained. This technique further offers flexibilities to control thickness and electrical properties of the grown layers as growth rate and amount of external dopants can be strictly controlled during the growth. This allows tailoring the properties of the CdTe layers according to the device requirements. However, the large differences in the lattice constants and the thermal expansion coefficients between CdTe and Si, along with the difference in the nature of their chemical bonding characteristics make this growth extremely challenging. There are some reports on high quality single crystal CdTe grown on Si, which are typically a few μm thick.[11,12] These CdTe were mainly intended as a lattice-matched buffer layers for the subsequent HgCdTe growth for infrared detector development. Hence, x-ray, gamma ray detectors fabrication using thick CdTe epilayers with structure that employs carrier transport vertically across the epilayer/substrate junction is not fully explored.

We are developing nuclear radiation detector using thick single crystal CdTe epilayers grown on Si substrates. Despite above mentioned growth challenges, we already achieved high crystal quality thick single crystal CdTe layers ($>$260 μm) on the (211) Si substrates.[10,13] We particularly used (211) oriented Si substrate as it offers twins or double domains free growth. All grown CdTe layers were single crystalline, with the double crystal rocking curve (DCRC) FWHM values from the (422) reflection were in between 140 and 200 arc sec for layers thicker than 18 μm. The 4.2 K photoluminescence measurement showed sharp and high intensity bound excitonic emission, but very weak defect related deep emission, confirming the high crystalline quality of the grown layers.[13] We further developed detectors in a p-CdTe/n-CdTe/n$^+$-Si diode structure, and confirmed that they are capable of detecting x-rays, gamma rays, and spectrally resolve their energies.[10,13–15] The detector is operated by applying a positive bias at the electrode on the n$^+$-Si side (reverse-bias mode). Electric charge carriers are mostly generated in the thick CdTe layer due to photon absorption, transverse vertically across the junctions due to the applied bias, and generate electric signal at the electrodes. Hence, understanding of the charge transport through the junctions becomes necessary to improve the performance of these diode-type detectors further. We studied the charge transport property of the p-CdTe/n-CdTe/n$^+$-Si diode, which was performed by analyzing the current-voltage characteristics at different temperatures. Here we present detailed results of

[a]Author to whom correspondence should be addressed. Electronic mail: m.niraula@nitech.ac.jp.

 © 2013 AIP Publishing LLC

[This article is copyrighted as indicated in the article. Reuse of AIP content is subject to the terms at: http://scitation.aip.org/termsconditions. Downloaded to] IP: 133.68.125.22 On: Fri, 28 Aug 2015 05:45:09

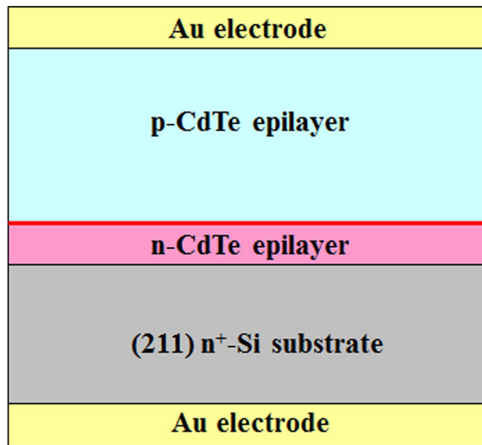


FIG. 1. Schematic diagram of the p-CdTe/n-CdTe/n$^+$-Si diode. The n-CdTe and p-CdTe layers were epitaxially grown by MOVPE and were typically 5 and 100 μm thick.

our study and discuss the charge transport mechanisms that satisfy the results experimentally obtained.

II. EXPERIMENTAL

Fig. 1 shows schematic diagram of the p-CdTe/n-CdTe/n$^+$-Si diode-type detector that was fabricated using single-crystal CdTe epitaxial layers grown directly on the (211) n$^+$-Si substrates in a custom-designed vertical-type MOVPE reactor.[10,13,14] Typically 5 μm thick n-CdTe layer was grown at 350 °C on 12 mm × 18 mm sized n$^+$-Si substrates. The n-CdTe layer was doped with ethyl iodide to an electron concentration of mid 10^{16} cm^{-3}. The p-CdTe layer, on the other hand, was typically 100 μm thick, grown at 560 °C, and not intentionally doped as we need high resistivity layer to fully deplete the diode. This layer exhibits a p-type conductivity with the typical net acceptor concentration (N_A-N_D) of 10^{14} cm^{-3}, derived from the capacitance-voltage measurement.[13] Finally, gold electrodes were evaporated on the p-CdTe side and on the back side of the n$^+$-Si substrate after proper surface treatments to make the ohmic contacts. The diode detectors were then diced into 1 mm × 1 mm pieces. The current-voltage (*I-V*) characteristics of the diodes were measured in dark on a probe-test station integrated with an Agilent power device analyzer (B1505A) and thermal control system. This measurement system allows us to measure the device current down to sub-pico ampere level, and precise control of temperature in a wide range.

III. RESULTS AND DISCUSSION

Fig. 2 shows the typical current-voltage characteristics of the p-CdTe/n-CdTe/n$^+$-Si diode at room temperature. It shows good rectification property, where a large current flows when a positive bias is applied on the contact on p-CdTe side (forward bias), but current is suppressed to a low value in the opposite case (reverse bias). Several diodes fabricated from the same or different growth runs essentially showed similar characteristics. However, both currents deviate from their ideal behavior described by the standard diode Eq. (1) below

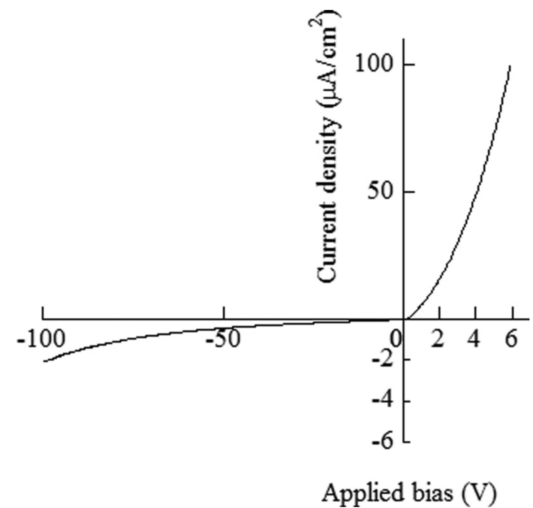


FIG. 2. Typical room-temperature current-voltage characteristics of the diode.

$$J \propto \exp\left(\frac{qV}{kT}\right), \tag{1}$$

where η is diode ideality factor, k is the Boltzmann's constant, and q is electronic charge. The forward current does not vary exponentially with applied bias, whereas the reverse current does not saturate but increase gradually with the applied bias. In order to determine the current transport mechanism, current-voltage characteristics were measured at different temperatures varying from 243 K to 333 K. Fig. 3 shows the forward *J-V* characteristics of the diode at various temperatures plotted in a semi-log scale. The characteristics show two distinct features depending upon the applied forward bias. At low forwards bias (<0.4 V), the *J-V* characteristics roughly follow exponential variation, however, at higher biases, the curves deviate and exhibit a power law dependence.

In the low forward bias region, the slope of the curves is almost independent of the temperatures. This indicates the current transport mechanism in this region is mostly temperature insensitive, and hence the forward current can be expressed by

$$J = J_o(T)\exp(AV), \tag{2}$$

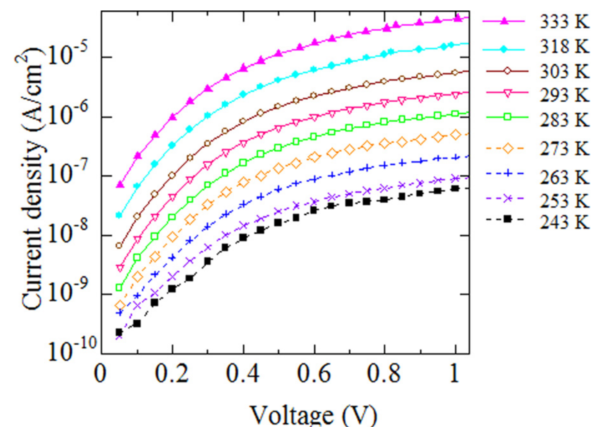


FIG. 3. Forward *J-V* characteristics of the diode at different temperatures.

[This article is copyrighted as indicated in the article. Reuse of AIP content is subject to the terms at: http://scitation.aip.org/termsconditions. Downloaded to] IP: 133.68.125.22 On: Fri, 28 Aug 2015 05:45:09

where A is a constant insensitive of temperature and $J_o(T)$ is the extrapolated intercept of the curve with the current axis. By fitting the forward current data to Eq. (2), we obtained A values between 12.34 and 13.65, which can be considered almost insensitive to temperatures. On the other hand, fitting the data with Eq. (1) yields η values greater than 2 for entire temperature range, which increases when the temperature decrease. These behaviors demonstrate that tunneling is the dominant current transport mechanism in our diodes in low applied forward biases.[16,17] Fig. 4 shows a plot of J_o as a function of temperature in a semi-log scale. The data fit well on straight line indicating J_o changes exponentially with T. This implies that the forward current in low bias region (<0.4 V) follows the multi-step tunneling through the defects in the depletion region.[16–18] We consider trapping centers are formed due to the electrically active defects at the p-CdTe/n-CdTe junction, which contribute to this tunneling. Below we explain the origin of these defects in our diode.

For forward bias above 0.4 V, the J-V characteristics follow a power law dependence, $J \propto V^2$, in all temperature ranges, which is characteristics of space-charge-limited current (SCLC).[19,20] The SCLC conduction is often reported in high resistivity wide bandgap semiconductors. Considering the undoped high resistivity p-CdTe layer with lower carrier mobility when compared to n-CdTe layer, it is likely that the space charge limiting of injected electrons from the n-CdTe in the p-CdTe layer dominates the junction current.[19]

Fig. 5 shows the reverse J-V characteristics of the diode measured at different temperatures. The current does not vary with the square root of the applied reverse bias, suggesting that space charge region generation is not the dominant mechanism. Moreover, the slope of the curves exhibits a weak temperature dependence, which implies that tunneling is a possible current transport mechanism. The reverse currents were plotted as a function of temperature (Arrhenius plot) at three different applied biases as shown in Fig. 6. A straight line fitting to the data yields activation energy, which was 0.46 eV at applied reverse bias of 0.5 V. However, the activation energies decrease from 0.46 eV to 0.33 eV when increasing the applied biases from 0.5 V to 30 V. This temperature dependence as well as field dependence suggests that thermally activated tunneling should be responsible mechanism for the observed reverse bias current of our diode.[21,22] It is considered that electrically active defects

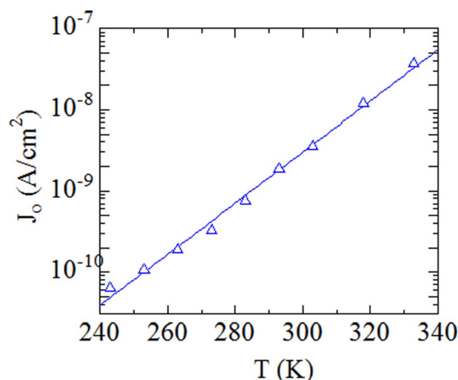


FIG. 4. Extrapolated values of J_o as a function of temperature.

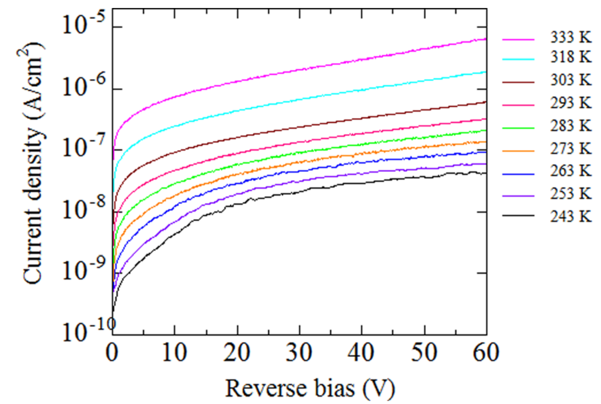


FIG. 5. Reverse J-V characteristics of the diode at different temperatures.

present at the p-CdTe/n-CdTe interface acts as trapping centers. Hence, the observed reverse current of our diode can be explained by using previously reported current transport mechanism for p-n or p-i-n junctions.[21–24] According to this mechanism, observed reverse current is considered due to electron tunneling from the valance band of p-CdTe to a trap at the interface followed by thermal emission into the conduction band of the n-CdTe (or the corresponding process for hole). The decrease of activation energy with increase of reverse bias, and hence the increase of currents can be explained because of the band bending effect. Due to the increased band bending at higher applied biases, traps of lower energies favor tunneling/thermal activation process.[21,23,24] Moreover, the effect of surface, which affects the depletion region width and contributes to tunneling or depletion region generation current as well as surface leakage current, is also considered another possible factor contributing to the observed reverse current in our diode.

Now we discuss the origin of the trapping centers and why we consider the junction formed at p-CdTe/n-CdTe determines the current transport, even though our diode possesses a complex structure of p-CdTe/n-CdTe homo-junction and n-CdTe/n$^+$-Si iso-type heterojunction. As explained earlier in introduction section, Si and CdTe have large differences in the lattice constants and the thermal expansion coefficients. This leads to strained layers, where the stress is relieved by generating high densities of dislocations when

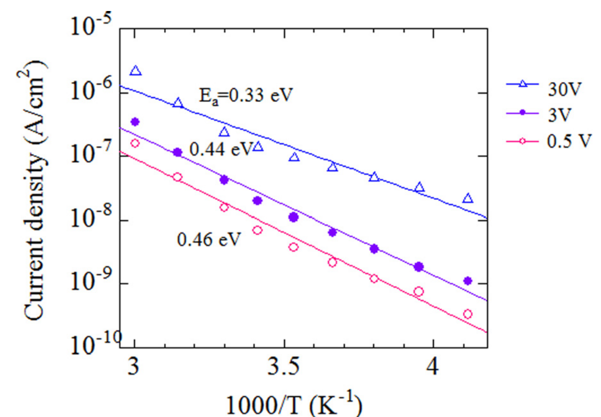


FIG. 6. Temperature dependence of reverse currents at different applied biases of 0.5, 3, and 30 V.

[This article is copyrighted as indicated in the article. Reuse of AIP content is subject to the terms at: http://scitation.aip.org/termsconditions. Downloaded to] IP: 133.68.125.22 On: Fri, 28 Aug 2015 05:45:09

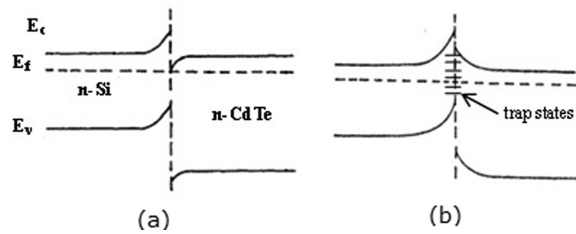


FIG. 7. Schematic energy band diagram of the n-CdTe/n$^+$-Si isotype heterojunction (a) ideal interface and (b) modified interface due to interface states.

CdTe layers are grown in Si substrates. These dislocations not only localize at growth interface of the n-CdTe/n$^+$-Si but also propagate upwards into the grown epilayers (n-CdTe and p-CdTe). Moreover, change in growth temperature from n-CdTe to p-like CdTe growth may be another source for generating electrically active defects; however, it needs further verification. Hence, these dislocations along with other growth-induced point defects and/or their complexes create trapping centers in the space charge region of p-CdTe/n-CdTe, and assist tunneling of carriers, as explained above. The iso-type heterojunction at n-CdTe/n$^+$-Si, on the other hand, offers an ohmic conduction at the junction and do not control the current conduction of the diode. Fig. 7 shows schematic energy band diagrams of the n-CdTe/n$^+$-Si junction based on Anderson model with an ideal interface and that with considering the interface states.[25,26] Because of large interface states, and also since n$^+$-Si is much more heavily doped when compared to n-CdTe, this junction offers ohmic behavior.[25,26] The ohmic conduction through the n-CdTe/n$^+$-Si junction was also confirmed experimentally by fabricating an n-CdTe/n+-Si junction and measuring the *I-V* after putting ohmic contacts on n-CdTe side and back side of the n$^+$-Si substrate.

We have already confirmed that this diode structure is capable of detecting gamma rays and resolving their energies. However, it seems that growth induced defects, mainly dislocations and other point defects, control the reverse leakage current, and limit the detector performance. Further reduction of crystal defects is necessary to improve the performance of the detector further. One of the possible ways to reduce the defect density at the interface would be performing the thermal cyclic annealing at the early stage of the growth. Our recent investigation shows that both *in-situ* cyclic annealing as well as rapid thermal annealing performed *ex-situ* on thin CdTe layers improve the crystal quality as revealed from the XRD and PL measurements. We are further optimizing these annealing conditions. Moreover, making the n-CdTe layer thicker and increasing the doping levels will be investigated to improve the device properties further.

IV. CONCLUSION

Charge carrier transport properties of p-CdTe/n-CdTe/n$^+$-Si junction that is used as a nuclear radiation detector is discussed. The diode-type detector was fabricated by growing n-CdTe and p-CdTe single crystal epilayers on (211) n$^+$-Si substrate using MOVPE. The diode fabricated exhibits good rectification properties, where forward current increases rapidly with applied bias, but the reverse current remains low and increases gradually with the applied bias. However, both currents do not follow the ideal behavior of p-n diodes. It was found that forward current was due to multi-step tunneling at lower applied biases, but changes to space charge limited current at higher biases. On the other hand, reverse current was mainly due to the thermally activated tunneling mechanism. It was found that trapping centers formed due to growth induced defects enhance the tunneling process. Moreover, the p-CdTe/n-CdTe junction mainly determines the current transports in both forward and reverse bias case, while conduction at the n-CdTe/n$^+$-Si junction was ohmic. Reduction of growth-induced crystal defects will be required to further improve performance of the detectors fabricated using this diode structure, which we think will be possible by performing annealing of the CdTe layers at the early stage of the growth.

ACKNOWLEDGMENTS

This work was supported in part by the Grant-in-Aid for Scientific Research of the Japan Society for the Promotion of Science (JSPS Grant No.: A 25242048).

[1]S. Watanabe, S. Ishikawa, H. Aono, S. Takeda, H. Odaka, M. Kokubun, T. Takahashi, K. Nakazawa, H. Tajima, M. Onishi, and Y. Kuroda, IEEE Trans. Nucl. Sci. **56**, 777 (2009).

[2]C. Szeles, S. A. Soldner, S. Vydrin, J. Graves, and D. S. Bale, IEEE Trans. Nucl. Sci. **55**, 572 (2008).

[3]M. Amman, J. S. Lee, P. N. Luke, H. Chen, S. A. Awadalla, R. Redden, and G. Bindley, IEEE Trans. Nucl. Sci. **56**, 795 (2009).

[4]P. J. Sellin, Nucl. Instrum. Methods Phys. Res. A **513**, 332 (2003).

[5]Y. Eisen, A. Shor, and I. Mardor, IEEE Trans. Nucl. Sci. **51**, 1191 (2004).

[6]L. Abbene, S. D. Sordo, E. Caroli, G. Gerardi, G. Raso, S. Caccia, and G. Bertuccio, J. Appl. Phys. **105**, 124508 (2009).

[7]S. D. Sordo, L. Abbene, E. Caroli, A. M. Mancini, A. Zappettini, and P. Ubertini, Sensors **9**, 3491 (2009).

[8]N. Lovergine, A. Cola, P. Prete, L. Tapfer, M. Bayhan, and A. M. Mancini, Nucl. Instrum. Methods Phys. Res. A **458**, 1 (2001).

[9]Q. Jiang, D. P. Halliday, B. K. Tanner, A. W. Brinkman, B. J. Cantwell, J. T. Mullins, and A. Basu, J. Phys. D: Appl. Phys. **42**, 012004 (2009).

[10]M. Yokota, K. Yasuda, M. Niraula, K. Nakamura, H. Ohashi, R. Tanaka, M. Omura, S. Minoura, I. Shingu, and Y. Agata, J. Electron. Mater. **37**, 1391 (2008).

[11]Y. Chen, S. Farrell, G. Brill, P. Wijewarnasuriya, and N. Dhar, J. Cryst. Growth **310**, 5303 (2008).

[12]S. R. Rao, S. S. Shintri, J. K. Markunas, R. N. Jacobs, and I. B. Bhat, J. Electron. Mater. **39**, 996 (2010).

[13]M. Niraula, K. Yasuda, H. Ohnishi, H. Takahashi, K. Eguchi, K. Noda, and Y. Agata, J. Electron. Mater. **35**, 1257 (2006); IEEE Trans. Nucl. Sci. **54**, 817 (2007).

[14]M. Niraula, K. Yasuda, H. Ichihashi, Y. Kai, A. Watanabe, W. Yamada, H. Oka, T. Yoneyama, K. Matsumoto, T. Nakanishi, D. Katoh, H. Nakashima, and Y. Agata, in *2009 MRS Spring Meeting – Symposium L – Nuclear Radiation Detection Materials*, edited by D. L. Perry, A. Burger, L. Franks, K. Yasuda, and M. Fiederie (Mater. Res. Soc. Symp. Proc., 2009), Vol. 1164, pp. 1164-L05-01.

[15]M. Niraula, K. Yasuda, S. Namba, T. Kondo, S. Muramatsu, H. Yamashita, Y. Wajima, and Y. Agata, IEEE Trans. Electron Devices **59**, 3450 (2012).

[16]S. S. Ou, O. M. Stafsudd, and B. M. Basol, Solid-State Electron. **27**, 21 (1984).

[17]H. Matsuura, T. Okuno, H. Okushi, and K. Tanaka, J. Appl. Phys. **55**, 1012 (1984).

[18]D. Yan, H. Lu, D. Chen, R. Zhang, and Y. Zheng, Appl. Phys. Lett. **96**, 083504 (2010).

[This article is copyrighted as indicated in the article. Reuse of AIP content is subject to the terms at: http://scitation.aip.org/termsconditions. Downloaded to] IP: 133.68.125.22 On: Fri, 28 Aug 2015 05:45:09

[19]Y. Tomita, T. Kawai, and Y. Hatanaka, Jpn. J. Appl. Phys., Part 1 **32**, 1923 (1993).
[20]M. Dutta and D. Basak, Appl. Phys. Lett. **92**, 212112 (2008).
[21]P. Tanner, S. Dimitrijev, and H. B. Harrison, in *Proceedings of Optoelectronic and Microelectronic Materials and Devices* (2008), p. 41.
[22]X. Shao, S. L. Rommel, B. A. Orner, J. Kolodzey, and P. R. Berger, IEEE Electron Device Lett. **18**, 411 (1997).
[23]Q. Shan, D. S. Meyaard, Q. Dai, J. Cho, E. F. Schubert, J. K. Son, and C. Sone, Appl. Phys. Lett. **99**, 253506 (2011).
[24]K.-W. Ang, J. W. Ng, G.-Q. Lo, and D.-L. Kwong, Appl. Phys. Lett. **94**, 223515 (2009).
[25]B. L. Sharma and R. K. Purohit, *Semiconductor Heterojunctions* (Pergamon Press, Oxford, 1974). pp. 16, 24–32.
[26]F. A. Kish, D. A. Vanderwater, M. J. Peanasky, M. J. Ludowise, S. G. Hummel, and S. J. Rosner, Appl. Phys. Lett. **67**, 2060 (1995).

[This article is copyrighted as indicated in the article. Reuse of AIP content is subject to the terms at: http://scitation.aip.org/termsconditions. Downloaded to] IP: 133.68.125.22 On: Fri, 28 Aug 2015 05:45:09