Howling Reduction by Analog Phase-Locked Loop and Active Noise Control Circuits

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***Abstract*— This paper proposes a howling reduction circuit using analog phase-locked loop (PLL) and active noise control (ANC) circuits. The proposed circuit reduces howling by generating a signal opposite in phase to howling. To make a signal with the same frequency as howling, we employed the PLL circuit. The ANC circuit was used to control the amplitude of the signal. In addition, we employed pseudo-lock avoidance and differential switch circuits to avoid noise generation. The results confirm the effects of howling reduction by the proposed circuit.**

***Keywords*—howling, active noise control, analog circuits, phase-locked loop.**

1. INTRODUCTION

Howling is a source of noise in acoustic systems, and techniques for howling reduction have been proposed by researchers [1-6]. These techniques typically employ digital circuits with analog/digital (A/D) converters and digital/analog (D/A) converters. In general, both the processing time periods in digital circuits and the latencies in the converters are significant. Some of the reported techniques [1-3] take more than 0.5 s before howling reduction is achieved. Such a slow operation is not adequate because human ears detect howling noise within milliseconds. Furthermore, a few techniques [4-6] predict howling signals and can reduce howling within 10 ms of operation. However, the prediction used in these techniques assumes that the howling frequency is dependent only on the distance between the microphone and speaker. In actual acoustic system environments, sound reflections are significant and their prediction is not possible. Therefore, howling reduction techniques that operate at high speed and do not rely on prediction must be established.

In contrast to digital circuits, analog circuits generally operate at high speed. We previously proposed an active noise control system with analog circuits and have demonstrated high-speed operation to cancel noise in a duct [7]. This active noise control circuit (ANC) controls the amplitudes of signals to cancel noises without any prediction. Therefore, it has the potential to reduce howling noise. However, this ANC cannot control the signal phase adequately, and thus, to effectively cancel noises, additional circuits are required to control the phase of signals [8]. In this paper, we propose a phase-locked loop (PLL) for controlling phase and frequencies, and, by using both the PLL and ANC, we demonstrate howling reduction by circuit simulations.

2. CONFIGURATION OF HOWLING REDUCTION CIRCUIT AND SIMULATION OF EACH PART

We employed the simulation program HSPICE for the circuit simulator with the OnsemiSanyo0.8 μm CMOS process rule. In acoustical systems, a sound is input to a microphone and the signal from the microphone is amplified. Then, the amplified signal is output by a speaker, which is fed back to the microphone through an acoustical path and this feedback signal causes howling. To emulate the howling, we employed a resistance and capacitance (RC) oscillation circuit shown in Fig. 1. Signals *input*, *output* and O_{ps} in the circuit are defined in this figure. Amp in Fig.1 indicates an amplifier, while the phase shift comprises the RC shown in Fig. 2. Add1 indicates an adder circuit. In this RC oscillation circuit, *input* is amplified by Amp and the resulting *output* is fed back with a delay due to the phase shift and superposed to *input* by Add1. At the frequency corresponding to the delay period, a gain from this RC oscillation circuit becomes infinity, and thus howling appears in *output*. Hereafter, signals obtained from this RC oscillation circuit are regarded as 'without (w/o) control'. A block diagram of the proposed howling reduction circuit is shown in Fig. 3 along with the RC oscillation circuit, and signals I_{hrc}, O_{mul}, O_{lpf}, O_{pll}, O_{del} and O_{anc} in the circuit are also defined. In this proposed circuit, from the output of Amp I_{hrc}, the PLL generates a signal with the same frequency as the howling signal in I_{hrc}. Because output from PLL O_{pll} is led 90° from I_{hrc}, we used a circuit shifting the phase of the signal by 90° (90° delay). ANC adjusts the amplitude of the output of the 90° delay O_{del} to that of the howling. The output of the ANC O_{anc} is superposed to the howling signal in I_{hrc} by an adder circuit Add2. This configuration using only the PLL, 90° delay and the ANC can typically reduce howling. However, the PLL does not necessarily output signals with the same frequency as the howling. To suppress signals with frequencies different from that of howling, we also implemented the pseudo-lock avoidance and differential switch circuits, shown in Fig. 3.

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Results obtained from the configuration in Fig. 3 are regarded as 'with control'. We describe details of each block in the following.

2.1 PLL

PLLs are commonly employed to synchronize the frequency of an output signal with that of an input signal [9]. A PLL comprises a phase comparator (PC), a low-pass filter (LPF) and a voltage-controlled oscillator (VCO). For the PC, a multiplier is employed in most cases, and it generates output voltage corresponding to the phase difference between two signals, the input and feedback from the VCO. The LPF removes high frequency noise from the PC output. The VCO is an oscillator with an output frequency controlled by the LPF output. The VCO output is used as an output of the PLL and is also fed back to the PC.

Various types of VCOs in PLLs have been proposed for different applicable oscillation frequencies [10-15], and those VCOs output signals with different duty ratios. For our purpose, oscillation at a kHz band is required. In addition, if we define the duty ratio D as

$$D = \frac{T_+}{T_+ + T_-} \times 100 \ [\%] \qquad (1),$$

where T_+ is the time of positive value and T_- is the time of negative value of the signal; D should be 50%. This is because the howling frequency is kHz and the D of howling is 50%. Therefore, we adopted a VCO with the kHz band with a D of 50%, shown in Fig. 4. In Fig. 4, V_b = 1 V which oscillates the VCO at a free-running frequency. V_{dd} and V_{ss} are voltage sources with 2.5 V and -2.5 V, respectively. We simulated the operation of this VCO, and obtained the dependence of output frequencies (O_{pll}) on the input (O_{lpf}) voltage, as shown in Fig. 5. The oscillation frequencies of the VCO were in the kHz band and were proportional to O_{lpf}. D was ~50% at any of the frequencies.

A wide-range Gilbert multiplier (WRM) is used for the PC [16], and a circuit diagram of the LPF adopted here (cut-off frequency = 26 Hz) is shown in Fig. 6. To check the operation of the PLL comprising these PC, LPF and VCO components, we input a sine wave with an amplitude of 1 V and a frequency of 4 kHz to I_{hrc}, and the resulting I_{hrc} and O_{pll} are shown in Fig. 7. We confirmed that O_{pll} oscillates at the same frequency as I_{hrc} and its phase was advanced by ~90° from I_{hrc}. Fast Fourier transform (FFT) spectra for I_{hrc} and O_{pll} are shown in Fig. 8, and as shown in this figure, O_{pll} oscillates at 4 kHz as I_{hrc}.

2.2 Pseudo-lock avoidance circuit

PLLs are not always locked at the howling frequency but can be locked in the harmonics of howling. Lock of the PLLs at the harmonics is generally called pseudo-lock. Figure 9 shows an example of pseudo-lock. When we used the circuit shown in Fig. 1 with a white noise as *input*, the resulting *output* without control oscillated at ~4 kHz. On the other hand, if we used the circuit only with the PLL, 90° delay and ANC, the resulting *output* oscillated at ~8.8 kHz, as shown in Fig. 9. Thus, the circuit with only the PLL, 90° delay, and ANC outputs a signal at nearly the same frequency as the second harmonic of howling. To avoid oscillation at the harmonics, we apply the pseudo-lock avoidance circuit which determines whether the PLL is locked at the harmonics.

Figure 10(a) shows the input of the PLL I_{hrc} and the output of the PLL O_{pll} in the case where the PLL is locked at a frequency of I_{hrc}. If we multiply O_{pll} by the signal led 90° from I_{hrc}, the multiplied signal is always positive. Therefore, the D of the multiplied signal D_{mul} is 100%, as shown in Fig. 10(a). Figure 10(b) shows I_{hrc} and O_{pll} in the case where PLL is locked at a third harmonic frequency of I_{hrc}. O_{pll} is a different frequency from I_{hrc}. If we multiply O_{pll} by the signal led 90° from I_{hrc}, the multiplied signal shows positive and negative values, as shown in Fig. 10(b). Figure 11 shows the calculated D_{mul} when PLL is locked in the harmonics of howling. D_{mul} is at a maximum of 67% at the third harmonic among the harmonics. Therefore, if we fabricate a comparator with a threshold of D_{mul} at ~70%, we can detect pseudo-lock.

The block diagram of the pseudo-lock avoidance circuit is shown in Fig. 12 with signals O_{difp}, O_{mulp}, O_{comp1}, O_{comp2}, O_{intp} and O_{pac} in the circuit defined in this figure. Figure 13(a) shows a circuit diagram of the DifferentiatorP, while the multiplier is a WRM. ComparatorP1 and ComparatorP2 are op-amp comparators, and a circuit diagram of the integrator is shown in Fig. 13(b). *Input* in Fig. 3 superposed with the feedback signal is amplified Amp and becomes I_{hrc}. DifferentiatorP outputs a signal O_{difp} led 90° from I_{hrc}. The multiplier multiplies O_{difp} by O_{pac} and outputs O_{mulp}. ComparatorP1 compares O_{mulp} with 0 V and outputs O_{comp1} of ~2.5 V when $O_{mulp} > 0$ V, and outputs ~−2.5 V when $O_{mulp} < 0$ V. The integrator integrates O_{comp1} and outputs O_{intp}. When $D_{mul} > 70$ %, O_{intp} becomes >1 V. ComparatorP2 compares O_{intp} with 1 V. O_{comp2} is ~2.5 V when $O_{intp} > 1$ V, and is ~−2.5 V when $O_{intp} < 1$ V. In Fig. 14, we show signals in the case of *input* in Fig. 3 with an amplitude of 2 V and a frequency of 4 kHz as an example. The PLL was initially not locked at 4 kHz and O_{comp2} was ~−2.5 V or unstable. After ~0.05 s, the PLL was locked at 4 kHz and $O_{intp} > 1$ V, and O_{comp2} was ~2.5 V. O_{comp2} controls the switch for the feedback of O_{pll}, and the switch outputs O_{pac}. When O_{comp2} was ~2.5 V, the switch closed and O_{pll} was fed back to the multiplier and the PLL. The switch closed at ~0.05 s when O_{comp2} was ~2.5 V, and thus this circuit detected D_{mul} and controlled the output frequency of the PLL. Using the pseudo-lock avoidance circuit, o*utput* with control oscillated at the same frequency as howling (without control), as shown in Fig. 9.

2.3 90° delay circuit

As shown in Fig. 7, O_{pll} was led 90° from I_{hrc}. To cancel howling, a circuit to delay O_{pll} by 90° is required. As a circuit to delay a signal by 90°, an integrator and a D flip flop can be considered [17]. When we used an integrator as a 90° delay, as in Fig. 3, the output of the integrator (O_{del}) had an offset voltage and the D of O_{del} was not 50%. On the other hand, when we used the D flip flop, it did not output offset voltage and showed outputs with 50% of D. Thus we adopted the D flip flop as the 90° delay. Figure 15 shows a circuit diagram of the 90° delay with a clock signal of O_{mul}.

2.4 ANC

The configuration of the ANC is the same as that in Ref. [7], consisting of two WRMs and an integrator. As the integrator in the proposed circuit, we used nMOSs instead of the resistances in Ref. [7] to reduce the circuit area, as shown in Fig. 16.

2.5 Differential switch

When howling does not occur, the howling reduction circuit should output no signal. However, the PLL always outputs a signal with an arbitrary frequency when the PLL is not locked. Therefore, if we use the simple configuration comprising the PLL, 90° delay and ANC as the howling reduction circuit, the circuit occasionally outputs noise. Figure 17 shows *output* without control and *output* from the configuration with only the PLL, 90° delay and ANC, when white noise was used as *input*. Output from the configuration with the PLL, 90° delay and ANC was larger than the howling (*output* without control), implying that the circuit generated noises other than howling. Therefore, we needed to detect the lock of the PLL and stop the signal during unlocked periods of the PLL. To realize such an operation, we fabricated a differential switch which observes the stability of the output of the LPF O_{lpf} and controls the output of the ANC to the Add2 in Fig. 3.

The block diagram of the differential switch and the PLL is shown in Fig. 18, and signals O_{difd}, O_{comd1}, O_{comd2}, O_{comd3}, O_{invd} and O_{add} in the circuit are also defined in this figure. Figure 19 shows a circuit diagram of the DifferentiatorD in Fig. 18. We show an example of the operation of the differential switch in Figs. 20(a)–20(b) with an I_{hrc} of a sine wave with an amplitude of 2 V and frequencies with initially 4.5 kHz and then changed to 4 kHz at 0.03 s. In addition, as O_{anc}, we used a sine wave with an amplitude of 1 V and a frequency of 3 kHz. Figure 20(a) shows O_{lpf} and O_{difd}. O_{lpf} was stable during locked periods of the PLL (0.013~0.031 s and after 0.036 s), and it was unstable during the PLL unlocked periods (before 0.013s and 0.031~0.036 s). DifferentiatorD differentiated the O_{lpf} and outputs O_{difd}. Therefore, O_{difd} was ~0 V during stable O_{lpf}. We defined thresholds of the stable O_{difd} to be ±1 mV and designed ComparatorD1 and ComparatorD2 with these thresholds. ComparatorD1 output O_{comd1} was negative in value when $O_{difd} > -1$ mV. The inverter reversed O_{difd} and output O_{invd}. ComparatorD2 outputs O_{comd2} which was negative in value when $O_{invd} > -1$ mV. The adder added O_{comd1} and O_{comd2}. ComparatorD3 compared O_{add} with 0.5 V. O_{comd3} was ~−2.5 V when $O_{add} > 0.5$ V, and it was ~2.5 V when $O_{add} < 0.5$ V. Figure 20(b) shows O_{comd3}, which was ~−2.5 V at stable O_{lpf}, and was ~2.5 V at unstable O_{lpf}. When O_{comd3} was ~−2.5 V, the switch for O_{anc} closed. As shown in Fig. 20(c), the switch closed during locked periods of the PLL.

2.6 High-Pass filter

High-pass filters (HPF, cut-off frequency = 1 kHz) were inserted between the Amp and PLL and between Add2 and the ANC in Fig. 3 to operate the howling reduction circuit at howling frequency but not at voice frequencies.

3 SIMULATION OF HOWLING REDUCTION CIRCUIT

3.1 Cancelling effect

We set 16 μs (R = 1.6 kΩ, C = 10 nF) as a time constant in Fig. 2 to set a howling frequency of ~4 kHz. A voice of a man with an amplitude of 10 mV, shown in Fig. 21, was used as *input* in Fig. 1. Figure 22 shows the time integration of absolute value of the *output* without control during 0.07–0.4 s (the input signal time) as a function of the gain in the Amp in Fig. 2. It increases proportionally with small gains in Amp. However, it suddenly increases at a gain of 33, which corresponds to the onset of howling. Therefore, as shown in Fig. 23, we compared the *output* without and with control in the case of an Amp gain of 33, and found that howling did not appear with control but did without control. In addition, the amplitude of the *output* with control was 0.327 V which was ~33 times the amplitude of the *input*. Therefore, *output* with control had nearly the same amplitude as signals multiplied by the gain. Figure 24 shows an initial period of *input* and *output* with and without control. *Output* with control showed nearly the same waveform as the *input*. On the other hand, *output* without control started oscillation at ~4 kHz at ~0.065 s. Therefore, the proposed circuit operated to reduce howling just after (less than 0.001s) the voice input.

Figure 25 shows FFT spectra of the *input* and *output* with and without control. For the FFT, we set a sampling frequency of 192 kHz and 9600 points from 0.2 s. In Fig. 25, howling appears at ~4 kHz in the *output* without control, while there is no peak at ~4 kHz for the *output* with control. Around 190 Hz and upwards, voice signals appear in all spectra. Therefore, the voice signal

in the *input* was not suppressed by the proposed circuit. We calculated a cancelling effect due to the proposed circuit by the following equation,

$$C_{eff} = 20\log_{10}\frac{\text{total voltage in signal without control at 20~20kHz}}{\text{total voltage in signal with control at 20~20kHz}} \quad (2),$$

and we obtained a C_{eff} of 19.9 dB.

We also simulated cases with time constants of 32 μs (R = 3.2 kΩ, C = 10 nF) and 64 μs (R = 6.4 kΩ, C = 10 nF) in Fig. 2. Corresponding howling frequencies are ~2 kHz for 32 μs and ~1 kHz for 64 μs. With the time constant of 32 μs, howling appeared at a gain in Amp of 32 without control, while it shows no howling signals with control. We obtained a C_{eff} of 19.4 dB using this gain. With a time constant of 64 μs, howling appeared at a gain in Amp of 31 without control, and a C_{eff} of 9.9 dB was obtained at this gain. We also used the voice of a different man with an amplitude of 8.7 mV and a frequency of 240 Hz, and the voice of a woman with an amplitude of 9.0 mV and a frequency of 950 Hz as *input*. When we used a time constant of 16 μs in Fig. 2, howling appeared at a gain in Amp of 33 for both voices. We obtained a C_{eff} of 21.5 and 19.0 dB for the voices of the second man and the woman, respectively. Therefore, at various time constants (howling frequencies) and with different voices, the proposed circuit was able to reduce howling signals.

3.2 Howling margin

The howling margin is defined as the extent to which gain can be increased without howling. To obtain the howling margin, we simulated the proposed circuit for various gains in Amp at a time constant of 16 μs, with the voice in Fig. 21 as *input*. Figure 26 shows the dependence of the time integration of absolute *output* with control on gains in Amp. Time integration of absolute *output* increased proportionally with a gain of up to 73 and then began to rapidly increase at 74. Therefore, howling started at a gain of 74. The howling margin can be calculated by the following equation,

$$20\log_{10}\frac{\text{maximum gain without howling with control}}{\text{maximum gain without howling without control}} \quad (3).$$

As noted above, *output* without control showed howling at a gain of 33. Therefore, we obtained a howling margin of 7.2 dB. With time constants of 32 μs and 64 μs, maximum gains without howling were 74 and 64 with control, respectively. Therefore, the howling margins were 7.6 and 6.6 dB, respectively. Previously reported howling margins were 3~4 dB [4, 18], and thus the howling margin of the proposed circuit is larger than those from the reported methods.

4 CONCLUSIONS

We proposed a howling reduction method based on analog circuits. Our results show that the proposed circuit worked in 1 ms and amplified voices without howling. We obtained significant cancelling effects and howling margins with the proposed circuit. The proposed circuit will be effective in reducing howling in audio systems.

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REFERENCES

[1] Leotwassana W, Punchalard R, Silaphan W. Adaptive howling canceller using adaptive IIR notch filter: simulation and implementation. Neural Networks and Signal Processing 2003;1:848–51.

[2] Nishimura S. An improved adaptive notch filter for detection of multiple sinusoids. IEICE Trans. Fundamentals 1994;77:950–5.

[3] Yasukawa H, Shimada S. An acoustic echo canceller using subband sampling and decorrelation methods. IEEE Trans. Signal Process. 1993;41:926–30.

[4] Sogami A, Kawamura A, Iiguni Y. An adaptive howling canceller based on distance measurement (in Japanese). IEICE Trans. Fundamentals 2008;J91-A:939–48.

[5] Sogami A, Kawamura A, Iiguni Y. Improvement of speech quality in distance-based howling canceller. IEICE Trans. Fundamentals 2009;E92-A:1039–46.

[6] Sogami A, Kawamura A, Iiguni Y. A high speech quality distance-based howling canceller with adaptive cascade notch filter and silent pilot signals. IEICE Trans. Fundamentals 2011;E94-A:2306–14.

[7] Kato M. Active noise control in a duct by an analog neural network circuit. Appl. Acoust. 2011;72:732–6.
[8] Hyodo T, Asakura G, Tsukada K, Kato M. Performance improvement of the analog ANC circuit for a duct by insertion of an all-pass filter. IEICE Trans. Fundamentals 2013;E96-A:824–5.
[9] Chung SK. Phase-locked loop for grid-connected three-phase power conversion system. IEE Proc. Electr. Power Appl. 2000;147:213–9.
[10] Craninckx J. A 1.8-GHz CMOS low-phase-noise voltage-controlled oscillator with prescaler. IEEE J. Solid-State Circuits 1995;30:1474–82.
[11] Zhenbiao L, Kenneth KO. A low-phase-noise and low-power multiband CMOS voltage-controlled oscillator. IEEE J. Solid-State Circuits 2005;40:1296–302.
[12] Hsieh HH. A high-performance CMOS voltage-controlled oscillator for ultra-low-voltage operations. IEEE Trans. Microw. Theory Techn. 2007;55:467–73.
[13] Kato K, Sase T, Sato H, Ikushima I, Kojima S. A low-power 128-MHz VCO for monolithic PLL IC's. IEEE J. Solid-State Circuits 1988, 23:474–9.
[14] Hwang IC, Kim C, Kang SM. A CMOS self-regulating VCO with low supply sensitivity. IEEE J. Solid-State Circuits 2004;39:42–8.
[15] Nicodimus RA, Takagi S, Fujii N. Wide tuning range voltage-controlled ring oscillator. IEICE Trans. Electron. 2003;E86-C:1085–8.
[16] Mead C. Anlog VLSI and neural systems, Addison-Wesley Publishing Company, Massachusetts; 1989, p. 90–96.
[17] Weste N, Eshraghian K. Principles of CMOS VLSI design: a systems perspective. Reading, MA: Addison-Wesley; 1985, 213–215.
[18] Chisaki Y, Matsuo K, Usagawa T. Howling canceller using interaural level difference for binaural hearing assistant system. Acoustical Science and Technology 2007;28:90–7.