

# Development of Large-Area Imaging Arrays Using Epitaxially Grown Thick Single Crystal CdTe Layers on Si Substrates

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*Abstract*—Optimization of CdTe crystal growth by adjusting effective Te/Cd ratio at the growth surface, as well as growth-interrupted annealing together with detector array fabrication techniques were studied to achieve large-area, uniform x-ray spectroscopic imaging arrays. The p-CdTe/n-CdTe/n<sup>+</sup>-Si heterojunction diode-type detector arrays were fabricated by using epitaxially grown thick single crystal CdTe layers on n<sup>+</sup>-Si substrates, where pixels were patterned by making deep vertical cuts on p-CdTe side using a dicing saw. The study was first focused on development of 2D (8x8) array using 12.6 mm x 11.4 mm size wafers, which confirmed uniform dark current distribution among the pixels. We further demonstrated possibility of making larger arrays by fabricating (18x18) array using a 25 mm x 25 mm size uniform single crystal CdTe epilayer grown on Si substrate.

*Index Terms*: CdTe epitaxy, large-area array, dark current distribution, imaging, response uniformity

## I. INTRODUCTION

CdTe and CdZnTe are now considered as the most promising materials for the development of high resolution x-ray, gamma ray spectrometers and imaging arrays operable at room temperature<sup>1-5</sup>. To construct efficient imaging arrays for specific applications, large-area single crystals with better material uniformity are needed<sup>1-5</sup>. For this reason, we have been studying metalorganic vapor-phase epitaxy (MOVPE) growth of thick single crystal CdTe layers on Si substrates, and detector development since past several years<sup>6-9</sup>. This vapor-phase growth technique offers large-area and uniform CdTe crystal, and further allows strict control of electrical properties of the crystal, such as conduction types and carrier densities, by impurity doping. Hence, it offers flexibilities in detector design in accordance with the target applications. Despite this huge potential, epitaxial growth of high-quality and thick CdTe on Si is extremely difficult. The large differences in the lattice constants and the thermal expansion coefficients

between CdTe and Si, along with the difference in the nature of their chemical bonding characteristics make this growth extremely challenging. Besides, the strong native oxide present on the Si surface imposes additional difficulties in growing CdTe on Si. This results in inferior quality layers that exhibit a poor substrate adhesion and difficulty in retaining substrate orientation.

We overcame those growth challenges and obtained high crystalline quality and thick single crystal CdTe directly on large-area (211) Si substrates<sup>6-9</sup>. We further developed pixel-type imaging arrays based on p-CdTe/n-CdTe/n<sup>+</sup>-Si heterojunction diodes structure, and confirmed they could be applied in energy discriminated imaging purpose<sup>10,11</sup>. However, some non-uniformity in x-ray counting response among the pixels was observed, which affected the array's imaging performance. It was found that inhomogeneity of crystal properties, which led to the spatial variation of pixels' reverse dark currents as well as the charge transport properties, were responsible for the observed array response<sup>12</sup>. This crystal inhomogeneity was, in turn, found to be due to the non-uniform variation of effective tellurium to cadmium precursor's ratio (Te/Cd ratio) at the growth surface<sup>12</sup>.

In this study, we focused on optimization of growth conditions, particularly adjustment of effective Te/Cd ratio at the growth surface and growth-interrupted annealing, to achieve large area crystals with highly uniform material properties. We further optimized the array fabrication technique to achieve large area imaging arrays that exhibit uniform distribution of dark currents among the pixels. Details on the large-area crystal growth and array fabrication and their performances are presented.

## II. CRYSTAL GROWTH DETAILS

The growth was carried out in a vertical-type MOVPE reactor working at an atmospheric pressure, using dimethylcadmium (DMCd) and diethyltelluride (DETe) precursors. The substrate temperatures for the iodine doped n-CdTe layer and undoped high resistivity p-like CdTe layers were 350 and 650 °C, respectively. The Te and Cd precursors were introduced into the reactor through multiple feed lines that allow strict control of precursor's flow rates and ratios. CdTe growth details, such as Si substrate pre-treatments and growth sequences are already reported elsewhere<sup>6-9</sup>. We further employed a growth-interrupted rapid thermal annealing

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(RTA) at the initial growth stage in a separate chamber in hydrogen environment at 900 °C by covering the growth surface with a bulk CdTe wafer. This annealing process improves crystallinity, and reduces the detector dark current<sup>13</sup>. The grown epilayers were characterized by X-ray diffraction ( $\theta$ - $2\theta$  scan and rocking curve measurement).

### III. DETECTOR ARRAY FABRICATION

The pixel type detector array, as shown schematically in Fig. 1, consists of a p-CdTe/n-CdTe/n<sup>+</sup>-Si heterojunction diode structure. The detector array was fabricated in the following manner: A thin n-CdTe layer was first grown on the highly conductive (211) n<sup>+</sup>-Si substrate and then subjected to the RTA as described in Section II. Afterward, the growth of the n-CdTe layer was continued on the annealed layer to make the total n-CdTe layer thickness typically 5  $\mu$ m. Subsequent growth of undoped high resistivity p-like CdTe (~100  $\mu$ m) was then performed. Gold electrodes were then evaporated on the p-like CdTe side and the back side of n<sup>+</sup>-Si substrate after some surface treatments to make ohmic contacts.

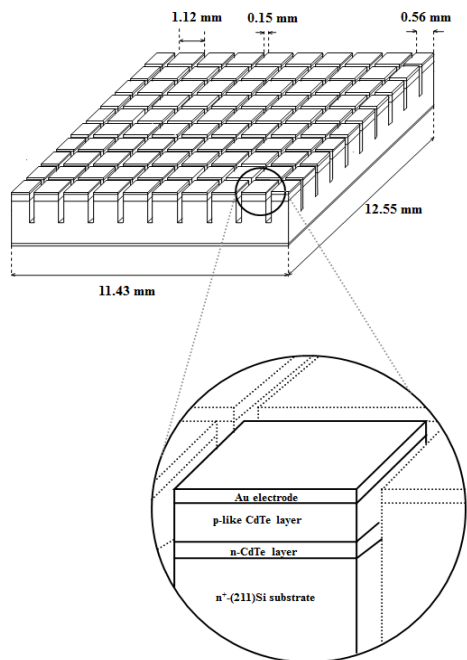


Fig. 1. Schematic diagram of the 2D pixel array. Inner (8x8) pixels, 1.12 mm x 1.12 mm size and 1.27 mm pixel pitch, constitute the active elements of the array. The enlarged portion shows the pixel structure in detail.

The array consists of a full-area electrode on the n<sup>+</sup>-Si side, while pixels with segmented electrodes were formed on the p-CdTe side using a dicing saw. The detail on pixel patterning is reported in<sup>10-12</sup>. In order to achieve good interpixel isolation and hence suppress the charge sharing problem in adjacent pixels, the depth of the cuts was extended down to half of the Si substrates as shown in the enlarged portion of Fig. 1. In the present study, we first made 2D (8x8) array on a 12.6 mm x 11.4 mm size CdTe crystal that was cut out from our standard 18 mm x 12 mm size single crystals grown on Si substrates.

The array has 1.12 mm x 1.12 mm size pixels in a 1.27 mm pixel-pitch.

We measured reverse dark currents from all pixels in the array using a measurement system that consists of an Apollowave manual probe station connected to an Agilent power device analyzer. The system is capable of evaluating whole wafer with high precision positioning, temperature control, and current measurement down to sub-picoampere level. We measured reverse dark currents from all pixels to study their variation among the pixels. Based on these array evaluation results, we further optimized crystal growth and array fabrication techniques to fabricate (18x18) pixel array using a 25 mm x 25 mm sized single crystal CdTe on Si substrate.

### IV. RESULTS AND DISCUSSION

#### A. (8x8) Array

The (8x8) array was fabricated using a 12.6 mm x 11.4 mm size CdTe epitaxial layer on Si substrate. Each pixel in the array possesses a p-CdTe/n-CdTe/n<sup>+</sup>-Si heterojunction diode structure. The array is operated by applying a positive bias on the continuous electrode on the back side of the n<sup>+</sup>-Si substrate (reverse bias mode). We measured the dark currents from all 64-pixels in the array by applying reverse biases from 0 to 250 V at room temperature. Fig. 2, right, shows the dark current distribution among the pixels in the array measured at 200 V applied bias. Except than some edge pixels, the dark current distribution is highly uniform. The dark current distribution of one of our previous arrays is also shown in the Fig. 2, left, for comparison. It shows nearly concentric circular variation of the dark currents among the pixels, with higher values for top left pixels, which gradually decrease towards the bottom pixels. This variation suggests the non-uniformity in the crystalline property of the grown crystal, which could be related to the radial variation of effective ratio of Te to Cd precursors at the substrate surface<sup>12</sup>. This Te to Cd ratio variation was responsible for the formation of different deep level defects, with portion having larger concentration of

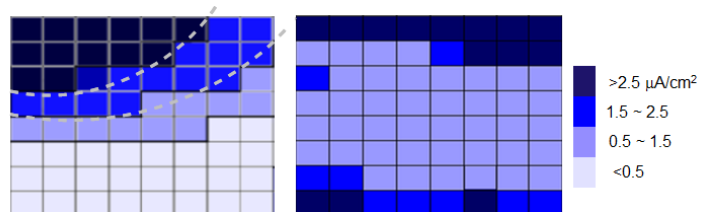


Fig. 2. Distribution of dark currents from all pixels in the (8x8) array measured at room temperature when applying 200 V reverse bias. Left- previous array for comparison which shows nearly concentric circular variation (broken lines are used for clarity). Right- recent array, which shows uniform current distribution except for some edge pixels.

defects exhibited larger dark currents. We overcame this problem in our recent arrays by optimizing the growth parameters. With further adjustment of the precursors flow patterns (number and spacing of the feed lines) as well as source flow rates and ratios, we were able to achieve a uniform effective Te to Cd ratio at the growth surface. As a result, dark current uniformity of the array improved significantly.

### B. Fabrication and Evaluation of Larger Arrays

With our improved growth and annealing conditions, we were able to obtain high quality, and uniform single crystal CdTe layers on Si substrates of sizes as large as 25 mm x 25 mm. This is nearly three times larger than our previous crystals which were typically grown on 18 mm x 12 mm size Si substrates. Fig. 3 shows photograph of one of our recent large-area crystals, along with our previous crystal for comparison. Our recent crystal shown in figure is about 40  $\mu\text{m}$  thick, and exhibits very good thickness uniformity throughout the wafer. The x-ray diffraction measurements performed at different portions of the wafer exhibited single diffraction peak corresponding to CdTe (422). This indicates the grown layer is monocrystalline throughout the crystal with no twinned regions, and the growth orientation parallel to the (211) Si substrates. The DCRC FWHM values were typically 200 arcs throughout the wafer.

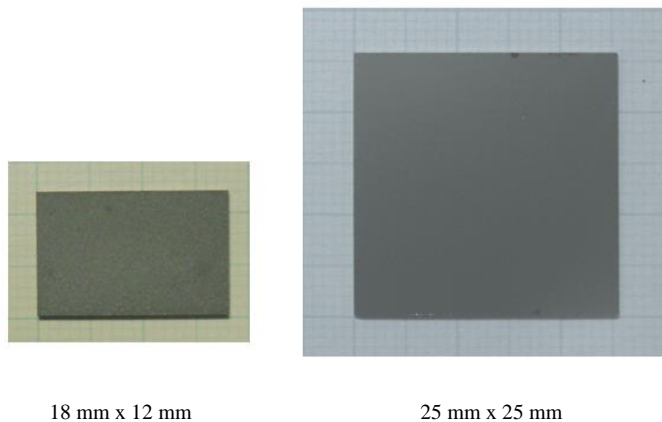


Fig. 3. Right- photograph of CdTe crystal grown on 25 mm x 25 mm size (211) Si substrate. The crystal was grown by optimizing the growth and annealing conditions. Our previous crystal grown (18 mm x 12 mm size) is also shown on the photo (left) for comparison

In order to examine the material uniformity over the whole wafer area, we fabricated 2D array using these large-area crystals grown on 25 mm x 25 mm size Si substrates. The array fabrication technique as well as the pixel size and pitch were same as described in Section III. We measured dark current from all 324 pixels in the (18x18) array using our measurement system. The examination of dark current values at a fixed applied bias and their pixel-to-pixel variation allows us to evaluate the material uniformity of the crystal. Fig. 4

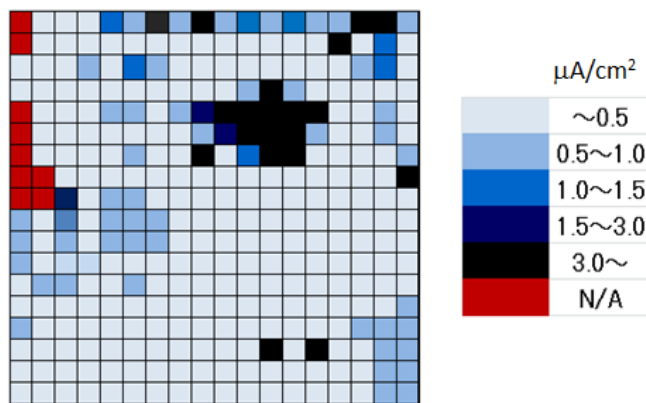


Fig. 4. Distribution of dark currents from all pixels in the (18x18) array fabricated using a 25 mm x 25 mm size CdTe single crystal on Si substrate. The dark currents were measured at room temperature by applying a reverse bias of 50 V.

shows distribution of dark currents from all pixels in the (18x18) array measured at room temperature by applying a reverse bias of 50 V. The result shows very uniform distribution of the dark current, where majority of the pixels showed dark current less than  $0.5 \mu\text{A}/\text{cm}^2$ . This dark current value is, however, higher than our previous smaller sizes arrays as shown in Fig. 2, but the uniformity in whole wafer area is promising. Fig. 5 shows temperature dependence of the dark currents in  $-20$  to  $60^\circ\text{C}$  range plotted for a fixed applied reverse bias of 50 V (Arrhenius plot) for two different pixels from the array; one selected from the lowest current region and another from the highest current region chosen arbitrarily. The characteristics follow the thermally activated generation process with an activation energy mentioned in the figure. This shows that the current conduction is dominated by a single

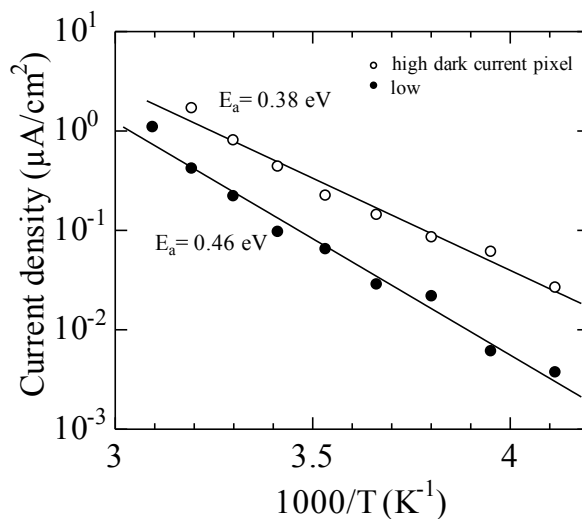


Fig. 5. Arrhenius plot of reverse dark currents of two different pixels in the array at 50 V applied bias. One pixel was selected from the portion exhibiting highest dark current and another from the portion exhibiting lowest.

level located in the band gap around 0.4 eV above the valence band, possibly attributed to ionized Cd-vacancy<sup>14,15</sup>. Comparing this to our previous arrays<sup>12</sup>, where similar dark current measurements on pixels selected from different regions on the (8x8) array gave different energy levels, 0.6 and 0.4 eVs, responsible for the current conduction. This could be related to non-uniform variation of effective Te/Cd ratio at the wafer surface, producing different energy levels in different concentrations<sup>12</sup>. The single energy level observed in our recent array implies that this array has improved material uniformity at the whole wafer surface. However, concentration of the 0.4 eV level should be lowered to decrease the dark current values further, which needs further optimization of both post-growth crystal annealing, as well as growth conditions. Furthermore, some edge pixels and some pixels in the middle of the array exhibit somewhat high dark currents, as well as there are some damaged pixels which need to be reduced. We consider these are due to handling damage, and can be eliminated with further optimization of array fabrication techniques, which is in progress.

## V. CONCLUSION

We studied optimization of CdTe crystal growth and detector array fabrication techniques to achieve large-area x-ray spectroscopic imaging arrays that exhibit uniform response. The array was fabricated using MOVPE grown thick single crystal CdTe layers on n<sup>+</sup>-Si substrates. Each pixel in the 2D array consists of a p-CdTe/n-CdTe/n<sup>+</sup>-Si heterojunction diode structure which was formed by subsequently growing n- and p-CdTe epitaxial layers on the n<sup>+</sup>-Si substrate. The pixels were patterned by making deep vertical cuts orthogonally from the p-CdTe side using a dicing saw. With the adjustment of effective Te to Cd precursor ratio at the growth surface, as well as optimization of the annealing conditions, CdTe layers with homogeneous material properties were achieved. We first confirmed the highly uniform dark current distribution among the pixels by fabricating a 2D (8x8) array using a 12.6 mm x 11.4 mm size CdTe wafer. We further demonstrated possibilities of making larger arrays using this epitaxial growth technique by fabricating (18x18) array based on a 25 mm x 25 mm size single crystal CdTe layer grown on the n<sup>+</sup>-Si substrates, which exhibited uniform dark current distribution.

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