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Enhanced two dimensional electron gas transport characteristics in Al_2O_3/AlInN/GaN metal-oxide-semiconductor high-electron-mobility transistors on Si substrate

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The authors report on $Al_2O_3/Al_{0.85}In_{0.15}N$/GaN Metal-Oxide-Semiconductor High-Electron-Mobility Transistor (MOS-HEMT) on Si fabricated by using atomic layer deposited Al_2O_3 as gate insulator and passivation layer. The MOS-HEMT with the gate length of 2 μm exhibits excellent direct-current (dc) characteristics with a drain current maximum of 1270 mA/mm at a gate bias of 3 V and an *off-state* breakdown voltage of 180 V for a gate-drain spacing of 4 μm. Also, the 1 μm-gate MOS-HEMT shows good radio-frequency (rf) response such as current gain and maximum oscillation cut-off frequencies of 10 and 34 GHz, respectively. The capacitance-voltage characteristics at 1 MHz revealed significant increase in two-dimensional electron gas (2DEG) density for the MOS-HEMT compared to conventional Schottky barrier HEMTs. Analyses using drain-source conductivity measurements showed improvements in 2DEG transport characteristics for the MOS-HEMT. The enhancements in dc and rf performances of the $Al_2O_3/Al_{0.85}In_{0.15}N$/GaN MOS-HEMT are attributed to the improvements in 2DEG characteristics.
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AlInN/GaN based high electron mobility transistors (HEMTs) have recently attracted a great deal of research interest. The AlInN/GaN HEMTs are expected to deliver higher drain current (I_{DS}) because of its polarized two dimensional electron gas (2DEG) density, (N_s) higher than AlGaN/GaN HEMTs. This makes AlInN/GaN HEMTs promising for high power and radio-frequency (rf) applications.[1] Deeply scaled short-channel HEMTs with sub-micron gate footprints have delivered a high output current density as well as excellent rf performance.[2] However, AlInN/GaN based high voltage devices require longer gate length (L_g) and relatively long gate-to-drain distance (L_{gd}), respectively.[3] In addition, the lattice matched AlInN/GaN devices using longer L_g could not achieve a high output current >1 A/mm as expected.[4–7] In contrast, the AlInN/GaN heterostructures with lower In composition <17% are potential candidates to deliver high current because of its high N_s due to in-built piezoelectric and spontaneous polarization effects.[8] Such AlInN/GaN heterostructure with high conductivity and/or N_s is required for attaining low on-resistance (R_{on}) which is essential for high power switching applications. This can be realized in slightly tensile strained AlInN/GaN heterostructure with high conductivity and N_s values delivering a low sheet resistance (R_{sh}) $\sim$ 182 $\Omega/\square$.[9]

In spite of these advantages, metal-organic chemical vapor deposition (MOCVD) growth of AlInN/GaN heterostructure typically on Si substrate is challenging because of large lattice and thermal mismatches for GaN-on-Si.[10] Besides growth difficulties, the AlInN/GaN Schottky barrier HEMT (SB-HEMT) is prone to detrimental gate leakage current (I_G), which often degrades the subthreshold device characteristics such as On/Off current ratio (I_{On}/I_{Off}) and subthreshold-swing slope (SS). To minimize I_G and to improve device characteristics, several oxides have been investigated for AlInN/GaN metal-oxide-semiconductor HEMTs (MOS-HEMTs). These MOS-HEMTs employed various oxides and different deposition techniques such as: pulsed laser deposited (PLD) Y_2O_3,[4] reactive ion sputtered (RIS) Al_2O_3,[5] MOCVD grown Al_2O_3, $GdScO_3$,[6] ZrO_2,[7] atomic layer deposited (ALD) Al_2O_3,[11] and plasma enhanced CVD (PE-CVD) SiO_2.[12] Considering the available choice of insulators and their deposition techniques, ALD Al_2O_3 emerges as an attractive gate dielectric and passivating material for III-V nitrides owing to its large band gap ($E_g \sim 7$ eV), high dielectric constant ($\varepsilon \sim 9$), and breakdown field strength ($\sim$10 MV/cm) in combination with its high degree of conformity in deposition. By using ALD-Al_2O_3 as gate insulator, improved transport characteristics have been reported for AlGaN/GaN MOS-HEMTs.[13,14] Recently, AlInN/GaN HEMT passivated with ALD-Al_2O_3 has also proved good candidate for millimeter wave power generation.[15] However, still there is a lack of detailed report on the direct-current (dc) and rf performance and the transport properties of $Al_{0.85}In_{0.15}N$/GaN MOS-HEMT on Si by using ALD-Al_2O_3 as gate oxide as well as passivating material. In particular, a majority of the available reports for AlInN/GaN devices are on sapphire or SiC substrates.[5–7,12,15,16] Addressing the issues aforementioned, we have fabricated $Al_{0.85}In_{0.15}N$/GaN MOS-HEMT typically grown on Si. The MOS-HEMT fabricated by using ALD-Al_2O_3 as gate insulator shows reduction in I_G by 10^5 orders and improvements in dc and rf

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performances compared to SB-HEMT. The channel conductivity analyses on the MOS-HEMT reveal enhanced carrier transport properties.

The AlInN/GaN heterostructure was grown using Taiyo Nippon Sanso (SR 4000) MOCVD system on 4 in. silicon substrate. In an effort to maximize output dc characteristics with low R_{on}, the AlInN/GaN heterostructure was designed with a 10 nm AlInN barrier and the In composition was measured as 15%. The GaN layer thickness was 1 μm, and a 1 nm AlN spacer layer was grown between the GaN and barrier layer to improve channel conductivity by minimizing alloy disorder and/or interface roughness scattering of 2DEG. To complement the growth of device grade AlInN/GaN/Si heterostructure, a 110 nm buffer layer and a thick strained layer superlattice (SLS) of 3 μm, similar to our buffer design for MOCVD grown AlGaN/GaN/Si heterostructure was introduced.[17]

The AlInN/GaN MOS-HEMT fabrication is started with a mesa isolation by using BCl_3 plasma based reactive ion etching. Ohmic patterns were formed by using conventional photolithography followed by metallization of Ti/Al/Ni/Au (15/80/12/40 nm). The ohmic contacts were annealed at 800 °C for 30 s in N_2 ambient using rapid thermal annealing (RTA). For MOS-HEMTs, a 10 nm ALD-Al_2O_3 was deposited at 300 °C by using trimethylaluminum (TMA), water vapor (H_2O), and ozone (O_3) as precursors. Post deposition annealing of Al_2O_3 layer was carried out to improve the oxide/semiconductor interface. Gate metals Pd/Ti/Au (40/20/60 nm) was deposited directly on the Al_2O_3 layer. As reference, AlInN/GaN/Si SB-HEMT without the passivation layer was also fabricated simultaneously. The dc current-voltage (I_{DS}-V_{DS}) characteristics and rf characteristics were measured using Agilent B1500A semiconductor parameter analyzer and N5247A PNA-X network analyzer. Circular shaped SB and MOS-diodes of area 7.07×10^{-4} cm^2 were used for capacitance-voltage (C-V) measurements at 1 MHz. The ohmic characteristics of the fabricated devices were investigated by transmission line method (TLM). TLM measurements show a low contact-resistance (R_c) and R_{sh} values of 0.5 Ω·mm and 187 Ω/□ for the MOS-HEMT. The SB-HEMT without the Al_2O_3 passivation layer shows relatively high R_c and R_{sh} values of 0.9 Ω·mm and 212 Ω/□, respectively. A lower R_{sh} value with a better R_c value for MOS-HEMT with Al_2O_3 passivation signifies better conductivity that leads to an increased in N_s-μ product as R_{sh} can be defined as ($R_{sh} \sim 1/qN_s\mu$), where q is the electronic charge and μ is the 2DEG mobility.

Figure 1 shows the comparison dc I_{DS}-V_{DS} characteristics of MOS-HEMT and SB-HEMT. The MOS-HEMT showed a well-behaved I_{DS}-V_{DS} characteristics with a drain current maximum ($I_{DS,max}$) of 1270 mA/mm at gate-source bias (V_{GS}) of 3 V. This accompanied a low $R_{\rm on}$ value of 3.2 Ω·mm for a source-drain distance (L_{SD}) of 10 μm. A high $I_{DS,\,max}$ was achieved for AlInN/GaN MOS-HEMT with the device width and gate length (W_g/L_g) of 15/2 μm and is the highest reported on Si. For SB-HEMT with similar device dimensions, the $I_{DS,max}$ and $R_{\rm on}$ values at V_{GS} of 2 V were 1020 mA/mm and 4.2 Ω·mm, respectively.

Figures 2(a) and 2(b) show the semi-log and linear scale transfer characteristics at $V_{DS} = 8$ V for MOS-HEMT and

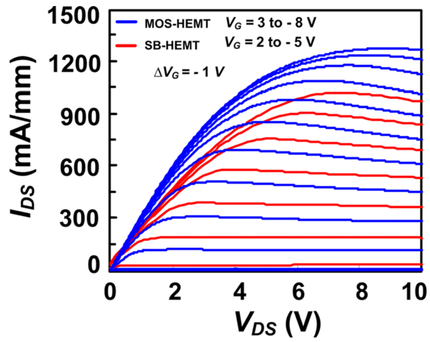

FIG. 1. (a) Typical dc I_{DS}-V_{DS} characteristics of Al_2O_3/AlInN/GaN MOS-HEMT and (b) AlInN/GaN SB-HEMT.

SB-HEMT, respectively. In MOS-HEMT, the detrimental gate leakage was suppressed by order of magnitude $\sim 10^5$ compared to SB-HEMT that leads to enhanced subthreshold characteristics, namely, I_{On}/I_{Off} value of 10^8 and SS value of 62 mV/dec. In contrast, the SB-HEMT shows a I_{On}/I_{Off} value of 10^3 and SS of 114 mV/dec. The H_2O and O_3 assisted high quality ALD-Al_2O_3 insulating layer is believed to be responsible for the mitigation of gate leakage in MOS-HEMT. Recent studies using H_2O and O_3 assisted ALD-Al_2O_3 oxide layer have proved effective to reduce the gate leakage and interface density for AlGaN/GaN MOS-HEMT.[18] And the observed improvements in subthreshold characteristics of Al_2O_3/AlInN/GaN MOS-HEMT also suggest such high quality gate insulator.[19] As shown in Fig. 2(b), the AlInN/GaN SB-HEMT and MOS-HEMT exhibits complete pinch-off characteristics with the threshold voltage (V_{th}) of −4 and −7 V, respectively. For the AlInN/GaN MOS-HEMT, the transconductance maximum (G_M) was 186 mS/mm which is only 5% lower than G_M value of 195 mS/mm for SB-HEMT in spite of the negative V_{th} shift due to increased gate-to-channel separation.

As observed from the dc output characteristics, the on-current drive for the MOS-HEMT was significantly higher. Although identical AlInN/GaN/Si heterostructure was used for the device fabrication, the MOS-HEMT shows increase in saturation drain current ($I_{DS,sat}$) compared to conventional SB-HEMT with a high access resistance. A high I_{DS} could be expected for MOS-HEMT as $I_{DS}/W_{\rm G} = q.N_s.\nu_d$, where ν_d is the drift velocity of electrons and depends on intrinsic transport properties of the channel. In the literature, the drain current improvements due to enhanced drift mobility (μ_d) have been reported for AlInN/GaN MOS-HEMT by using

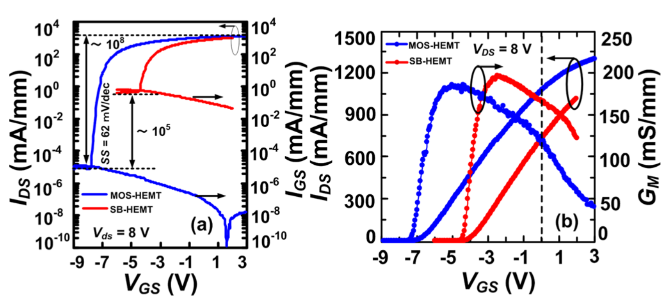

FIG. 2. (a) Semi-log scale transfer and I_{GS}-V_{GS} characteristics of AlInN/GaN based MOS-HEMT and SB-HEMT ($W_g/L_g = 15/2$ μm). (b) Transfer and transconductance characteristics of SB-HEMT and MOS-HEMT.

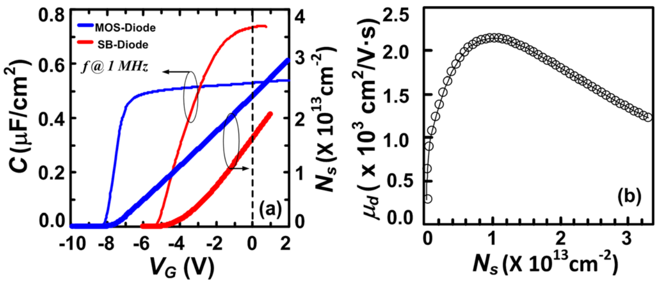

FIG. 3. (a) Typical C-V and N_s-V_G characteristics of AlInN/GaN MOS-diode and SB-diode. (b) Extracted drift mobility (μ_d) as a function of 2DEG density (N_S) for Al_2O_3/AlInN/GaN MOS-HEMT.

MOCVD Al_2O_3 gate oxide.[20] Wang *et al*. observed 20% improvement of current density for AlInN/GaN HEMTs passivated with ALD-Al_2O_3 layer.[21] Therefore, the observed enhancement in output current for the AlInN/GaN MOS-HEMT is believed to be due to an increased N_s and/or $N_s \times \mu_d$ product.

To quantify this, channel transport properties of the AlInN/GaN MOS-HEMT were assessed by using channel conductivity along with C-V measurements. Conductivity measurements were carried out on long-gate "FAT-HEMT" with $W_g/L_g = 200/100\,\mu$m present on the same wafer, where W_g and L_g are the channel width and length, respectively. The drift mobility was extracted according to the equation[22]

$$\mu_d = \left(\frac{L_G}{W_G}\right)\left(\frac{G_{Ch(V_G)}}{qN_s}\right), \tag{1}$$

where G_{Ch} is the channel conductance at a low drain bias (0.1–0.3 V). Due to relatively severe gate leakage, the channel conductivity could not be measured for SB-HEMT. Typical C-V characteristics of the AlInN/GaN based SB-diode and MOS-diode are shown in Fig. 3(a). As shown, the C-V curve of MOS-diode shows a sharp transition from depletion to accumulation regime suggesting good Al_2O_3/AlInN interface. The N_s was extracted from the integration of respective C-V curves using the equation

$$N_S = \frac{1}{qA}\int_{V_{TH}}^{V_G} C(V_G)dV_G, \tag{2}$$

where A is the diode area. As shown Fig. 3(a), the MOS-diode shows a significant increase in N_s values in comparison with SB-diode. At $V_G = 0$ V, the N_s values for MOS and SB-diodes were 2.3×10^{13} and $1.6 \times 10^{13}\,cm^{-2}$, respectively. An N_s increase by 49% for MOS-diode is due to surface passivation effects by high quality ALD-Al_2O_3 and is consistent with the observed drain current enhancements. Maeda *et al*.[23] reported similar observations of about 50% increase in N_s for AlGaN/GaN MIS-structure by using electron-cyclotron resonance (ECR) plasma sputtered Al_2O_3. Figure 3(b) shows the extracted drift mobility for AlInN/GaN MOS-HEMT as a function of effective N_s in the channel. As shown, the μ_d increases with smaller N_s and reaches a peak μ_d of 2145 cm^2/V·s at N_s value of $9.6 \times 10^{12}\,cm^{-2}$. For N_s values exceeding $\sim 1 \times 10^{13}\,cm^{-2}$, the μ_d changes slope and decreases with N_s. Nevertheless, the extracted μ_d is over 1500 cm^2/V·s even at higher N_s values. The zero-bias μ_d and corresponding N_s values were 1678 cm^2/V·s and $2.3 \times 10^{13}\,cm^{-2}$, respectively. The extracted zero-bias mobility value is comparable with the ALD-Al_2O_3/AlGaN/GaN channel MOS-HEMT,[14] although a high 2DEG density is confined in the present AlInN/GaN channel MOS-HEMT. The presence of the 1 nm AlN spacer layer should also be accounted for the observed high mobility as it helps to reduce the alloy disorder and interface roughness scattering.[24] The enhancement in $N_s \times \mu_d$ product for the MOS-HEMT is due to the device grade AlInN/GaN/Si heterostructure and the incorporation of high-quality gate oxide which gives better gate controllability over the channel.

To study the passivation effectiveness, dynamic drain current characteristics were compared. Figure 4(a) shows the comparison of dynamic I_{DS}-V_{DS} characteristics measured at $V_{GS} = 0$ V. A pulse width and period of 500 μs and 10 ms were applied during the measurement. The gate and drain was set at a quiescent bias condition of 0 V. Compared to the SB-HEMT, the MOS-HEMT shows a 48% increase in dynamic $I_{DS,sat}$ (from 743 to 1098 mA/mm) suggesting good degree of passivation due to ALD-Al_2O_3 layer. The presence of ALD-Al_2O_3 layer further reduces remote Coulomb scattering of the 2DEG and effectively passivates the surface traps.[25]

The MOS-HEMT was also subjected to three-terminal *off-state* breakdown voltage (BV_{off}) measurements at a constant gate bias of −8 V. The BV_{off} is defined as the drain bias at which a drain current of 1 mA/mm was observed. As shown in Fig. 4(b), the MOS-HEMT shows lower gate-leakage current and a BV_{off} value of 180 V for an $L_{gd} = 4\,\mu$m. The dc performances of fabricated AlInN/GaN based SB-HEMT and MOS-HEMT in this work are compared with

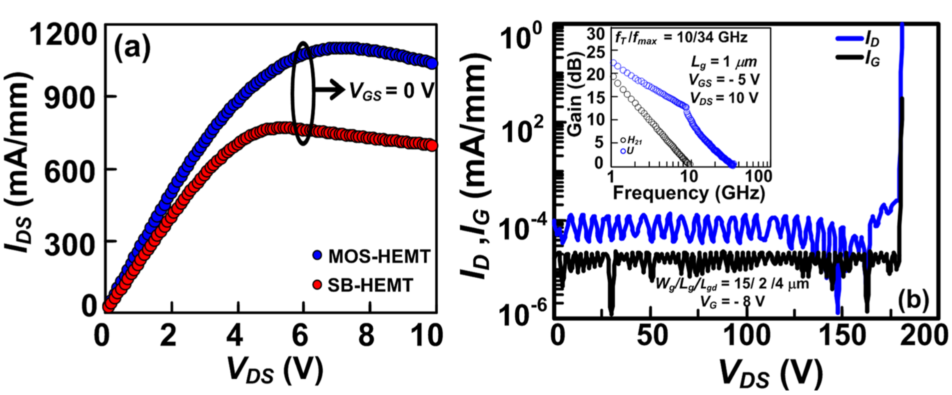

FIG. 4. (a) Dynamic I_{DS}-V_{DS} characteristics of AlInN/GaN based MOS-HEMT and SB-HEMT. (b) 3-Terminal breakdown voltage characteristics of MOS-HEMT with a $L_{gd} = 4\,\mu$m. The inset shows rf performance of MOS-HEMT with ($W_g/L_g/L_{sg}$ L_{gd}) = (2 × 50)/1/3/3 μm.

TABLE I. Comparison of dc characteristics of lattice-matched AlInN/GaN based devices reported in literatures with this work.

Oxides	T_{ox} (nm)	Deposition technique	L_g (μm)	$I_{DS,\ max}$ (A/mm)	$G_{M,\ max}$ (mS/mm)	Reverse I_{GS} (A/mm)	Substrate	Ref.
Y_2O_3	15	PLD	2.0	0.60	NA	NA	Si	4
Al_2O_3	7	RIS	4.0	0.29	45	1.0×10^{-6} at -10 V	Sapphire	5
Al_2O_3	12.5	MOCVD	2.0	0.77	142	1.2×10^{-8} at -5 V	Sapphire	6
ZrO_2	19	MOCVD	2.0	0.76	NA	1.0×10^{-7} at -15 V	Sapphire	7
SiO_2	10	PECVD	1.8	1.60	290	4.0×10^{-9} at -6 V	SiC	12
…	…	…	0.5	1.00	310	1.0×10^{-8} at -10 V	SiC	16
…	…	…	2.0	0.70	160	5.0×10^{-2} at -5 V	Sapphire	6
…	…	…	**2.0**	**1.02**	**195**	$\mathbf{6.0 \times 10^{-4}}$ **at** $\mathbf{-6}$ **V**	**Si**	**This work**
$\mathbf{Al_2O_3}$	**10**	**ALD**	**2.0**	**1.27**	**186**	$\mathbf{1.0 \times 10^{-8}}$ **at** $\mathbf{-9}$ **V**		

The dc characteristics of AlInN/GaN based SB-HEMT and MOS-HEMTs on Si are highlighted.

those reported in literatures as shown in Table I. It can be seen that the $Al_{0.85}In_{0.15}N$/GaN SB-HEMTs shows higher drain current $\geq$1 A/mm than those lattice-matched $Al_{0.83}In_{0.17}N$/GaN HEMTs on sapphire[6] or SiC.[16] For the $Al_{0.85}In_{0.15}N$/GaN MOS-HEMT on Si, the drain current is further improved to 1.27 A/mm.

On-wafer rf characteristics were measured for the MOS-HEMT with the dimensions of $W_g/L_g/L_{sg}/L_{gd} = (2 \times 50)/1/3/3\ \mu$m and by biasing at $V_{DS} = 10$ V and $V_{GS} = -5$ V. The MOS-HEMT exhibits excellent frequency response with a unit current gain cut-off frequency and maximum oscillation frequency (f_T/f_{Max}) values of 10/34 GHz as shown in inset of Fig. 4(b). In spite of its longer gate ($L_g \sim 1\ \mu$m) and source-drain spacing ($L_{sd} \sim 7\ \mu$m), the MOS-HEMT still delivers the product of $f_T \times L_g = 10$ GHz μm which is better than previous reports for AlInN/GaN short channel devices on SiC[2,16] or Sapphire.[11] The effective electron velocity (V_{eff}) in the MOS-HEMT channel is estimated to be 0.6×10^7 cm/s by using $V_{eff} = 2\pi \cdot f_T \cdot L_g$. A high effective electron velocity considering the large periphery of the MOS-HEMT is due to enhanced carrier transport properties. By vertical and lateral scaling down of these MOS-HEMTs, they are capable of achieving higher f_T and f_{Max} values.[26] The improvements in dc and rf performances are due to the observed enhancements in the two dimensional electron gas transport properties of $Al_{0.85}In_{0.15}N$/GaN MOS-HEMT on Si.

In summary, we have designed and characterized high-quality $Al_{0.85}In_{0.15}N$/GaN MOS-HEMT on Si with ALD-Al_2O_3 as gate oxide. The fabricated MOS-HEMT shows good gate control over the channel and exhibits excellent dc and rf characteristics with reduced gate leakage current. A maximum drain current of 1270 mA/mm and an *off-state* breakdown of 180 V were achieved for the MOS-HEMT. The 1 μm-gate MOS-HEMT also exhibits f_T and f_{Max} values of 10 and 34 GHz, respectively. A zero-bias mobility value of 1678 cm^2/V·s and corresponding N_s of 2.3×10^{13} cm^{-2} were extracted for the MOS-HEMT using channel conductivity and capacitance measurements. The enhanced carrier transport characteristics in $Al_{0.85}In_{0.15}N$/GaN channel MOS-HEMT are responsible for the observed improvements in dc and rf performances. The results demonstrate the promising features of utilizing ALD-Al_2O_3/$Al_{0.85}In_{0.15}N$/GaN MOS-HEMTs on Si and their ability to deliver high-output current density for future high-power devices.

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