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Thermal stability of an InAlN/GaN heterostructure grown on silicon by metal-organic chemical vapor deposition

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The thermal stabilities of metal-organic chemical vapor deposition-grown lattice-matched InAlN/GaN/Si heterostructures have been reported by using slower and faster growth rates for the InAlN barrier layer in particular. The temperature-dependent surface and two-dimensional electron gas (2-DEG) properties of these heterostructures were investigated by means of atomic force microscopy, photoluminescence excitation spectroscopy, and electrical characterization. Even at the annealing temperature of 850 °C, the InAlN layer grown with a slower growth rate exhibited a smooth surface morphology that resulted in excellent 2-DEG properties for the InAlN/GaN heterostructure. As a result, maximum values for the drain current density ($I_{DS,max}$) and transconductance ($g_{m,max}$) of 1.5 A/mm and 346 mS/mm, respectively, were achieved for the high-electron-mobility transistor (HEMT) fabricated on this heterostructure. The InAlN layer grown with a faster growth rate, however, exhibited degradation of the surface morphology at an annealing temperature of 850 °C, which caused compositional in-homogeneities and impacted the 2-DEG properties of the InAlN/GaN heterostructure. Additionally, an HEMT fabricated on this heterostructure yielded lower $I_{DS,max}$ and $g_{m,max}$ values of 1 A/mm and 210 mS/mm, respectively. © *2015 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4937902]

I. INTRODUCTION

The InAlN/GaN heterostructure is a promising material for high-power and high-frequency applications. It is believed that InAlN/GaN-based high-electron-mobility transistors (HEMTs) with an In content of 17%–18% can be lattice matched to GaN thereby mitigate strain related defects and improve their reliability over that of AlGaN/GaN HEMTs.[1–5] Moreover, a higher AlN content in the barrier layer is expected to increase the two-dimensional electron gas (2-DEG) and thus the output current density, because of the enhanced spontaneous polarization of AlN.[6,7]

In spite of these advantages, the growth of InAlN/GaN/Si heterostructures is still technically challenging because of the conflicting growth conditions for InN and AlN binary alloys. For metal-organic chemical vapor deposition (MOCVD) growth of InAlN/GaN heterostructures, a relatively lower growth temperature is preferred for the InAlN barrier layer than for the GaN channel, which results in a poor surface morphology. As a consequence, the ohmic contact characteristics of InAlN/GaN HEMTs tend to degrade when the ohmic contacts are annealed at high temperatures, which is typically 850 °C. Some studies have shown the influence of the ohmic contact annealing temperature upon the stability of electrical properties and surface morphologies for InAlN/GaN HEMTs.[8] Also, it is necessary for InAlN/GaN HEMTs that ohmic contact annealing is done at low temperatures to prevent the degradation of the surface morphology and the electrical characteristics.[9,10] Therefore, a systematic study of MOCVD-grown InAlN/GaN/Si heterostructures is required for the optimization of ohmic contact annealing temperatures and to understand its influence upon the surface and electrical characteristics. This work focuses on InAlN/GaN/Si heterostructures fabricated with varying growth rates for the InAlN barrier, and the dependence of the stability of surface morphologies and electrical properties upon the ohmic annealing temperatures.

II. EXPERIMENTAL

The InAlN/GaN heterostructures were grown on 4 in.-diameter Si (111) substrates by means of the MOCVD method. Trimethyl gallium (TMGa), trimethyl aluminum (TMAl), and trimethyl indium (TMIn) were used as group III element raw materials, while ammonia (NH_3) was used as the group V element raw material. After thermally cleaning the Si substrate, subsequent layers were deposited sequentially comprising a 100-nm-thick AlN nucleation layer, a 900-nm-thick composition-graded AlGaN buffer layer, a 1.5-μm-thick GaN channel, a 1-nm-thick AlN spacer, and a 10-nm-thick $In_{0.18}Al_{0.82}N$ barrier. A slower growth rate of 2.5×10^{-2} nm/s (sample A) and a faster growth of 1.0×10^{-1} nm/s (sample B) were chosen exclusively for the InAlN barrier layer. In the growth process, the V/III flux ratio of InAlN was fixed at 2000, while the growth rate was controlled by changing the supply quantity of the group III element raw material. After growth, the In composition in the barrier layer was confirmed

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to be 18%, and the InAlN barrier thickness was determined to be 10 nm by reciprocal space mapping from X-ray diffraction measurements and by X-ray reflectivity (XRR) measurements. Measurements of the surface morphology and of the crystal quality of the InAlN/GaN/Si heterostructures were carried out using an atomic force microscope (AFM; Seiko Instruments, Inc.), X-ray diffraction (X'pert PRO, PANalytical B.V.), and cross-sectional transmission electron microscopy (TEM) observation. Optical characterizations by photoluminescence (PL) were performed at 10 K using the fourth harmonic generation of a Ti:sapphire laser ($\lambda = 210$ nm) as an excitation source. Also, to investigate the thermal stability of the 2-DEG electrical characteristics, the Hall effect measurement was carried out for samples subjected to ohmic annealing temperatures ranging from 700 to 850 °C. In the Hall effect measurements, Ti/Al was used as the ohmic metal, and the ohmic annealing was carried out for 30 s in an N_2 ambient atmosphere. A transmission line model (TLM) measurement was also used to study the thermal stabilities of the ohmic contact characteristics, namely, the contact resistance (R_c), specific contact resistance (ρ_c), and sheet resistance (R_{sh}).

Finally, HEMTs were fabricated on both samples A and B simultaneously to evaluate and compare the device characteristics. The device fabrication began with mesa isolation using BCl_3 plasma-based reactive ion etching, and a 100-nm-thick electron beam evaporated SiO_2 layer was subsequently deposited for device passivation. Conventional ultraviolet photolithography was used to define the source/drain ohmic contacts, whereupon the ohmic electrodes were formed by annealing the alloy metals (Ti/Al/Ni/Au: 15/72/12/40 nm) at 800 °C for 30 s in an N_2 ambient atmosphere. Finally, the gate lithography was performed, and the gate metals (Pd/Ti/Au: 40/20/60 nm) were deposited on the InAlN layer. The drain current–voltage (I_{ds}-V_{ds}) and typical transfer (g_m-V_{GS}) characteristics of the HEMTs were measured using an Agilent B1500A semiconductor device analyzer (Agilent Technologies).

III. RESULTS AND DISCUSSION

The crystal quality is characterized by the full width at half maximum of the peaks in the X-ray rocking curve for the (0004) and (10 − 10) crystal faces of GaN. The densities of the screw (D_{screw}) and edge (D_{edge}) dislocations of the GaN layers for both samples A and B are nearly same, with calculated values of $D_{screw} = 5.0 \times 10^8\,cm^{-2}$ and $D_{edge} = 5.0 \times 10^9\,cm^{-2}$. Figures 1(a) and 1(b) show the AFM images of the surface morphologies of the as-grown samples A and B, respectively, measured across a scan area of $2 \times 2\,\mu m^2$. The measured root mean square (RMS) roughness values are seen to increase from 0.25 nm for sample A to 0.55 nm for sample B, which is a function of increasing growth rate of the InAlN layer. The RMS roughness value of sample A is smaller than the previously reported values of 0.53 and 0.37 nm for the InAlN/GaN heterostructures grown on sapphire[11] and SiC[12] substrates, respectively. The smooth surface morphology in sample A is believed to be caused by the decreasing supply rate of TMAl, TMIn, and ammonia, which facilitates a larger surface

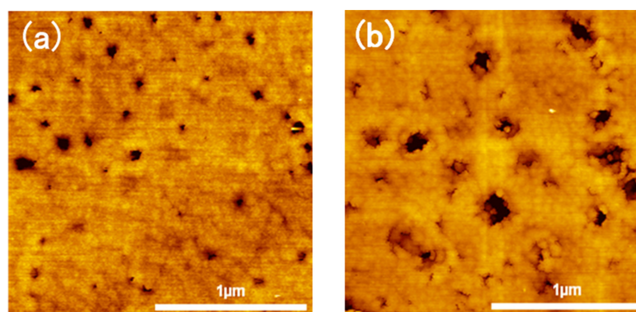

FIG. 1. AFM images of the $In_{0.18}Al_{0.82}N$/GaN surface morphology with a scan area of $2 \times 2\,\mu m^2$ for (a) sample A with a slower growth rate for the InAlN layer and (b) sample B with a faster growth rate for InAlN layer.

diffusion length for the adsorbed species. The slower growth rate leads to improvements in the surface morphology owing to the reduced parasitic gas-phase reactions and to the increased diffusion length of the adsorbed species on the surface for AlN-rich alloys.[13] On the other hand, increasing the growth rate tends to increase the surface roughness because the adsorbed species have a shorter diffusion length for migration to the surface. It should be noted that the difference in the surface morphology between samples A and B is not the density of surface pits but the pit size. Sample A contains shallow pits with an average depth and diameter of 5 and 40 nm, respectively, whereas sample B contains large V-shaped pits with an average depth and diameter of 10 and 160 nm, respectively.

To characterize these V-shaped pits, cross-sectional TEM observations were made for sample B. It can be seen in Fig. 2 that the V-shaped pits originate from the heterointerface between InAlN/GaN near the threading dislocations. Thermal stability of the surface morphologies was analyzed by varying the annealing temperatures from 700 to 850 °C and measuring the RMS roughness by AFM (Fig. 3). As shown in Fig. 3, the surface morphology of sample A remains stable even at 850 °C, while the surface morphology of sample B tends to degrade when the annealing temperature is raised to 850 °C. Further, an increase in surface roughness suggests that significant compositional inhomogeneities may form within the InAlN layer during high-temperature annealing as a consequence of desorption or diffusion phenomena, and especially at the surface.[14,15] These compositional inhomogeneities in turn can cause fluctuations in

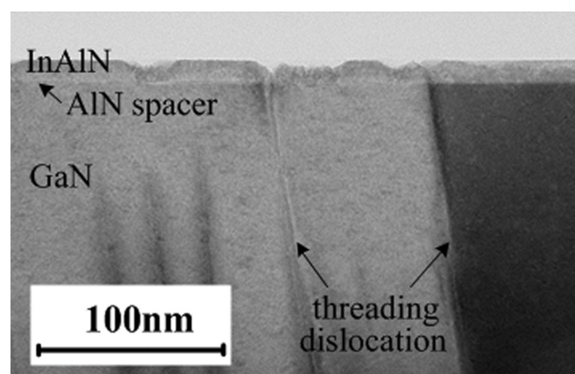

FIG. 2. Cross-sectional TEM image of sample B showing the spread of the V-shaped pits at the InAlN/GaN heterointerface.

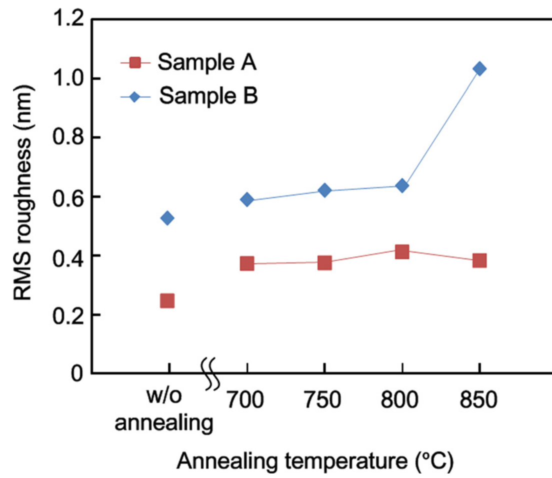

FIG. 3. Measured RMS roughness as a function of annealing temperature for samples A and B.

2-DEG characteristics especially at high annealing temperatures.

To study the influence of the ohmic annealing temperatures upon the 2-DEG characteristics, Hall effect measurements were carried out for samples A and B. The measured sheet carrier density (n_s), sheet resistance (R_{sh}), and the 2-DEG mobility (μ_{2DEG}) at various ohmic annealing temperatures for both samples are shown in Figs. 4(a)–4(c), respectively. Sample A exhibits increased stability of the 2-DEG characteristics when the annealing temperatures are increased from 700 to 850 °C. Even at the high annealing temperature of 850 °C, sample A shows an n_s of $2.2 \times 10^{13}\,\mathrm{cm}^{-2}$, a low R_{sh} of 198 Ω/sq., and a μ_{2DEG} of $1430\,\mathrm{cm}^2$/V s. These values are superior to those previously reported for InAlN/GaN heterostructures on Si substrates.[10,16] This improvement is due to the improved heterointerface property induced by adopting a slower growth rate for the InAlN layer. On the other hand, the 2-DEG characteristic of sample B degrades with increasing ohmic annealing temperature, especially at 850 °C. Although an increase in n_s over that of sample A to a value of $3.3 \times 10^{13}\,\mathrm{cm}^{-2}$ is observed, sample B also exhibits a poor μ_{2DEG} value of $582\,\mathrm{cm}^2$/V s and a high R_{sh} value of 323 Ω/sq.

When the 2-DEG characteristics of samples A and B are compared, the heterointerface of sample B is found to be inferior to that of sample A owing to the existence of the large V-shaped pits. The strength of the scattering depends upon the 2-DEG characteristics of the wave function because the electron scattering is most prominent for the electrons closest to the interface. The centroid of the electron distribution shifts to the interface and, with increased 2-DEG density, more severe interface roughness scattering occurs.[17,18] Hence, by adopting a slower growth rate for the InAlN barrier layer, the heterointerface and surface morphologies are improved, resulting in thermally stable 2-DEG characteristics.

Figures 5(a)–5(c) show the ohmic contact characteristics from the TLM measurements as a function of the annealing temperature. Consistent with the Hall effect measurements, sample A exhibits superior stability in the ohmic contact characteristics for annealing temperatures between 750 and 850 °C. Sample B exhibits dependence of the ohmic

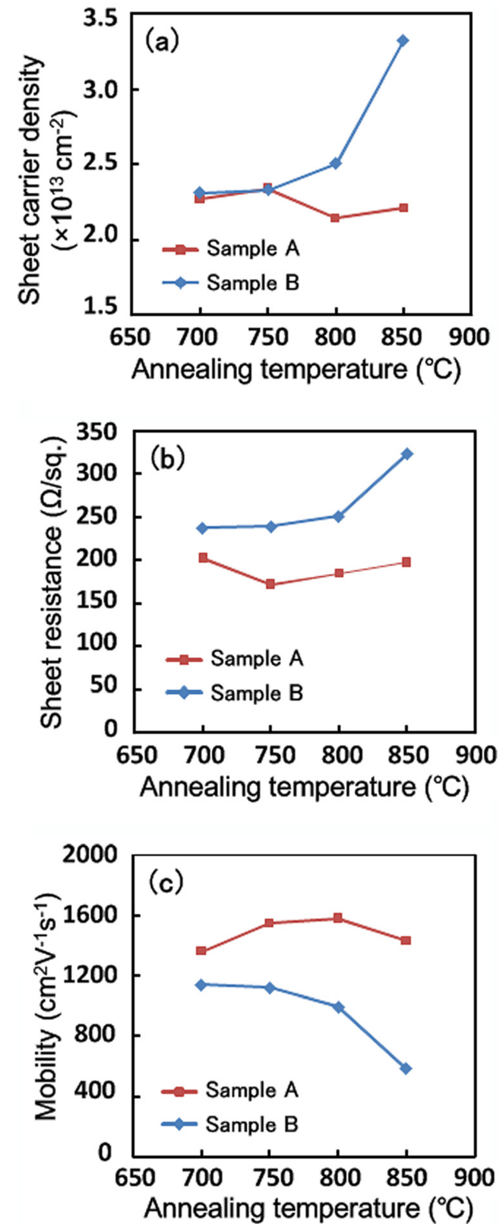

FIG. 4. 2-DEG characteristics comprising the (a) sheet carrier density, (b) sheet resistance, and (c) mobility plotted as a function of annealing temperature for samples A and B.

characteristics upon the annealing temperature, and with increasing annealing temperature from 750 to 850 °C, the R_c decreases from 4.5 to 1.1 Ω mm and the ρ_c also decreases from 1.1×10^{-3} to $6.6 \times 10^{-5}\ \Omega\,\mathrm{cm}^2$, which are comparable with those of sample A. However, the sheet resistance increases from 274 to 326 Ω/sq. This degradation of the sheet resistance at high-temperature annealing (850 °C) as found by TLM measurements is comparable with the Hall effect observations shown in Fig. 4(b).

The observed increase of the n_s of sample B with the ohmic contacts annealed at 850 °C is believed to be due to fluctuations in the InAlN barrier thickness and/or compositional instabilities arising at the high annealing temperature. To understand if the InAlN barrier layer undergoes any thickness change, XRR measurements were carried out for sample B before and after annealing at 850 °C. As shown in Fig. 6,

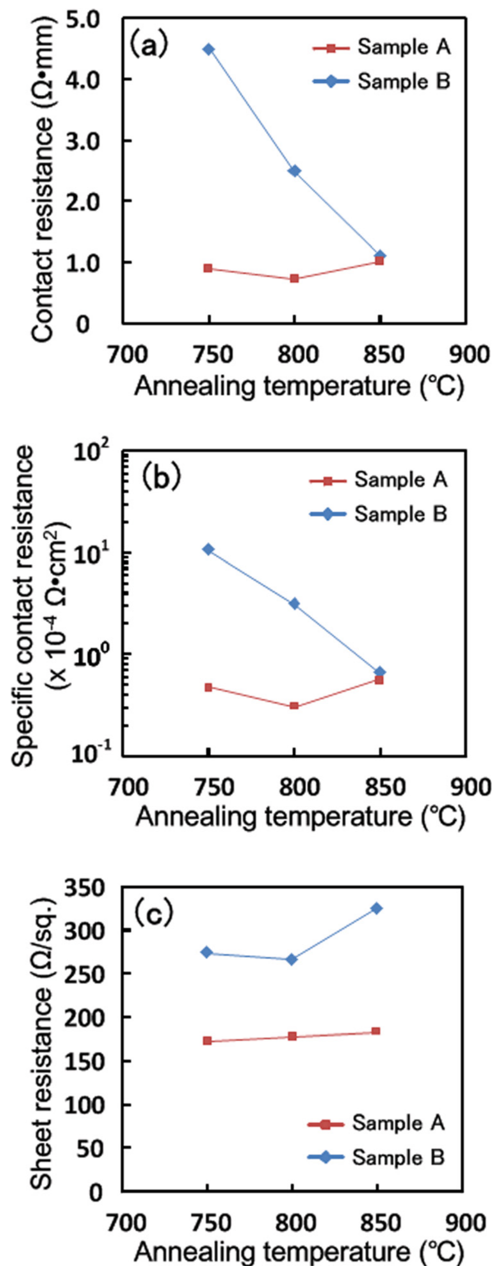

FIG. 5. Ohmic contact characteristics comprising the (a) contact resistance, (b) specific contact resistance, and (c) sheet resistance plotted as a function of annealing temperature for samples A and B.

the interface fringes from the XRR curves can be matched between the as-grown and annealed samples of B, suggesting that the InAlN barrier layer thickness is relatively unchanged.

Next, PL spectra were recorded to determine if compositional inhomogeneities occur in the InAlN layer for sample B annealed at 850 °C, and the spectra of the as-grown and annealed samples of B are shown in Figs. 7(a) and 7(b). A sharp band-edge emission peak at 360 nm corresponding to the GaN layer is observed in the as-grown and annealed samples, whereas after annealing at 850 °C an anomalous peak adjacent to the GaN emission peak is also observed. This peak is believed to be due to compositional inhomogeneity near the GaN channel, which results from the diffusion of In atoms from the barrier layer into the GaN channel at the high annealing temperature. The signature PL emission peak

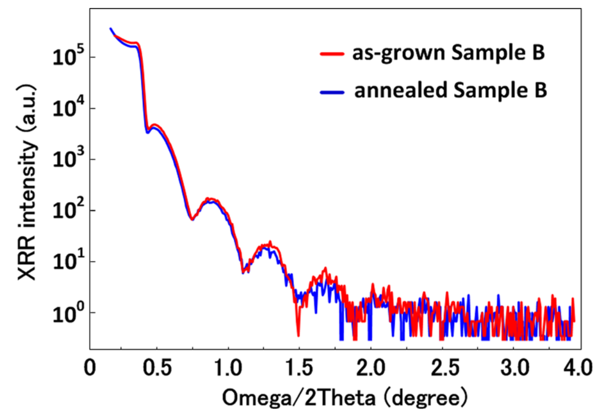

FIG. 6. XRR curves acquired from sample B, for both the as-grown material and that annealed at 850 °C.

existing at relatively lower energy in the spectra from the annealed sample B might also suggest the presence of the $In_xGa_{1-x}N$ ternary alloy with a very low In content.[19] As shown in Fig. 7(b), a broad emission peak at a shorter wavelength of 330 nm due to the band-to-band emission from the InAlN layer is also observed that, after annealing at 850 °C, exhibits a slight blue shift, suggesting a reduced InN content or an AlN-rich barrier layer.[20] To confirm these findings, PL spectra are recorded at several positions on the sample B wafer annealed at 850 °C where, irrespective of the wafer position, similar PL spectra are observed owing to barrier layer composition inhomogeneity (data not shown). The significant changes in the surface morphology of sample B revealed by AFM RMS roughness measurements (Fig. 3) further suggest the compositional inhomogeneities that arise in the InAlN layer during high temperature annealing, which is also influenced by the presence of the V-shaped defects.[14,21,22] This also supports the earlier observations of increased n_s value and 2-DEG mobility degradation when ohmic contact annealing was performed at 850 °C, which is due to a higher AlN content in the barrier.[23] In contrast, sample A annealed at 850 °C exhibits neither an anomalous emission peak adjacent to the GaN emission peak nor a blue shift in the InAlN emission peak, as shown in Figs. 7(c) and 7(d), respectively. Similar to what was done for sample B, these observations for sample A annealed at 850 °C are also confirmed by multiple PL spectra recorded at various wafer positions (data not shown). Because of this consistency of the sample A composition with annealing, no significant changes in the 2DEG characteristics are observed when ohmic contact annealing is as high as 850 °C. From the electrical and optical characterizations of InAlN/GaN heterostructures and their thermal dependencies, it can be ascertained that the InAlN/GaN heterostructures with a slower growth rate for the InAlN barrier layer are thermally stable even at 850 °C and do not undergo surface morphology degradation or barrier composition in homogeneities.

To confirm the effects of the thermal stability upon real device applications, InAlN/GaN/Si HEMTs were fabricated using samples A and B, wherein the gate lengths and widths were 1.8 and 15 μm, respectively. Figure 8(a) shows the comparison of I_{ds}-V_{ds} characteristics for a drain voltage of 0–10 V

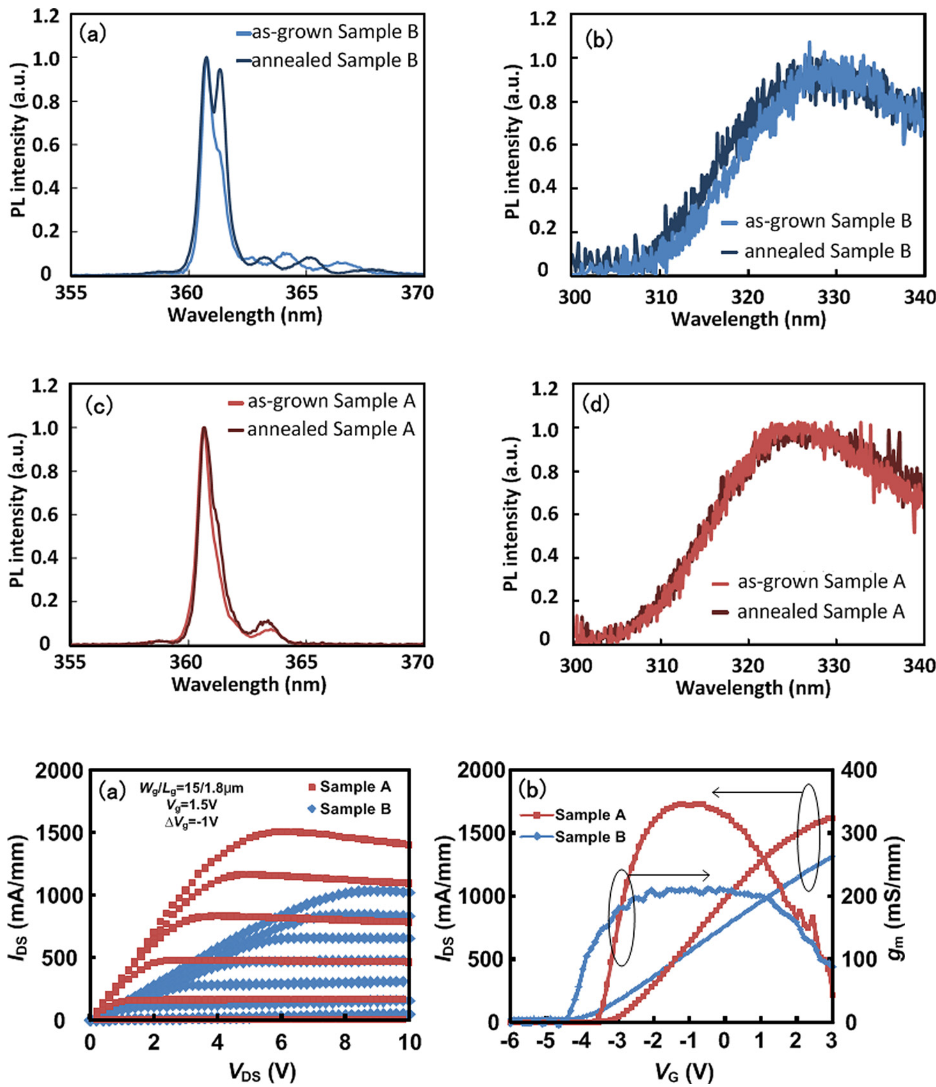

FIG. 7. PL spectra (at 10 K) of the material as-grown and annealed at 850 °C for (a, b) sample B and (c, d) sample A.

FIG. 8. Comparison of the (a) I_{ds}-V_{ds} characteristics and (b) transfer characteristics of the $In_{0.18}Al_{0.82}N$/GaN HEMTs fabricated on samples A and B.

and a gate bias (V_g) of +1.5 V with a step of −1 V. The transfer characteristics at drain bias (V_{ds}) of 8 V are also shown in Fig. 8(b), where it can be seen that a maximum drain current density ($I_{ds,max}$) and transconductance ($g_{m,max}$) value of 1500 mA/mm and 346 mS/mm are achieved for the HEMT on sample A. These excellent device performances for InAlN/GaN HEMTs on Si are even compatible with similar MOCVD-grown InAlN/GaN HEMT structures on sapphire substrates.[24] In contrast, the HEMT on sample B yields relatively low $I_{ds,max}$ and $g_{m,max}$ values of 1034 mA/mm and 210 mS/mm, respectively. The improvements in the device characteristics of sample A is a result of the smooth surface morphology and the thermally stable 2-DEG characteristics of the MOCVD-grown InAlN/GaN/Si heterostructure.

IV. CONCLUSIONS

We have studied thermal stabilities of the lattice-matched InAlN/GaN/Si heterostructures by using a faster and a slower growth rate for the InAlN barrier layer. The InAlN/GaN/Si heterostructure grown with a slower growth rate for the InAlN barrier layer exhibited suppression of the V-shaped pits near the heterointerface and a better surface morphology. Excellent thermal stability of the surface morphology, compositional homogeneity, and electrical properties was achieved in these InAlN/GaN/Si heterostructures. A high sheet carrier density of $2.1 \times 10^{13}\,cm^{-2}$ and a mobility value of $1580\,cm^2/V\,s$ were observed with a low sheet resistance of 185 Ω/sq. at an ohmic annealing temperature of 800 °C. The as-fabricated HEMT exhibited maximum drain current density and transconductance values of 1.5 A/mm 346 mS/mm, respectively, which resulted because of the excellent 2-DEG characteristics at the InAlN/GaN heterointerface. In contrast, the InAlN/GaN heterostructure with a faster growth rate for the InAlN layer results in poor surface morphology with degraded 2-DEG properties at an annealing temperature of 850 °C. These findings are promising for the MOCVD growth of high quality InAlN/GaN/Si heterostructures and their potential application in high-power and high-voltage devices.

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