On the Electrical characterization of Platinum Octaethylporphyrin(PtOEP)/Si hybrid device

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Abstract:

The electrical properties of Au/ PtOEP /p-Si/Al and Au/ PtOEP /n-Si/Al devices were studied in terms of current-voltage I-V characteristics at different temperatures ranging from 308 to 388 K. The two diodes were fabricated with the same qualifications. They showed a rectification behavior. The conduction mechanisms at forward and reverse bias and diode parameters as a function of the temperature for these devices were determined and discussed. The variation of the C^{-2}-V characteristics for two diodes exhibited a straight line fit which supports the abrupt diode type. The interface state density N_{ss} was determined from the I-V and C-V data using Card and Rhoderick's model. Also, the impedance spectroscopy plots for the two diodes and suitable equivalent circuit model were established to evaluate the details of interface carrier transfer and recombination processes.

Key words: PtOEP, Schottky diodes, I-V and C-V measurements, Interface states, Impedance spectroscopy

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1. Introduction

Hybrid inorganic-organic devices have been experienced an explosive growth over the last few years as a promising candidate to overcome the efficiency limitation of purely organic devices [1]. The charge transfer properties of the organic/inorganic and interfacial layer in metal/semiconductor M/S are played a vital role in flexible electronic devices such as Organic Field Effect Transistor (OFET), Organic Light Emitting Diode (OLED) and Organic Photovoltaic (OPV)[2, 3]. Charge injection and transport through the interface are not only important in the understanding of the characteristics the devices, but also a primary challenge in developing and optimizing devices performance. More flexibility in fabricating and controlling devices can be obtained through the modifying interfacial layer. The organic semiconductors are often studied as an interfacial layer in metal/semiconductor M/S structures as these semiconductors can structurally be modified to engineer the rectification properties of M/S [2-4]. The understanding of the basic transport mechanisms in M/S devices is very helpful in differentiating between the influence of the interfacial and bulk effects on the electrical properties of the organic/inorganic semiconductors based devices. Such information would help to select the most difficult parts of the hybrid devices and ways for optimization of the device fabrication technology [5]. Several previous studies have been examined and discussed the effect of the organic layer in M/S, they found that effective Schottky barrier could be either increased or decreased by using an organic thin layer on the inorganic semiconductor. For example, Cakar et al. [6] have been designed the Cu/pyronine-B/p-Si, Au/ pyronine-B/p-Si, Al/pyronine-B/p-Si and Sn/pyronine-B/p-Si diodes they found that barrier heights of diodes larger than the conventional metal/p-Si contacts. Also, Farag et al. [7] and Ozaydin et al [8] they have been found that the barrier height of Au/ Oxazine/n-Si and Al/Copper (II) complex/n-Si, respectively less than the barrier height of the conventional Au/n-Si and Al/n-Si diodes. This behavior due to the realignments between the lowest unoccupied molecular orbital (LUMO), the highest occupied molecular orbital (HOMO) of the organic semiconductor and the work function of the metal, in the electron affinity of the semiconductor at the organic/inorganic semiconductor interface can cause a decrease or increase in barrier height. Indeed, modification of semiconductor surfaces by molecules can lead to the changes in the electronic properties of the metal–semiconductor devices [6, 7-9]. Moreover, Au/ NiPc/p-Si/Al [10], Au/ NiPc/n-Si/Al[11], Au/ TPP/n-Si/Al[12], Au/ TPP/p-Si/Al[13] have been exhibited the same behavior. However, the exact basic transport mechanisms in M/S devices is not fully understood and still requires further understanding of the role of the interface layer, in fabrication high-performance metal/organic /Si devices substrates. In recent years, porphyrin and its derivatives have been considered as a valuable material in both fundamental science and technology because of its excellent properties, such as high chemical and thermal stability and efficient light absorption ability in the visible and near-infrared. Also, porphyrin and its derivatives have the conjugated system consisting of 18π and the ability to self-assemble on surfaces as well

as these can easily be deposited as thin films with high quality by thermal evaporation without dissociation electrons. These unique properties including optical, electronic, and structural properties make porphyrin very promising for wide applications of in future electronics. Among of porphyrin derivatives Platinum octaethylporphyrin (PtOEP) which is it recently used as active layer in field-effect transistors and solar cells [14, 15]. Furthermore, (PtOEP) has been studied as a red phosphorescence material for OLED and it has shown a short phosphorescence lifetime due to the mixing of singlet and triplet excited states caused by platinum [16, 17].Through our previous work we have been studied the structure and optical properties of PtOEP thin films beside the AC conductivity dielectric measurements [18-20]. However, the electrical conduction mechanisms and impedance spectroscopy of PtOEP /Si have not been extensively studied yet. Therefore there is an urgent need for the deepest study of the mechanisms of the carrier transport mechanism. The present work focuses on the charge transport mechanism through Au/ PtOEP /p-Si/Al and Au/ PtOEP /n-Si/Al Schottky diodes using the I-V, C-V and impedance spectroscopy measurements.

2. Experimental techniques

The Platinum octaethylporphyrin (PtOEP) (dye content 98 %) purchased from Aldrich and used without further purification. Schottky junctions were designed and fabricated using p-type <100> single crystal silicon (Boron-doped) wafer with a doping concentration of 1.6×10^{15} cm^{-3}.While the n-type <100> single crystal silicon(phosphorus-doped) wafer with a doping concentration of 2×10^{16} cm^{-3},also all silicon substrates have a thickness of 0.5 mm and were purchased from Sigma-Aldrich Chem. Co. The p-Si and n-Si substrate were etched using chemical etching solution of HF: HNO3: CH3COOH in the ratio of 1:6:1. After etching, the Si substrates were washed with distilled water and then by ethyl alcohol several times. The ohmic contact was made by evaporating 99.99% purity Al metal on the back of the substrate with a thickness of 300 nm and deposition rate 0.5 nm/s. After this stage, the samples were annealed at 450 C for 10 min in the N_2 atmosphere. PtOEP thin film with a thickness 120nm was evaporated with deposition rate 0.3 nm/s. Evaporation of the PtOEP was carried out with a quartz crucible heated by a tungsten coil, the distance between the source and the substrate is about 25cm with a substrate temperature (25 C^o). The Schottky contacts were made by evaporating 200 nm of gold (Au-mesh) onto the PtOEP at a rate of 0.2 nm/s. All the layers (Al, PtOEP, and Au) were evaporated using thermal evaporation technique, under a vacuum of 10^{-6} Torr (Edwards, E306A). Also, the thickness, as well as the rate of deposition, were controlled using quartz crystal thickness monitor (Edwards, FTM5) and confirmed by Tolansky's interferometric technique [21]. The schematic diagram of the Au/PtOEP/p-Si/Al and Au/PtOEP/n-Si/Al diodes structure is shown in **Fig.1.** High impedance programmable electrometer (Keithley, model 2635A) used to study the dark current-voltage (I-V) measurements of the fabricated junction at temperatures range (308-388 K). The temperature was measured directly by NiCr-NiAl thermocouple. All measurements were performed in a complete dark oven. The dark (C-V) characteristics of

the fabricated devices were measured at room temperature and frequency 1 MHz, using a computerized (C-V;410 meter, model 4108). Also, the impedance spectroscopy was measured at room temperature in the air in the frequency range of 25 Hz to 1MHz using an impedance analyzer (Agileny, model 4284A).

3. Results and discussion

3.1. Dark current–voltage (I-V) characteristic.

Analysis of I–V characteristics is particularly useful to identify the transport mechanisms and determination of related parameters such as Rectification Ratio RR, barrier height Φ_B, ideality factor n, series resistance R_S. **Fig. 2(a) & (b)** shows the semilogarithmic dark current-voltage (I-V) characteristics of Au/PtOEP/p-Si/Al and Au/PtOEP/n-Si/Al diodes, respectively in a temperature range 308 to 388 K in the voltage range (0–2 V) in both forward and reverse directions. The curves exhibit diode-like behavior in the two diodes which are influenced by increasing temperature. This behavior is attributed to the formation of the depletion region between the PtOEP and Si single crystal [22]. As shown in **Fig. 2(a) & (b)** the semilogarithmic plots of the forward current-voltage characteristics for the two devices are consisting of two distinct regions. At low positive voltage ($V \leq 0.5$ volt-Region (I)) for Au/PtOEP/p-Si/Al diode and ($V \leq 0.4$ volt-Region (II)) for Au/PtOEP/n-Si/Al, the current increases exponentially with the applied voltage. While at the high positive voltage the current is deviated from the straight line due to a voltage drop across the series resistance associated with the neutral region of a semiconductor and interface states. Also, the results show the existence of a weak leakage current in the reverse bias direction and it proves a good rectification performance for the two diodes. The important parameters of two diodes such as rectification ratio RR, series resistance R_S, shunt resistance R_{Sh}, ideality factor n and barrier height Φ_B can be determined by the analysis based on **Fig. 2(a) & (b)**. At ±1 V, the rectification ratio RR which is defined as the ratio between the forward and reverse bias current at a fixed potential is found to be 7.77 and 22.13 for Au/PtOEP/n-Si/Al and Au/PtOEP/p-Si/Al diodes, respectively. This indicates that Au/PtOEP/p-Si/Al diode has better performance than Au/PtOEP/n-Si/Al diode. The R_S and R_{Sh}, are determined from the plot of the diode junction resistance R_J against voltage [23], where, which can be determined from the I-V curves A plot of R_J versus V is shown in **Fig. 3(a) & (b).** The average values of Rs and R_{Sh}, at different temperatures for Au/PtOEP/n-Si/Al and Au/PtOEP/p-Si/Al diodes are listed in **Table 1**. The very high series resistance (Rs= 2957±0.1 Ω) behavior in the case of Au/PtOEP/n-Si/Al may be attributed to the decrease in the exponentially increasing rate in current due to space-charge injection into the PtOEP organic film at higher forward bias voltage [24]. The very high series resistance behavior were observed in a lots of organic/n-Si devices such as Al/GO: C8-BTBT/n-Si/Au; Rs= 4619 Ω [25], Au/Anthracene/n-Si/Al; Rs= 58000 Ω [26], Au /PLiMMA/n-Si; Rs= 8096 Ω [14] and Au/β-carotene/n-Si/Al; Rs= 19237 Ω [27]. It has been noted that the values of Rs and R_{Sh} decrease with increasing

temperatures. Such behavior can be owing to the particular density distribution of interface and rearrangement of interface charge at the interface with the increasing temperature [28, 29]. At relatively low forward applied voltages, the relation is linear and the current of the device can be described by the thermionic emission theory expressed through [30, 31]:

$$\mathrm{I} = \mathrm{I}_o\left(\exp\left(\frac{qv}{nK_BT}\right) - 1\right) \quad (1)$$

Where Io is the saturation current and it is defined by [29, 30]:

$$\mathrm{I} = \mathrm{AA}^* T^2 \exp\left(\frac{-q\Phi_B}{k_{BT}}\right) \quad (2)$$

Where A is the effective area ($0.2cm^2$) and A^* is the Richardson constant that takes values of 32 $A/cm^2\ K^2$ and 120 $A/cm^2\ K^2$ for p-Si and n-Si [32]. Also, Φ_B is the zero-bias barrier height which is expressed by [29]:

$$\Phi_B = \frac{k_BT}{q}\ln\left(\frac{AA^*T^2}{I_o}\right) \quad (3)$$

The value of the ideality factor n is calculated from the slope of the linear portion of forward bias of I–V characteristic using the following equation [29]:

$$n = \frac{q}{k_BT}\left(\frac{\mathrm{dV}}{\mathrm{d\ ln\,I}}\right) \quad (4)$$

Using Eqs. (3) and (4), the experimental values of the Φ_B and the ideality factor n for each temperature are determined from the intercept and slope of the relation ln(I) vs. V for low forward applied voltages. The average values of n and Φ_B with temperatures are presented in **Table 1** for Au/PtOEP/n-Si/Al and Au/PtOEP/p-Si/Al diodes. It was observed that n and Φ_B values are ranging from 3.88 to 3.73 and 0.63 to 0.77 eV, respectively in the case of Au/PtOEP/p-Si/Al diode. Moreover, in the case of Au/PtOEP/n-Si/Al diode, the values of n and Φ_B are extending from 3.74 to 3.29 and 0.771 to 0.887eV, respectively in the same temperature range (308 to 388 K). As detected, the behavior of n and Φ_B with increasing the temperature much like to the behaviors of Au/p-Si [33, 34] and Au/n-Si diodes [35-38] and Au/organic/Si substrate such as Au/ NiPc/p-Si/Al[10], Au/ NiPc/n-Si/Al[11], Au/TPP/n-Si/Al[12], Au/TPP/p-Si/Al[13]. The decrease in n and increase in Φ_B with increasing temperature can be explained on the base of a particular distribution of the interface states or an alternative approach to the lateral inhomogeneities that are found in the Schottky barrier interfaces, i.e. the Schottky barrier contained laterally inhomogeneous patches of different barrier heights. The patch with lower barrier height yields a larger ideality factor and vice veers [36, 38-40]. It is observed that the deviations in the ideality factor and barrier height may be due to spatially inhomogeneous barrier height and

1 the potential fluctuations at the interface that consist of the low and high barrier heights. The charge carries
2 transport across the PtOEP/Si interface is a temperature activated process so, the charge carries at low
3 temperatures are able to surmount the low barriers and therefore charge carries transport will be dominated by
4 the current flowing through the patches of low barrier height. With increasing temperature, more charge
5 carriers acquire enough energy resulting in surmounting higher barriers [36, 37, 41-43]. Also, the linear
6 relationship between the Φ_B and the n in the temperatures range (308 to 388 K) show in **Fig.4**, according to
7 Schmitsdroff et al [43] this behavior confirmed the lateral barrier inhomogeneities in two diodes. Deviation of
8 n far from unity may be attributed to either recombination of electrons with holes in the depletion region,
9 and/or the increase in the diffusion current due to increasing the applied voltage [7]. The higher values of n
10 may be attributed to factors such as interfacial layer thickness, leakage, shunting, bulk series resistance, or any
11 resistive loss [44, 45]. The barrier height (0.63 eV) of the tested Au/PtOEP//p-Si and is higher than that of the
12 conventional Au/p-Si Schottky diode (0.33 eV) [32]. Also, the barrier height (0.771 eV) of the tested
13 Au/PtOEP//n-Si is lower than that of the conventional Au/n-Si Schottky diode (0.79 eV) [46]. This behavior
14 suggests that the PtOEP organic layer modifies the barrier height value. This behavior may be owing to the
15 realignments between the (LUMO) and (HOMO) of the PtOEP besides the work function of the metal. The
16 Schottky barrier height is defined differently for n-type and p-type semiconductors (being measured from the
17 conduction band edge and valence band edge, respectively). The alignment of the semiconductor's bands near
18 the junction is typically independent of the semiconductor's doping level. Therefore the n-type and p-type
19 Schottky barrier heights are perfectly related to each other by ($\Phi_B^n + \Phi_B^p = E_g$), i.e., The sum ($\Phi_B^n + \Phi_B$p) of
20 barriers on p-Si and n-Si for the same metal is equal, within the limits of experimental error, to the energy gap
21 of Si (E^{Si}_g =1.12 eV) [32]. However, in our diodes, we have found that (Φ_B (PtOEP/p-Si) + Φ_B (PtOEP/n-Si >
22 E^{Si}_g). Briefly, we have demonstrated that the Au/PtOEP/n-Si/Al and Au/PtOEP/p-Si/Al diodes can be
23 characterized by the barrier heights that are larger than those which are obtained for the conventional Au/p-Si
24 and Au/n-Si contact. That is, the barrier height can be enhanced or modified using the thin PtOEP films. The
25 forward current as a function of applied voltage at high forward biasing a different mechanism is operating. As
26 observed in **Fig. 5(a) & (b)** the current shows a power-law exponent of the form I αV^m for Au/PtOEP/p-Si/Al
27 and Au/PtOEP/n-Si/Al diodes, respectively. The slope of the ln(I)-ln(V) characteristics, is about 2, clarifying
28 that the forward biased current is space-charge-limited current (SCLC) controlled by a single dominating trap
29 level. According to Lampert`s theory, the current was given by the following expressed [47]:

30 $$I = \frac{9}{8}\varepsilon_i\varepsilon_o\mu\theta\frac{N_v V^2}{N_t d^3}\exp\left(\frac{-E_t}{K_B T}\right) \quad (5)$$

Where ε_o is the permittivity of free space, ε_i is the relative permittivity of the PtOEP thin film which equals 2.52 [18, 19], μ is the hole mobility (taken as 10^{-4} cm^2 $V^{-1}s^{-1}$ [48]), θ is the trapping factor and d is the thickness of the PtOEP thin film. Where, N_v is the effective density of states in the valence band (taken as 10^{21} cm^{-3} for organic materials [22]) and N_t is the total trap concentration situated at energy level E_t above the valence band edge. The temperature dependence of the current in SCLC region (V=1.5 Volt) is shown in **Fig. 6** for Au/PtOEP/p-Si/Al and Au/PtOEP/n-Si/Al diodes. The value of E_t and N_t for two diodes are determined from the slope and intercept of the Plot $\ln I_f$ versus 1000/ T For Au/PtOEP/p-Si and Au/PtOEP/n-Si diodes, the obtained values of E_t and N_t were determined as 0.244eV, 2.34×10^{22}, and 0.171eV, 1.54×10^{22} cm^{-3} respectively. The reverse I-V characteristics give further information on the conduction mechanism of Au/PtOEP/p-Si and Au/PtOEP/n-Si diodes are shown in **Fig.7 (a) & (b),** respectively. The reverse current increases exponentially with increasing voltage and display the strong dependence of temperature. With the increase of the applied electric field, different leakage mechanisms may occur and become dominant. The current transport mechanism dominating the reverse leakage current in the Au/PtOEP/p-Si and Au/PtOEP/n-Si diodes is investigated using the electric field dependence considering by Poole-Frenkel emission or Schottky emission. The Schottky emission mechanism can be expressed as [49]:

$$I_R = AA^*T^2 \exp\left(\frac{-\Phi_S}{k_B T}\right) \exp\left(\frac{\beta_S V^{1/2}}{k_B T d^{1/2}}\right) \quad (6)$$

Where Φ_s is the Schottky barrier height at the injected electrode interfaces and βs is the Schottky coefficient. The Poole- Frenkel emission mechanism can be expressed as [49]:

$$I_R = I_S \exp\left(\frac{\beta_{FF} V^{1/2}}{k_B T\, d^{1/2}}\right) \quad (7)$$

Where β_{PF} is the Poole Frenkel field-lowering coefficients, respectively. Theoretical values for both β_s and β_{PF} are given by [49]:

$$\beta_{FF} = 2\beta_S = \left(\frac{q^3}{\pi \varepsilon_o \varepsilon_i}\right)^{1/2} \quad (8)$$

The dominant conduction mechanism for the reverse current can be understood by plotting the I-V characteristics in the form of $\ln I_R$ versus $V^{1/2}$ at the different temperature as shown in **Fig. 7(a) &(b)** for Au/PtOEP/p-Si/Al and Au/PtOEP/n-Si/Al diodes. It can be seen from the figure that, the current is characterized by two linear segments with different slopes, which may be interpreted in terms of two different conduction mechanisms. Also, the Poole–Frenkel and Schottky mechanism can be distinguished by their different field-lowering coefficients. As seen in Eq. (8) the Poole–Frenkel field-lowering coefficient is twice

the Schottky field-lowering coefficient. The theoretical values of these coefficients are β_{PF}=4.77x10^{-4} eV cm$^{1/2}$ V$^{-1/2}$and β_S=2.38x10^{-4} eV cm$^{1/2}$ V$^{-1/2}$. The mean values β calculated from the slopes of **Fig. 7(a) & (b)** and are found to be β=4.26x10^{-4} eV cm$^{1/2}$ V$^{-1/2}$and β=2.18x10^{-4} eV cm$^{1/2}$ V$^{-1/2}$ for the lower (LR) and higher (HR) voltage regions, respectively in the case of Au/PtOEP/p-Si/Al. While, β=3.96x10^{-4} eV cm$^{1/2}$ V$^{-1/2}$and β=2.08x10^{-4} eV cm$^{1/2}$ V$^{-1/2}$ for the lower and higher voltage regions, respectively in the case of Au/PtOEP/n-Si/Al. It is observed that the experimental values of β in low voltage region are twice its values in high voltage region; this indication that Pool-Frenkel conduction mechanism is operating in low voltage region. While Schottky emission mechanism is functioning in high voltage region.

3.2. Capacitance-voltage characteristics

Each junction has a specific capacitance due to the formation of a space charge in the depletion layer. It relates to the width of the depletion region and therefore it depends on the applied voltage. Electrical junction parameters such as carrier concentration, built-in potential, and depletion layer width are obtained from the capacitance– voltage (C-V) relation. The high frequency (1MHz) is used to investigate diodes capacitance because the data obtained from the C-V measurement in the low frequencies range represents the sum of the space charge capacitance and the interface capacitance. As the frequency increases, the interface capacitance contribution to the device capacitance decreases. **Fig. 8(a) & (b)** shows the dark capacitance-voltage(C-V) and (C^{-2}-V) characteristics of Au/PtOEP/p-Si/Al and Au/PtOEP/n-Si/Al diodes at room temperature. The reversely biased capacitance was found to be decreased with the increase of reverse-biased voltage. This decrease may be attributed to the increase in the barrier width of the depletion layer at the interface of the heterojunction. The linearity of this dependence indicates that the junction is considered as an abrupt heterojunction [32]. The junction capacitance can be expressed by the following [10, 49]

$$C^{-2} = \frac{2(V_{bi}-V)}{qA^2 N_D \varepsilon_i \varepsilon_o} \quad (9)$$

Where A is the effective area (0.2cm^2), V_{bi} is diffusion potential or the built-in voltage at zero bias, V is the applied voltage, N_D is the charge carrier concentration distributed through the depletion region, q is the electronic charge, ε_o is the permittivity of free space and ε_i is the relative permittivity of the PtOEP thin films [18, 19]. The built-in potential (V_{bi}) calculated from the intercept at C^{-2} = 0, while N_D calculated from the slope of the straight line. The obtained average values of V_{bi} and N_D for the two diodes are listed in **Table 2**, also the average capacitance of the device (C_o) at zero bias for the two diodes are given in **Table 2**. The width of the depletion layer (W_D) and the maximum barrier field (E_{max}) of Au/PtOEP/p-Si/Al and Au/PtOEP/n-Si/Al diodes are calculated using the following relations [10, 49]:

1 $$W_D = \sqrt{\frac{2\varepsilon_i \varepsilon_o V_{bi}}{qN}} \quad (10)$$

2 $$E_{max} = \frac{2V_{bi}}{W_D} \quad (11)$$

3 The value of the barrier height Φ_B (C-V) can be obtained by the following relation [49-51]:

4 $$\Phi_C(C - V) = V_{bi} + E_F - \Delta\Phi_B \quad (12)$$

5 Where $\Delta Ø_B$ is the image force barrier lowering and E_F is the Fermi energy level. The average values of W_D,
6 E_{max} and Φ_B (C-V) for the two diodes are obtained and listed in **Table 2**. This disagreement between the
7 values of Φ_B (I-V) and Φ_B (C-V) may be due to nature of the C-V and I-V measurement techniques or can
8 be explained by a distribution of Schottky barrier height due to the inhomogeneities [50, 51]. The mechanism
9 of a Schottky junction solar cell can be understood qualitatively by plotting the energy band diagram [52]. The
10 schematic energy band diagrams of forward-biased single p-Si and n-Si Schottky junction solar cells under
11 illumination were displayed in **Fig. 9(a) & (b)**, respectively. Depending on work functions φ, electron
12 affinities χ and energy gaps of two semiconductors [53]. The band profile of PtOEP /Si can be constructed.
13 PtOEP has a band gap of 2.21[18, 19] and PtOEP exhibits p-type conductivity [54].In this work, we found that
14 for two diodes:

15 $$\chi_{Si} > \chi_{PtOEP}\, ,\varphi_{Si} > \varphi_{PtOEP}\ \&\ E_g^{Si} < E_g^{PtOEP} \quad (13)$$

16 Built-in potential (V_{bi}) forms in the Si near the PtOEP/Si interface, the carriers around the interface in Si tend
17 to move to the PtOEP side, and therefore, the energy levels near the Si surface will bend downward for p-Si
18 (see **Fig. 9(a)**).The same behaviors have been observed for TPP/p-Si [13], NR/p-Si [55], FeTPPCl/p-Si [56],
19 InPcCl-D/p-Si [57]. While in the case of PtOEP /n-Si, Si surface will bend upward for n-Si, due to charge
20 transfer, free holes and free electrons are accumulated in space charge layers (see **Fig. 9(b)**). Also, the same
21 behavior has been observed for GO–Fe3O4 nanocomposites/n-Si [58], P3HT/n-Si [59] and PEDOT: PSS/n-Si
22 [60].

23 **3.3. Determination of the interface state density**

24 Interface states seem to play the vital role in the transport characteristics of the interfacial structure of
25 PtOEP/Si. For a diode having interface states in equilibrium with the semiconductor, the ideality factor n
26 becomes greater than unity as proposed by Card and Rhoderick [61]. The voltage-dependent ideality factor
27 n(V) is given by[62]:

28

$$n(V) = \frac{q}{k_B T}\left(\frac{V - IR_S}{ln(^I/_{I_o})}\right) = 1 + \frac{\delta}{\varepsilon_i}\left(\frac{\varepsilon_S}{W_D} + qN_{SS}(V)\right) \quad (14)$$

Interface state density N_{SS} is given by [62]:

$$N_{SS} = \frac{1}{q}\left(\frac{\varepsilon_i}{\delta}(n(V) - 1) - \frac{\varepsilon_S}{W_D}\right) \quad (15)$$

Where δ is the thickness of the interfacial layer, W_D is the width of the space charge region calculated from corrected $1/C^2$ at 1 MHz. Also, εi and ε_s are the relative permittivity of PtOEP and silicon semiconductor, respectively. The value of δ/ε_i was determined using the following [63]:

$$\frac{\delta}{\varepsilon_i} = \left(\frac{\varepsilon_S}{W_D}\left(\frac{1}{\beta_r} - 1\right)\right)^{-1} \quad (16)$$

Where $\beta_r = (kT/q)(d(\ln I)/V)$ is the slope of the I-V characteristics. In p-type semiconductors, the energy of the interface states E_{SS} with respect to the top of the Valence band at the surface of the semiconductor is given by [63]:

$$E_{SS} - E_V = q(\emptyset_e - V) \quad (17)$$

Where E_V is the Valence band edge and V is the applied voltage drop across the depletion layer. Also, in n-type semiconductors, the Ess with respect to the bottom of the conduction band at the surface of the semiconductor is given as [64]:

$$E_C - E_{SS} = q(\emptyset_e - V) \quad (18)$$

Where E_C is the conduction band edge. The effective barrier height $\emptyset_e$ is assumed to bias dependent due to the presence of an interfacial PtOEP layer and interface states located between interfacial layer and semiconductor interface, and is given by [64]:

$$\emptyset_e = \emptyset_B + \beta(V - IR_S) = \Phi_B + \left(1 - \frac{1}{n(V)}\right)(V - IR_S) \quad (19)$$

Where β is the voltage coefficient of the effective barrier height Φe. A plot of N_{ss} versus E_V–E_{ss} and E_C–E_{ss} are shown **Fig. 10(a) & (b),** respectively. The average values of Nss are in the ranges from 1.74x1013 cm^{-2} eV^{-1} to $5.99\text{x}10^{12}$ cm^{-2} eV^{-1} for the Au/PtOEP/p-Si/Al diode. While, the values of Nss are extended from$1.52\text{x}10^{12}$ cm^{-2} eV^{-1} to $3.99\text{x}10^{11}$ cm^{-2} eV^{-1} in the case of Au/PtOEP/n-Si/Al diode. These variations can be attributed to the decrease in recombination center and the existence of the interfacial electronics states in the PtOEP organic layer between the metal and inorganic substrate [65, 66]. As can be seen in **Fig. 10(a) & (b),** the exponential growth of the interface state density from mid-gap towards the bottom of the valance band in the case of Au/PtOEP/p-Si/Al diode and from the mid-gap towards the top of the conduction band in the case of Au/PtOEP/n-Si/Al diode. Also, the obtained values of N_{SS} decrease with applied voltages.

In this structure, deposition of PtOEP on the inorganic semiconductor (p-Si or n-Si) can generate a large number of interface states at the semiconductor surface that strongly influence the properties of the diode.

3.4. Impedance spectroscopy

Impedance spectroscopy is a powerful technique widely used to study the interface charge transport processes and the charge transfer and recombination through the device [67-69]. **Fig.11 (a) & (b)** displays the Nyquist (Cole-Cole) plots of impedance spectroscopy spectra for Au/PtOEP/p-Si and Au/PtOEP/n-Si diodes, respectively. The impedance spectroscopy spectra are recorded for the two diodes in the frequency range from 25 to 1 MHz and bias voltage 0.6 V and display large semi-circle at high-frequency and small semi-circle reminiscent at a lower-frequency in a complex impedance plane, with a large difference in magnitude for two different diodes. The equivalent circuit is shown as an inset in **Fig.11 (a) & (b)** is used to fit the impedance spectroscopy data. The Rs in this equivalent circuit model is the series resistance of contacts, wires. The large semi-circle (R_j C_j element) in the high-frequency range describes the charge transfer/recombination processes at the PtOEP / Si, however the small semi-circle in the low-frequency range (R_b C_b elements) is related to the charge transfer/recombination processes at the Al/Si interfaces [67]. The minority carrier lifetime of charge carriers before recombination at two interfaces (PtOEP / Si and Al/Si) can be obtained from the relationship [67]:

$$\tau_j = R_j C_j \quad (20)$$

$$\tau_b = R_b C_b \quad (21)$$

Where τ_j is the carrier lifetime at the PtOEP / Si interface, while τ_b is the carrier lifetime at the Al/ Si interface. The bode phase of impedance spectroscopy spectra as shown in **Fig. 12** display the characteristic frequency peaks in the low- and high-frequency regions, which are used to estimate the τ_b and τ_j, respectively. The average values for all impedance spectroscopy parameters such as R_b, C_b, R_j, C_j, τ_j and τ_b are listed in **Table .3**. As results of the Al, this acts as a p-type dopant [70, 71]. Therefore, the potential barrier at the p^+- (p-Si) junction is smaller than p^+- (n-Si) [71-73] junction. Then this in turn ultimately leads to reduce the value of C_b and in contrast increase the value of R_b values in the case of Al/n-Si interface.

4. Conclusions

The temperature dependence of I-V characteristics of Au/PtOEP/p-Si/Al and Au/PtOEP/n-Si/Al Schottky diodes were studied in the temperature range of 308–388 K. The influence of the temperature on the diode parameters such as Φ_B, n, and R_s, R_{sh} indicates observable temperature dependence. The value of n is

decreased with the increase in temperature but Φ_B is increased. The I-V conduction mechanisms for the two diodes were explained on the basis of thermionic emission under low forward bias with considering the inhomogeniety due to the mismatch at the interface and SCLC under high forward bias. Under reverse bias, the current is dominated by the Poole–Frenkel effect at low voltage region, whereas Schottky emission is the dominant mechanism at the higher voltage region. From the C-V measurements at high-frequency 1MHz, one can obtain information about the depletion layer extending in the Si side. These characteristics are reasonably interpreted by assuming the abrupt heterojunction model. The interface state density N_{SS} is determined from the I-V and C-V data using Card and Rhoderick's method for two diodes at room temperature. The values of N_{SS} are in the ranges from $1.74x10^{13}$ cm^{-2} eV^{-1} in (0.722-E_V) eV to $5.99x10^{12}$ cm^{-2} eV^{-1} in (0.820-E_V) eV for the Au/PtOEP/p-Si/Al diode. While Nss ranges from $1.52x10^{12}$ cm^{-2} eV^{-1} in (Ec-0.52) eV to $3.99x10^{11}$ cm^{-2} eV^{-1} in (Ec-0.61) eV for Au/PtOEP/n-Si/Al diode. In the impedance spectroscopy spectra, the large semi-circle (R_j C_j element) in the high-frequency range describes the charge transfer/recombination processes at the PtOEP / Si, while the small semi-circle in the low-frequency range (R_b C_b elements) is related to the charge transfer/recombination processes at the Al/Si interfaces.

Acknowledgments

This work was financially supported by South Valley University, Egypt.

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Figure caption

Fig. 1. The schematic cross section of the Au/ PtOEP/p-Si/Al and Au/ PtOEP/n-Si/Al diodes.

Fig. 2. Dark J-V characteristics under forward and reverse bias at different temperatures for the (a) Au/ PtOEP/p-Si/Al and (b) Au/ PtOEP/n-Si/Al diodes.

Fig. 3. The junction resistance R_J versus the applied voltage V for (a) Au/ PtOEP/p-Si/Al and (b) Au/ PtOEP/n-Si/Al diodes measured at different temperatures.

Fig. 4. The zero-bias barrier height (Φ_B) versus the ideality factor (n) for (a) Au/ PtOEP/p-Si/Al and (b) Au/ PtOEP/n-Si/Al diodes measured at different temperatures.

Fig. 5. Variation of ln J_f versus lnV for (a) Au/ PtOEP/p-Si/Al and (b) Au/ PtOEP/n-Si/Al diodes measured at different temperatures.

Fig. 6. Plot of lnJ_f versus 1000/ T for Au/ PtOEP/p-Si/Al and Au/ PtOEP/n-Si/Al diode in SCLC region (V=1.5 Volt).

Fig. 7. The plot of ln J_R versus $V^{1/2}$ for (a) Au/ PtOEP/p-Si/Al and (b) Au/ PtOEP/n-Si/Al diodes measured at different temperatures.

Fig. 8. C-V and C^{-2}-V characteristics for (a) Au/ PtOEP/p-Si/Al and (b) Au/ PtOEP/n-Si/Al diodes measured at room temperatures.

Fig. 9. Energy band diagram for a) Au/ PtOEP/p-Si/Al and (b) Au/ PtOEP/n-Si/Al diodes.

Fig. 10. The interface state density N_{ss} for (a) Au/ PtOEP/p-Si/Al and (b) Au/ PtOEP/n-Si/Al diodes measured at room temperatures.

Fig. 11. Nyquist plots of (a) Au/ PtOEP/p-Si/Al and (b) Au/ PtOEP/n-Si/Al diodes measured at room temperatures. Inset shows the basic RC model of the equivalent circuit for studied diodes.

Fig. 12. Bode phase plots for Au/ PtOEP/p-Si/Al and Au/ PtOEP/n-Si/Al diodes measured at room temperatures.

Table caption

Table 1. The dark J-V parameters for Au/PtOEP/p-Si/Al and Au/PtOEP/n-Si/Al diodes.

Table 2. The C-V parameters for Au/PtOEP/p-Si/Al and Au/PtOEP/n-Si/Al diodes.

Table 3. The Impedance spectroscopy parameters for Au/PtOEP/p-Si/Al and Au/PtOEP/n-Si/Al diodes.

1 **Figures**

2 **Fig.1**

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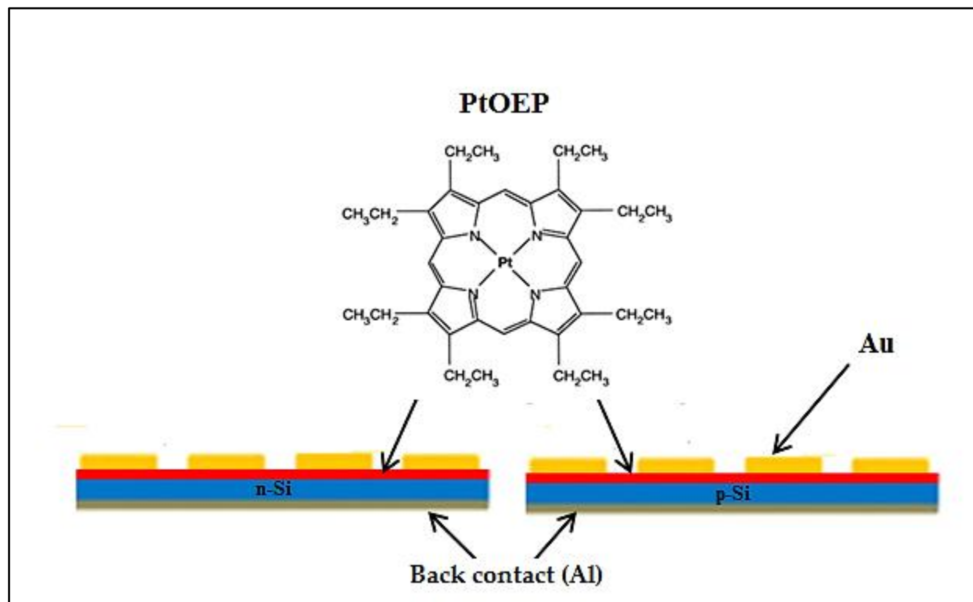

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1 **Fig.2**

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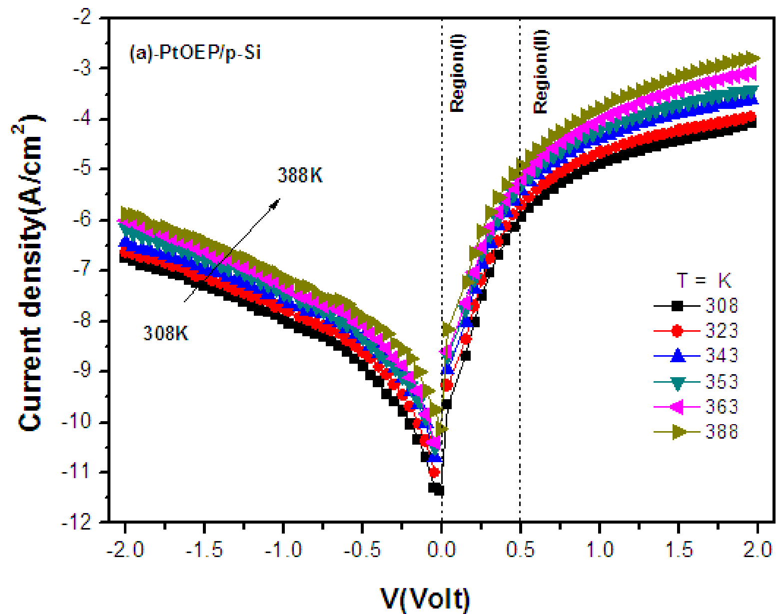

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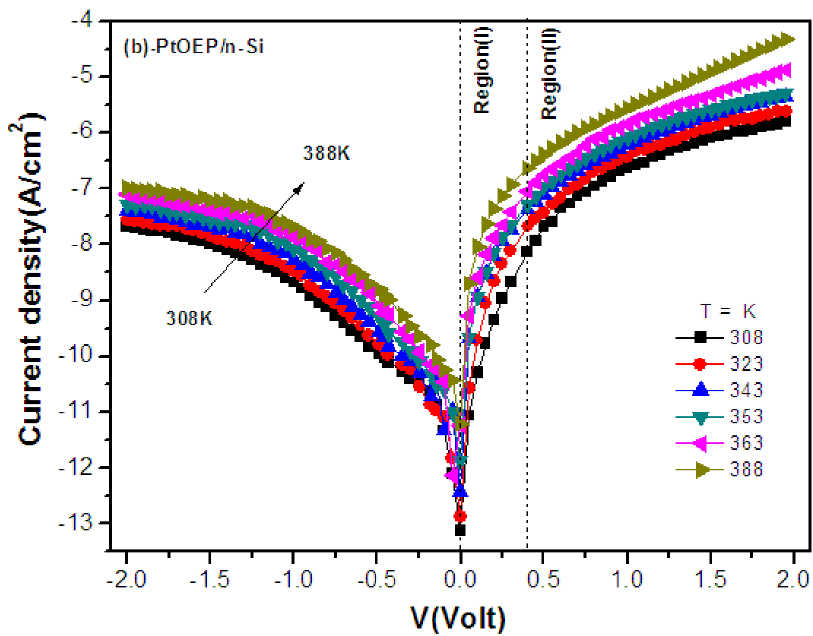

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1 **Fig. 3.**

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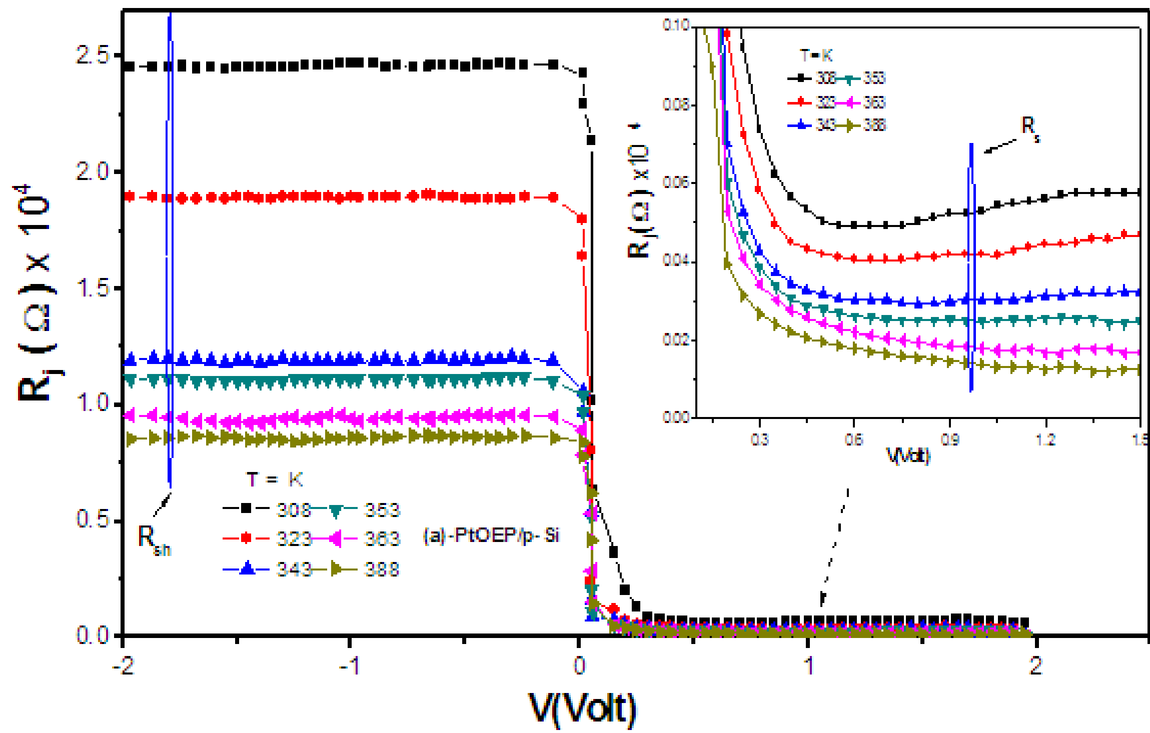

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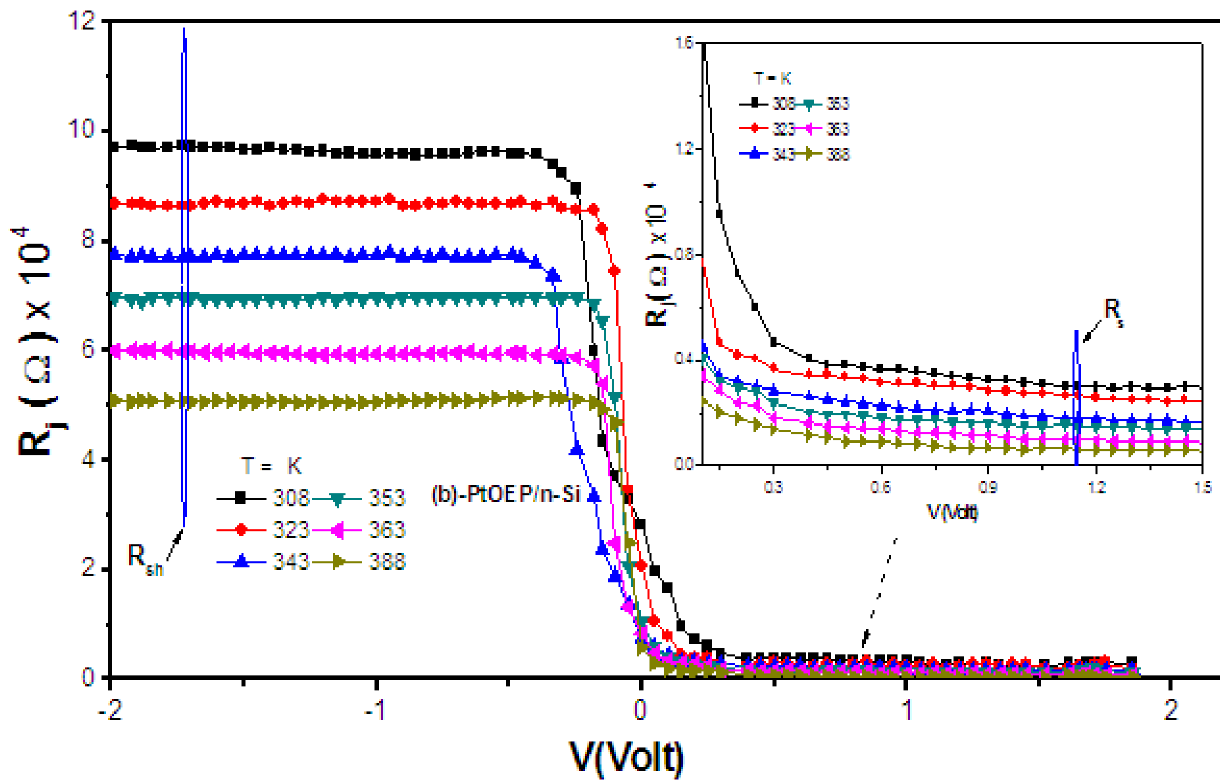

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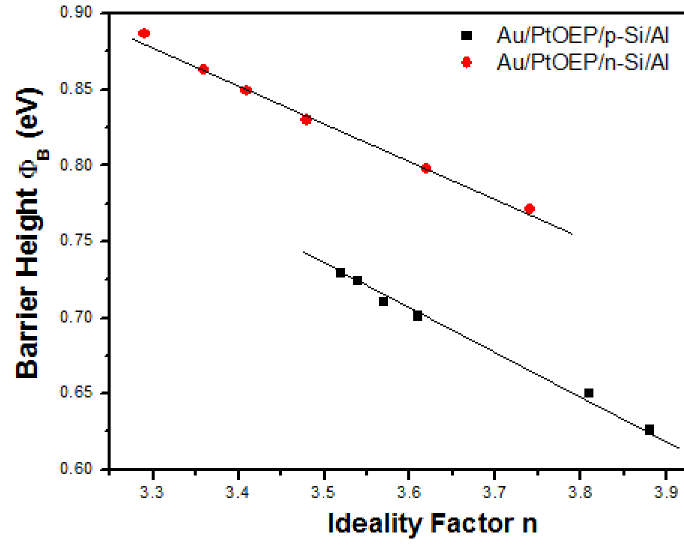
1 **Fig.4**



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1 **Fig. 5.**

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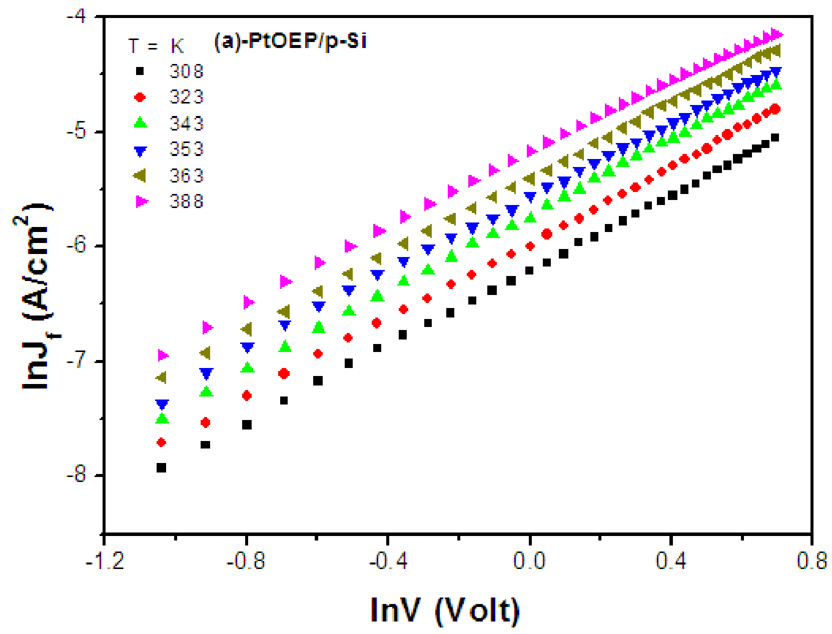

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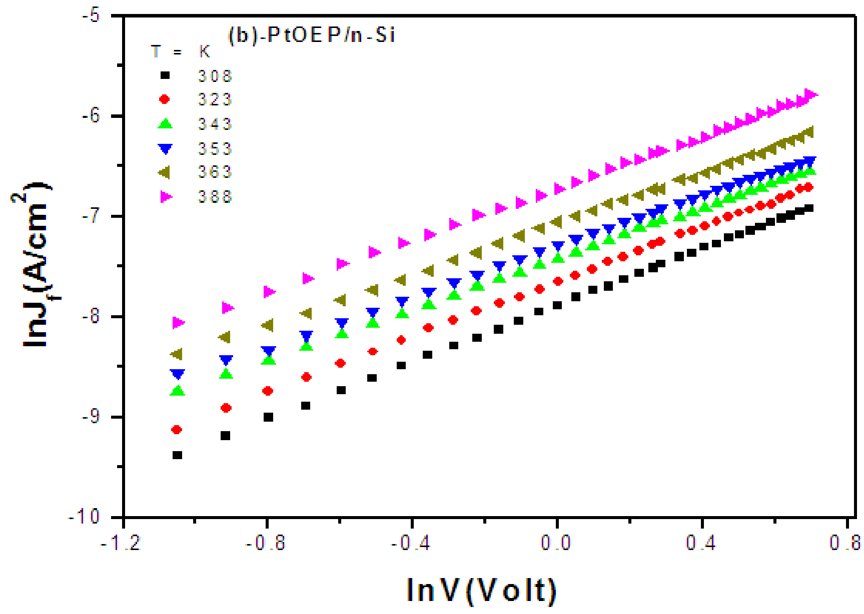

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1 **Fig. 6.**

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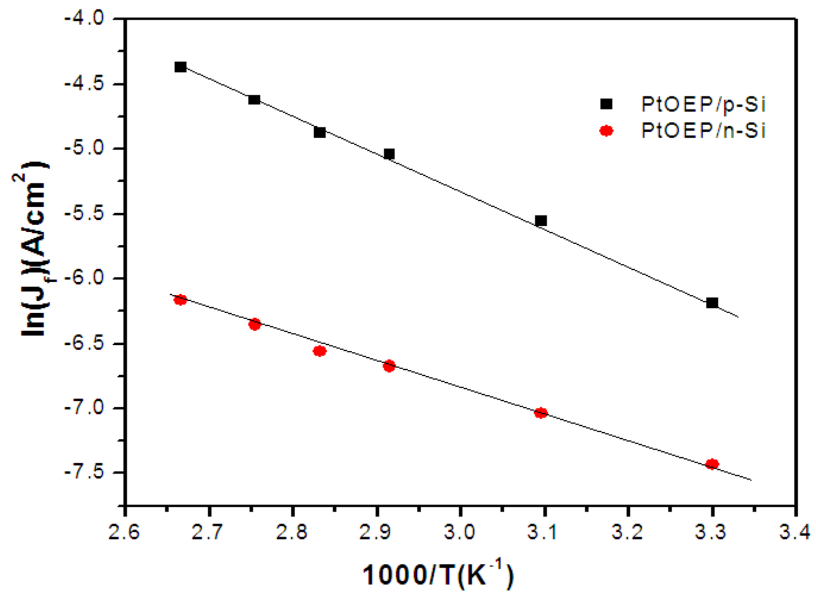

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1 **Fig. 7.**

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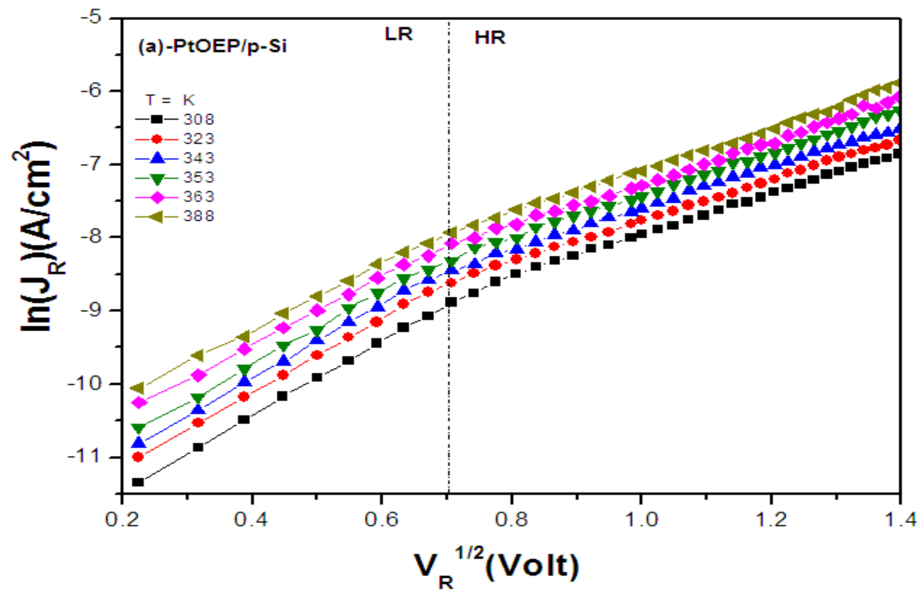

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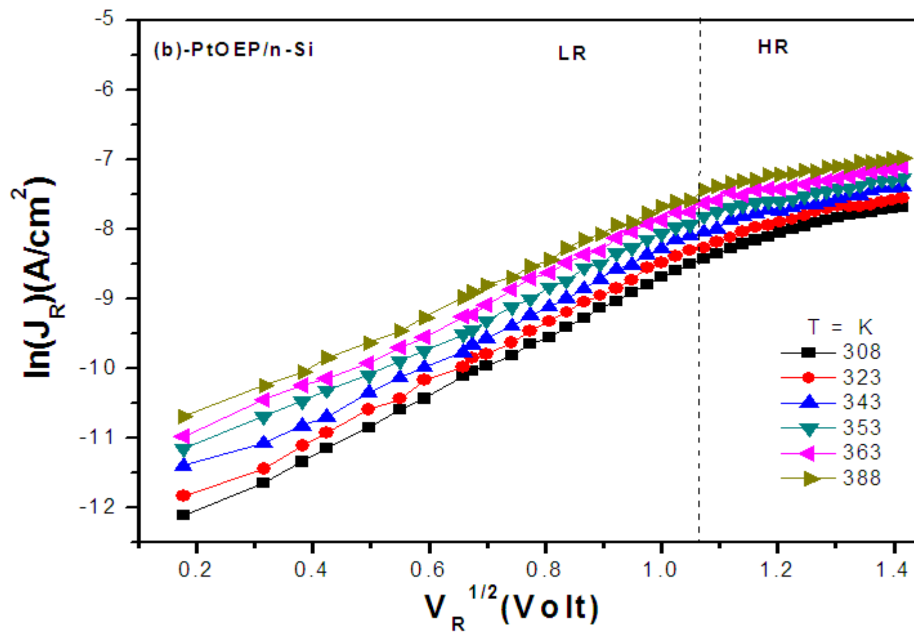

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1 **Fig. 8.**

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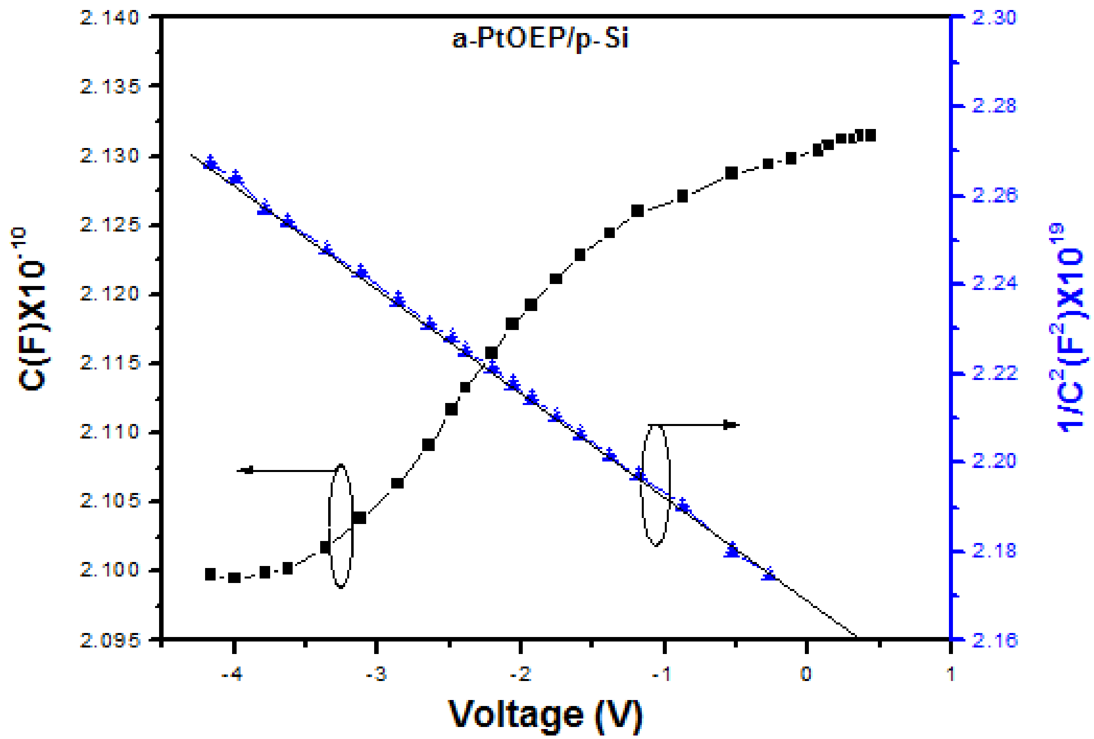

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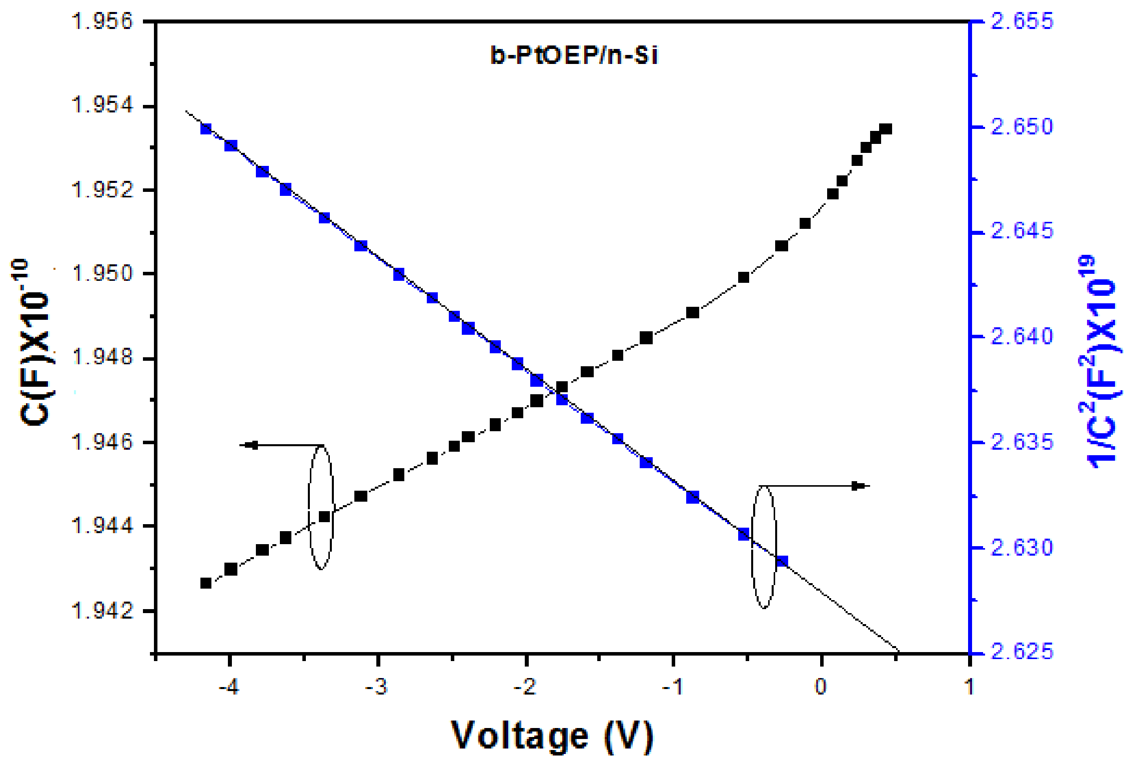

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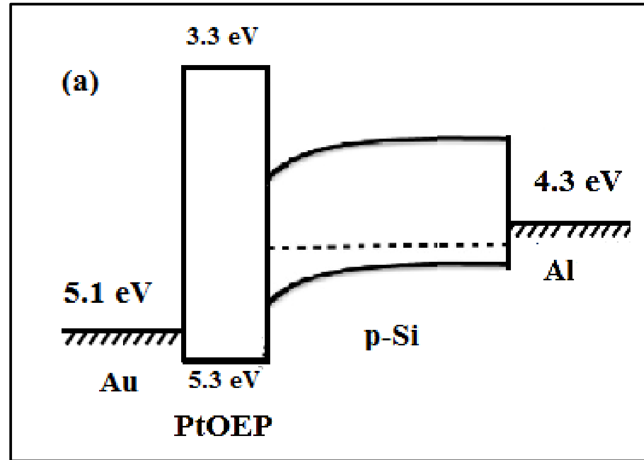
1 **Fig. 9.**



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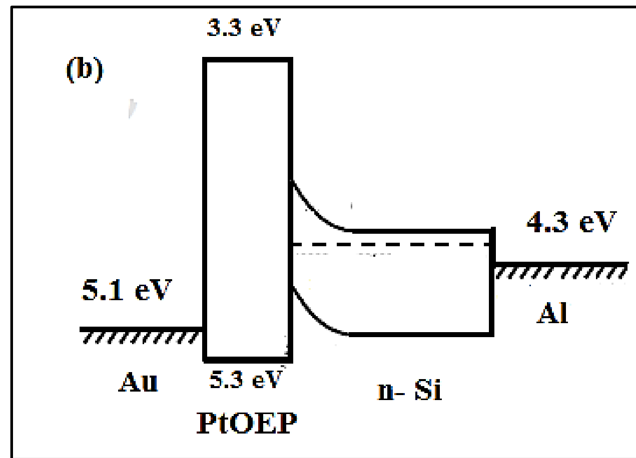

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14 **Fig. 10.**

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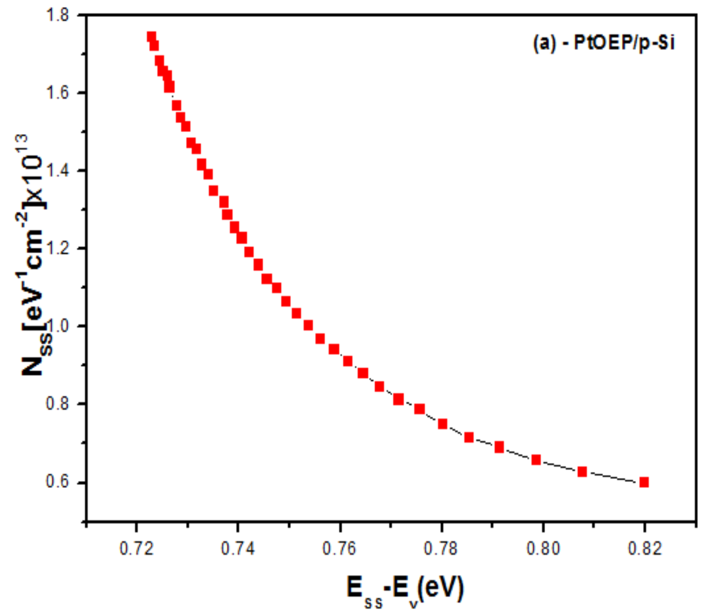

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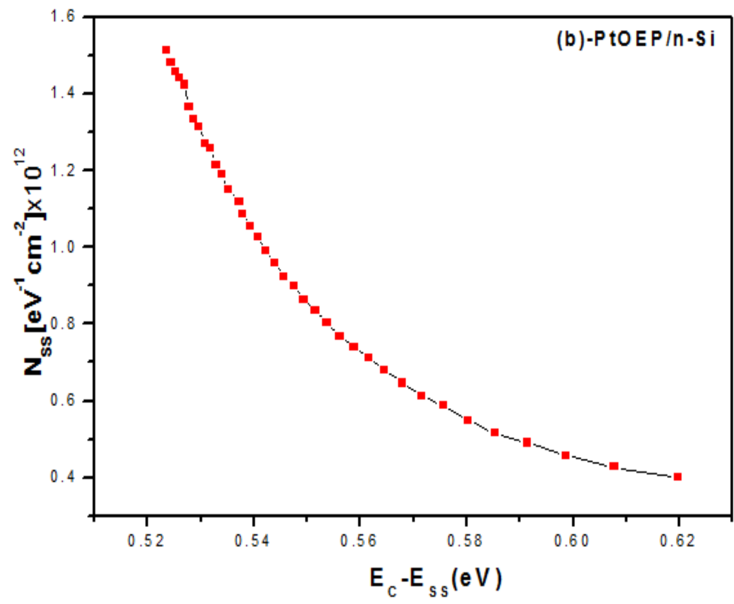

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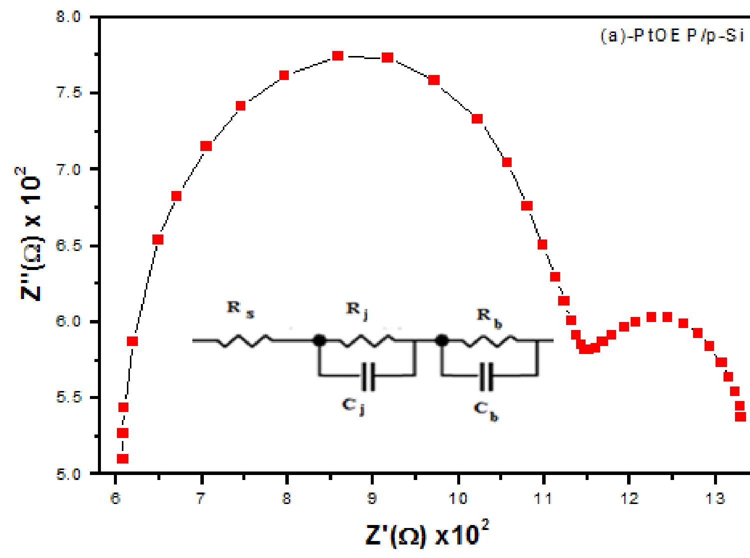
10 **Fig. 11.**



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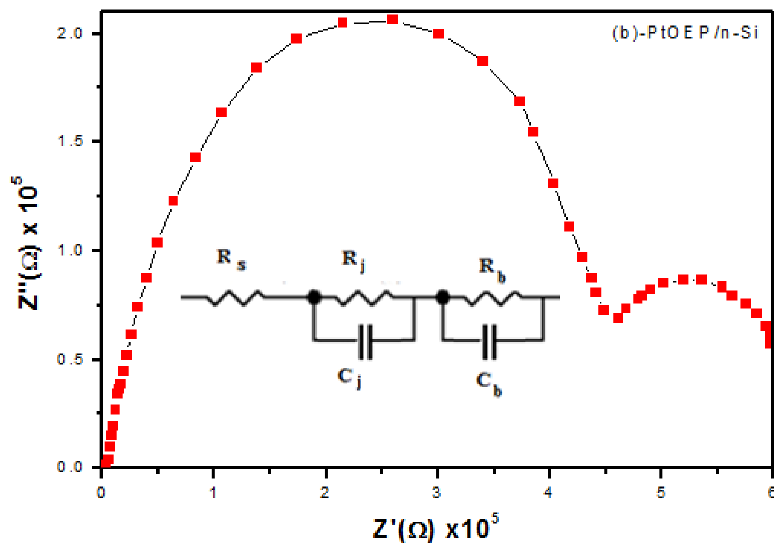

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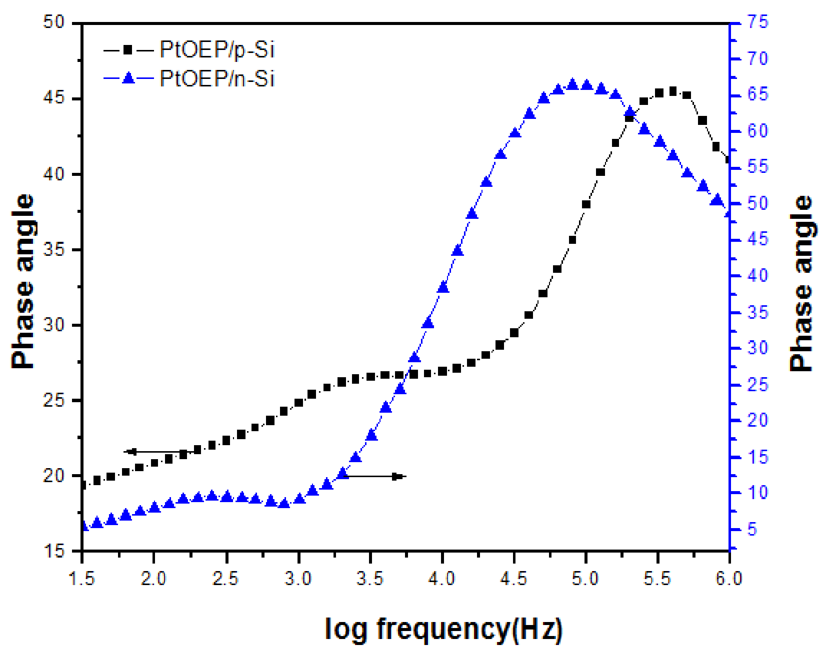
11 **Fig. 12.**



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1 **Table 1.**

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T(K)	PtOEP/p-Si				PtOEP/n-Si			
	R_{sh} (Ω)	R_s (Ω)	n	Φ_B(eV)	R_{sh} (Ω)	R_s (Ω)	n	Φ_B(eV)
308	24604	566	3.88	0.626	96009	2957	3.74	0.771
323	18919	411	3.81	0.650	87083	2519	3.62	0.798
343	11942	308	3.61	0.701	77343	1623	3.48	0.830
353	11136	247	3.57	0.710	96551	1393	3.41	0.849
363	9524	206	3.54	0.724	60061	676	3.36	0.863
388	8603	123	3.52	0.729	50920	315	3.29	0.887

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5 **Table 2.**

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Diode	V_{bi} (V)	N (cm^3)	C_o (F)	W_D (cm)	E_{max} (V/cm)	Φ_B [C-V] (eV)
PtOEP/p-Si	0.37	3.96×10^{17}	2.14×10^{-10}	$1.4x10^{-6}$	4.28×10^{5}	0.529
PtOEP/n-Si	0.55	1.75×10^{16}	1.65×10^{-10}	$8.9 x10^{-6}$	1.12×10^{5}	0.645

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9 **Table 3.**

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Diode	R_s (Ω)	R_j (Ω)	C_j (nF)	R_b (Ω)	C_b (nF)	τ_j (sec.)	τ_b(sec.)
PtOEP/p-Si	607.2	545.52	72.9	177.32	359.2	3.98×10^{-7}	6.36×10^{-5}
PtOEP/n-Si	3032	4.58×10^{5}	4.34×10^{-3}	1.36×10^{5}	4.66	1.99×10^{-6}	6.34×10^{-4}

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