Study on low-dimensional nanomaterials for next-generation electronic devices

次世代電子デバイスに向けた低次元ナノ材料に関する研究

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Contents

Chapter 1 – Introduction

1.1 Research backgrounds of low dimensional nanomaterial

One-dimensional (1D) or two-dimensional (2D) materials are expected as future electronic devices. Various 1D semiconductor materials such as Si, Ge, GaN, ZnO, Fe, and Ag are synthesized and studied for unique properties and potential applications. The structure and morphology of copper oxide nanowires and cupric oxide thin films are being studied. Electronic devices containing various rare metals produced so far are very expensive for commercial use. With regard to current rare materials, we will focus on copper oxide nanowires, a 1D case currently being studied, very stable, inexpensive, non-toxic material that can be obtained from readily available precursors. It is also one of the potential choices for an inexpensive device.

CuO nanowires are synthesized by heating Cu foil at ambient conditions. Copper foil samples are oxidized in air at 400-700 °C. The nanowire diameter can be controlled by changing the annealing temperature. Increasing the oxidation temperature can reduce the density, but the nanowires are straightened because the diameter and strength of the nanowires increase. Annealing temperature affects the aspect ratio, ie, the diameter and high density of the nanowires, while annealing time affects the length of the nanowires.

In addition, the isolation of van der Waals-coupled 2D crystals, which is expected as a future electronic device, has led to significant advances in materials research for applications in

electronics, photonics, and energy devices. Recently starting with graphene, several 2D crystals such as transition metal dichalcogenide (TMD) and transition metal oxide (TMO) have been studied, graphene is considered a substitute for silicon because of its high carrier mobility. Emitters, sensors, transparent electrodes, lithium-ion battery storage, etc. have already been reported

There are various publications on the synthesis of graphene due to its excellent properties. Graphene was the dream material of silicon after the death of electronic applications, however it is important how long it takes to get to the market. In order to avoid the CVD transfer process, it is necessary to directly grow graphene on an insulating substrate, and low temperature growth is highly desirable for substrates with low heat resistance. For this purpose, CVD is a better method, however there are few report of low-temperature growth, attempts to grow below 300 °C using a solid-liquid-solid reaction has been done.

1.2 Introduction of 1D CuO nanowire

1.2.1 Introduction of 1D materials and basic properties of copper oxide

One-dimensional (1D) nanostructures, such as nanowires, nanobelts, nanorods, and nanotubes, have become one of the focus of intensive research due to their unique physical properties and potential applications [1]. Nanowires of semiconductor materials, including Si, Ge, GaN, ZnO, Fe, Ag, and so on have been synthesized for future applications. Various growth methods are adopted, such as vapor-liquid-solid growth (VLS) [2], epitaxial growth [3], vapor-solid (VS)

growth [4], wet chemical growth [5], or electrospinning [6]. In the case of VS growth, it has been known since the middle of the 20th century that the oxidation of metal elements such as Cu, Zn, and Fe forms a high density oxide wire on the surface [7]. CuO nanowires, (nanorods, nanowhiskers, nanosheets) can be synthesized by CuC_2O_4 precursor thermal decomposition [8], hydrothermal decomposition [9], autocatalytic growth [10]).

Furthermore, there is increasing interest in developing CuO 1D nanostructures for device such as critical temperature superconductors [11], sensors [12, 13], memories [14], catalytic nanodevices [15-17] or emitters [18].

Cupric oxide (CuO) and cuprous oxide (Cu_2O) are stable and Cu_2O is also insoluble in organic solvents. Cu_2O is contained underground as some red rock mineral copper ore. When exposed to oxygen, copper spontaneously oxidizes to Cu_2O, which takes a long time. Artificial formation occurs at high temperature or high oxygen pressure, and when heated further, Cu_2O becomes CuO. It is the black solid with the ionic lattice that melts over 1200 °C and is generated by the loss of oxygen. When copper is heated in air, it forms with Cu2O. Therefore, it can be prepared more appropriately by heating copper nitrate (II), copper hydroxide (II), etc. ($2Cu(NO_3)_2 \rightarrow 2CuO + 4NO_2 + O_2$, $Cu(OH)_2 \rightarrow CuO + H_2O$ or $CuCO_3 \rightarrow CuO + CO_2$). Since CuO is a basic oxide, it dissolves in hydrochloric acid, sulfuric acid, and nitric acid, etc. to produce copper (II) salt. ($CuO + 2HNO_3 \rightarrow Cu(NO_3)_2 + H_2O$, $CuO + 2HCl \rightarrow CuCl_2 + H_2O$ or $CuO + H_2SO_4 \rightarrow CuSO_4 + H_2O$).

Cu_2O is known to be a p-type semiconductor [19], and deviations from stoichiometry are due to the analysis of quenched samples [20], thermogravimetric analysis [21-23] and high temperature solid-state coulometric titration [24]. These were related to temperature and oxygen partial pressure. Several models have been suggested for the defect of Cu_2O. These contain neutral atoms, first-ionized copper vacancies, first-ionized oxygen interstitials, and double-ionized oxygen interstitials [20-23, 25, 26].

The temperature and oxygen partial pressure dependence during cation-tracer diffusion of Cu_2O were measured [31]. The results suggest that both neutral and monovalent copper vacancies mainly contribute to cation self-diffusion. The electrical conductivity of Cu_2O is dependent on temperature and oxygen partial pressure [25, 27-33]. The conductivity of oxygen partial pressure up to 10^{-6} atm was measured in the temperature range of 700-1100 °C in the Cu_2O phase [32]. It was suggested that the valence defect pair may become important with increasing oxygen partial pressure to explain the observed oxygen partial pressure dependence.

1.2.2 Oxidation of copper

The multiphase structure of Cu_2O and CuO forms on Cu oxidized in oxygen or air at high temperatures due to the thermodynamic stability of the oxide [21, 35, 36]. The parabolic rate constant for the oxidation depends on 1/4 of the oxygen partial pressure when only Cu_2O is formed. Bulk transport of copper in the reaction mainly involves neutral copper vacancies

[37-40]. This means that the effective charge of most of the copper vacancies in the outer layer is zero.

Onay and Rapp performed oxidation of copper at 10^{-4} atm, 300 °C [30]. Their results were that a multi-layer scale is formed by dissociation of the Cu_2O scale. Thickness loses contact with the copper substrate, and formed to micro channels and rich CuO in Cu_2O scales.

Kaufman and Hawkins performed photoluminescence measurements on thin films of Cu_2O on copper [41]. They suggest that the rate of copper oxidation is limited by the diffusion of copper vacancies.

The formation of one-dimensional metal oxide nanowires has been intensively studied due to their interest in characteristic structures and technical applications [42]. Considerable attention has been given to the formation of metals by thermal oxidation, primarily in an oxygen atmosphere [43–51], leading to various theories about the mechanism of formation of native oxide nanowires. Some are based on evaporation and condensation process, which are the vapor-solid model [55, 56], or a diffusion short circuit of the nanowire [57–61]. Other studies suggest that the nanowire growth occurs as the accumulation and mitigation of compressive stress at the oxidation [62-64]. Alternatively, it is also suggested that CuO could be presence in three magnetic phases with anisotropy [53].

In the past, various nanowires materials have been studied. As an example, the transport properties of a unite SnO_2 nanowire show a strong correlation of temperature-dependent

conductivity compared to a bulk or thin film of SnO_2 [54]. For SnO_2 nanofibers used as anode material for Li-ion batteries, longer cycle life and higher rate performance have been reported comparing to bulk [55]. Although the phenomenon of oxide nanowire formation is not linked to typical metals, copper oxidation is still the most representative [60, 62–68]. It has been proposed that the driving force for the formation of CuO nanowires is related to the compressive stress resulting from large differences in the molar volumes of metals and oxides [60, 69, 70]. Also since both CuO and Cu_2O are anion-deficient p-type oxides, oxides have been shown to grow by diffusion of cations during Cu oxidation [71]. Several experiments suggested that CuO nanowires grew from the tip during oxidation of the Cu substrate and were not pushed out of the base layer [60]. On the other hand, it was suggested that oxide nanowires grow primarily by surface diffusion from the base to the tip of the nanowire along the tunnel to the center of the screw dislocation [57–63]. However, such proposals contradict many experimental observations that reveal that oxide nanowires have a bicrystalline or single-crystal structure [51, 63, 66, 68]. Therefore, as a model system to understand the nanowire growth mechanisms, it is important to identify the mass transport mechanisms that govern the growth of one-dimensional nanowires. This p-type semiconductor material has many interesting properties that lead to countless technical applications including energy conversion, solar energy conversion, photocatalysts, fuel cells, emitter, lithium ion batteries cathode material, gas sensing, and catalysis for hydrocarbons conversion.

1.2.3 CuO nanowires synthesis methods

In the past few years, 1D CuO nanowires have been synthesized by various methods, including sonochemical methods [72]. To promote CuO crystallization with polyvinyl alcohol, it is performed as follows. Add the initial polymer CuO nanoparticles to the hexamethylenetetramine (HMT) high temperature solution and HMT turns into ammonia and formaldehyde. At this time, copper oxide is set in polyvinyl alcohol.

On the other hand, Xu obtained CuO in the form of nanorods by thermal decomposition of CuC_2O_4 [73]. $C_2O_4^{2+} + Cu_2+ \rightarrow CuC_2O_4$, $CuC_2O_4 \rightarrow CuO + CO_2$. After mixing and pulverizing CuC2O4 and NaCl powder, it is annealed on the porcelain in the alumina tube. This is the chemical method to obtain powdered CuO nanorods.

Wang produced a CuO nanowire by the method of the solid-state reaction of a surfactant [74]. $CuCl \cdot 2H_2O(s)+2NaOH(s) \rightarrow CuO(s)+2NaCl+3H_2O$. After mixing and grinding $CuCl_2$ and solid NaOH, the surfactant is added. Next dry the product in the oven, at this time, CuO nanowires are set in a nonionic surfactant.

This method also can be adopted to obtain other nanowires such as CuS, ZnS, NiS, FeS, and so on. However, manufacturing methods based on precursor templates require complex procedures and knowledge to synthesize nanorods with selectable diameters. In addition, the length of the nanorods is less than 1 micron, which is unlikely to be a way to control the aspect ratio.

From the perspective of nanostructure manufacturing, it must be suitable for mass production and controlling the aspect ratio of nanowires. Compared to complicated chemical methods, thermal annealing is a useful and rapid way to synthesize nanowires of CuO.

1.3 Introduction to 2D graphene

1.3.1 Introduction to graphene and synthesis methods

As shown in Fig. 1.1, graphene is a thin layer of carbon sp^2 hybrid orbitals arranged in a honeycomb structure. On the other hand, natural graphite is an arrangement in which its layers are joined together by van der Waals forces [75]. As for the study of graphene and 2D materials, surprising physical and electrical properties of single-layer graphene have been reported since single-layer graphene on SiO2 [76-78]. Mobility is up to 200k cm^2 / Vs, thermal conductivity is up to 5000 W / mK, high Young's modulus is 2.0 TPa. [79, 80].

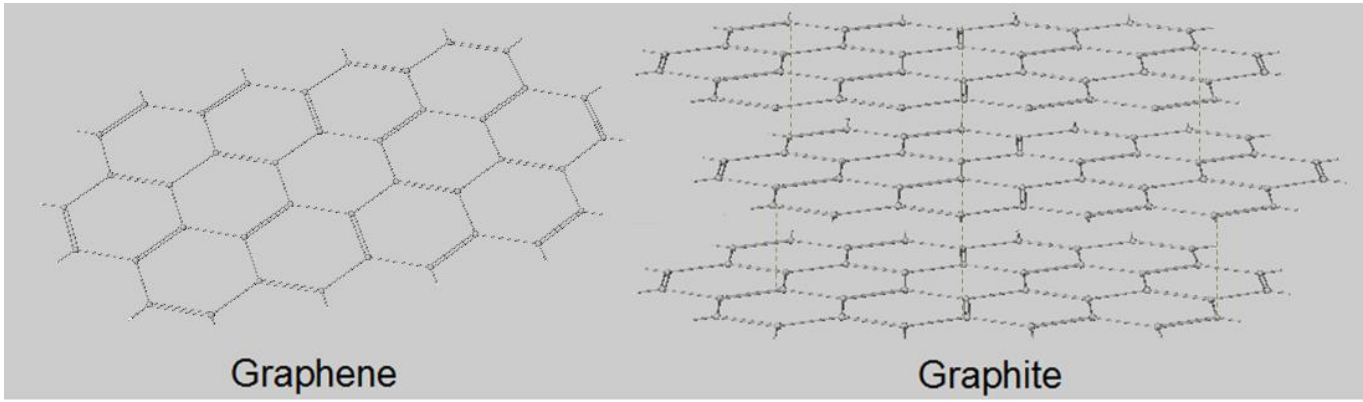

Fig. 1.1. Atomic configuration of graphite and graphene

Fig. 1.2 shows a synthesis method hierarchical diagram. While graphene can be easily extracted from graphite using scratch tape [81], industrial synthesis has been achieved in several ways. Top-down method, a physical or scientific exfoliation of graphite [83, 84]. And the reduction of graphene oxide is for mass production, however the obtained graphene has reduced electrical properties compared to the original [82].

Bottom-up method, epitaxial growth on silicon carbide (SiC) surface. Although it is high cost, it is the most admired method for producing large area graphene for electronic applications [85].

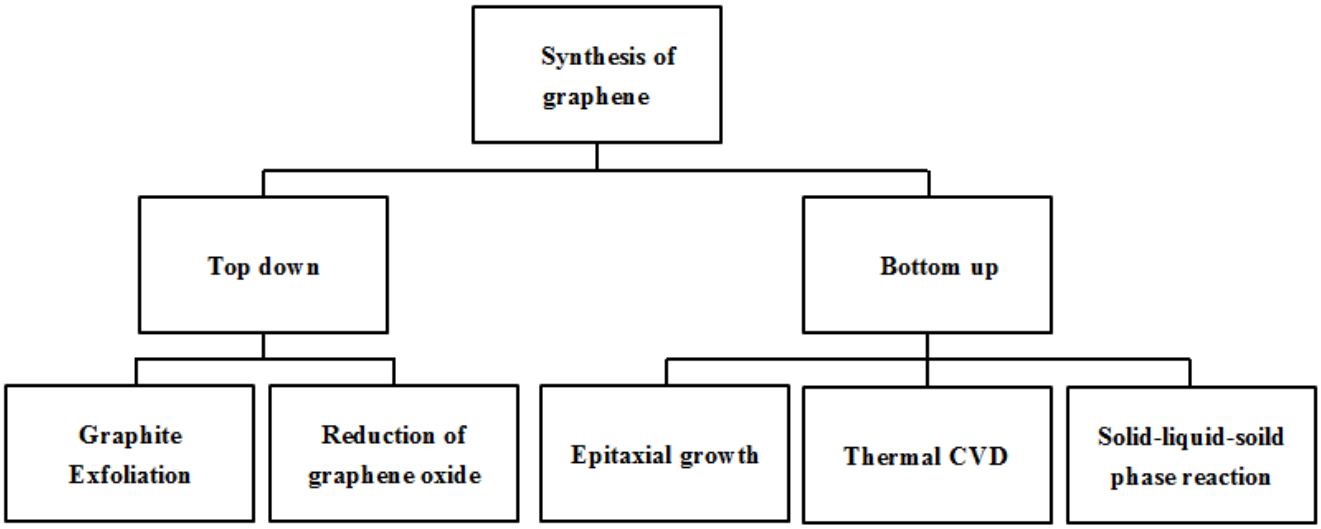

Fig. 1.2. Graphene synthesis methods

Thermal CVD is the cheapest way to easily product graphene that is the desired layers, large areas, and good quality on a variety of substrates. There are various types of CVD, such as, low, high, atmospheric pressure CVD and plasma. There are other alternatives, such as arcing, solid-liquid solid-state reactions, and thawing of carbon nanotubes (CNTs) [86-89].

The formation mechanism of graphene by the CVD method is considered to be the most prominent at present.

First, carbon gas, which is a raw material for graphene, flows into the sample chamber, and the carbon gas is decomposed by heat or plasma. The decomposed carbon dissolves in the

metal substrate, and then becomes supersaturated in the process of cooling the substrate, and graphene is synthesized on the substrate in the process of precipitating the carbon dissolved in the catalyst on the surface. Therefore, the number of graphene layers generated varies depending on the cooling rate of the substrate. This generation model is thought to occur in metallic materials with high carbon solubility such as nickel.

The next most prominent generation mechanism is the surface diffusion model. This is because carbon adsorbed on the metal surface is combined with other carbon in the process of running on the substrate, and graphene is generated. This is mainly caused by metal materials with low carbon solubility such as copper.

1.3.2 Microwave plasma chemical vapor deposition (Microwace Plasma CVD)

Microwave Plasma Chemical Vapor Deposition (Microwace Plasma CVD Method, MPCVD) method is of activating a raw material gas using a microwave to promote a chemical reaction. When a molecule is bombarded by high energy electrons, the electrons in the molecule transition to a higher energy level. In this inelastic collision, the molecules are in the same state as if they were thermally heated at a high temperature, and promote the chemical reaction. Therefore, even if the reaction is thermodynamically impossible at a low temperature, the reaction is possible and the speed is increased in the plasma.

In practice, a catalyst is deposited on a catalytic metal plate or substrate to grow graphene on the substrate.

The MPCVD method uses the kinetic energy of electrons because the kinetic energy given to the ions in the plasma is smaller than that of the high-frequency plasma, so that the ions hardly vibrate and only the electrons vibrate. A device with a frequency band of 2.45 GHz is installed inside the waveguide as a microwave transmitter, and film formation is performed under vacuum. Parameters such as microwave, substrate temperature, source gas, vacuum system, and plasma distance are closely linked, so these are separately controlled for film formation.

1.3.3 Applications of graphene

Due to the extraordinary properties, graphene can be applied to a variety of potential applications. Graphene-based emitters, sensors, transparent conductive film, and lithium ion battery storage have already been produced [90-96]. Graphene was considered a substitute for silicon materials because of its high carrier mobility [97]. It can also help to significantly increase data capacity to meet future demand growth [98-101]. Another application is solar cells, and carbon solar cells can reduce costs, but need to improve the efficiency of solar cells. Carbon solar cells are made possible by doping nitrogen or boron to change n-type or p-type, respectively [102-104].

Graphene is considered a substitute for silicon material, but does not have the band gap required for electronic devices. According to the International Technology Roadmap for Semiconductors (ITRS) [105], silicon technology may be replaced after 2020. Numerous methods have been reported for introducing band gaps into graphene, including quantum

confinement and chemical modification [106-111], however fail to open band gaps above 0.36 eV [113]. In addition, opening the bandgap causes carrier mobility degradation, which is undesirable for electronic applications [114]. On the other hand, the conversion by doping enabled the band gap opening without deteriorating the characteristics [115]. In theoretical studies, arsenic and tin doping may lead to band gaps of up to 0.6 eV, the largest in current work [116].

1.4 Purpose and structure of the thesis

The growth mechanism by which such one-dimensional and two-dimensional materials are formed is not fully understood, and there are many unclear points. In addition, there has been little research on the large area required in the future. and it is linked to area increase by using these growth mechanisms. These applications require large areas and large amounts of active device materials to enable production and utilization on a realistic scale. Therefore, focusing on copper oxide nanowire and graphene which is expected to be a transparent conductive film, we elucidated the growth mechanism, increased the area, and performed direct synthesis at low temperatures. This paper describes copper oxide nanowires grown by thermal oxidation of copper foil or transparent conductive film FTO, and graphene grown directly on an insulating substrate by plasma CVD.

Chapter 1 introduces nanowires and graphene and describes general synthesis methods. It also describes copper oxide films, cupric oxide nanowires and their synthesis methods, graphene characteristics, plasma CVD synthesis methods, and supplementary prospective dopes.

Chapter 2 describes the surface diffusion growth process of copper ions in the copper oxide nanowire growth process. Experimentally explain that copper particles begin to collect on the wire when the air flow rate is reduced in a sealed space in copper oxide nanowire synthesis. Transmission, electron microscopy (TEM) and scanning electron microscopy (SEM) were used to analyze morphology, composition, and structure. Structural analysis was performed using energy dispersive X-ray spectroscopy (EDX).

Chapter 3 explains the mass production method of CuO nanowires on flat substrates from the viewpoint of tensile and compressive stress and growth of CuO nanowires. As the industrial process of copper, if the copper substrate is flat, the stress distribution will cause damage to the copper substrate, rather than producing nanowires. In the proposed study, however, this was made possible by changing the structure of the substrate at the bottom of the CuO nanowire. The nanowire substrate on the FTO is not a flat surface but a plurality of hemispherical protrusions

Chapter 4 describes the direct graphene growth on the insulating substrate using microwave plasma CVD Graphene obtained by using CO_2 and ozone treatment has high transmittance, low

sheet resistance and increased sheet carrier mobility at low temperatures. The growth of graphene achieved at low temperatures also expands the range of direct growth on insulating substrates or semiconductors at lower temperatures

Chapter 5 provides overall conclusions and recommendations for future work in this research area.

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Chapter 2 - Direct evidence to suggest activity of copper ions surface diffusion on nanowire in growth process

2.1. Introduction

Copper oxide (CuO) has been extensively studied because of its close connection to high-Tc superconductors [1, 2].

This material is useful for active layer of solar cell and shows a number of interesting properties such as low cost, good mobility, abundance, and the semiconductor layer formation process is simple [3, 4]. Although it is one of the oldest semiconductor materials known to solid state physicists, not much technological improvement has been achieved.

Cupric oxide is a semiconductor having the band gap of about 1.21 eV so it can absorb the visible light to make electricity, the theoretical limit of the energy conversion efficiency of a cupric oxide solar cell is hidden about 20% [3-5].

Nanostructured materials have attracted much scientific attention due to their interesting size-dependent chemical and physical properties and potential technological applications. One-dimensional (1D) structures such as nanorods and nanowires have become important building blocks of nanodevices and integrated nanosystems [6, 7].

Nanowires are 1D nanocrystal with large aspect ratio (height / diameter) and diameter up to about 200 nm. Indeed, oxide whiskers growing on the surface of copper during oxidation were observed nearly half a century ago [8]. Whiskers are characterized to have a short length (<

5μm), a large diameter (> 100 nm) and very low density. Based on the reports above, nanowires can also be named as nanowhiskers.

Various growth techniques have been employed, including the vapor-liquid-solid growth [9], epitaxial growth [10], vapor-solid growth [11], wet chemical methods [12], and electrospinning [13].

In comparison to complex these chemical methods, thermal annealing of copper foil provides simple, convenient, and fast method for synthesizing CuO nanowires. Thermal oxidation is becoming an increasingly attractive method for the synthesis of nanostructures.

A variety of views in the copper oxide nanowires growth mechanism has been speculated [14-18]. However, on one of the leading paper of the mechanism of the wire occurrence, there is suggestion of the grain boundary diffusion and surface diffusion of copper ions [19, 20].

When the Cu substrate was heated in the air, two thermodynamically stable oxide layers, namely Cu_2O layer and the topmost CuO layer were formed. In the order of differences of these molar volumes, stresses were generated by the substrate inside, therefore these caused grain boundaries of Cu_2O and CuO layers, through those gaps Cu ions began to pass.

In the growth process of the wire, Cu ions diffused the grain boundaries from the Cu base and reached to the CuO top surface. Then copper ions cause the wire source, diffusing surface in the planar direction on top CuO. Ultimately copper ions started to form a wire tip, diffusing surface in a vertical direction on CuO wire while assembling to the tip.

However most of the experimental observations about CuO nanowires growth mechanisms have not been carried out, as the author stated [20].

In this present report, under the general condition that copper oxide nanowires occur [11, 21-24], we describe peculiarities of the structure and the growth process of nanowires obtained by only lowering the air flow rate.

2.2. Experimental procedure

For synthesis of CuO nanowires, the copper sheets were used as a substrate. The industrial grade copper sheets (Nilaco Corp. 0.1 mm thickness and 99.999% purity) are cut into standard sizes of 1cm×1cm. The substrates were cleaned with acetone and methanol and deionized water under an ultrasonic bath for 5 min, and dried by N_2 flow.

The cleaned Cu substrate was positioned in the middle of a quartz tube that is mounted a horizontal tube furnace. This tube furnace was completely enclosed, moreover one end of the quartz tube was attached to the pure air cylinder (Taiyo Nippon Sanso) and other to the gas bubble.

The tube furnace was heated to the set-point temperature and flow rate was adjusted at 0.5 L/min and less range (HORIBA, PE-D20) from the air cylinder.

The morphology of the CuO nanowires were characterized by scanning electron microscope (SEM, Hitachi S-3000H) operated at 15 kV. The wire part characterizations were per-formed

by field emission scanning electron microscopy (FE-SEM, JEOL JSM7001FF) equipped with EDS (THERMO SCIENTIFIC NSS). Transmission electron microscopy TEM (JEOL JEM-4000 EXII) observation and electron diffraction investigation were carried out.

2.3. Results and discussions

In atmospheric pressure it is explained CuO nanowires are mainly successfully synthesized in the vicinity of 500 ℃ and the length is mainly affected by synthesis time [11,21-24]. Therefore the parameter temperature was set 500 ℃ as a general synthesis temperature and the synthesis time was fixed to 60 minutes for growing CuO nanowires. Then, as regards an electric furnace preparing from an air flow late 0.5 L/min [24], where the air flow rate was made drop down to set gradually, when nanowires differing from the straight line appeared, we stopped lowering to set. Under in the vicinity of approximately 0.01 L/min, a certain changed peculiarity of the wire has appeared in the low probability of 10-20%.

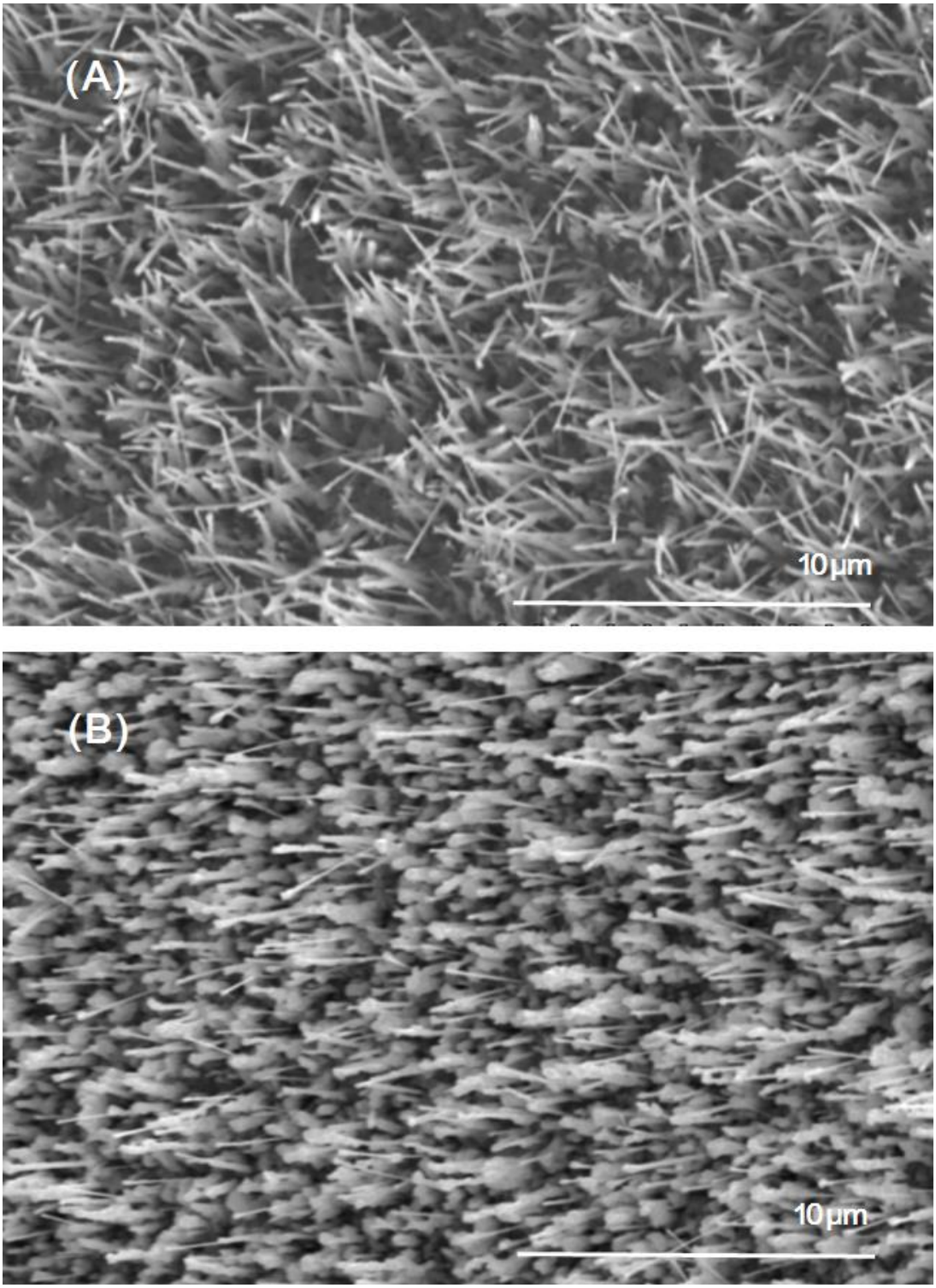

Fig. 2.1. SEM images of CuO nanowires attached grains at an annealing temperature of 500 ℃ for 60 min in an air flow (A) 0.010 and (B) 0.005 L/min.

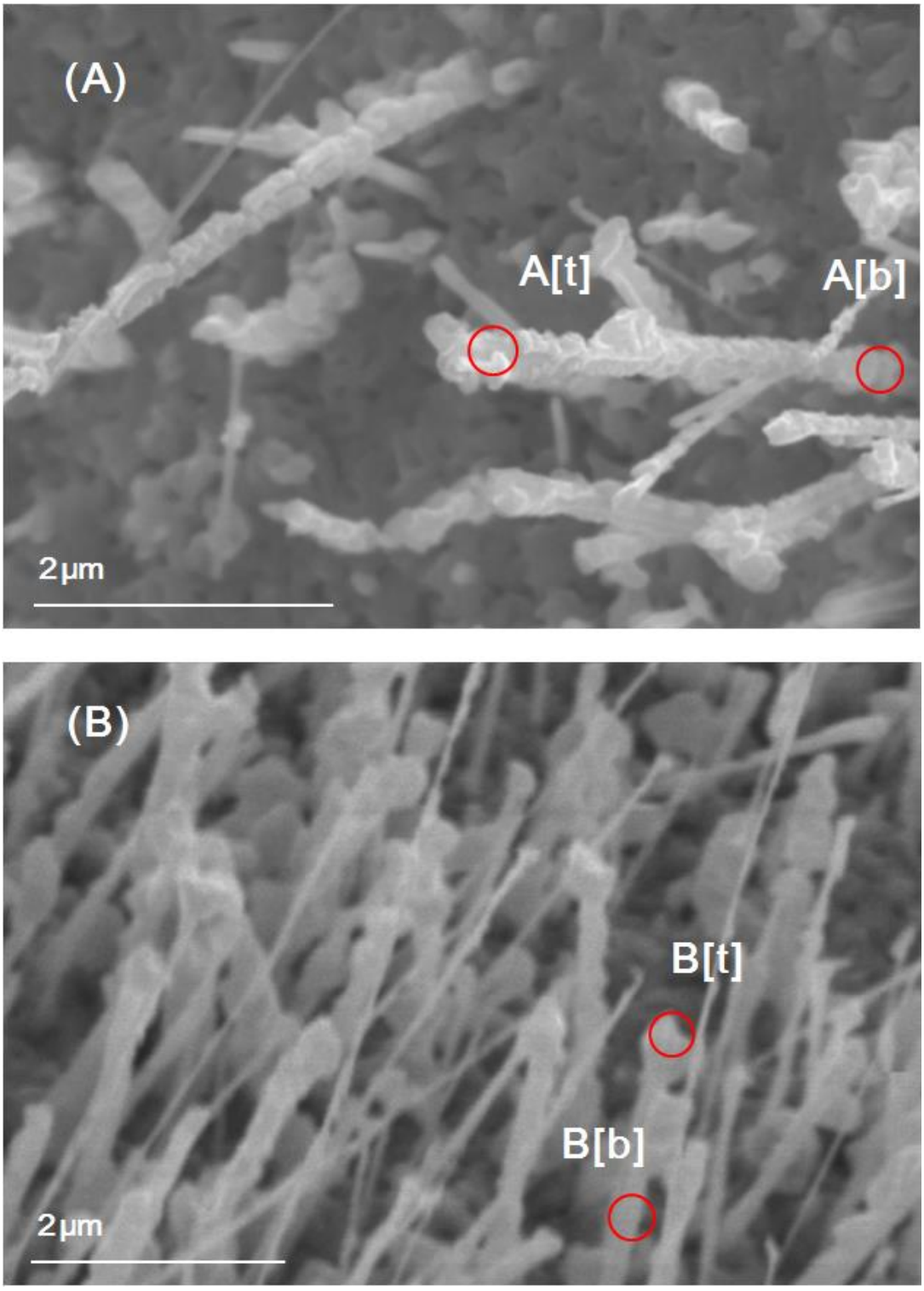

Fig. 2.2. Enlarged SEM images of other areas Fig. 2.1 (A) and (B) samples which are sparse parts of CuO nanowires attached grains to observe a unit nanowire. EDS points on circles.

In Fig. 2.1 SEM images (A) is an air flow rate 0.010 L/min, (B) is 0.005 L/min. The case air flow was suppressed, a result of the shape was obtained that the wire differed considerably. Unlike the normal liner nanowires, those of granular on the wire are visible. When lowered the air flow rate, (A) it began particles adhere around the wire. Moreover the air flow rate was depressed further, (B) particle assemblages on the wire expanded.

Fig. 2.2 (A) and (B) are magnified sparsity parts of Fig. 2.1 (A) and (B) for examining a unit nanowire, respectively.

In order to observe the particle adhered to the wire in Fig. 2.2 (A), nanowires (A) 0.010 L/min cut off to a piece applied ultrasonic vibration, it was investigated by TEM.

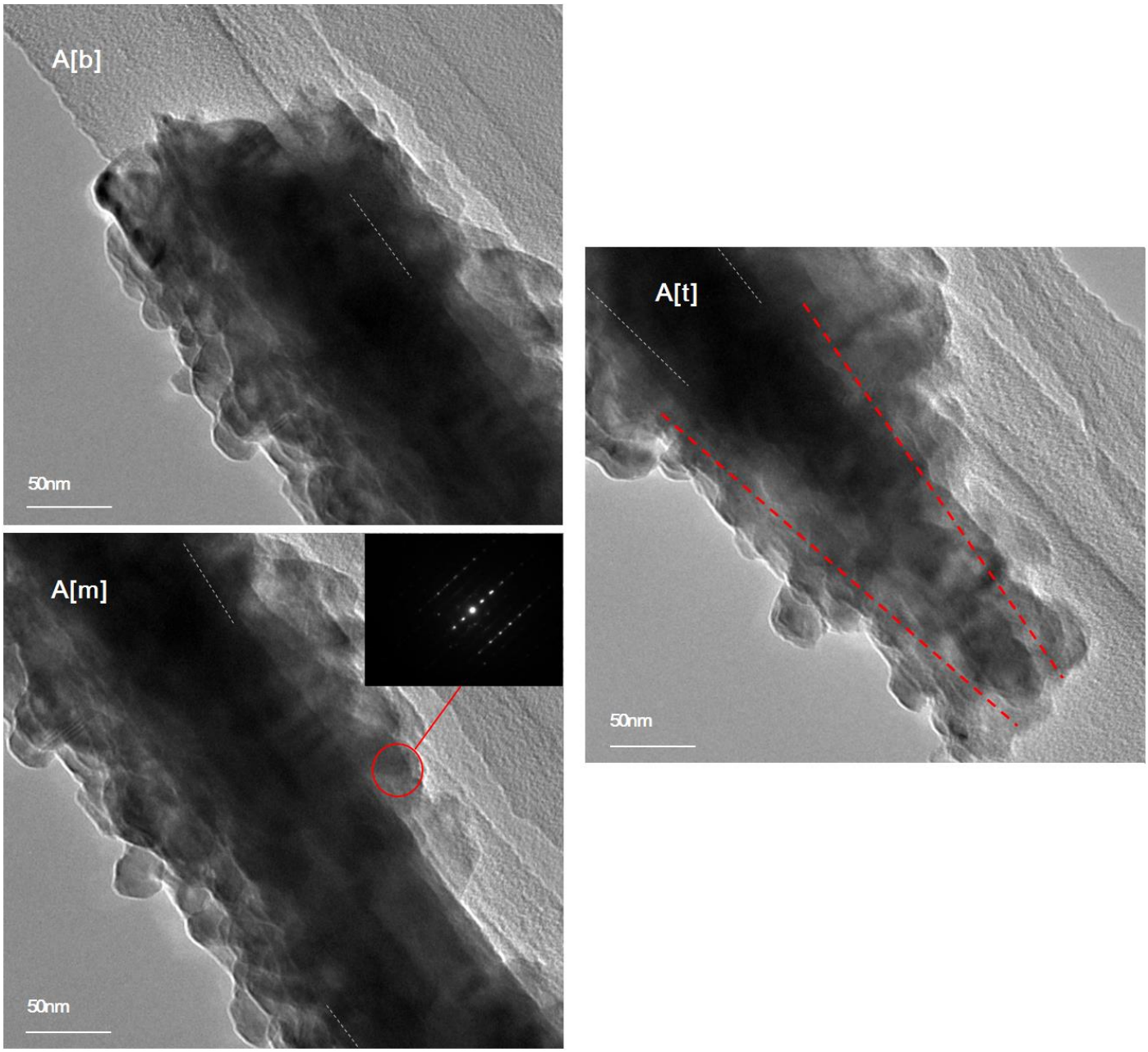

Fig. 2.3. TEM images of a CuO nanowire attached grains at 500 ℃ for 60 min in an air flow (A) 0.010 L/min. A[b] is the base side of a cut wire of the sample (A) 0.010 L/min. A[m] is its middle part. A[t] is its tip.

In Fig. 2.3, A[b] is the base side of a cut nanowire (A) 0.010 L/min, A[m] is its middle part, and A[t] is its tip. As far as observed in Fig. 2.3, particles were attached around the wire. Then,

in Fig. 2.3 A[b] and A[m] for the most part it was clearly observed that particles were attached after the wire had completely occurred. On the other hand, in Fig. 2.3 A[t] as red dotted lines the wire tip sidewall has been synthesized with the attached particles.

Electron diffraction was carried out for adhered particles by TEM. In the red circle in Fig. 2.3, the particle was a single crystal which arranged neatly also a wire similarly [23].

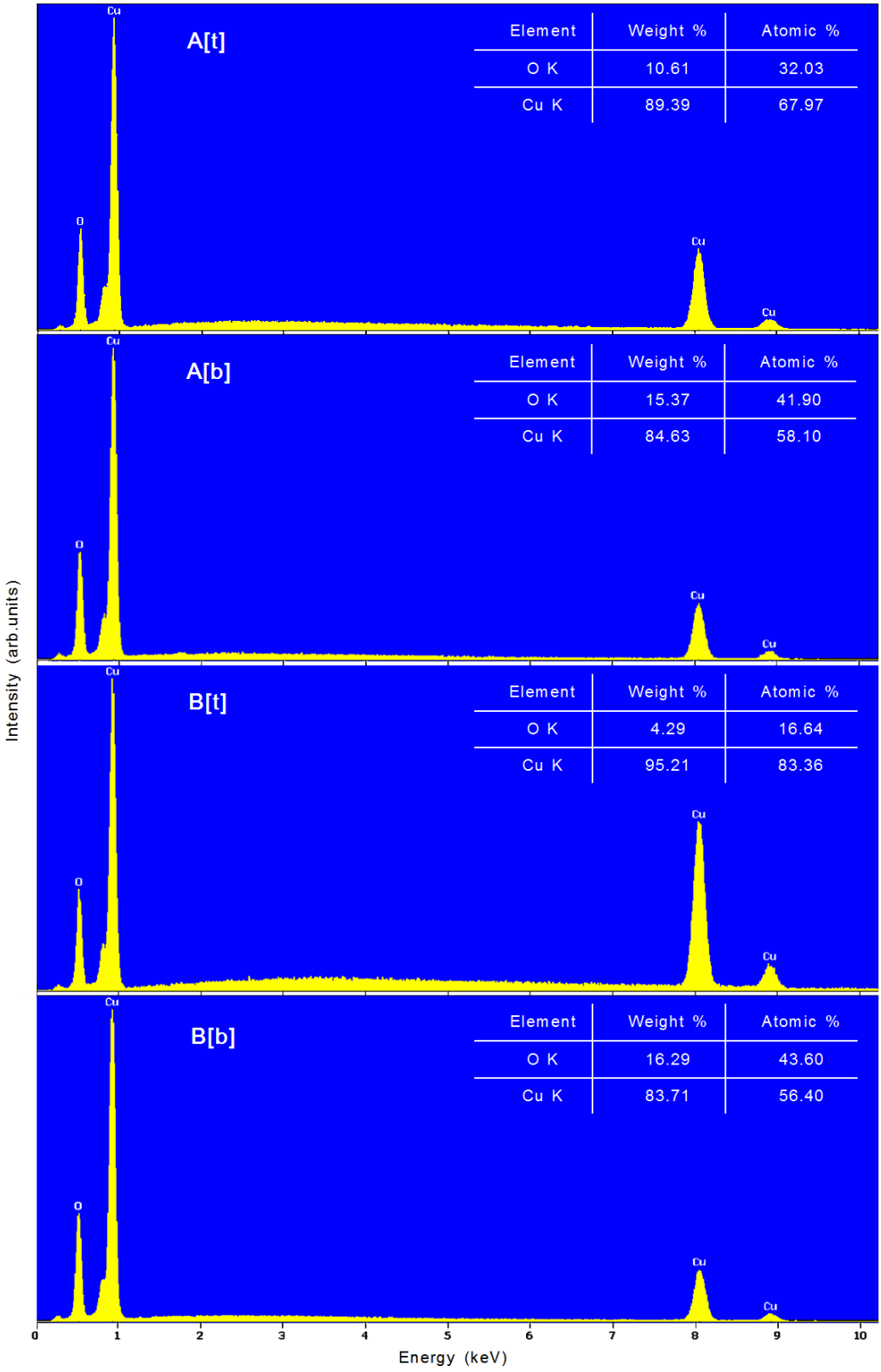

Fig. 2.4. EDS of CuO nanowires attached grains of A[t], A[b], B[t] and B[b] in Fig. 2.2.

Fig. 2.4 is the compositions created nanowire particles which were investigated in fixed points in the red circle of Fig. 2.2 by EDS. A unit nanowire tip and base of red circle in Fig. 2.2 (A) refer to Fig. 2.4 A[t] and A[b], moreover tip and base in Fig. 2.2 (B) refer to Fig. 2.4 B[t] and B[b], respectively. Particularly in Fig. 2.2 B[b] it was observed no particles on the base of a wire where seen exposed.

Here in our laboratory with regard to a unit nanowire, substrate was composed of Cu, a film upon the substrate was Cu_2O, the wire base upon the Cu_2O film and a wire was CuO, as discussed in [23]. Furthermore, general CuO nanowire EDS spectrum is Cu having K line about 8.04 and 8.90 keV as well as L line about 0.93 keV, moreover O having K line 0.53 keV [25].

This time we observed a wire portion, on nanowires both (A) and (B) in the K line, Cu and O did not approach in the same ratio, the content of Cu tended to be higher. Moreover as the tip parts of both (A) and (B), the content of Cu tended to be stronger. In the same K line both Cu and O in particular as for the tip with a larger grain at (B), Cu became extremely high. In this way, when the assemblage of grains is larger the Cu content shows to be high, thus grains should be defined as a concentrated Cu atoms sets.

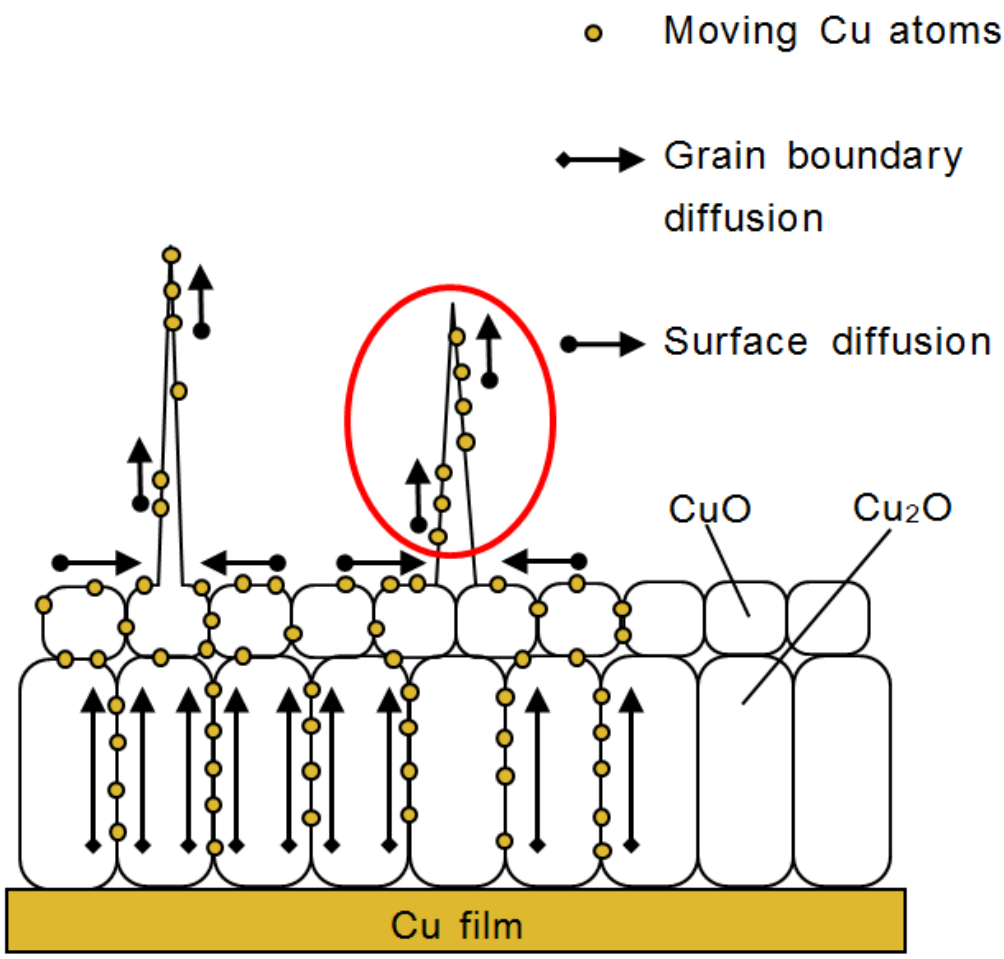

Fig. 2.5. Growth process model of CuO nanowires proposed by Mingji Chen. 2012. J. Appl. Phys. 111, 104305. The red circle was seen in this experiment to become copper grains.

Driving force for CuO nanowire growth is explained to be a stress generated in the formation of Cu_2O and CuO layer by applying heat energy [19, 20]. Molar volumes are the order of Cu < Cu_2O < CuO, further, the stress gradient is in the direction from the Cu / Cu_2O interface to the

CuO surface outward. As Fig. 2.5, grain boundaries caused by this stress, through those gaps Cu ions are diffused to CuO upper surface. Next Cu ions that have reached the surface are able to diffuse the sidewall of the wire continuing to form the wire tip.

The important point is Cu ions continue to assemble and form toward the tip as Fig. 2.3 A [t] dotted red lines and the result Fig. 2.4 A[t], B[t], although the boundary of the sidewall Fig. 2.3 A[m], A[b] was often seen clearly. That indicates the reason why CuO nanowire synthesis time mainly affects in the wire length.

On the other hand, the wire sidewall also slightly can chance to be formed as Fig. 2.3 A[b], A[m], therefore the effect over the wire diameter slightly come out during extending process. We assume that since the temperature could not be realistically fixed at the minimum part of near the wire for occurring slight variations between the temperatures, this affects the wire diameter during growth. However, that is modicum in comparison with the impact of the tip.

Since the annealing temperature was 500 ℃ in Fig. 2.1, copper particles were not be able to reach the boiling point, therefore not be released to the gas sublimation from the solid in atmospheric pressure by only lower energy of 500 °C. It is clear that copper solid ions rose along the wire surface having moved to sew grain boundaries from copper base, rather than the particles evaporated from the base surface, adhered to the wire.

Moreover, the same can be explained even observing at the particles between red dotted lines in Fig. 2.3 A[t] synthesized oftenly with the wire sidewall, although other areas A[m], A[b]

were not be able to accompany to react. This is in the nanowire growth process, these results there is a possibility to suggest the existence that copper ions diffuse on surface of the nanowires.

As the flow rate was close to minimum, copper grains began to appear on the wire. By causing a flow rate in the copper oxide nanowire synthesis, such as heat CVD, wires were completely synthesized like a liner wire [22, 24], never particles were created on it. We assume this is because that in either oxidation to open the furnace at atmospheric pressure, or synthesis by causing a flow to the enclosed furnace, the sufficient gas for reacting can be fed around the nanowire.

Conversely, in a completely sealed environment there is no oxygen flow by heating around the substrate at all ideally, naturally CuO nanowires in themselves cannot be growth to take time since oxygen is not enough around the wire. Only in a quasi-sealed environment such as enclosed furnace to cause a very small flow rate as much as possible not to synthesis, grains begin to set on the growing nanowire. It can conjecture to occur if near the wire is very close to the middle of the poor and the sufficient oxidizing.

Moreover, there can be a similar phenomenon in the nano-structure growth mechanism of other materials which generated from the tip of the nano-structure.

2.4. Conclusions

Under a general copper oxide nanowires occurring condition, in atmospheric pressure 500 degrees C and 60 min, in an enclosed space as dropping down an air flow rate approximately 0.01 L/min or less in the copper oxide nanowire synthesis, copper particles begin to set on the wire successfully. This was consistent with the discussion that copper ions diffuse on the wire surface in the copper oxide nanowire growth process.

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Chapter 3 - Macroscale synthesis of CuO nanowires on FTO plane substrate

3.1. Introduction

One-dimensional (1D) nanostructures such as nanowires, nanobelts, nanorods, and nanotubes have become the focus of intensive research as a result of their unique properties and potential usages [1]. Nanowires and nanorods of various semiconductor materials including Si, Ge, GaN, ZnO, and so forth, have been the focus of intense studies in the past years. Different approaches, such as vapor liquid- solid [2], vapor-solid [1], and template-mediated [3] growth methods, have been used for the preparation of 1D nanostructures of semiconducting materials.

Since Xuchuan Jiang et al. reported the surface synthesis of copper oxide (CuO) nanowires on copper substrates by direct annealing in air [4], the vapor-solid thermal oxidation has been considered as simple and effective method for synthesizing nanowires. CuO nanowires have been synthesized on several substrates, such as Cu substrate [4-6], roughened Cu substrate [7], Cu foil [8-12], porous Cu substrates [13], glass substrate [14], silicon substrate [15-17], copper powder disk substrate [18], and CuO spherical grain [19].

Generally, even if the copper foil is annealed, a higher density of nanowires is not obtained over the entire region.

Then, as the constituent elements of the CuO nanowires, Cu base material is the lowermost

substrate, then the Cu layer followed by the intermediate Cu2O film, and CuO film and CuO nanowires at the top [20]. Also, for the CuO nanowire to grow, tensile stress is required from the substrate.

In this study, we focused on two types of stresses, namely tensile and compressive stresses. The nanowires became dense when a tensile stress was applied to the substrate's surface in the plane direction. On the contrary, when compressive stress was exerted, the wires would become sparse [21, 22, 23]. Since the tensile stress acted only on a certain part of the surface, the nanowires were formed only on portions corresponding to these parts.

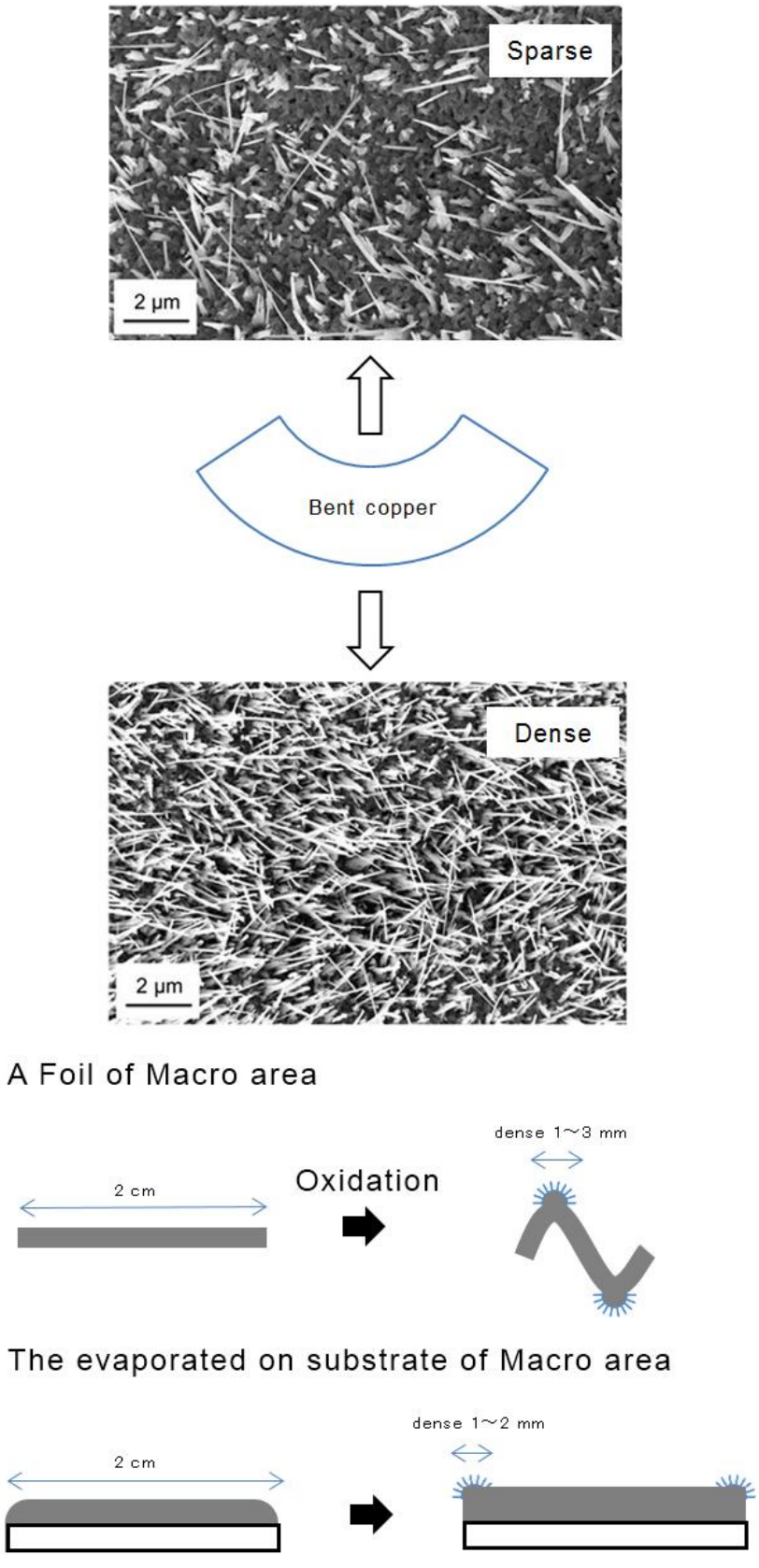

Fig. 3.1. According to R. Meme's proposal [22], in the treatment by annealing of an industrial grade copper plane substrate, bending of the copper foil occurred due to the thermal stress, and only the portion where the tensile stress acted upon that the nanowires were densely formed. Conversely, in the portion where the compressive stress acted upon, the wires were sparsely formed.

For example, as shown in Fig. 3.1, during the annealing of an industrial grade copper plane substrate, the copper foil bent due to the thermal stress, and the nanowires were formed densely only on those portions where the tensile stress was applied [21, 22, 23]. Since the adjacent sections were compressed, the wires could not be formed nor could be made sparse. Moreover, depressions could be created by compressive stresses. Thus, the macro area infrastructure was distorted by this stress, making it more challenging to create dense and uniform nanowire on a flat plane base.

In our experimental work, CuO nanowires were synthesized on the surface of an FTO glass sheet [24]. The synthesis of CuO nanowires on an FTO glass substrate is an important technique for the fabrication of optical devices with transparent conductive layers such as photovoltaic devices. However while annealing the deposited copper on a flat base, the defined tensile stress acted only at the corner of the substrate. Therefore, the nanowires into a film were concentrated only in the order of tens of micrometers of the part of the entire micro area, or at the end portion of the sample, but not on the entire macro surface.

From the viewpoint of stress and nanowires growth, this method is not effective for producing nanowires in the macro area of a continual plane substrate.

By manufacturing CuO nanowires on the entire plane, the number of nanowires can be increased in the planar direction, therefore, the CuO nanowires can be utilized in macro-sized devices such as flat large solar cells.

3.2. Experimental procedure

For the synthesis of CuO nanowires, fluorine-doped tin oxide (FTO) glass sheets were used as a substrate. An industrial grade FTO glass sheets (thickness, 0.1 mm and purity, 99.999%) were then cut into a standard size of 2.0 × 2.0 cm. The substrates were consecutively cleaned with acetone, methanol, and deionized water in an ultrasonic bath for 5 min, and were then dried by flowing N_2. Then, a 50 nm-thick copper thin film was deposited onto the cleaned FTO glass substrate using vacuum e-beam evaporation.

For electroplating, this deposited FTO glass substrate was used as a cathode, while the pure copper chip (Kojundo Chemical Lab. Co. Ltd.) was used as an anode. A 500-nm thick copper film was deposited in a high concentration of $CuSO_4$ solution at a voltage, current, and rotational speed of 0.25 V, 0.13, and 250 rpm for 1 min, respectively. After preparing the sample, it was washed in 20 mL of acid (0.1%) solution for 10 s. It was then ultrasonically cleaned with deionized water for 5 min and was dried under an N2 flow. The cleaned Cu substrate was placed inside an electric box furnace (KOYO, KBF-828 N). The oxidation was carried out at 500°C for 1 h in static air.

The SEM images were obtained using a microscope (Hitachi S-3000 H), which was operated at an acceleration voltage of 5 kV. The X-ray diffraction (XRD) patterns were recorded using a Rigaku RINT-2100 diffract-meter (40 kV, 30 Ma, Cu-Kα radiation, λ= 1.540598 Å) at a scanning speed of 0.02°/s in the 2θ ranging from 25° to 70°.

3.3. Results and discussions

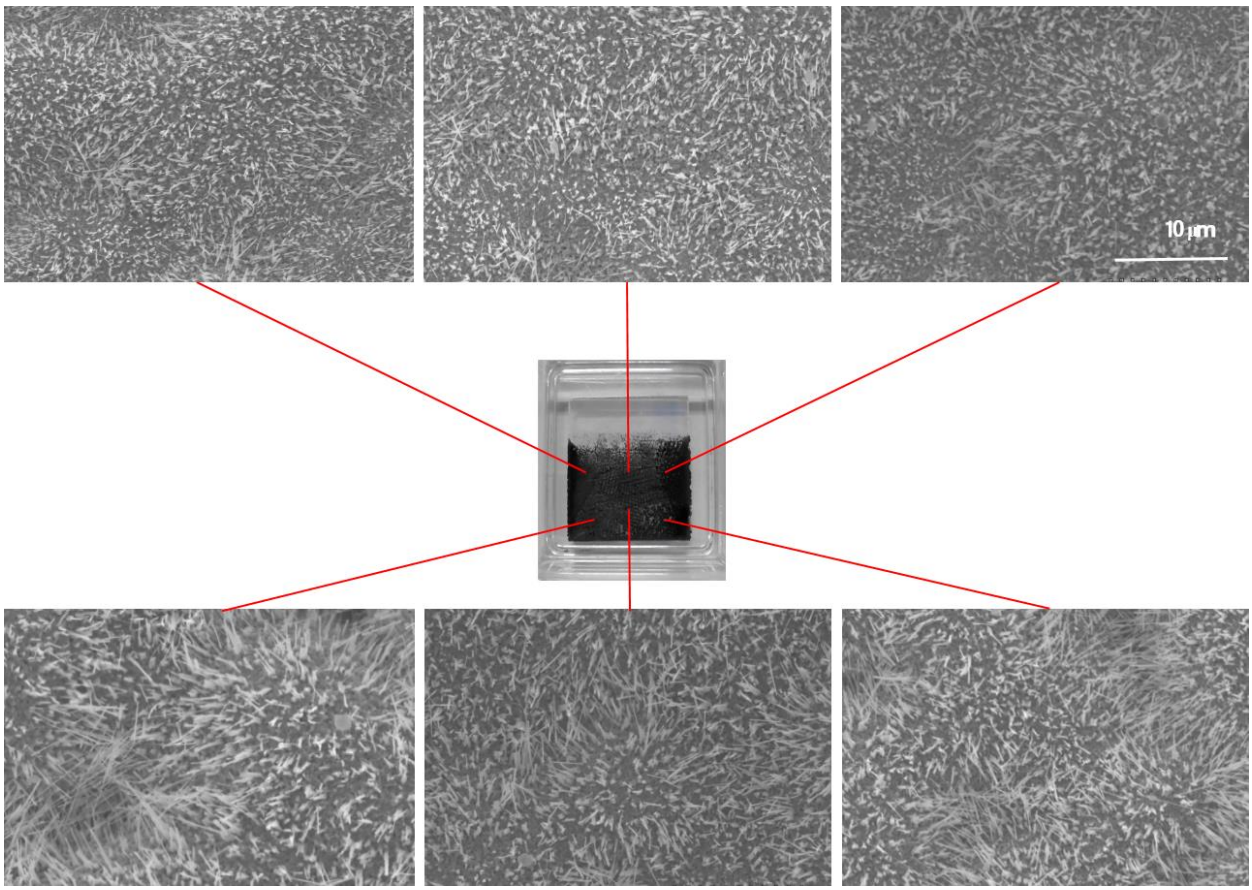

Fig. 3.2. SEM images of CuO nanowires on the 3/4 of the overall region of 2.0 cm × 2.0 cm FTO glass sheet.

Fig. 3.2 shows the SEM images of CuO nanowires produced uniformly and across an FTO sheet (a planar and flat glass surface area) using the proposed method. This CuO nanowire sample was affixed on the entire flat surface of the FTO glass substrate of the 3/4 region of 2.0 ×2.0 cm.

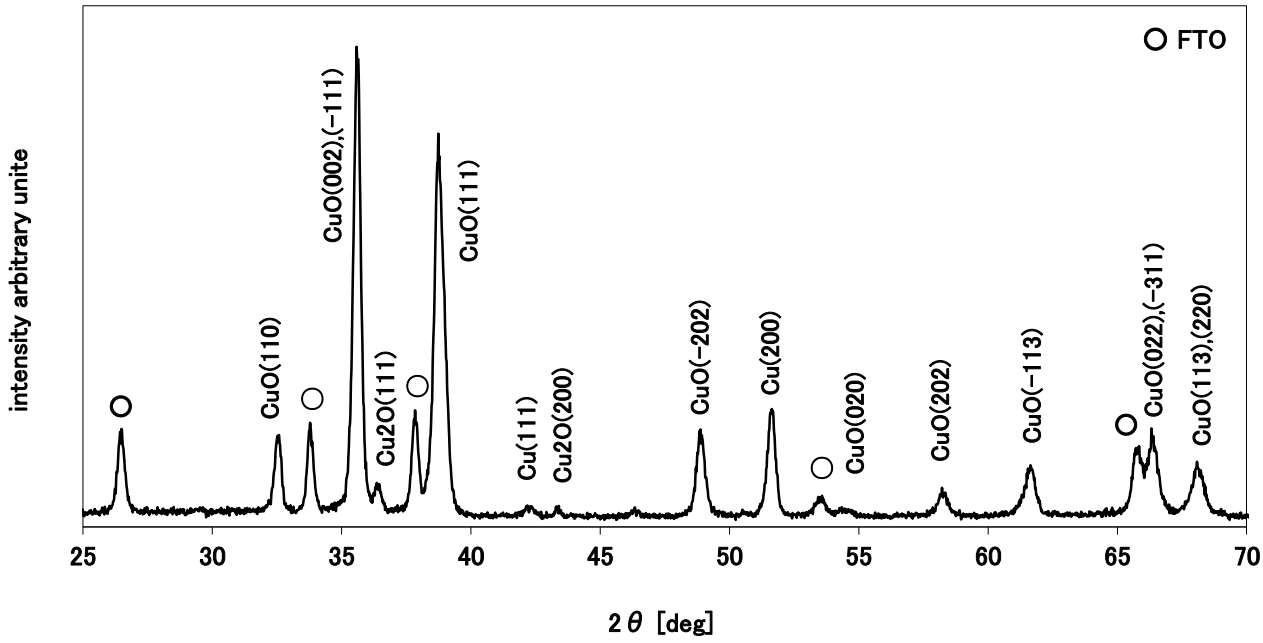

Fig. 3.3. The XRD results of the CuO nanowires that comprised CuO, Cu, Cu_2O phases at the annealing temperature of 500 ºC

Fig. 3.3 shows the XRD results, where CuO, Cu, and Cu2O phases, which are required for forming CuO nanowires, were observed.

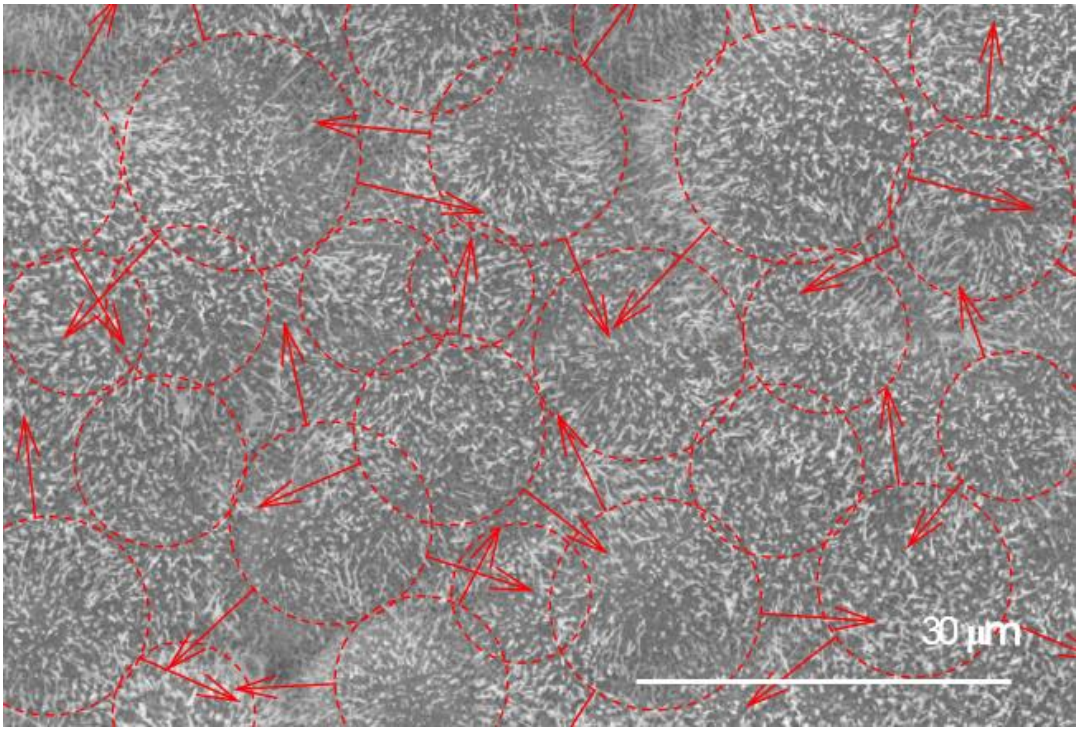

Fig. 3.4. An enlarged view of the sample surface. Dotted circles represent the convex portions, while the arrow's direction shows an example of a region where the tensile stress acted upon.

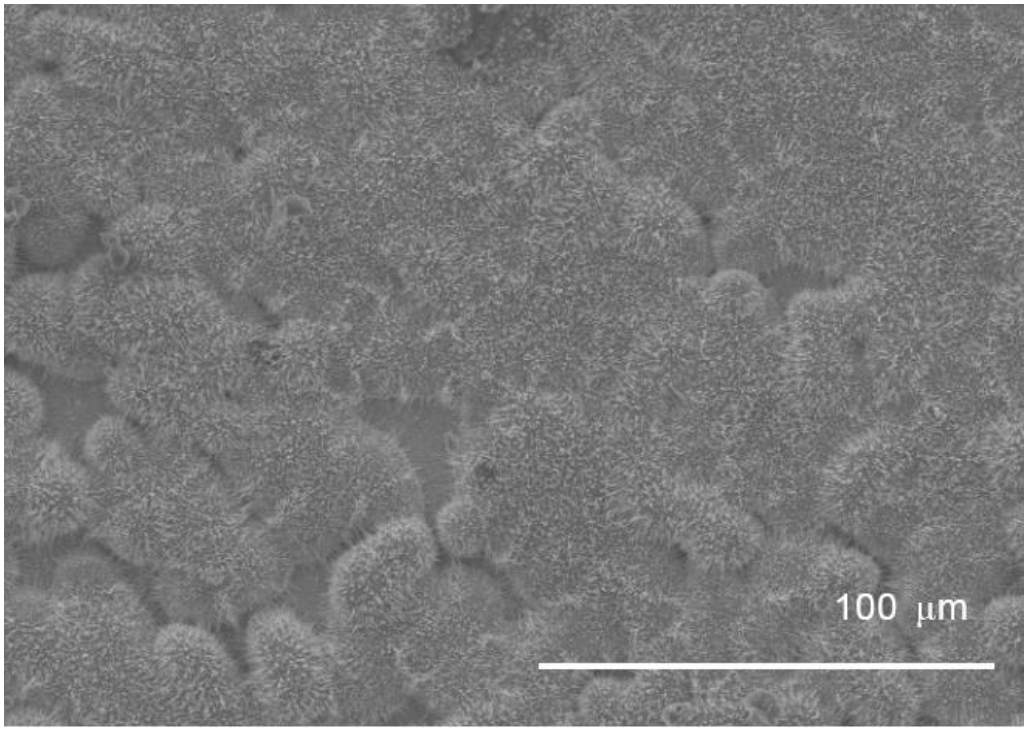

Fig. 3.5. An enlarged view of Fig. 3.4.

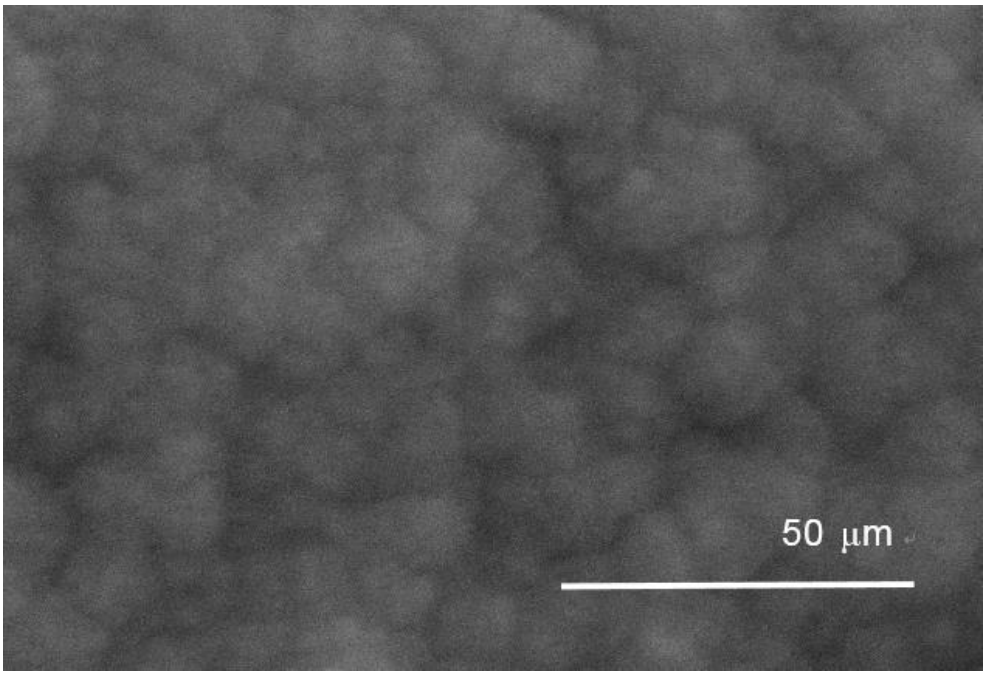

Fig. 3.6. The convex portions formed on the substrate before annealing in this experiment.

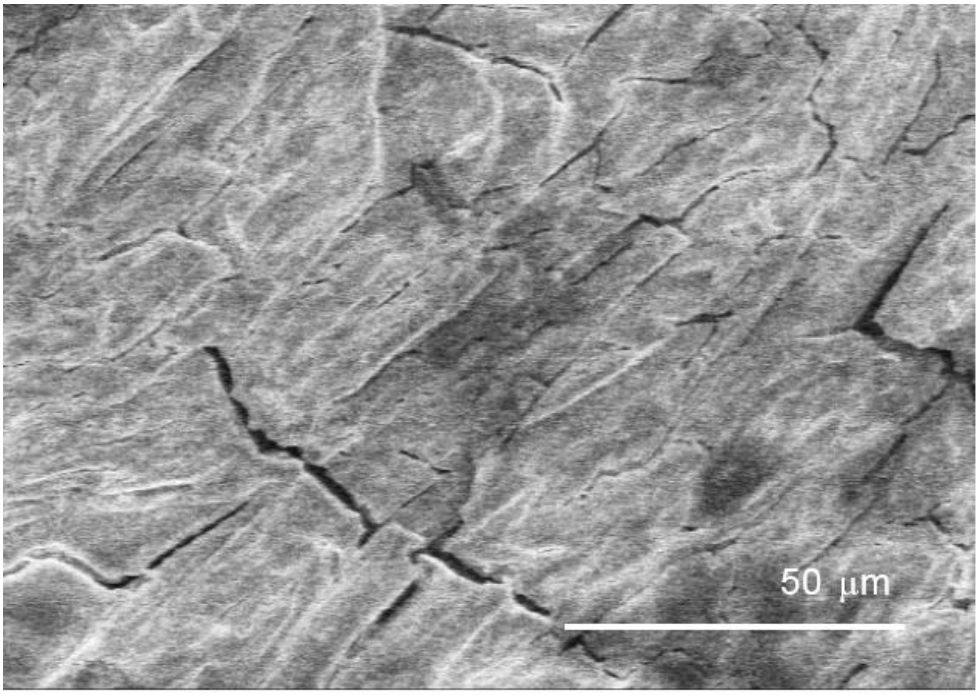

Fig. 3.7. The surface of the substrate after the reproducible industrial treatment.

As shown in Fig. 3.4, the nanowires formed on the FTO substrate had a plurality of hemispherical projections instead of a generally flat surface plane. The radius of the convex was approximately 10-20 μm. If the plating voltage was too low, the convex shape could not be formed, and the planarization, hence the nanowires could not be created either. Fig. 3.5 displays an enlarged area of Fig. 3.4.

Fig. 3.6 shows the convex portions on the substrate before annealing. In a majority of the industrial surface preparation of the copper film, the extremely flat surface of copper film is produced by acids after the electrode position. Fig. 3.7 shows the surface of the substrate after the reproducible industrial process.

As shown in Fig. 3.8, if the surface was annealed after produced a flat top by acids, the top surface expanded in the vertical and horizontal directions, but the total stress acting on the top surface of the CuO did not change much significantly. Therefore, the nanowires were primarily discarded at the top. The tensile stress tended to concentrate at the corner across the height and the top surface, where the surface area was enlarged regularly and sufficiently.

On the contrary, as can be seen in Fig.3.8, the Cu convex portions were formed on the substrate by the electroplating adjusted the voltage. If this convex portion remained and expanded due to annealing, the surface area, where the tensile stress was acted upon sufficiently, increased. Due to the tensile stress, the nanowires were densely formed. Fig. 3.9 shows the state in which one convex portion was expanded, as proposed by Rediola Mema et al.

[22].

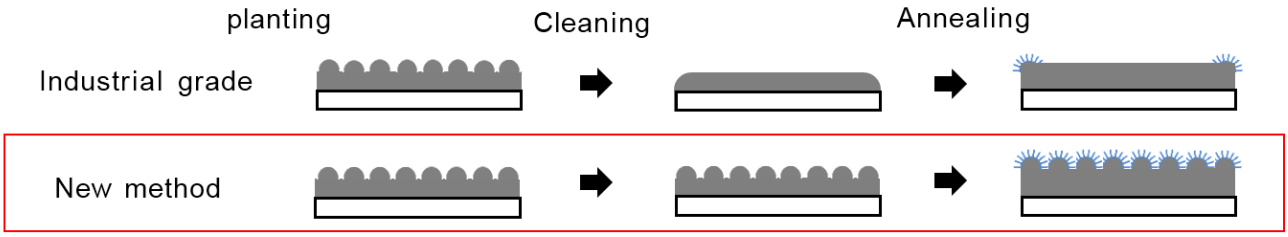

Fig. 3.8. (upper chart) The conventional method for CuO nanowires formation by an industrial grade process. (lower chart) The new method for CuO nanowire formation on a flat base proposed by our group.

Fig. 3.9. The CuO nanowires formation process in the case of convex expansion based on the study by Rediola Mema et al.

Similar to the CuO nanowires, other oxides materials used for nanostructures growth could also be manufactured base on the applied stress on a planar substrate with a similar method.

3.4. Cautions

CuO nanowires are in the form of a pointed tips like as asbestos. However, the safety risk of CuO nanowires is yet to be fully reported.

Therefore, in the case of mass production of CuO nanowires, there is a probability that the nanowires can cause the same kind of hazards as asbestos, it is necessary to be cautious.

3.5. Conclusions

The synthesis of CuO nanowires became possible on a macroscale on the plane area of the FTO grass substrate by formed Cu convex portions via electroplating adjusted the voltage and washing to keep the convex shape.

By manufacturing the CuO nanowires on the entire surface, it is possible to increase the number of wires in the planar direction, therefore, CuO nanowires could be applied to macro-sized devices, such as flat and large-surface solar cells.

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Chapter 4 - Direct Synthesis of Large-Area Graphene on Insulating Substrates at Low Temperature using Microwave Plasma CVD

4.1 Introduction

Numerous publications have been reported on various methods of synthesis of graphene and possible future applications, after successful stripping of monolayer graphene by Geim et al, in 2004, important electrical and optical And chemical properties were revealed [1-10]. Among various synthetic methods, thermal chemical vapor deposition (TCVD) has proven to be the simplest and most cost effective method for industrial grade graphene synthesis [11-15].

However, the use of a catalyst during graphene growth in TCVD creates special challenges for researchers, such as removal of the catalyst and transfer of graphene from such catalyst material to the desired substrate [16-19]. Future applications of graphene, such as transparent conductive electrodes (TCE), are also delayed due to the use of catalysts and inevitable transfer processes during graphene synthesis using TCVD.

In addition, TCVD is generally a high temperature process, and the substrate temperature used for graphene growth is typically above 1000 ^{o}C. Researchers have been looking for better alternatives to synthesize graphene directly on the desired substrate at low temperatures, and have ended the search for alternatives to indium tin oxide (ITO) for 20 years [20]. To overcome these problems, many researchers have attempted to grow graphene directly on an insulating substrate using TCVD.

In 2010, Ismach and colleagues reported the direct growth of graphene on various insulating substrates. However, using 1000 ° C as the working temperature used to evaporate copper is not feasible for a variety of boards that cannot withstand such high temperatures [21]. In a recent report, Song et al, also attempted to grow transition free graphene on an insulating substrate by using a copper vapor similar to that reported above [22]. To produce roll-to-roll graphene, Sony applies electrical current to the copper catalyst sheet to selectively heat the copper sheet and synthesize graphene up to 100m.

However, the authors admit that if the temperature of the copper sheet rises to about 1000 ° C during the Joule heating process, graphene may be defective at higher temperatures [23]. It would always better if the synthesis temperature was lowered and the transfer process was avoided in order to obtain graphene of almost the same quality as previously reported graphene.

Apart from TCVD, other methods such as plasma CVD have also been used by researchers to synthesize graphene directly on an insulating substrate without the use of a catalyst [24-26]. The advantage of using plasma CVD is that unlike TCVD, high temperature heating of the substrate is not required [27]. Sun et al, synthesized plasma graphene directly on a variety of insulating substrates at temperatures ranging from 400 °C to 600 °C using plasma enhanced CVD. However, it led to the formation of carbon nanowalls, and vertical growth was more dominant than lateral graphene growth [28]. Munoz et al. recently reported a 300 nm graphene

crystal formed using plasma CVD with a sheet resistance of 1.8 kΩ/□ [29].

In another report, Yamada et al, used plasma CVD, roll-to-roll synthesis of graphene, the transmittance of PET film is about 89% and the sheet resistance is on the order of 106 kΩ/□ [30]. Plasma CVD, which allows roll-to-roll direct graphene growth at low temperatures, encouraged many researchers to choose graphene over TCVD. So far, the direct growth of graphene has been limited to either a small area of graphene or a high sheet resistance [31,32].

In this chapter, a large area graphene is directly grown on an insulating substrate such as quartz or glass using magnetron-generated microwave plasma CVD (PCVD) at a substrate temperature of 300 ^{o}C, and ozone (O_3) treatment of synthetic graphene is performed. The effect was studied to improve the sheet resistance and transmittance of graphene.

4.2 Experiment

Experiments with quartz and micro slide glass, (2 x 2 x 0.1 cm, Matsunami Glass Industrial Co. Ltd.) using plasma CVD (Shinko Seiki, Japan) with a quartz plate followed by another quartz plate with apertures. It has been reported that when a quartz plate with holes is used, the density does not jump and high density plasma is generated compared to a flat plate. High-density plasma can be generated on a metric scale, and large-area deposition can be easily achieved using such plasma CVD.

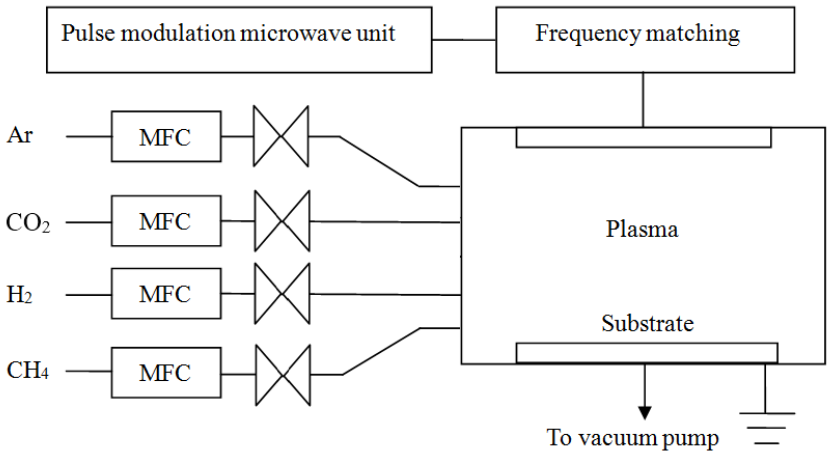

Fig. 4.1. Schematic of microwave plasma CVD.

A schematic diagram of the system used for graphene film growth is shown in Fig. 4.1. Graphene is deposited using a mixed gas of methane (CH_4), hydrogen (H_2), carbon dioxide (CO_2) and argon (Ar), with flow rates of 4, 15, 0.3, 15 sccm (minutes per standard cubic centimeter), Respectively, were selected in all experiments after optimization. A microwave power of 1000W was used so that fluctuation was negligible. Graphene was deposited on a microslide glass using a gas composition pressure of 10 Pa for 4 minutes and sonicated in acetone for 15 minutes.

After deposition, the insulating substrate was treated with ozone to further improve the sheet resistance and transmittance of carbon films deposited on glass and quartz. Ozone was generated using a high voltage power supply (9kV) between stainless steel meshes 8mm apart.

The substrate was characterized by Raman spectroscopy with a 532 nm laser excitation energy on a Renishaw InVia laser Raman microscope and X-ray photoelectron spectroscopy

(XPS) using a PHI 5000 VersaProbe. Optical imaging with Keyence VHX-6000 optical microscope, scanning electron microscope (SEM), JSM-6510 and Innova Atomic Force Microscopy (AFM) Bruker was used to analyze the surface morphology of the deposited carbon film. Using the JASCOV570 spectrophotometer, UV-Vis-NIR was used to characterize the light transmittance of the carbon deposition surface.

The sheet resistance of the carbon film was measured by the 4-probe method (RT-70V-Napson Corporation, Japan). Hall effect measurements were made using the Lake Shore 8400 Series (Toyo Corporation, Japan) and the van der Pauw technique.

4.3 Results and discussion

The experiment was performed at 800 W initial microwave power with different CO_2 concentrations with CH_4, H_2 and Ar. It has been found that the CO_2 concentration, which was higher than the 0.3 standard cubic centimeter (sccm) sheet resistance of the deposited carbon film, increases dramatically. In terms of sheet resistance and transmission, acceptable results were obtained with 0.3 sccm of CO_2 and CH_4, H_2 and Ar.

Fig. 4.2 shows that the sheet resistance and transmittance of the as-deposited substrate change with CO_2 concentration. After finding the optimal concentration of CO_2 and

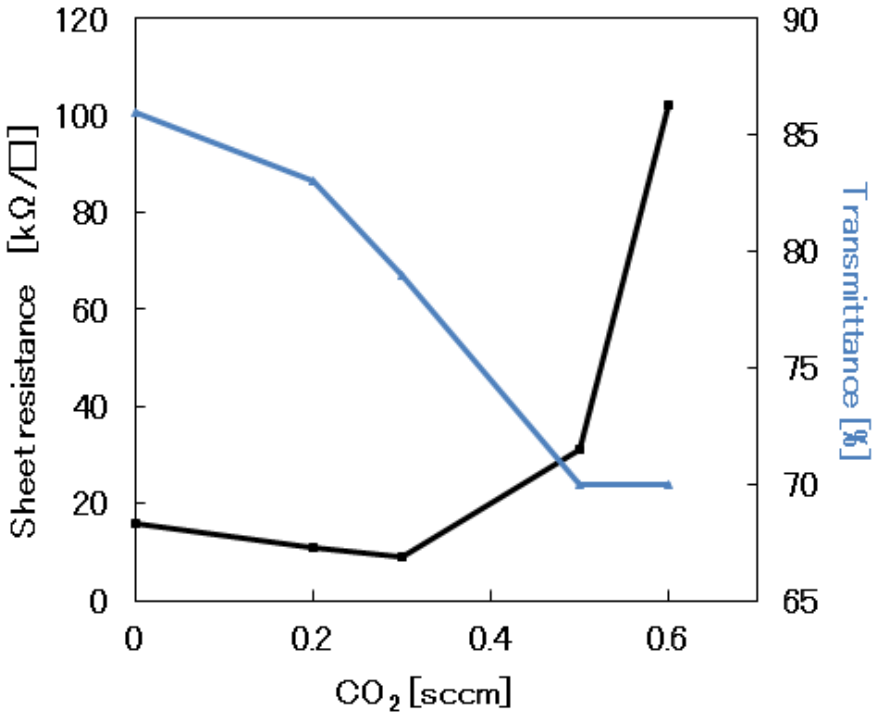

Fig. 4.2. Dependence of sheet resistance and transmittance of glass on CO_2 concentration.

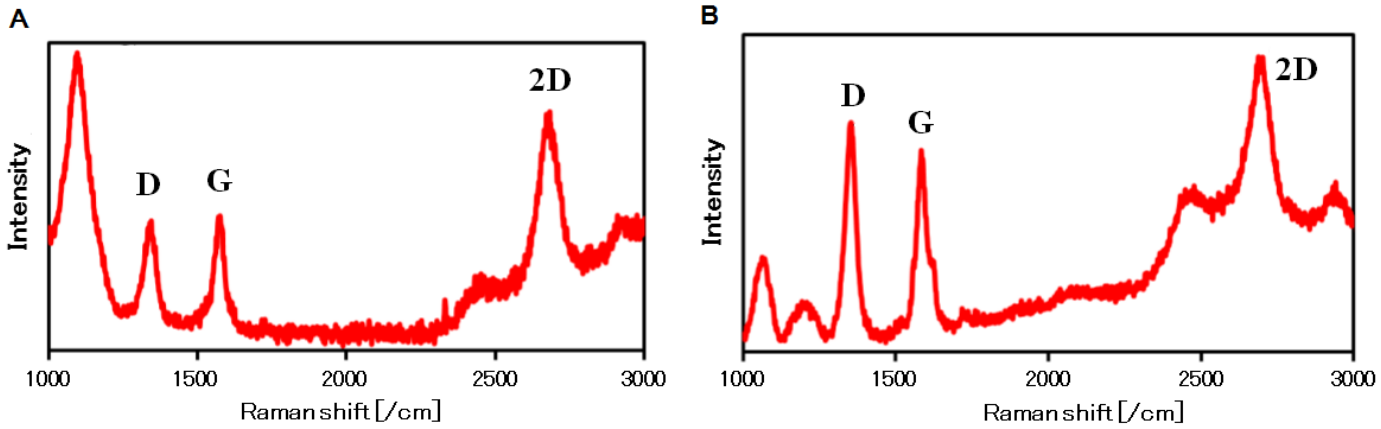

Fig. 4.3. Raman spectra of (A) glass and (B) quartz surfaces after carbon film deposition using PCVD during graphene growth.

experiment with other microwave powers, it was found that acceptable deposits were obtained at 1000W in 700-1200W microwave power. After all optimization, a substrate with a

sheet resistance of 1.3 kΩ/□ and a transmission of 80% was obtained. The synthesized film on glass and quartz was first characterized by Raman spectroscopy.

Fig. 4.3(A) shows a typical Raman spectrum of graphene on the glass surface. The 1350 cm^{-1}, 1580 cm^{-1} and 2682 cm^{-1} peaks corresponding to the D, G and 2D peaks, respectively, confirm the formation of several layers of graphene on the glass surface. Similarly, the Raman spectrum of quartz shown in Fig. 4.3(B) confirms the formation of graphene. The D peak in the Raman spectrum is due to defects in the synthetic graphene.

It has been observed from previous reports that plasma CVD forms vertically grown carbon walls much more easily than lateral graphene growth [33],[34]. Such vertical carbon walls can cause defect peaks in the Raman spectrum. Therefore, a detailed surface morphology inspection was performed using optical imaging, AFM and SEM analysis to evaluate the as-synthesized graphene morphology.

Fig. 4.4(A) shows an optical image of the quartz surface after graphene growth. In optical image observation, there is no clear evidence of carbon wall formation. Also SEM image of the Fig. 4.4(B), it clearly shows that the graphene has grown laterally. AFM analysis also confirmed that no carbon wall formation occurred, and the line profile on the quartz surface showed that graphene grew laterally on the quartz substrate with a surface roughness of a few nanometers.

Since it is clear from surface morphology examination that lateral graphene has formed, the

cause of the d-peak in the Raman spectrum may have been caused by oxygen impurities

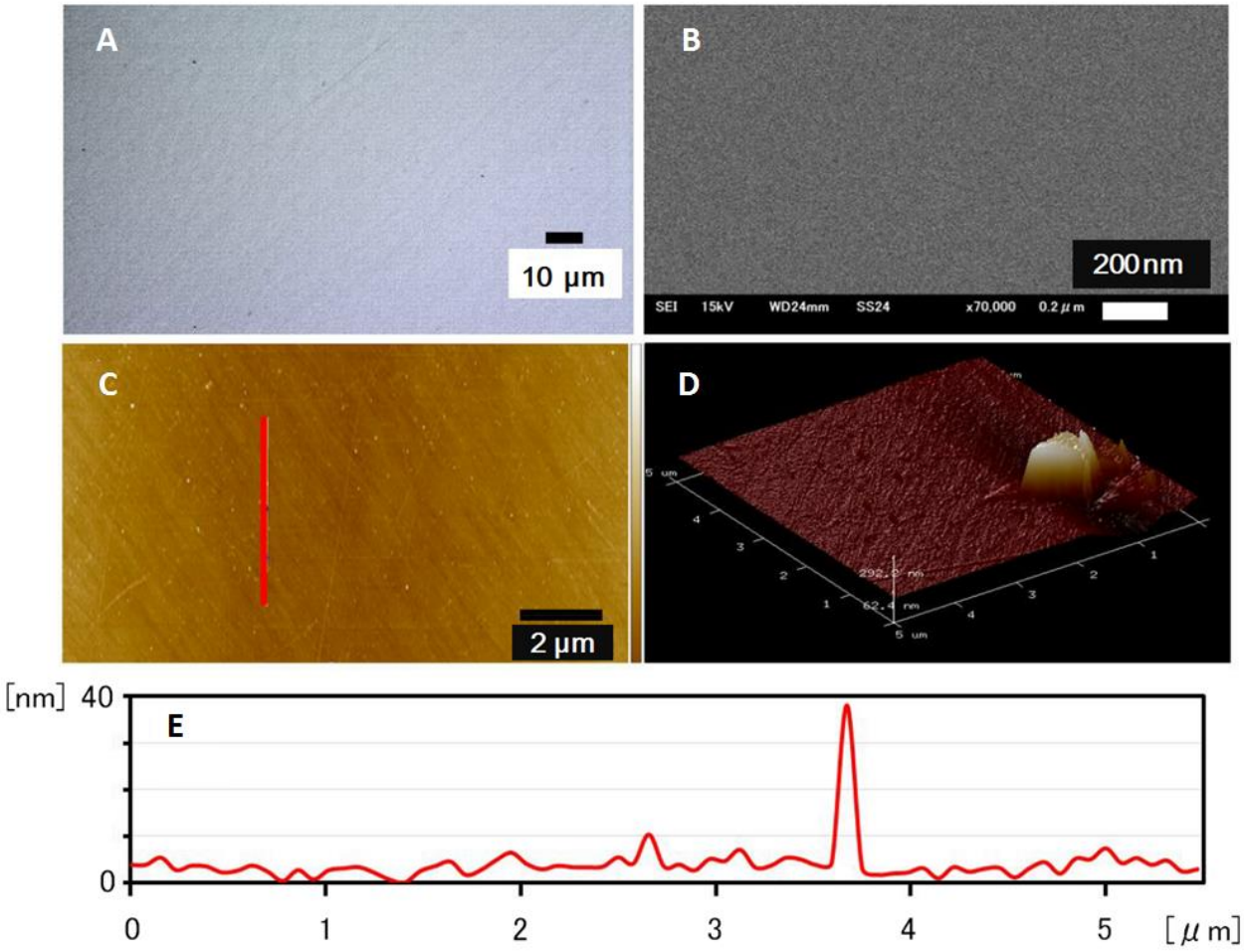

Fig. 4.4. (A) Optical image, (B) SEM image, (C) AFM image, (D) three-dimensional AFM image, and (E) line profile of a graphene/quartz surface.

resulting from the use of CO_2 or surface contamination during the synthesis process. However, using 0.3 sccm CO_2 during the synthesis process significantly improved sheet resistance and transmission, and helped control the vertical growth of carbon. This information is useful for lateral graphene growth using plasma CVD with improved sheet resistance and transmission.

To estimate the thickness of graphene, we scratched the continuous graphene/SiO_2/Si surface

and performed AFM measurements. Graphene was deposited directly on SiO_2/Si, especially for AFM analysis to obtain a clear contrast between the surface and graphene. The contrast of the SiO_2/Si surface with the graphene layer makes it easier to spot scratches during optical observations during AFM measurements. Fig. 4.5(A) shows an AFM image of the graphene/SiO_2/Si surface, with a scratch on the left side of the rectangular image and a graphene (yellowish part) on the right side. The figure also confirms lateral graphene growth on the SiO_2/Si surface that complements the previous explanation. The line profile in Fig. 4.5(B) shows that several layers of 1.2 nm thick graphene are formed on the SiO_2/Si surface.

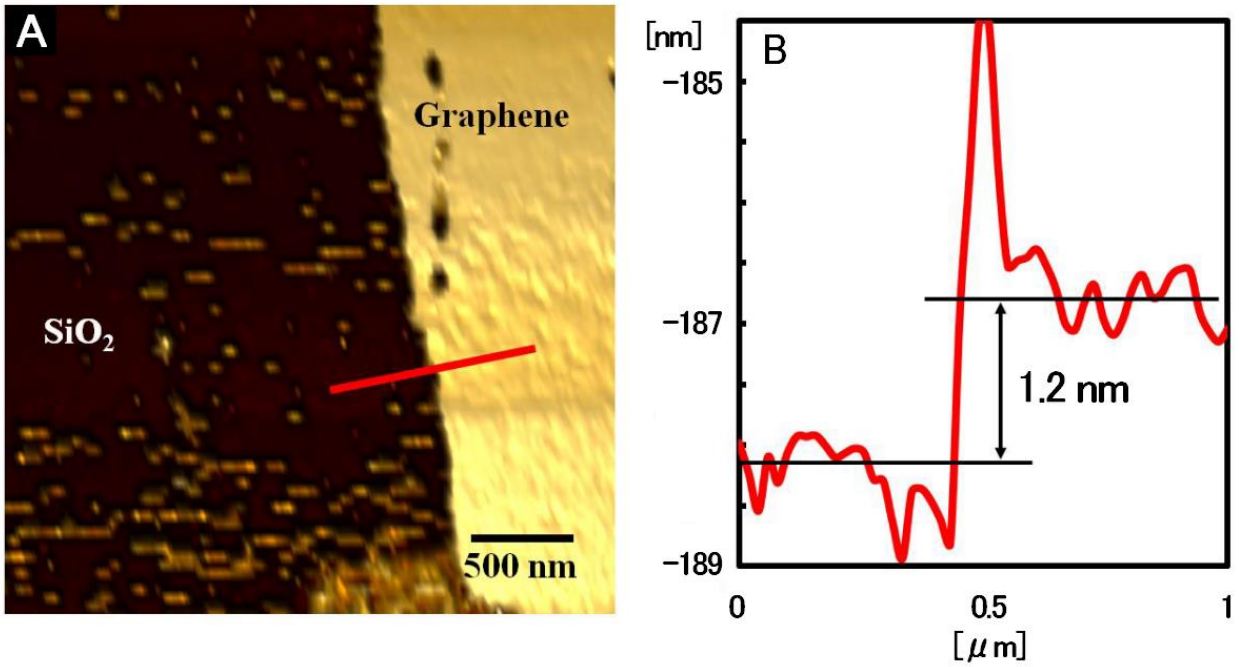

Fig. 4.5. (A) AFM image and (B) Line profile of graphene/SiO_2 surface.

When sheet resistance was measured using four probe technologies, graphene was formed in the range of 2.1 kΩ/□ to 2.8 kΩ/□ as shown in Fig. 4.6(A), and the transmittance of Fig.

4.6(B) was observed. Both blue lines show between 74% and 80%. Under the above growth

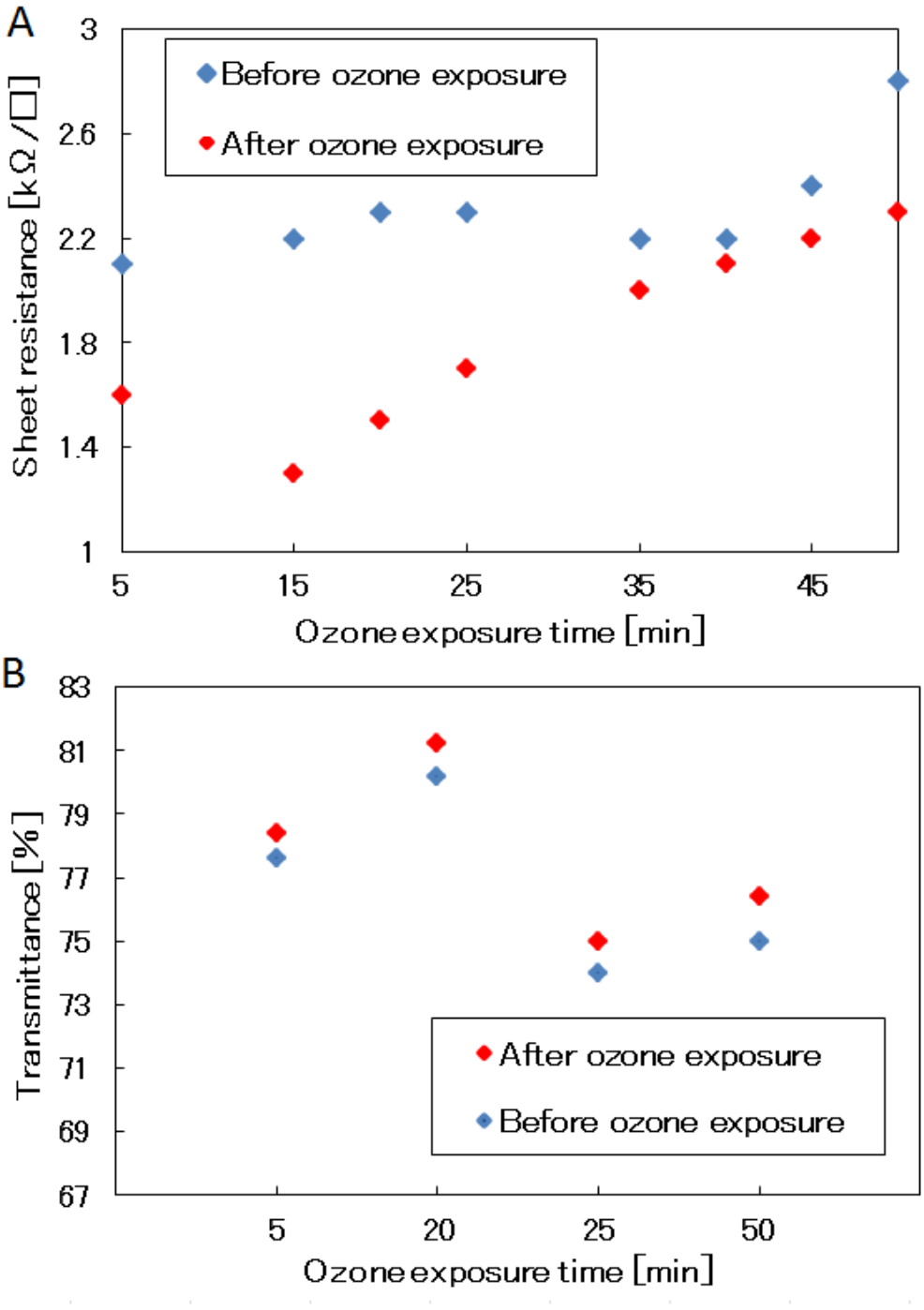

Fig. 4.6. Effect of Ozone treatment on (A) sheet resistance and (B) transmittance of PCVD -synthesized graphene.

conditions, nanometer-thick large area graphene cannot be synthesized on an insulating substrate at a temperature of 300 °C. Directly synthesized graphene on an insulating substrate with a sheet resistance of 2-3 kΩ/□ and a transmittance of 70-80% removes surface contamination or surface impurities, assuming that ozone treatment cleans amorphous carbon or other surface contamination. In order to be treated with ozone for various time periods, Li et al reported that 10 minutes of UV ozone treatment of graphene promotes metal-graphene contact by removing surface contamination. Also, such short exposure of UV ozone did not cause damage to the synthesized graphene [35]. Fig. 4.6 shows the change in sheet resistance of graphene after ozone treatment. As can be seen, graphene exposed to ozone for 15-20 minutes has superior quality in terms of sheet resistance and transmittance compared to as-synthesized graphene. The ozone exposure device improved the graphene sheet resistance by 30 to 35% and at the same time improved the transmittance by 1%.

In order to investigate the effect of ozone treatment on graphene, XPS analysis was performed on as-grown ozone-treated graphene samples. Fig. 4.7(A) shows an XPS survey of the graphene / quartz surface before and after ozone treatment showing the presence of silicon (Si), carbon (C) and oxygen (O). The display of the Fig. 4.7(B) C1s spectrum confirms the formation of the sp^2 carbon with a peak of 284.25 eV assigned to the C-C bond [36]. The shift of the C1s peak is clearly seen in Fig. 4.7(B) to 284.25 eV from 284.4 eV after ozone treatment. This 0.15 eV shift to lower binding energy may be due to the physisorption of ozone

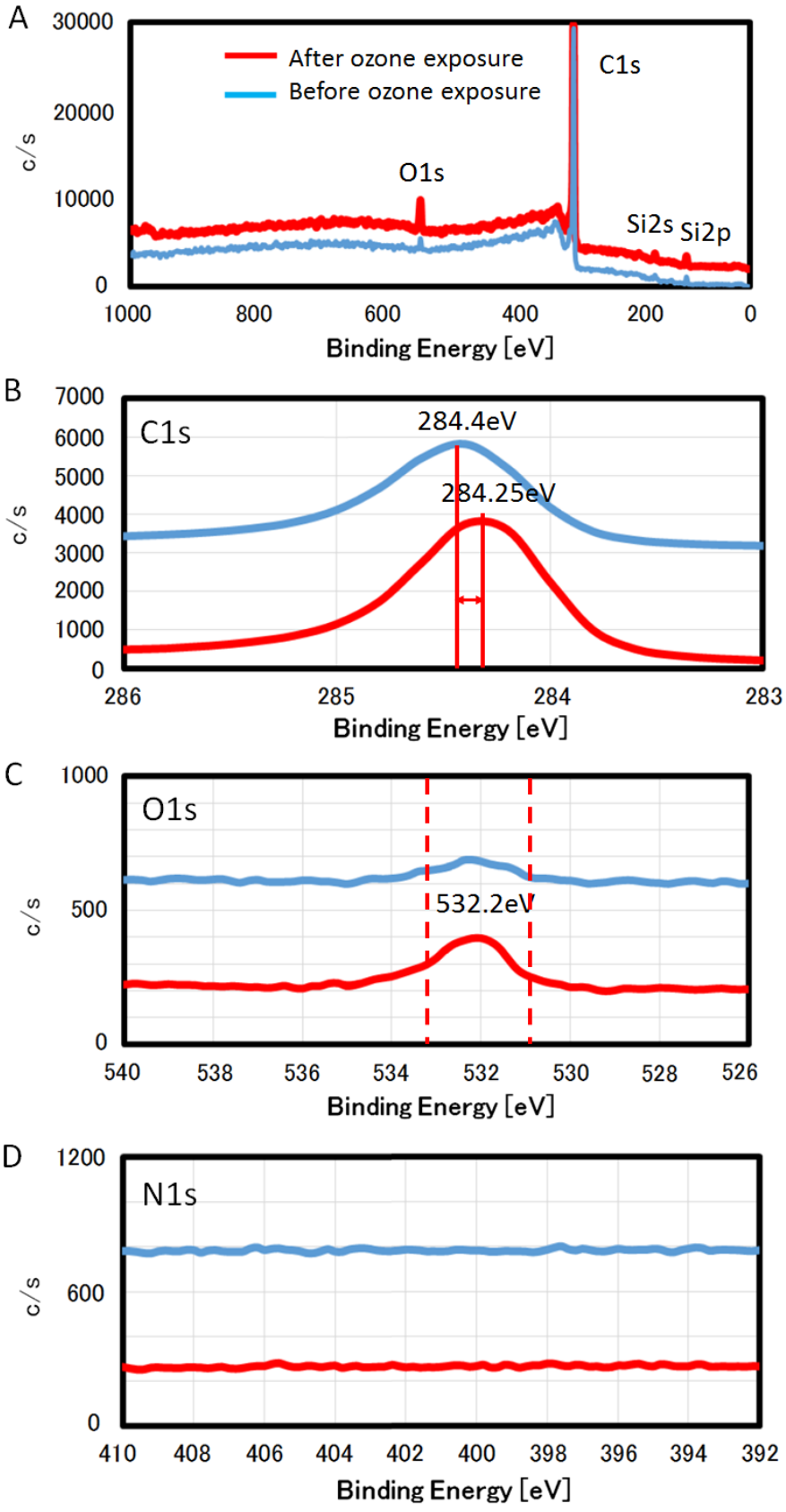

Fig. 4.7. (A) XPS survey spectrum, (B), (C), (D) C1s, O1s and N1s spectra respectively for as-grown and Ozone treated graphene.

molecules on graphene [37]. The physisorption binding energy of ozone to the graphene surface is less than 0.3 eV [38]. As reported by Jandhyala et al, this physisorbed ozone causes an upshift of the Dirac point and leads to p-type doping of graphene. An increase in p-type doping can be expected to improve electrical conductivity [39]. When graphene is treated with ozone for more than 20 minutes, epoxide groups are formed on the bottom of the graphene due to chemisorption of ozone. This increases the surface defects of graphene and increases the sheet resistance [40]. Aside from TCVD-grown graphene, there are reports on sheet resistance and mobility enhancement using ozone treatment for exfoliated graphene [41].

Table 4.1 Effect of O treatment on Hall mobility and carrier concentration of graphene.

		As grown graphene	O_3 treated graphene
μH	Hall mobility[$cm^2/V{\cdot}s$]	9.64	97.5
nsheet	Sheet carrier concentration [$1/cm^2$]	2.89E+14	5.09E+13

Table 4.2 Surface composition of graphene grown on quartz surface.

	C1s [%]	N1s [%]	O1s [%]	Si2p [%]
As grown graphene	97.2	0.0	1.5	1.3
O_3 treated graphene	94.7	0.0	3.5	1.8

Table 4.1 shows the effect of ozone treatment on graphene sheet carrier mobility and sheet

carrier concentration. Hall mobility increases by up to 350% with a slight decrease in sheet carrier concentration after ozone treatment. The oxygen detected in the O1s spectrum shown in Fig. 4.7(C) may have come from either the use of CO_2 during the synthesis process, the quartz surface under the graphene film, or C-O bond formation. The O1s spectrum also shows hump formation to higher binding energies after ozone treatment. This hump may be due to the Si-O bond. This indicates that the quartz surface is exposed to more X-rays after ozone treatment. O1s spectral hump formation confirms that ozone treatment removes surface contamination and forms physisorbed ozone on the graphene surface. This helps improve the mobility and sheet resistance of graphene sheet carriers.

Fig. 4.7(D) confirms that there is no as-grown graphene or nitrogen after ozone treatment. In addition, Table 4.2 shows that ozone treatment helped to remove surface contamination of graphene, as the carbon percentage decreased and the transmission increased by 1%. On the other hand, the increase in O and Si atom concentrations may cause X-rays to easily detect SiO_2 under the graphene to remove of unwanted impurities.

4.4 Conclusion

Direct growth of graphene on a 2x2 cm insulating substrate was achieved at a temperature of 300 °C using magnetron-generated plasma CVD. Graphene growth is controlled using a small amount of CO_2. Furthermore, after treatment with ozone, graphene with a sheet resistance of

1.3 kΩ / □ and a transmittance of 80% was obtained. It was observed that ozone treatment cleans the surface and increases graphene permeability and sheet carrier mobility.

These results help to grow graphene directly at low temperature on an insulating substrate to expand the applicability of graphene in optoelectronics.

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Chapter 5 - Conclusion

5.1 Conclusion of this work

One dimensional (1D) and two dimensional (2D) materials are expected as future electronic devices. Electronic devices containing various rare metals produced so far are very expensive for commercial use. With respect to the current rare materials, copper oxide nanowires and graphene are examples of 1D and 2D currently being studied that are very stable, inexpensive and non-toxic materials that can be attained from precursors well nature available. It has a potential for solar cell materials, and bring significant advances in materials research for applications in electronics, photonics, and energy devices. These applications require analysis of their structure, large areas, and large amounts of active device materials to enable production and utilization on a realistic scale.

Under conditions where general copper oxide nanowires are generated, it is possible to synthesize copper oxide nanowires at an atmospheric pressure of 500 ° C for 60 minutes and an air flow rate of about 0.5 L in the enclosed space. When the air flow rate is reduced to 0.01 L / min in a closed space in the synthesis of copper oxide nanowires, copper particles begin to collect on the wire. Furthermore, the particles that have moved from the substrate are formed from the wire tip to show why the synthesis time of the CuO nanowire mainly affects the wire length. This agrees experimentally with the argument that copper ions are diffused on the surface of the copper oxide nanowire growth process and grow toward the tip of the wire. We

experimentally demonstrated the surface diffusion of copper ions on the nanowires in such a 1D CuO nanowire with a mechanism formed by stress.

From the viewpoint of tensile and compressive stress and growth of nanowires, CuO nanowires mass production on a flat substrate is difficult. If the copper substrate is flattened as in the case of the industrial manufacturing method of copper, the dispersal of stress will cause damage to the copper substrate rather than the nanowires being manufactured. In the proposed study, however, this was made possible by changing the structure of the substrate. The nanowire substrate on the FTO is not a flat surface but a plurality of hemispherical protrusions the radius of the convex part is about 10 to 20 μm and forms a CuO plane. From the growth process of 1D CuO nanowires using stress, it has become possible to increase the area of a planar substrate with a large number of nanowire elements by a simple synthesis method.

Direct graphene growth on an insulating substrate using microwave plasma CVD is controlled using a small amount of CO_2. After further treatment with ozone, graphene with a sheet resistance of 1.3 kΩ/□ and a transmittance of 80% was obtained. It can be seen that ozone treatment cleans the surface and increases graphene permeability and sheet carrier mobility. The growth of graphene achieved at a temperature of 300 °C increases the range of direct growth to an insulating substrate or semiconductor that can be grown directly at lower temperatures. We also focused on graphene, which is expected to be a transparent conductive film as a two-dimensional material, and were able to increase the area and quality by direct

synthesis at low temperatures, which will be necessary in the future.

5.2 Suggestions for future study

CuO nanowires still experimental to the laboratory. Several early experiments have shown how to use them to build next-generation electronic devices. The first important step in creating active electronic devices is to dope to nanowires chemically. This has already been conducted for individual nanowires to change p-type or n-type semiconductors.

The next way is to find to make a p-n junction of the simply electronic devices. The main purpose of this paper is to produce solar cells from copper oxide nanowires that can be run for very low cost, non-toxicity, and stability. The heterojunction of p-type copper oxide nanowire and n-type zinc oxide devices will be a future purpose of this study.

As for plasma CVD graphene, this time it was in the range of 2x2cm, but by improving the plasma CVD stage and discharge quartz plate, it is possible to grow graphene directly over a wider range. These results help to grow graphene directly at low temperature on an insulating substrate to expand the applicability of graphene in optoelectronics. The challenge is to further improve the quality of graphene films by optimization of plasma conditions.

Furthermore this film formation technology can be handled not only as a single carbon solar power value but also as a transparent conductive film that can replace rare metals. As a transparent conductive film, this technology can be applied to various semiconductors such as

direct growth on n-type zinc oxide and p-type copper oxide nanowire layers created as solar cells.

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List of publication

[1] Direct existence to suggest activity of copper ions surface diffusion on nanowire in growth process

Yota Mabuchi, Norhana Mohamed Rashid, Jian Bo Liang, Naoki Kishi, Tetsuo Soga

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[2] Macroscale Synthesis of CuO Nanowires on FTO Plane Substrate

Yota Mabuchi, Rashid Norhana Mohamed, Xuyang Li, JianBo Liang, Naoki Kishi,

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[3] Direct Synthesis of Large-Area Graphene on Insulating Substrates at Low Temperature using Microwave Plasma CVD

Riteshkumar Vishwakarma, Rucheng Zhu, Amr Attia Abuelwafa, Yota Mabuchi,

Sudip Adhikari, Susumu Ichimura, Tetsuo Soga, Masayoshi Umeno

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Conference

Formation of graphene thin films by microwave surface plasma pulsing

Yota Mabuchi, Tetsuo Soga, Masayoshi Umeno 2018 79th JSAP Autumn Meeting, Plasma deposition, detail 2018-09-21-[21p-PB1-8]