Characterization of Fine-Pixel X-ray Imaging Detector Array Fabricated by Using Thick Single-Crystal CdTe Layers on Si Substrates Grown by MOVPE

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***Abstract*—A novel approach for developing a large-area, high spatial resolution X-ray imaging detector is presented. This approach uses metalorganic vapor-phase epitaxy (MOVPE) grown thick single crystal CdTe layers grown directly on Si substrates. The detector consists of a p-CdTe/n-CdTe/n$^+$-Si heterojunction diode structure, where the n-CdTe and the p-CdTe layers are successively grown on the n$^+$-Si substrate. An array of (128x128) pixels were formed on the p-CdTe side, where each pixel is 60 μm^2 in a 80 μm pixel pitch. The detector array was bump-bonded to a charge integration type CMOS read-out ASIC. The basic performance of this detector array was evaluated by measuring the dark currents, spatial resolution as well as taking X-ray images of some objects. The results were promising which confirmed that the detector developed can be applied in high spatial resolution X-ray imaging.**

***Index Terms*—CdTe, Epitaxial growth, High spatial resolution, Imaging array, Large-area**

I. Introduction

CDTE is an ideal material for the development of high-sensitivity X-ray, gamma ray spectrometers and imaging arrays operable at room temperature. These devices are currently fabricated using melt-grown bulk crystals, and their superior energy resolving capacity as well as spectroscopic imaging property have been demonstrated [1]-[4]. However, melt growth of a large-area crystal with uniform material quality has been extremely difficult. Because of this material constrains, current imaging detectors are limited to relatively smaller sizes, but with somewhat larger pixel pitches varying from several hundreds of micrometers up to the millimeter range [5]- [6]. Developing a large-area monolithic detector with fine pixel pitch is not presently viable. The only possible option available for constructing larger detector is rigorously tiling several carefully-screened small-area detectors in mosaic array [7], [8]. However, this method imposes additional complexities and system cost, and not always feasible. Besides these CdTe crystals are very fragile and highly vulnerable to suffer from manufacturing process induced damages, resulting the detector performance degradation.

Vapor-phase epitaxy is a promising way to obtain large-area crystals with controlled crystal properties by performing growth on easily available large-area substrates, such as Si or GaAs. This growth technique further eases the crystal handling as the CdTe crystals are supported by robust substrates thereby eliminating the process induced damage. Epitaxial growth of single crystal CdTe on Si substrates has been intensively studied using molecular beam epitaxy (MBE) [9], [10]. However, these growths were intended for infrared detector applications with crystal thicknesses of a few micrometers, which are far from sufficient for X-ray detector applications. On the other hand, there are limited reports on thick CdTe polycrystalline layers, but these polycrystals are not suitable for spectroscopic imaging applications [11].

We have been studying metalorganic vapor-phase epitaxy (MOVPE) growth of thick single crystal CdTe layers on Si substrates, and detector development since past several years [12]-[15]. Using this technique, we have grown up to 260 μm thick single crystal CdTe directly on (211) Si substrates. The details are reported elsewhere [12], [13]. We also developed p-CdTe/n-CdTe/n+-Si heterojunction diodes type spectrometers [13], as well as (8x8) pixel monolithic detector arrays and confirmed they could be applied in spectroscopic imaging applications [14], [15].

In this study, we developed a fine pixel (128x128) X-ray imaging array using single crystal CdTe grown on a 25x25 mm^2 Si substrate. Here we report on the detector fabrication and characterization, mainly the array dark current properties as well as X-ray imaging properties. These results confirm that this array fabrication technique is highly potential for making a large-area and high spatial resolution X-ray imaging arrays. We further discuss on the crystal orientation of CdTe on Si using some X-ray imaging data obtained from one of our earlier arrays. This result shows that the grown CdTe is single crystalline throughout the wafer with growth orientation exactly parallel with that of the Si substrate.

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II. Detector Array Fabrication Details

The detector array was fabricated using CdTe epitaxial layers grown directly on the 25x25 mm^2 sized (211)-oriented n$^+$-Si substrates in a custom-designed MOVPE reactor. It should be noted that though our growth system can handle up to 4-inch substrate, for ease of processing such as substrate pretreatments, device fabrications, etc., we are currently doing growth on two 25x25 mm^2 and two 20x20 mm^2 Si substrates simultaneously per grown run.

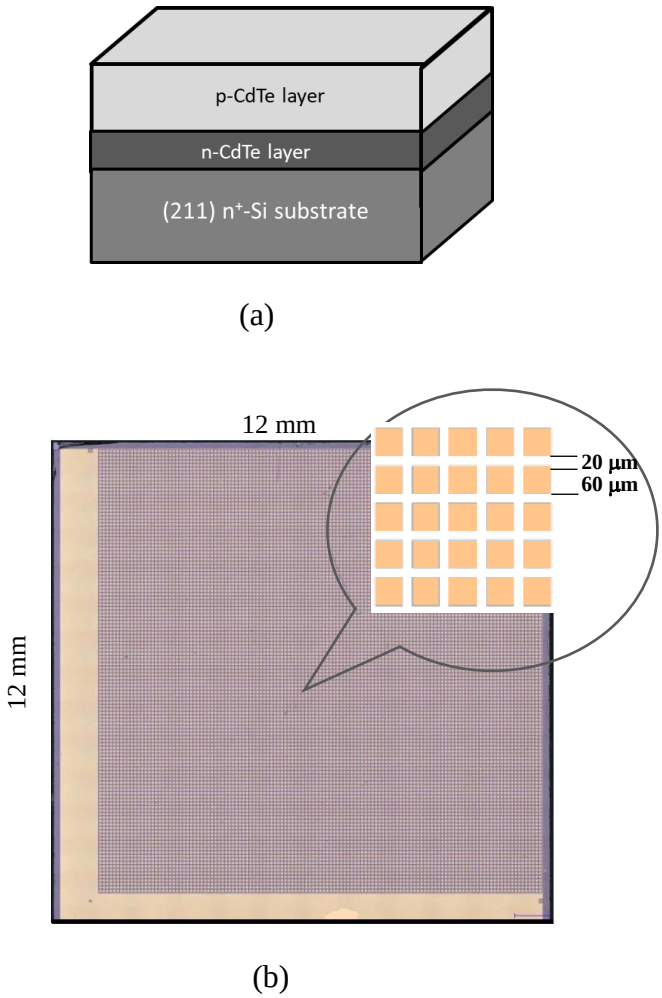

Fig. 1. (a) Schematic diagram of heterojunction diode-type detector structure, (b) a photograph of the (128x128) pixel imaging array fabricated before bonding it to the readout electronics.

Fig. 1(a) shows the detector structure, where a thin n-CdTe layer (typically 3-5 µm) is first grown on the n$^+$-Si substrate, followed by the growth of thick undoped p-like CdTe layer (~100 µm). After the p-like CdTe growth, a chemo-mechanical polishing was performed to make the crystal surface flat, followed by gold electrodes deposition on this and back side of the n$^+$-Si substrate. Finally, gold contact pads with a 60x60 µm^2 size in a 80 µm pitch and an outer guard ring contact was developed on the CdTe side to make (128x128) pixel array using a standard photolithography process. Fig. 1 (b) shows a photograph of the array developed before bonding it to the readout electronics. As seen in the figure, the width of the guard-ring on the top and on the right side of the array is different than that on the bottom and on the left side, which is due to the design criteria of the ASIC. The array fabricated has a heterojunction diode structure, which is operated in a reverse bias mode by applying a positive bias on the n$^+$-Si backside contact. The X-ray generated charge carriers travel in the vertical direction. It should be noted that though we are using a 25x25 mm^2 size epitaxial CdTe crystal, the active area of the array developed is 12x12 mm^2, which was diced out from the larger crystal. We had to make the array size smaller to adjust it with the pixel pitch and geometry of the readout ASIC. After dicing, the detector array was bump-bonded to a charge-integration type CMOS-ASIC. The 128x128 channels ASIC is a hole-collecting type, which has bonding pads that match the pixel size and pitch on the detector. The ASIC integrates the charge in the detector pixels, and readout them sequentially from each row by the charge-sensitive pre-amplifier. In this investigation, we used a frame rate typically 100 fps, but it can be varied. The readout system converts the analog signal to digital data using a 14 bit A/D converter. Detector crystal growth and array fabrication was performed at our laboratory using in-house facility, whereas array bonding and acquisition of the X-ray images were carried out with the cooperation from outside vendor.

The basic performance of this detector was evaluated by measuring the array dark currents and X-ray generation current as well as taking X-ray image of some objects. Spatial resolution was measured by taking X-ray image of a resolution test pattern (Fluke 07-525). In this investigation, a RQA5 quality x-ray radiation (average photon energy 50 keV) was used and measurements were performed at room temperature (25 ºC).

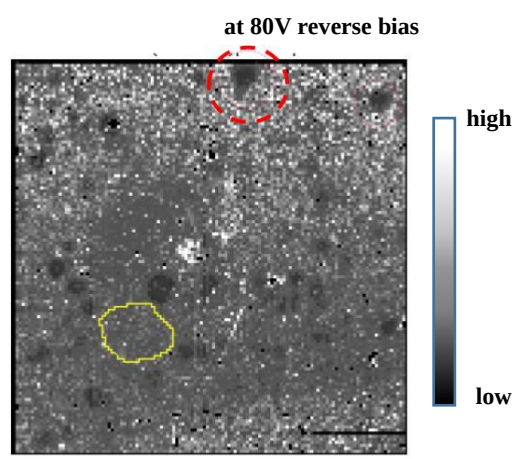

Fig. 2. Distribution of dark currents across all pixels in the array. The dark current was evaluated at room temperature by applying a 80V reverse bias. Most of the pixels (eg. solid line marked) exhibited dark current equal to 1 µA/cm^2. However, some pixel or cluster of pixels (marked with dashed circle) showed extremely low dark current which may be due to non-functional electronics or some bonding problem.

III. Detector Evaluation Results

The dark current of the array was measured at room temperature by applying a +80V bias on the n^+-Si back contact, and dark currents were read from the entire pixels. Fig. 2 shows the distribution of dark current across all pixels in the array. The result shows there are some variation in the dark current values. The white pixels lying in the upper half portion of the array show high dark currents, while the dark pixels low. Most of the pixels such as pixels marked with solid line exhibit a dark current about 1 $\mu A/cm^2$. We will discuss about the array dark currents further in section IV.

We further measured the X-ray generation current. The detector bias voltage was varied from 30 to 80 V, and the RQA5 quality X-ray was irradiated through the Si side. The X-ray dose was 8.8 mGy/min for this measurement and the data were taken from the several pixels exhibiting low dark currents (portion marked with solid line in Fig. 2) and their values were averaged. Shown in this figure is the extracted values of X-ray generation current (where the pixel dark current has been subtracted). The result shows the X-ray generation current increases linearly with the applied bias from 30 to 60V, where it saturates afterwards. This suggests that the detector is fully depleted at 60V bias. In fact, capacitance-voltage measurement performed separately on other arrays also show similar results. The capacitance values saturate when the reverse bias exceed beyond 50V, indicating the full depletion of the detectors with these bias ranges. However, a slight decrease in current observed at 80V bias is not clear at this moment. This could be due to response fluctuation of some pixels because of trapping, but needs further confirmation.

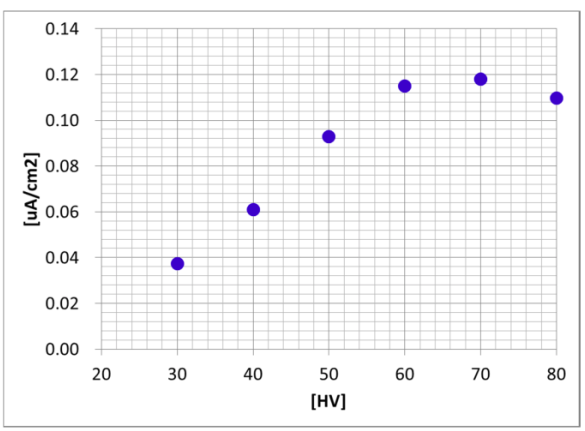

Fig. 3. X-ray generation current measured at room temperature as a function of applied bias. The generation current was measured from several pixels (inside the marked solid yellow line in Fig. 2), and their averaged value is plotted.

Preliminary X-ray images of a ball-point pen and a screw nut were taken with the detector array, which is shown in Fig. 4. The image was obtained at room temperature by applying a 60 V bias. Details about the X-rays used is mentioned in the respective figures and no filters were used while taking these images. The objects in these images can be clearly identified. These results are promising and confirm that the detector array developed can produce good quality images. In Fig. 5 images of a resolution chart pattern are shown. The detectors were biased at 60 V and the image were taken at room temperature. The lines corresponding to 8.0 lp/mm is clearly visible in the image. This spatial resolution is close to the theoretical value of 8.33 lp/mm as calculated from the Nyquist frequency for a 60 μm pixel array.

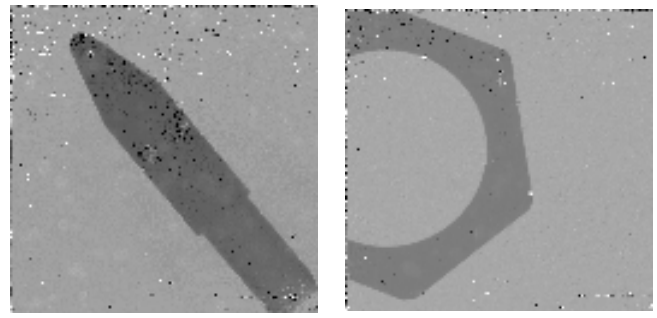

Fig. 4. X-ray image of a ball-point pen (left) and a screw nut (right) obtained with the detector array. Both images were obtained at room temperature by applying a reverse bias of 60V on the detector. The X-ray was set at 50 kVp, 3mA for left image, while 40 kVp, 2mA while taking the right image. The integration time was 7ms, and these are light-field corrected images.

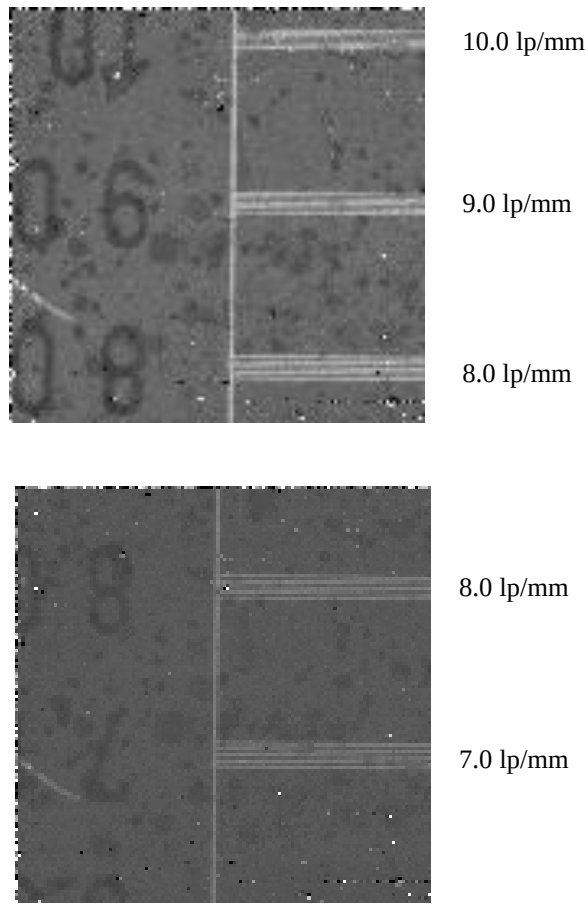

Fig. 5. Images of a resolution test pattern (Fluke 07-525). The detector was biased at 60 V, and images were taken at room temperature. The RQA5 quality X-rays were used.

IV. Discussion and Future Prospective

Test results from our detector array are very promising, which make this technique very attractive for the development of large-area imaging arrays. Though the detector in this investigation was operated in a charge integration mode due to the type of ASIC available, however it can also be operated in photon counting mode. We have previously reported the spectroscopic performance of these epitaxially grown CdTe detectors fabricated in the similar manner [16]. Hence, by selecting a suitable readout electronics, our detectors can be operated in both charge-integration as well as photon counting modes.

Furthermore, currently these detectors are operated in a hole-collection mode because of their device structure. By fabricating electrons collecting detector further improvement in performance can be expected because of the superior charge transport property of the electrons. Using design flexibility offered by our detector fabrication technique, such electron collecting detectors can also be easily fabricated by using a p^+-Si substrate and growing p-CdTe, n-CdTe successively on the substrate to make n-CdTe/p-CdTe/p^+-Si heterojunction diode structure [17]. Our detector fabrication technique further open new possibilities of integrating the detector array and the read-out electronics into the same silicon substrate, making a large-area monolithic array system.

However, to utilize the full potential of this technology, further improvements in CdTe crystal growth as well as device fabrication are needed to obtain detectors with highly uniform and low values of dark currents. As shown in Fig. 2, there is a variation in dark current distribution among the pixels, where pixels from the upper half portion of the array exhibit higher dark currents. Our previous investigation of the dark current distribution of an array showed that variation of concentrations of Te and Cd precursors at the growth surface was responsible for the dark current variation [14]. Hence, arrays with low and uniform dark currents can be achieved by making the concentrations of these precursors uniform throughout the growth surface [16]. On the other hand, dislocations in the CdTe layer are also a source of the dark current. These dislocations are generated due to the large difference in the lattice constants (~20%) and in the thermal expansion coefficients between the CdTe and Si. To decrease this dark current, dislocation density in the CdTe should be minimized. This can be achieved by subjecting these n-CdTe and p-CdTe to thermal annealing during the crystal growth [18]. The average dark current of this array is about 1 $\mu A/cm^2$, which is higher than that of our previously reported value of 0.5 $\mu A/cm^2$ at 50 V bias [16]. This may be due to the increased surface leakage currents. Contrary to our present detector, our previous detector arrays had larger size pixels isolated electrically from the surrounding pixels by making deep trenches [14], [16]. Such isolations make them less susceptible to surface leakage. Decrease of surface leakage currents of these fine-pixel arrays can be expected by application of surface passivation. All these investigations can be easily performed during our crystal growth and the detector fabrication process and are under progress.

Finally, we present an interesting result obtained from one of our arrays that was fabricated during early stage, when the array fabrication process was yet to be optimized. The result shown in Fig. 6 is an X-ray image of a bar-pattern, which reveals an important relationship between the crystallographic alignment of CdTe layer to the Si substrate. In the figure, several white straight lines corresponding to pixels with high dark currents are observed. These lines are aligned mutually at 60° on the CdTe surface. These white lines are generated due to cleaving of (211) CdTe layers which occurred on (011) and its equivalent planes of (101) and (110). Since the cleaving is a characteristic of single crystal, these lines show that the CdTe layer is single crystal. However, no cleaving lines could be detected on the CdTe surface with microscopic observation, which suggest that the cleaving has been occurred in the CdTe internally. Moreover, as seen on the figure, one of the white lines on the CdTe surface is aligned parallel to the wafer edge of Si substrate which is aligned to [0-11] direction. This result confirms that despite a large (about 20%) difference of lattice constants between CdTe and Si, CdTe layers grow epitaxially on the Si substrate, where each [0-11] and equivalent directions are parallel. Although X-ray diffraction (XRD) measurement of these thick CdTe layers clearly shows they are (211) orientated single crystals, however, their exact crystallographic alignment to the Si substrate could not be determined by XRD. Because X-ray used in the XRD measurement is mostly absorbed in the top surface layers of CdTe because of its high X-ray absorption. Hence, this is the first confirmation of crystallographic alignments of thick (211) CdTe layers grown on (211) Si substrates by MOVPE.

The internal cleaving of CdTe crystal may have been caused by some undesirable mechanical stresses resulted due to inadequate wafer handling during array processing. Also, residual tensile strain in the CdTe crystal may be another reason that enhanced the cleaving. By optimizing fabrication process as well as by improving the crystal property, internal cleaving of the crystals has been eliminated in our current arrays.

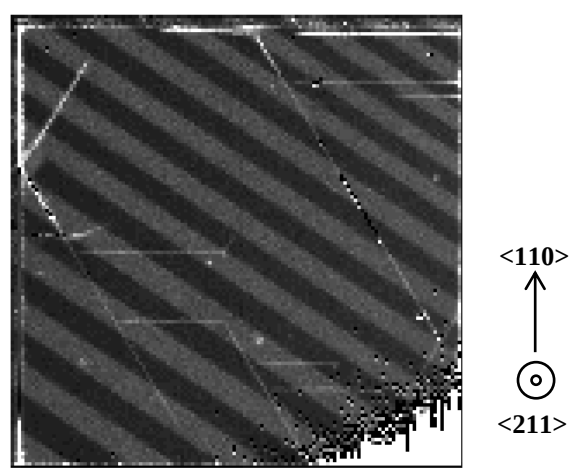

Fig. 6. X-ray image of a bar pattern obtained with one of our earlier (128x128) pixels imaging arrays. White lines in the image corresponds to pixels exhibiting larger dark currents.

V. Summary

A new technique of developing a large-area fine pixel X-ray imaging sensor using epitaxially grown thick single crystal CdTe layers on Si substrate is presented. The sensor consists of a p-CdTe/n-CdTe/n^+-Si heterojunction diode structure grown successively on the n^+-Si substrate. An array of (128x128) pixels were formed on the p-CdTe side, where each pixel is 60 μm^2 in area with a 80 μm pixel pitch. The detector array was bump-bonded to a charge integration type CMOS read-out ASIC. The basic performance of this sensor was evaluated by measuring the array dark currents, X-ray generated current, as well as spatial resolution and taking the X-ray images of objects. The results presented here demonstrate that this detector fabrication technique is very promising for developing high spatial resolution X-ray imaging sensors. Furthermore, discussion on the growth orientation of CdTe on the Si substrate based on X-ray imaging data is also presented. The result suggests that the grown CdTe is single crystal with crystallographic alignment exactly parallel to the Si substrate.

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