Single-Stage Three-Phase Differential Inverter Utilizing Single-Ended Primary-Inductor Converters

By

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A thesis submitted for the degree of Doctor of Philosophy

Graduate School of Engineering

Department of Electrical and Mechanical Engineering

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To Whom IT MAY CONCERN

We hereby certify that this is a typical copy of the original doctor thesis of

Mr. Ahmed Shawky Mohamed Hussein

Thesis Title:

Single-Stage Three-Phase Differential Inverter Utilizing Single-Ended Primary-Inductor Converters

(SEPIC コンバータを用いたシングルステージ三相差動インバータ)

Official seal of the institute

Declaration of Originality

I, at this moment, certify that the final developed research reported in this thesis and the thesis itself was composed and originated entirely by myself in the Graduate School of Engineering, Department of Electrical and Mechanical Engineering at the Nagoya Institute of Technology.

Ahmed Shawky Mohamed Hussein

Dedication

To my beloved father,
To my dear mother,
To my sweetheart wife, Omnia,
To my darlings, Hana and Youssef,
To my beloved sister, Heba,
To my beloved Brothers, Hussein and Mohamed,
To the spirit of my dear brother Abdel-Rahman,
To all members of my family,
Those people's love is always the source of my motivation.

Abstract

In recent years, the world is moving toward Renewable Energy Sources (RES) to produce clean and efficient energy and reduce global warming introduced by CO2 emissions. RES provides power to vast numbers of residential, commercial, and industrial customers using the utility grid's transmission lines. Among many exciting RES types, Photovoltaic (PV) has proven its competencies for many fundamental reasons. Grid-connected applications are becoming more popular due to fast PV penetration and new architectures, such as PV module architectures. This success has been stimulated by a considerable cut in PV installed price of PV modules, storage batteries, inverters, and other controllers.

DC-AC inverters are among the most critical parts of the PV module architectures. They are vital players for successful operation by converting the Direct Current (DC) power of the PV to Alternating Current (AC) power needed by the grid. Many categories of inverters with different ratings were proposed in the last three decades. Single-phase inverters are conventional in many applications, such as centralized, string, and micro-inverters. However, this solution has many severe problems, such as the double-line frequency component and its electrolyte capacitors. This issue disturbs the normal connection between the PV modules and the grid. Nowadays, three-phase micro-inverters are the best topology to solve double-line frequency. The balance between DC and AC power exists, and no electrolyte capacitors are required.

This project surveys many three-phase inverters topologies for grid-connected applications. Between dozens, single-stage differential-based inverters have been selected. Differential inverters replace every leg of traditional VSI inverter with a DC-DC converter. This configuration gives many properties such as single-stage, modularity, and isolation using isolated DC-DC converters. One DC-DC converter's connection per phase provides the inverter's uniform operation and enhances power density. It facilitates the power extension (scalability) by adding parallel converters without adding control complexity. They have step-up/down voltage gain with bi-directional power ability by utilizing the appropriate DC-DC converters.

This project contemplates a single-stage three-phase isolated differential inverter utilizing Single-Ended Primary-Inductor Converters (SEPIC). The SEPIC includes two power

switches, one inductor, a single High-Frequency Transformer (HFT), and two small Film capacitors. This low number of components produces a compacted and cheap inverter. According to differential characteristics, each SEPIC converter possesses one-third of the total power. Therefore, small components with low power ratings are utilized. The SEPIC converter has the lowest energy storage of passive elements. Finally, it provides voltage isolation and continuous input current with no extra components.

The project develops a simple control strategy for injecting active power at the utility grid. It is depend on the d-q synchronous frame and achieves little Total Harmonic Distortion (THD). The Negative Sequence Harmonic Component (NSHC) is a common issue in differential inverters and generating from the circulating currents between the DC-DC converters. That is because the alternating output voltage is greater than the input DC voltage. A NSHC detection circuit has been proposed by adding a three-stage Low Pass Filters (LPF) to mitigate this issue. The proposed controller's feasibility with NSHC compensation is proven by using a real-time Power Simulator (PSIM). Finally, a simple DSP board has been programmed for the proposed control because it has a small computational burden.

The project also develops a three-phase Modular Differential Inverter (MDI) by utilizing three SEPIC converters per phase. It processes a triple power by using identical nine SEPIC converters. A mismatch of ±20% in each SEPIC converter parameters has been investigated to confirm the inverter performance and its modular feature. The proposed MDI utilizes the proposed control strategy without extra circuits. Finally, the proposed inverter utilizes Silicon Carbide (SiC) MOSFET devices for better operation at a high switching frequency. A laboratory prototype validates the proposed inverter with 200V grid-side voltage, 100V DC, 1.6kW, and 50 kHz switching frequency.

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In the name of Almighty ALLAH, the Most Gracious and The Most Merciful. I would like to explicit my profound thankfulness and recognition to ALLAH for granting me the blessings to do this project. With the help and permission of ALLAH, I achieved many things, including this thesis. Indeed, without the relief of ALLAH, nothing is carried out. Many most profound blessings for Prophet Mohammed (Peace be upon him) because he guides us for ALLAH. We ask ALLAH to help us to follow his message and get forgiveness in the hereafter.

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Ahmed Shawky Mohamed Hussein

15-12-2020 Nagoya, Japan

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Acronyms and Abbreviations

DC	Direct Current
AC	Alternating Current
RMS	Root-Mean Square
EIA	Energy Information Association
TWH	Tera Watt Hour
Co2	Carbon Dioxide
RES	Renewable Energy Sources
PV	Photo Voltaic
EPIA	European Photovoltaic Industry Association
VRE	Variable Renewable Energy
IOT	Internet of Things
EV	Electric Vehicles
DG	Distributed Generation
MW	Mega Watt
KW	Kilo Watt
VSI	Voltage Source Inverter
MPP	Maximum Power Point
MPPT	Maximum Power Point Tracking
DMPPT	Distributed Maximum Power Point Tracking
MIC	Module Integrated Converter
MII	Module Integrated Inverter
CMV	Common Mode Voltage
EMI	Electro-Magnetic Interference
HFT	High Frequency Transformer
LFT	Low Frequency Transformer
THD	Total Harmonic Distortion
SiC	Silicon-Carbide
GaN	Gallium-Nitride
ZVS	Zero-Voltage Switching
ZCS	Zero-Current Switching
ZVZCS	Zero-Voltage Zero-Current Switching
PWM	Pulse Width Modulation
SPWM	Sinusoidal Pulse Width Modulation

ZSI	Z-Source Inverter
ST	Shoot Through
SCVD	Switched-Capacitor Voltage-Doubler
ANPC	Active-Neutral-Point-Clamped
SEPIC	Single-Ended Primary-Inductor Converter
NSHC	Negative Sequence Harmonic Component
CMS	Continuous Modulation Scheme
DMC	Discontinuous Modulation Scheme
MCMS	Modified Continuous Modulation Scheme
POL	Point-of-Load Converter
PFC	Power Factor Correction
PI	Proportional Integral
PID	Proportional Integral Derivative
PR	Proportional Resonance
LPF	Low Pass Filter
BPF	Band Pass Filter
PCB	Printed Circuit Board
PSIM	Power Simulator
RHP	Right-Half Plane
LHP	Left-Half Plane
MDI	Modular Differential Inverter
IPOP	Input-Parallel Output-Parallel
DSP	Digital Signal Processing
FFT	Fast Fourier Transform
UPS	Uninterruptible Power Supply

Chapter 1: Introduction and Literature Review

1.1 Overview

Many technological applications have been introduced and enhanced in daily world environments, from Nano-technologies to massive industrial technologies to simplify human life. These applications are very hungry for energy, especially the electrical energy type, which is considered the easy-facilitated source of current world energy. According to international energy reports, specifically from Energy Information Administration (EIA), as depicted in Fig. 1.1, the world net electricity generation increases from 21.5 to 26.3 TWh between 2012 and 2020. It will increase to 69% by 2040 due to the fastest consumption of many end-users. Also, it considered the steadily grown energy demand for many decades [1].

Historical and current electricity production systems are predominated by fossil fuels such as coal, oil, and gas in addition to nuclear power, as illustrated in Fig. 1.1. Unfortunately, fossil fuels are running out very fast due to the excessive use of several societies [2]. Also, the produced carbon dioxide (CO2) introduced by fossil fuel consumption presents a high percentage of greenhouse gas emissions and have a severe environmental impact. It increases the earth's temperature and imposes many other challenges, which are considered essential in the debate about world climate change [3]. Nuclear power is hazardous and needs a very high level of security. This oversized issue interprets the noticeable world transition from this type of energy to alternatives having a low risk.

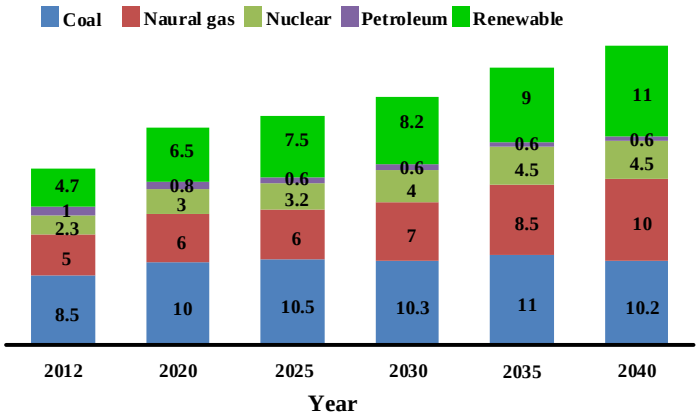


Figure 1.1: World net electricity generation (TWh) and its expectation until 2040.

Although the energy sources mentioned above have been used for a long time, previously adverse effects need a significant and concerted transition to a promising alternative. Political and economic communities all over the world highlight and follow this trend. Renewable Energy Sources (RES) are considered an excellent alternative energy sources, as feasible in Fig. 1.1, because of its unlimited resourcing and being eco-friendly [4]. RES sources include biomass, wind, solar, tidal, and geothermal. Although RES development is still expensive, its electricity production has increased rapidly. The maximum global capacity for RES-based power plants, residential plants, and other installations raised from 1223 GW to 2532 GW between 2010 and 2019 [5]. It is foreseen that the generation capacity estimation of RES will rise to 60% by 2040 per global energy outlook developed by the European Photovoltaic Industry Association (EPIA) [5].

The RES share in developed countries like Japan is fascinating. Fig. 1.2 illustrates the total RES generation, including self-consumption, using different types in the period 2014:2018. Between 2017 and 2018, it boosted from 16.4% to 17.4%. The japan policy aims to increase this rate to 24% by 2030 [6]. That is why fossil fuel percentage has decreased from 81% to 78% in the same period, which is still high and needs consequential decisions. Solar Photovoltaic (PV) power generation has grown three times, specifically from 1.8% to 6.5%. Furthermore, Variable Renewable Energy (VRE), comprising Solar PV and wind power, stepped up to 7.2% in 2018, with only 6.3% in 2017. It is worth noticing that biomass and wind power also improved electricity generation by 2.2% and 0.7%, respectively.

On the other hand, RES types such as Hydro and geothermal power still have constant power generation capacity. Hydropower is restricted now and reached its saturation point because of the limited locations on rivers and waterfalls to build new stations and generate more power. Furthermore, building additional dams harms climate change all over the world.

By area, 30% of Japanese RES-based generation capacity comes from Tohoku Electric Power and Hokuriku Electric Power. In addition to Shikoku electric power, Kyushu Electric Power raised the VRE portion to 12% in 2018. In the whole world, the RES share of power generation has risen annually by more than 30% in many developed countries, especially in Europe. For the USA, RES generation capacity exceeded 11% in 2018.

Finally, Germany targeting one-hundred percent of its electricity generation from RES in 2030[7].

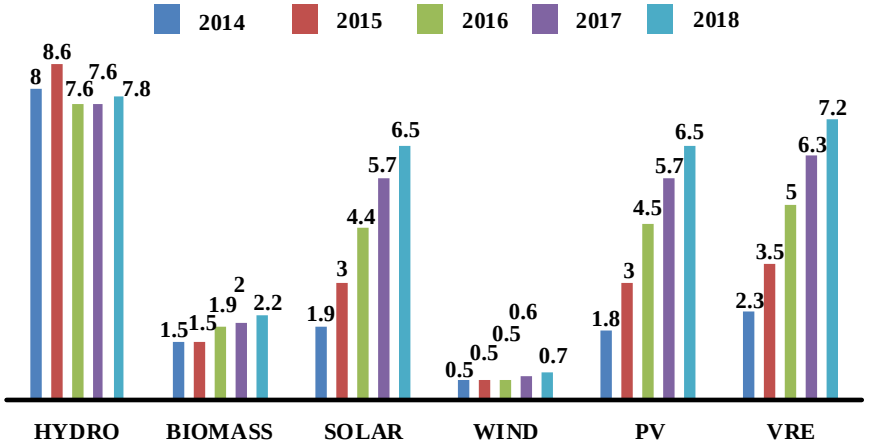


Figure 1.2: Percentage of RES share at Japan using many types from 2014 to 2018.

It is worth noticing that, among many types of RES, PV solar power units are earning more concern due to (a) clean and pollution-free technology, (b) great return on investment, and (c) abundant availability. Its promising features have augmented, in these days, by extensive research efforts that decrease components' cost, maximize power conversion efficiency, and boost overall reliability and stability. Moreover, the research efforts drive the strength of the market and industry. The projection of world electricity generation based on PV systems will increase to 300% in the next 20 years, according to the EPIA outlook 2017 [5]. Moreover, globally installed PV capacity increased by 16.6 GW in 2010 with a 131% increase from the year prior. Nearly seven times the amount (2.4 GW) was established in 2007 [8]. According to the EPIA, the leading country of cumulative installed PV capacity is Germany [5].

All this success is stimulated by a considerable cut in PV installed price of PV modules, storage batteries, inverters, and other controllers [9]. The price of installed residential and commercial PV systems decreased from 12 to 4.3 €/W during 2000–2014. The PV module prices fell from 4 to 1.02€/W for the same period and will decrease to about 0.03$/W in the next five years [7]. Storage elements that are incorporated in standalone systems improved the overall system performance by solving unpredictable outputs of PV sources [8–10]. The current edge applications, like the Internet of Things (IoT), distributed generations (DGs), and electric vehicles (EVs), force more improvements and cause

rising concerns [11, 14].

On the other hand, the grid-connected PV architectures are more convenient than standalone systems due to cost reduction and higher capacity, as shown in Fig. 1.3. Compared to standalone systems, the residential systems' price decreased to 9, 8.5, and 8.5€/W for the USA, Japan, and Germany. The storage feature, with its additive cost, is not required [15]. In 2018, the price decreased to unprecedented values less than 4€/W. The lowest price is for Germany with 1.2€/W. Moreover, it was 2.3 and 3.3€/W for Japan and the USA, respectively. The noticeable higher prices for PV systems in Japan and the USA in the 2007:2010 and 2014:2016 periods respectively result from local currency exchange, not the advancements in PV systems. For example, at this time, the federal tax of USA customers compounded to 30%. Fortunately, after this period, the PV prices went down again as it has for a long time. Motivated by this, much research has sophisticated to decrease prices by investigating and discussing grid-connected PV architectures' merits, especially the crucial part, the inverter [16].

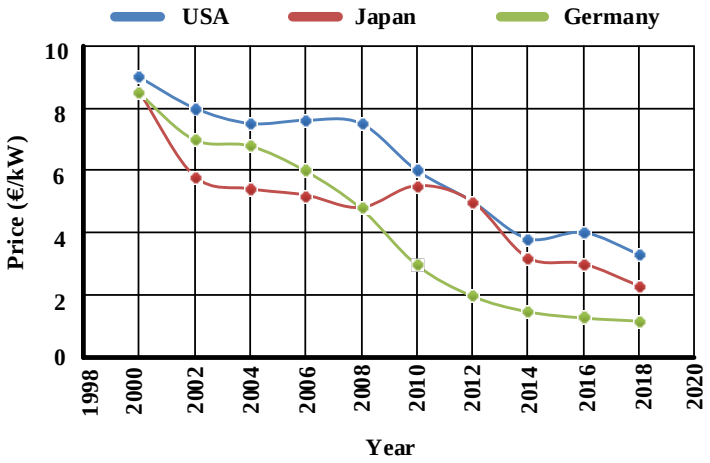


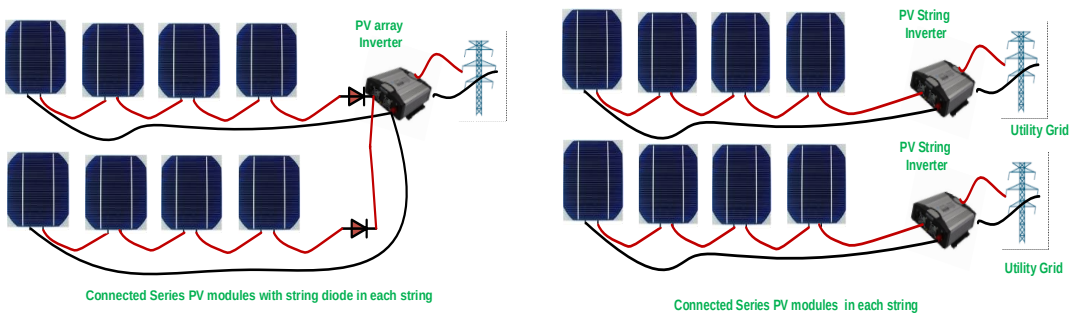
Figure 1.3: Price of residential grid-connected PV systems of 2000-2020.

1.2 Traditional and Recent PV Architectures

PV's power plants provide power to vast numbers of residential, commercial, and industrial customers by using the utility grid. Up to 2009, most grid-connected PV architectures have built at a small level. They have linked to the distribution utility grid. The established PV system in Florida connected to transmission level (230 kV) draws the world's attention to a higher power scale [17]. This PV architecture is known as

centralized PV architecture, as shown in Fig. 1.4-a. The PV modules are linked in series to construct a PV string with sufficient output voltage. Many PV strings are paralleled to attain the desired power levels. A DC-AC centralized inverter is linked to transform PV DC power to appropriate AC power. This inverter rating in the Mega Watt (MW) scale and uses a three-phase grid. Moreover, classical Voltage Source Inverter (VSI) topologies were used for many years in this architecture because the voltage gain is unnecessary [18]. However, the PV array's partial shading conditions disturb the Maximum Power Point Tracking (MPPT) control and diminish the total DC voltage for the PV architecture. Non-regular disturbance at tracking the actual Maximum Power Point (MPP) is possible when partially shadowing is existed. It is introducing different local MPPs and mismatches between PV modules [19]. This architecture also needs high-voltage DC cables among the modules and the inverter, which can undergo a single failure point and make the whole PV system unable to operate. Also, this requires string diodes to mitigate circulating current between strings. The reduced DC voltage was solved by integrating a DC-DC boost converter among the centralized inverter and PV to step-up the voltage. However, the other mentioned drawbacks still existed and may violate the performance of this architecture.

String architectures utilize a Distributed Maximum Power Point Tracking (DMPPT) concept to enhance overall performance. This concept was performed by separating the PV array into different strings. It effectively deviated the string diodes. An individual MPPT controller and inverter are then applied to every string, as shown in Fig. 1.4-b. Therefore, partial shading and module mismatching problems were significantly reduced in this configuration [19].



a- Centralized architecture b- String architecture

Figure 1.4: Traditional PV system architectures.

By doing this, the PV architecture efficiency increases about 1–3% larger than the central inverter [20] because the losses generated from string diodes and string mismatch losses have mitigated. Commonly, the power capacity for one string is 5kW. The modularity of the system facilitates system expansion by adding more strings. Moreover, inverter per string enhance system reliability and increase flexibility. However, the total produced mismatch losses between PV modules at every string is not critically detected. Therefore, they cannot be removed in this PV architecture [16–20].

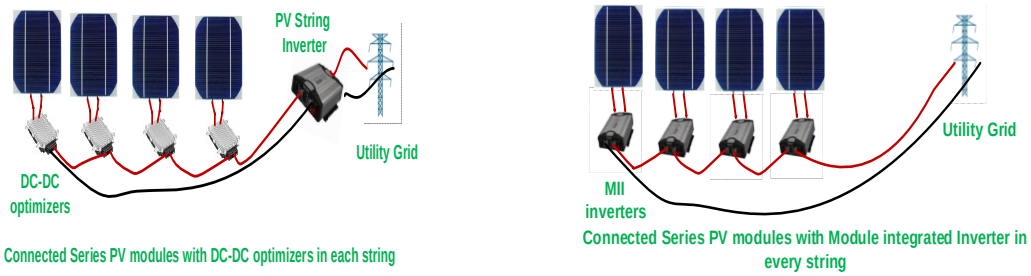
In addition to partial shading conditions and introduced mismatch losses in traditional architectures, its purpose is limited to energy harvesting's high power scale. Also, it needs customers to live close to centralized power plants to save power transmission costs. It adds new challenges because some customers live far away, which needs long transmission lines and introduces high power loss. In contrast, the DG system has smaller, decentralized sources that generate electricity much closer to those who use it. There are many producers, and even though they produce less individually (kW scale), they are all connected to the grid. Several technologies form the backbone of a DG system [21].

As the PV generation efficiency and power quality are a fundamental issue for PV architectures, many trials and improvements have been made to remove traditional architectures' main drawbacks. Therefore, the PV module architecture, which has recently been proposed, is the optimal solution. It completely mitigates the mismatch losses between modules by using DMPPT per module, as shown in Fig. 1.5 [22]. It has the following features:

- ✓ Low cost powered by mass production.
- ✓ High modularity and simple design.
- ✓ Easy integration at DG systems
- ✓ Minimum installation time due to easy plug-and-play feature.
- ✓ Low mismatch losses.
- ✓ High safety without hazardous high voltage DC cables.

This architecture has two different configurations: MIC and MII [23–27]. Module Integrated Converter (MIC) utilizes a DC-DC converter having an internal MPPT controller for every module. The required high DC bus voltage is then provided by connecting many MICs in series. Then the interface between the PV side and utility grid

is physically implemented by a string inverter. The exciting feature of this configuration is the similarity with the string PV architecture. It uses the string inverter but adds a DC optimizer for every module. It is worth noticing that MIC is popularly called DC optimizer in much literature works [25]. It completely disconnects between the PV modules and reconnects them via DC optimizers on the DC bus. It completely decouples the mismatched modules, and the shaded modules inject less current than unshaded ones. Form the cost point of view, this architecture is significant to replace the traditional string inverters without redesigning and integrating the DC optimizers.



a- MIC configuration b- MII configuration

Figure 1.5: Advanced PV module architectures.

The second configuration performs the individual PV module power directly by Module Integrated Inverters (MII). Here, an inverter with its MPPT controller per PV module removes the DC bus and decreases previous configuration costs, leading to flexibility and scalability. This configuration is known as AC PV modules in many research and industrial societies because it can attach MII in the PV module's backward, as shown in Fig. 1.6. It produces a PV module with AC output power [23].

Figure 1.6: AC smart PV module.

These days, it is clear that the DMPPT concept achieved in the recent PV modules adds many advantages. The reduction of PV modules for each inverter diminishes the mismatch losses from one side. It increases system modularity and plug-and-play operation for PV architecture expansion or periodic maintenance on the other side [27]. This promising feature makes the researchers move further than this by developing PV sub-modules and PV cell architectures [82-29]. It is useful for low-power applications, rather than electricity harvestings, such as portable devices and IoT applications. These applications, in general, are exposed to many severe levels of partial shading.

However, specifically for energy harvesting, optimization between the number of PV modules and inverters is necessary because it is tightly reflected upon the overall system cost. Moreover, it depends on the level of partial shading conditions. The PV architecture's feasibility depends on two interconnected factors: the total cost and partial shading level. When the partial shading level is small, that may happen in many conditions, the mismatch losses between two closet PV modules are negligible. This situation draws the attention to connect one or two or even three modules per inverter to make a significant cost-based architecture. To make a flexible solution, researchers and designers proposed micro-inverters in many research pieces of literature [30]. Technically, it worth mentioning that the micro-inverter becomes more general and flexible than the MII. It’s because the former is independent of the PV module ratings and has utilized several PV modules. On the other hand, MII has utilized only one PV module, making it restricted to specific scenarios.

1.3 Micro-inverter topologies

As mentioned above, Micro-inverters are considered the central fatal processing units in recent PV module architectures due to its high feasibility for performance and cost [30]. Single-phase inverter topologies are dominant in this direction. They have witnessed extraordinary market success, such as Solar Bridge, SMA, Enecsys, and Enphase inverters [31-32]. Moreover, single-phase inverters' voltage gain capability using isolated and non-isolated converter topologies has been discussed and classified [33-37]. Different connection configurations of single-phase micro-inverters have been also introduced to improve the overall efficiency and grid features [30]. However, single-phase inverter

topologies has two crucial technical drawbacks.

1.3.1 Double-line Frequency Component

In this topology, the DC power of one or more PV modules supplies the inverter's DC side. It achieves the maximum power operation by using MPPT controllers. However, a double-line frequency harmonic component is introducing at the inverter's input. The source of this component is the discrepancy among the PV modules' instant DC power, and the AC delivered single-phase sinusoidal power. This component is the main issue to develop the smooth operation of MPPT controllers and inverter control. The straightforward solution is to integrate a high storage element between PV modules and inverter for decoupling this component. A bulky electrolyte capacitor forms this balance by filtering the resulting double-line frequency form the inverter input.

Unfortunately, this capacitor is the central defect because it has a short lifetime. The lifetime of capacitors is inversely proportional to its capacitance. To get the same decoupling power capability, increasing the voltage at the electrolyte capacitor location decreases the required capacitance and allowing small values. This technique replaces the electrolyte capacitor with a reliable film one, such as film capacitors. However, using a dedicated film capacitor with a long life needs an additional circuit called a decoupling circuit to increase the voltage [33].

For Example, Fig. 1.7 shows a single-phase VSI inverter with an additional leg and small capacitor. In addition to a small film capacitor, this leg is responsible for decoupling the double-line frequency component from the DC side [38]. There are many types of decoupling circuits. It depends on the decoupling circuit location such as the PV side, DC link side, and AC side. Also, it was discussed and covered by several literature reviews [33, 34]. However, this circuit adds more challenges for control and the general performance of single-phase micro-inverter topologies. Also, all their trials introduce additional components as well as additive costs.

1.3.2 Limited power scale

All accomplished single-phase inverter topologies have been limited to small-scale single-phase (110 and 120 AC voltage) residential and commercial PV installations [39-40]. With time, customers getting more significant energy loads with more powerful

energy consumption. Large air conditioners and pool heaters are some of the famous examples. Also, electric vehicles have become more familiar for many customers and need high-power-rated inverters for quick charging. For this reason, many homes will need a three-phase configuration by providing three live wires instead of one wire in a conventional single-phase configuration. Although three multiple single-phase inverters are recently used to perform three-phase power, it has many complications, especially the power balance.

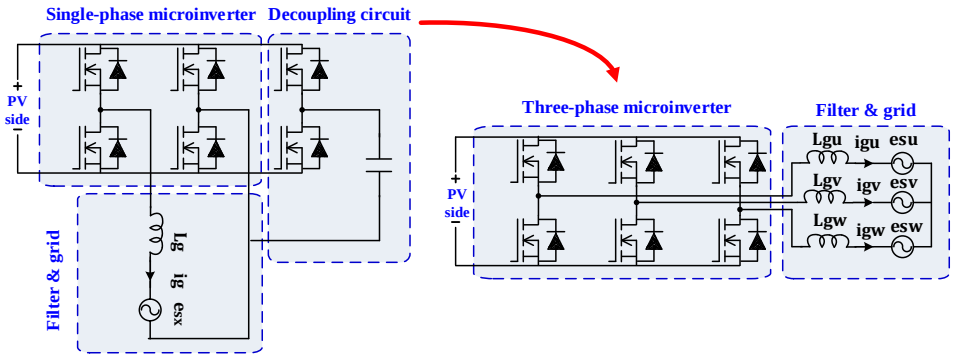


Figure 1.7: Comparison between single-phase micro-inverter with decoupling leg and three-phase micro-inverter.

1.3.3. Why Three-Phase Micro-inverters

The previous drawbacks draw attention to three-phase inverter topologies. As illustrated in Fig. 1.7, the single-phase having the decoupling circuit has the same component counts as a three-phase micro-inverter. Moreover, the third leg processes additional power in the three-phase micro-inverter instead of the decoupling function in the single-phase one. This solution avoids the expense of less reliability (electrolyte capacitors) and more system complexity (decoupling circuits) [33-34]. Furthermore, three-phase micro-inverters based on identical modular three legs (photo 2) have more straightforward control and are the most preferably used ones. Three-phase micro-inverters also have the following advantages [39-40]:

- ✓ The electrolyte capacitors' presence provides low voltage ripple components on the PV side, DC link voltage, and the grid where the double line frequency component is disappeared.
- ✓ This exciting feature opens the way for small and low-cost film capacitors to damp

only the high switching frequency harmonics and expand the PV module architecture's life and reliability.

- ✓ The low voltage ripple enhances the tracking efficiency of the MPPT controller.
- ✓ Multiple units are not required due to the inherent three-phase balancing feature.
- ✓ Reduction of cost using a single three-phase micro-inverter contrary to three single-phase units in high power purposes.
- ✓ It is naturally controlled through a three-phase central power system operation having symmetrical operation between all phases.
- ✓ For homes, the single-phase appliances are feeding on one active phase. Large loads such as electric cars are connected at all three-phases.

1.4 Standards, and requirements of three-phase micro-inverters

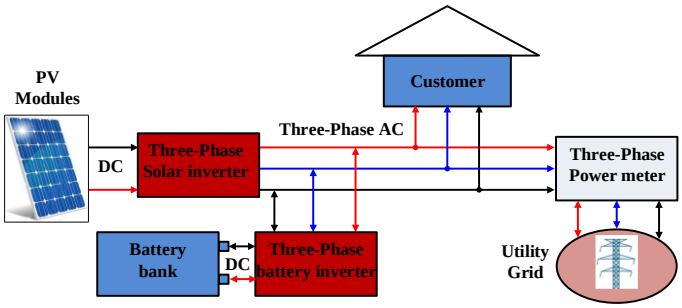
Fig. 1.8 shows the possible implementation of three-phase inverters at residential PV systems. The system's main parts are the DC side (PV or Battery) and the AC side (utility grid). Both of them have specific standards and requirements to process power simultaneously. Besides, the utilized micro-inverters should have some specific performance points such as small size, low cost, and high efficiency.

It is worth noticing that, as shown in Fig. 1.8-a, there are two independent three-phase inverters. The first process the power of PV modules. It needs high voltage gain and efficiency and unidirectional power capability. The second three-phase inverter, for the battery bank, processes the power in both directions.

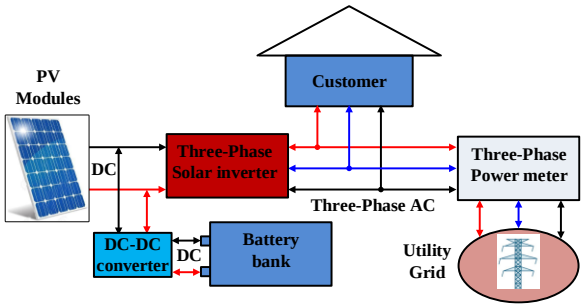
The interest of this configuration is the flexibility and low power ratings of both inverters. It raises the grid voltage during the discharging state of the battery and decreases commonly happening inverter tripping. It is useful only when the exported battery power more considerable than the PV modules' power. Moreover, the battery saving across all phases and mitigate phases unbalance.

Fig. 1.8-b shows the second configuration, which is cheaper than the first one. It uses a bidirectional DC-DC converter instead of the battery inverter. Therefore, the power connection is shifting to the PV DC side. However, this configuration increases the rating of solar PV inverter and needs bidirectional power processing capability. Per EIA standards, the PV modules, battery, and the grid's feature requirements are concerns

during the inverter topology selection and the design process for both configurations [1]. The required functions for each system part are summarized below.



a- First configuration of three-phase inverters



b- Second configuration of three-phase inverters

Figure 1.8: Possible implementations of three-phase inverters.

1.4.1 Required Features of PV Modules (DC Source)

In general, the PV modules are nonlinear energy sources with a V-I curve highly dependent on the irradiance and temperature. For energy harvesting optimization, The PV modules require to be operated at MPP with high tracking efficiency and zero leakage current by using MPPT controllers. Many MPPT controllers have been developed [40-44]. Whatever the presented micro-inverter topologies, the MPPT optimization degree depends on the following factors:

- ✓ High tracking efficiency: This is accomplished using micro-inverter topologies with continuous input current and has minimal input voltage and current ripple. There is an inverse relationship between MPPT tracking efficiency and input PV module ripples.
- ✓ Robust dynamic response: This factor depends on the control performance rather than the selected topology. This important factor can be easily implemented using simple

inverter topologies that possess a plain control technique.

- ✓ Low processing power and low execution time: This defines the chosen control boards for the selected inverter topology and the computational burden, defining the system cost and reliability.

In contrast, Low voltage PV module architectures employing transformer-less micro-inverter topologies are exposed to grounding issues [45]. That is why the distance between customer and PV modules is even closer. Using high-frequency switching and in the presence of the parasitic capacitance among the PV module cells and the ground introduces a leakage current which cannot be neglected.

This leakage current produces Common-Mode Voltage (CMV) on the PV modules resulting in many severe personal safety concerns. It accumulates the architecture losses, minimizes the grid-connected current quality, and stimulates severe radiated Electro-Magnetic Interference (EMI) [46].

There are two main concerns related to CMV, the common-mode loop path, and the source of CMV. However, many papers studied CMV reduction in non-isolated topologies of micro-inverters [30, 47, and 48]. The CMV has not been mitigated at most because the common-mode is highly dependent on switching patterns, inverter operation, and design. Therefore, High-Frequency Transformers (HFT) integration can cut the common mode loop path. Therefore, isolated topologies of micro-inverters are very reliable in reducing CMV [49].

1.4.2 Required Features of Grid Side

The rapid growth of the grid-tied PV-based micro-inverters and its influence on the grid performance must have addressed. Many national and international standards, such as IEEE 519-2014 and IEC 61727, are certified to evaluate micro-inverter performances. One of the most critical characteristics of micro-inverters is the injected power semblance. This semblance has been assessed by the Total Harmonic Distortion (THD) of the grid current. THD is disturbed through the harmonic distortion of the synchronized voltage on the grid and the harmonic emission on the PV side. The maximum value of the allowed THD is 5%. On the other hand, the inverter power and THD relationship must be considered for full optimization [50]. The THD usually increases when the inverter operates in light load [51].

The mismatch of output AC voltage components produced by micro-inverters can introduce a massive DC current injection. Well-designed micro-inverters must prevent this current and its destructive effects under satisfied limits, especially for transformer-less topologies. The DC current injection limit in IEEE 1547 standard is specified to be lower than 0.5% of the injected grid current [52].

1.4.3 Required Internal Features of Three-Phase Micro-inverters

First, the module PV architectures must have a small capacitor between the PV modules and the selected three-phase inverters to support PV characteristics. Moreover, it provides smooth DC voltages with tiny voltage ripples. However, some inverter topologies introduced reflected harmonics to the PV side due to its switching pattern and its inherent characteristics. These harmonics, especially the low-order harmonics, violates the system performance and needs additional capacitors in between. Three-phase topologies such as flying-capacitor multi-level and some Z-source inverter topologies are examples of these types of topologies. However, the integrated bulky capacitors used by these kinds of topologies have a small lifetime. The combined issues such as heat dissipation, humidity, and overcurrent deteriorated these capacitors' whole performance. Therefore, these topologies are not good options in PV module architectures.

Second, the step-up voltage gain in grid-tied micro-inverters is necessary because most commercial PV modules' DC voltage is lower than 40 V. Traditionally, cascaded two-stage or multi-stage micro-inverter topologies are proposed to solve this issue [19, 20]. The first stage is responsible for boosting the PV voltage using boost DC-DC converter topologies. Switched-inductor and switched-capacitor converters have proposed to generate high gain DC-DC boost converters [53]. The Voltage multipliers and the coupled inductor based boost converters are other topologies that have also been proposed to widen the voltage range and improve flexibility [54]. Typically, the second stage is an inverter to invert the DC voltage to a high-quality AC voltage. The main advantage of the two-stage structure is the flexibility of the controller design. However, the inverter's efficiency and reliability are relatively low due to multiple power processing and the high components count, which introduces increased system cost and complexity.

Recent advancements of single-stage inverter structures are preferred. They are highly

used to reduce the overall cost and complexity [55]. These single-stage structures not only perform voltage boosting, but they also can perform AC conversion. Unfortunately, these single-stage systems suffer from complicated control algorithms, sometimes requiring software rather than the hardware implementation.

Third, voltage isolation in the selected micro-inverter topology is essential to cut the CMV under acceptable limits. For safety purposes, a Line Frequency Transformer (LFT) is integrated among inverter and utility grid at traditional PV architectures. LFT is bulky, costly, and may pose efficiency challenges, especially for advanced PV architectures [56]. Therefore, compact HFT is considered a mandatory part of micro-inverters to achieve voltage isolation and provide additional voltage gain. HFTs perform bidirectional power isolation between PV modules and the utility grid, improving the overall system's reliability and providing more security for humans in the PV field. However, micro-inverters that utilize HFT have low efficiency and higher cost than transformer-less topologies [20, 39]. Therefore, using state-of-the-art technologies to integrate HFT into the next generation of micro-inverters are highly recommended considering these factors.

Fourth, as discussed before, the micro-inverters rating is between MII inverter and string inverters (100W-5kW, for example). So adding another PV module means more power. So if the selected inverter topology is capable of further extension or scalability, this will enhance the performance with less complexity. If not, the parallel connection of many inverters is the solution.

Fifth, increasing the micro-inverter's efficiency is vital because it has prominent and remarkable license access to PV industrial markets. Micro-inverters' efficiency depends on the characteristics of their inherent parts, such as semiconductor switches, passive elements, and switching strategy. It has recently shown that using advanced semiconductor technologies such as SiC and GaN switches can guarantee good performance and high efficiency [57–58]. Furthermore, the developing technologies in the passive elements are considered an added value for the inverter efficiency. Concerning the switching strategy, using high-frequency switching techniques and optimizing switching losses and conduction losses ratios improve the overall efficiency [59]. Also, soft switching methodologies such as Zero-Voltage-Switching (ZVS) and Zero-Current-Switching (ZCS) contribute significantly to improve inverter efficiency [60-61].

Finally, to push the market of PV-based three-phase micro-inverters, each part of the inverter should be investigated to reduce the overall cost. The micro-inverter cost in a PV system accounts for about 10% of the total cost [16]. The following factors positively define the overall cost of a micro-inverter:

- ✓ The number of components and their ratings.
- ✓ Low power loss and low heat dissipation will diminish heat sinks, which decrease the overall cost.
- ✓ Operating switching frequency because it determines the size and cost of passive elements.
- ✓ Power density improves the consumed Printed Circuit Board (PCB) area and its packaging technology.
- ✓ Type of the implemented controller: analog or digital, its effective MPP tracking, and the number of used loops can improve the overall system efficiency and related cost.

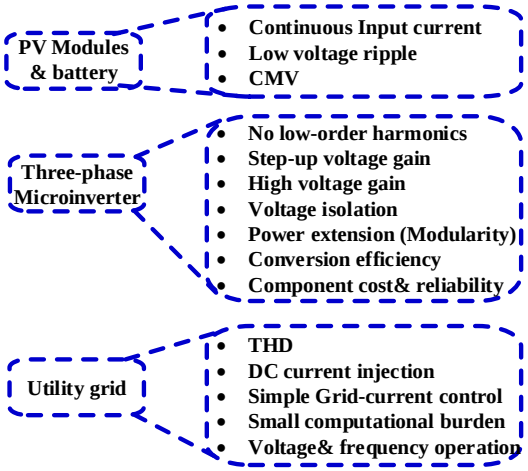


Figure 1.9: The critical parts of the three-phase inverters and their detailed features.

The field test data shows that the gap between micro-inverters' lifetime and the PV module is still large. Therefore, improving the reliability of PV inverters is a must. The micro-inverters failure effects on the overall PV system performance should be mitigated with modular and redundant topologies. Finally, Fig. 1.9 shows the list of all previously mentioned requirements.

According to previous discussions, three-phase micro-inverters' published topologies are presented and evaluated based on a new classification in this thesis. The simple topologies

that achieve a high percentage of previously developed standards and requirements are revised in detail among dozens of existing inverters. The developed classification has been used to identify the merits and demerits of the classified inverter topologies, according to Fig. 1.9.

A recommendation has then been given by selecting the differential inverters. This thesis also made a complete overview of the presented differential based inverters to find the best one. According to the previous overview, the Single-Ended Primary-Inductor Converter (SEPIC) carries many advantages that promote a well-functioning three-phase inverter. For this reason, differential inverter using SEPIC converters is proposed in this thesis for micro-inverter application. Furthermore, this thesis presents a novel grid-current control for achieving low THD and small computational burden. Besides, analysis and experimentation of a modular differential inverter, depend on many SEPIC converters, have also been proposed.

1.5 Thesis Objectives

Thesis objectives are shown in Fig. 1.10 and can be summarized as follows:

- Low-order Harmonic Components in the proposed SEPIC-based differential inverter; First, an in-depth mathematical model of negative-sequence harmonic component has been developed to know its source. Moreover, the effect of it on the output grid-current and DC side current has been investigated. Then, the parameters selection of the proposed SEPIC-based differential inverter is designed based on the developed model.
- Grid-current Control, in this thesis, two-loop based d-q synchronous fame grid-current control has been proposed. It has a simple structure and is easily validated at traditional DSP boards. In the first loop, PID, Type-II, and PI compensators are designed and implemented to achieve grid-current control and inject pure active power. The high-order of the SEPIC converters' open-loop transfer function needs rigid compensators for a stable and reliable performance. Therefore, better performance for the proposed inverter is achieved. The second loop utilizes a negative-sequence harmonic component detection circuit to mitigate it. This circuit is based on three-stage Low-Pass Filters. The performance of both control loops is

validated in simulations and experiments.

- A modular differential inverter is also proposed in this thesis for high power applications purposes. It incorporates many of the proposed SEPIC converters. The practical issues of differential inverter such as variable duty cycle, low order harmonics, and circulating power are presented during the design process. A mismatch in integrated SEPIC converters is also investigated to confirm the system performance. Moreover, a laboratory prototype of a simple modular differential inverter is provided to prove the authenticity of the proposed modular differential inverter.

1.6 Thesis Outline

The arrangement of this thesis is as follows:

Chapter 2 provides a well-supported detailed classification for the best three-phase inverter topologies between many dozens of published inverters. Single-input and multi-input inverter topologies using single-stage and two-stage conversion are evaluated and revised in detail. Differential inverters, Z source inverters, and Switched-capacitor inverters are an example of single-stage inverter topologies. Two-stage VSI is also discussed, especially for low power applications. In contrast, modular multi-level inverters and multi-input VSI inverter topologies are also presented. The component counts and voltage and current stress of screened topologies are compared. The final recommendation of using differential inverters in the rest of the thesis is selected and accompanied by micro-inverter application merits.

Chapter 3 presents a comprehensive analysis of the proposed SEPIC-based differential inverter. It includes the principal operation, modulation techniques, and differential inverters issues such as variable duty cycle, low-order harmonics, and circulating currents. A novel mathematical model is proposed to support this analysis. Then, the main advantages of the SEPIC converters is discussed. After that, a grid-current control is developed, where A PID compensator is designed to enhance the inverter's stability and compensate for the utilized SEPIC converters' phase-delay. A negative-sequence harmonic component detection circuit is introduced in the second loop of the developed control. The design details of passive elements and switching devices are also covered.

At final, the provided experimental, and simulation results prove the robustness of the presented control.

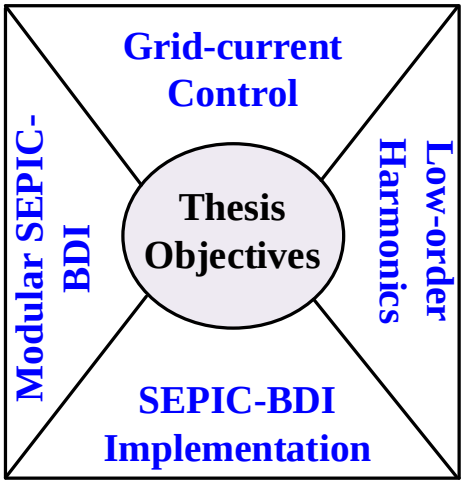


Figure 1.10: Objectives of the Thesis.

Chapter 4 presents a modified grid-current control, which is rigid for the proposed SEPIC-based differential inverter. The PID compensator is replaced with a Type-II compensator. This compensator is better due to its capability to eliminate the high switching harmonics of the proposed inverter. Therefore, it has successfully decreased the low-order harmonics and THD and showed its accuracy by satisfying the recent grid codes (<5%). Finally, a PI compensator is presented for the proposed inverter. The control burden is decreased and validates the usage of inexpensive DSP boards.

Chapter 5 presents the analysis and design of modular differential inverter based on nine SEPIC converters to process high power (three times of proposed one in previous chapters). The validation of the proposed inverter with mismatch parameters at SEPIC converters is investigated using numerical simulations.

Chapter 6 covers the thesis summary, influential contributions, and future ideas of the proposed inverter.

Chapter 2: Classification of Three-phase Micro-Inverter Topologies

2.1 Introduction

Traditional three-phase VSI topology is one of the most famous topologies which convert the PV power to pure sinusoidal AC power. In industrial markets of medium-voltage adjustable speed drives, the VSI design is reasonably efficient, has acceptable reliability with smooth dynamic response, and can run motors without de-rating. These promising features make it an excellent candidate to process the power between RES and grid using simple three legs, as shown in Fig. 2.1 [56]. It controls active and reactive power and injects AC grid-current with low THD.

The grid requirements, such as voltage isolation, are developed by adding LFT between RES and grid. For many years, this inverter was used in RES, especially in large-scale applications [56] because of the distinct advantages such as high efficiency, simple control, and easy implementation. However, in small scale RES connected to the grid distribution level (<5 kW), the new PV module architectures have independent PV modules with low input voltages [64]. Moreover, the partial shading scenarios force this voltage to be time-variant [63-65]. This characteristic of the new PV architectures introduces a voltage-gain limitation because the VSI AC output voltage is less than the PV DC voltage. The considerable size of LFT has additional limitations to inverter size and cost. Finally, VSI does not have continuous input current property.

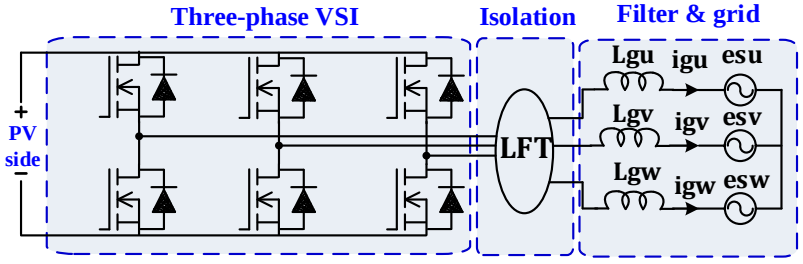


Figure 2.1: Three-phase VSI equipped with LFT for grid-connected applications.

Otherwise, the three-phase Current Source Inverter (CSI) provides a step-up output voltage with continual input-current, as shown in Fig. 2.2. PV modules supplied power behaved like a current source and is compatible with PV's inherent characteristics. Compared to VSI, the current of the CSI is controlled and limited by using input inductor [66]. The utilized switches are subjected to lower peak current due to the constant power supply. The CSI's negative link voltage capability enables the inverter to handle reactive or regenerative loads. However, it needs unidirectional switches composed of two switches and two diodes per leg and introduces additional components. The used DC inductor is relatively large to exhibit current source features. The large DC inductor also slows the current response. The load must be balanced; otherwise, the input current has high input harmonic components, making the input inductor size increase. Due to this disadvantage, the three-phase CSI is mostly used in three-phase high power RES applications.

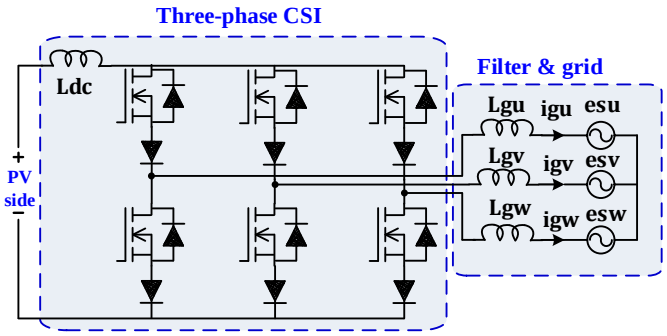


Figure 2.2: Schematic power circuit of three-phase CSI.

Although the traditional VSI and CSI represent an apparent success in many RES applications, previously mentioned properties have introduced many limitations. These limitations complicate their application in recent low-power PV modules architectures and their promising micro-inverter topologies. The voltage gain of both is still inapplicable. Galvanic isolation is still problematic. Adding another inverter with a parallel connection to the old one is the only solution for power extension or scalability. This issue needs a redesign of PV architecture and complicates its wirings.

Motivated by the problem statement mentioned above, many inverter topologies were proposed in the literature as candidate solutions. In between, the interesting topologies

for three-phase micro-inverters at PV module architectures have been classified as follows.

- Two-Stage VSI inverters.
- Single-Stage Z Source Inverters.
- Single-Stage Switched-Capacitor Inverters.
- Single-Stage Differential-Based Inverters.

2.2 Two-Stage VSI inverters

Three-phase VSI has a voltage step-down property. They are adding a boosting stage before VSI to provide the voltage step-up ability. It has a DC-DC boost or other boost-derived converters like buck-boost, isolated boost, isolated buck-boost, or full-bridge converters. In [67], a conventional boost converter is integrated with the three-phase VSI. The boost converter performs MPPT control and feed DC power, as demonstrated in Fig. 2.3. The presented system uses an adaptive DC link voltage by adjusting the reference DC link voltage based on the Common Point of Interconnection (CPI) voltage. The adaptive DC link voltage control helps in the reduction of switching losses. A feed-forward loop was also utilized to improve the dynamic behavior.

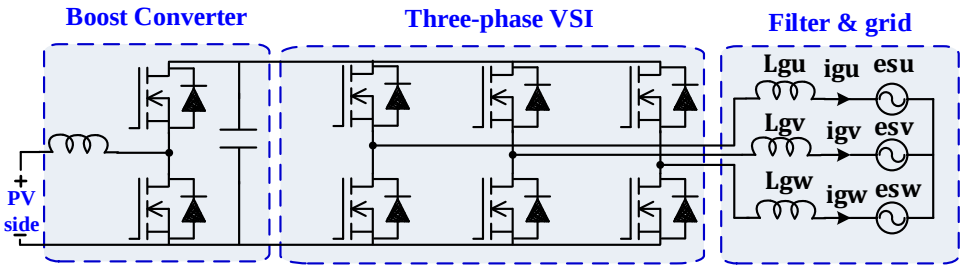


Figure 2.3: Three-phase two-stage VSI proposed in [67].

In [68], a two-stage three-phase grid-tied inverter was presented, as illustrated in Fig. 2.4. The presented ZVS technique improved inverter efficiency. The boosting stage is an LLC resonant DC-DC full-bridge converter with center point iterations MPPT algorithm. Full-bridge LLC resonant converter can sustain ZVS or ZCS operation for the full range of input voltages, improving the inverter efficiency. Moreover, the phase skipping control improve inverter efficiency under light load conditions. A triple loop control of ZVS is

also presented to guarantee the inverter's stability in PV applications [69]. Fig. 2.5 shows the two-stage three-phase VSI inverter proposed in [70]. The boosting stage is an isolated full-bridge DC-DC converter. The second stage is a three-phase VSI inverter. They used a soft switching technique based on Zero Voltage Zero Current Switching (ZVZCS) mechanism.

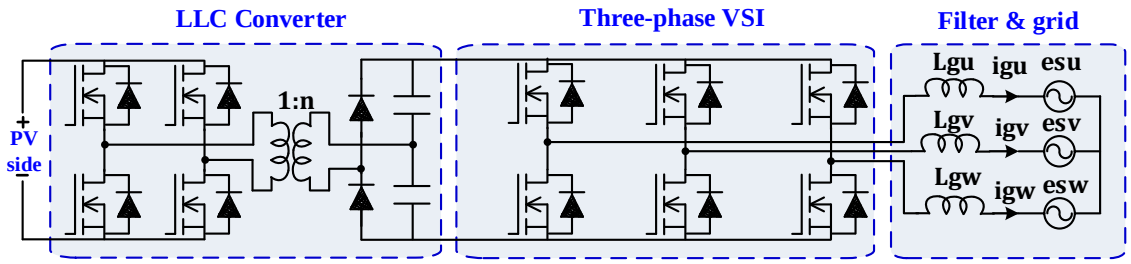


Figure 2.4: Three-phase two-stage VSI proposed in [68].

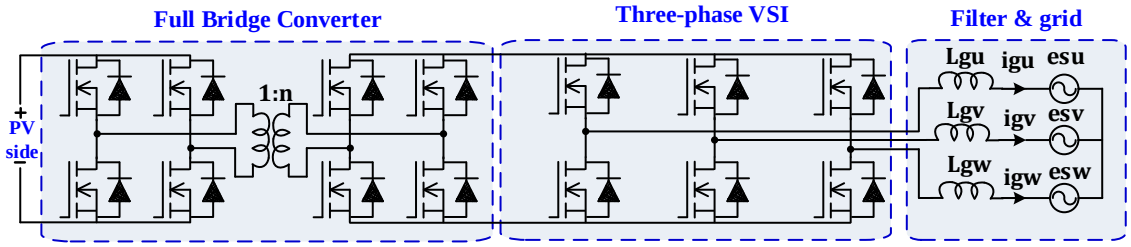


Figure 2.5: Three-phase two-stage VSI proposed in [70].

As shown in Table. 2.1, most previous topologies can perform MPPT with high tracking efficiency due to continuous input current. For topology V1, the DC link capacitor is only about $35\mu F$, so that the film capacitor has been utilized. For topologies V2 and V3, an electrolytic-less capacitor was still needed. For grid side, the reported THD is 5% for all. However, this topology needs DC link voltage control in addition to grid-current control. At the inverter topology, the CMV is reduced in isolated DC-DC converters. The component counts of these topologies is illustrated in Fig. 2.6. Although, V3 has the lowest number of components, overall component counts is still large.

On other hand, a multi-input three-phase VSI micro-inverter, shown in Fig. 2.7, is proposed [71]. It utilizes fewer switches per leg and reduces the component count and overall cost. The number of switches is reduced by one in each leg compared to traditional two-stage VSI. This topology's exciting feature is the power extension by adding PV and

its leg to the developed inverter. Moreover, each PV module stage's power extension is accomplished by using gate signals on the nearest two switches to the inductor. The middle switch in each leg is utilized for inverter operation. However, this topology still implement electrolyte capacitors. Moreover, it lacks voltage isolation.

Table 2.1: Performance characteristics of two-stage VSI topologies.

Topology		Power Rating kW	CMV	η	MPPT	Control	Switching	THD %
Fig./Ref	Boosting Stage							
2.3/67	V3 Boost	6.5	High	NR	INC	PWM	Hard	5
2.4/68	V1 LLC	0.4	Low	95.5%	CPI	PWM + ZVS	Soft	5
2.5/70	V2 Full Bridge	~1	Low	91.5%	-	PWM + ZVZCS	Soft	5

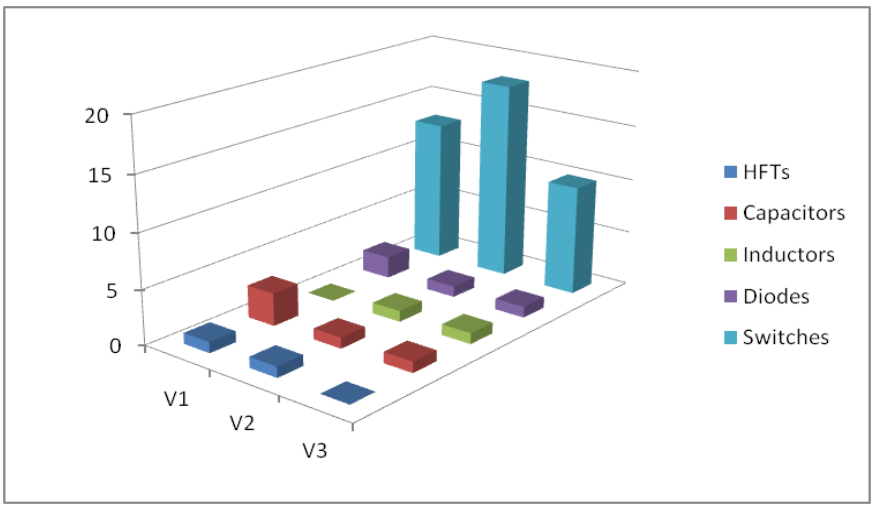


Figure 2.6: Component counts of three-phase two-stage VSI inverter topologies.

2.3 Single-Stage Z Source Inverters

Impedance Z-source Inverter (ZSI) is a single-input single-stage inverter with many interesting features. The ZSI can limit the VSI and current source topologies' problematic issues and provide a step-up voltage conversion solution. The classical ZSI has an extra circuit called the Z-network, as illustrated in Fig. 2.8. This network improves the inverter's features by increasing buck/boost conversion due to Shoot Through (ST) property. ST also eliminates the dead time required in conventional VSI topologies [72]. However, the classical ZSI topology has low voltage gain and high switching losses due to high voltage

stress. In the presented studies [73-74], different modulation techniques were proposed to increase the voltage gain without adding extra elements in ZSI power stage, enhancing the boosting capability over a complete range operation.

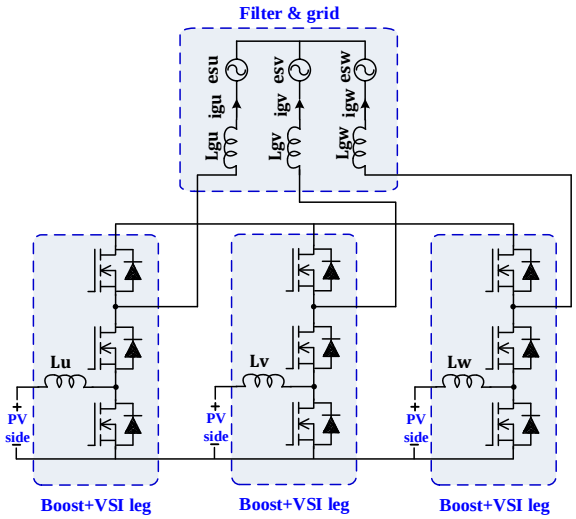


Figure 2.7: Multi-input three-phase two-stage VSI [71].

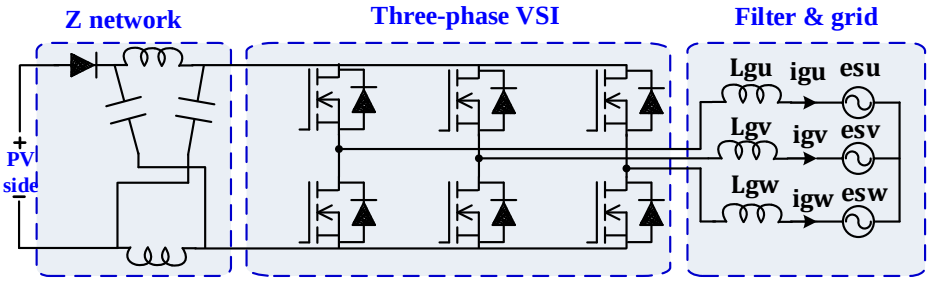


Figure 2.8: Classical three-phase Z source inverter.

In [75], high gain was achieved by defining the right choice of active vectors and ST states' placement. In this way, the voltage gain can be increased at high modulation indices. Also, with the inclusion of ST states, the number of switching is less, which results in low switching losses and low voltage stress, and the small size of the reactive components. Many topologies have been derived from classical ZSI (Z1) for micro-inverter applications, such as:

1. Z2-quasi ZSI (qZSI).
2. Z3- Inductor-based ZSI (L-ZSI) switched inductor (SL-ZSI).
3. Z4-Switched-inductor quasi ZSI (SL-qZSI).

4. Z5-Transformer based ZSI (Trans-ZSI).
5. Z6-Inductor-based ZSI (L-ZSI).

The qZSI topology, shown in Fig. 2.9, has the advantage of continuous input current, making it suitable for MPPT implementation of PV applications with high tracking efficiency. In [76], grid-current control depend on Finite Control Set Model Predictive Control (FCS-MPC) with reduced computation time had proposed.

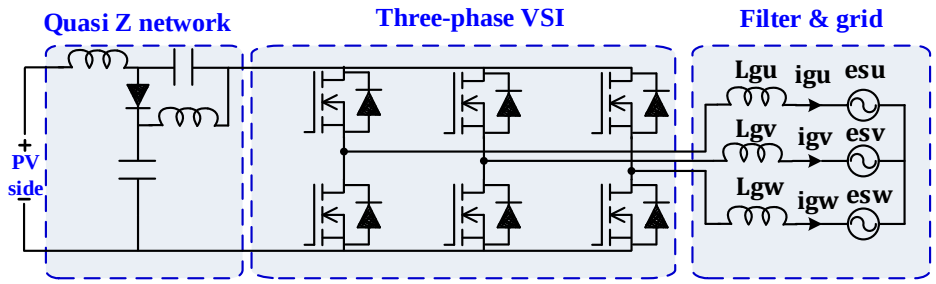


Figure 2.9: Structure of three-phase quasi Z-source invertor (ZSI) topology.

A modified ZSI (L-ZSI), involving only diodes and inductors for boosting the inverter's ratio, was proposed in [77] and is shown in Fig. 2.10. The L-ZSI is a modification on the SL-ZSI using fewer components. The proposed topology provides inrush input current suppression because no current flows to the start-up's circuit. It also provides a continuous input current with the common ground between PV modules and inverter.

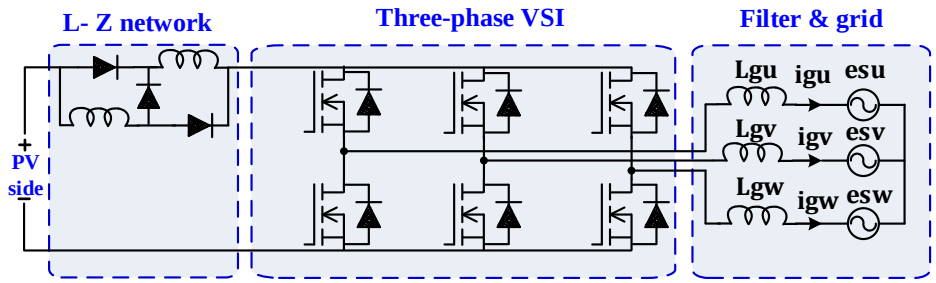


Figure 2.10: Power circuit of L-ZSI [77].

The trans-Z-source inverter topology utilizes the Z-network, a transformer, and a capacitor having reduced components count, as proposed [78]. Its circuit diagram is illustrated in Fig. 2.11. The voltage gain and stress are significantly improved using a transformer's turn ratio larger than one. Isolated Z-source inverter using HFTs is

presented in [79] for low voltage applications (Fig. 2.12). This isolated topology introduces extra components because the utilization of HFTs requires an additional power conversion stage.

On the other hand, four-leg quasi-ZSI was proposed in [80], as illustrated in Fig. 2.13. There, a Model Predictive Control (MPC) technique was used to overcome the drawbacks of the classical ZSI. MPC was used to control the load current and quasi ZS network capacitor voltage with high accuracy, leading to a fast response. The proposed controller handles each phase current independently. As a result, the proposed quasi ZS four-leg inverter provides fault-tolerant capability; for example, if one leg fails, the others can work usually. Finally, a three-phase four-leg inverter was employed to ensure the PV module architecture's reliable operation unbalanced load conditions.

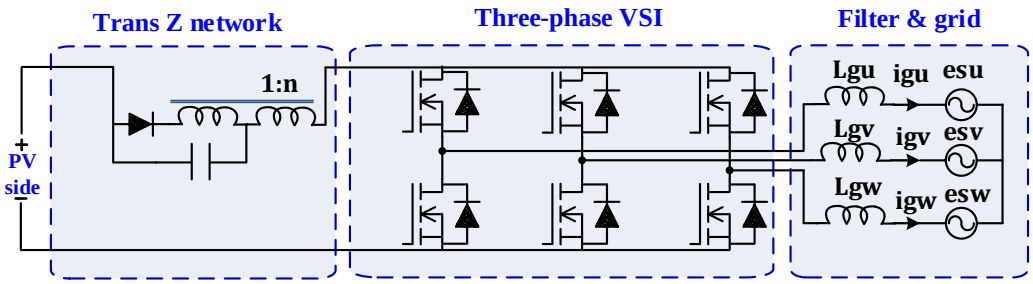


Figure 2.11: Power circuit of trans-ZSI [78].

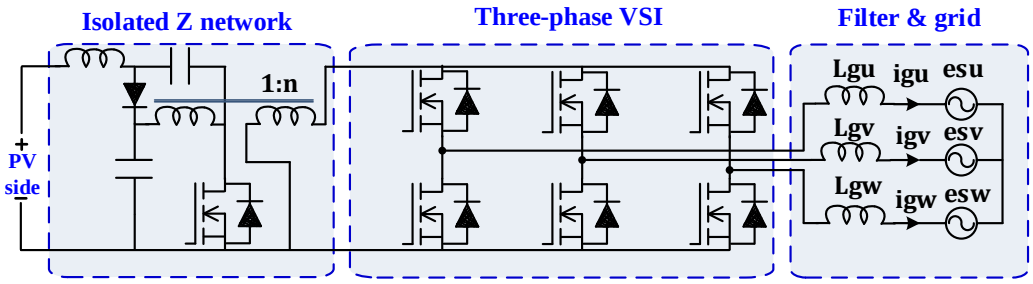


Figure 2.12: Power circuit of voltage fed isolated ZSI [79].

Table. 2.2 contrasts the previously discussed three-phase ZSI topologies, which are effectively utilized in micro-inverters. It is worth noticing that, for the high tracking efficiency of MPPT controllers, the continuous input Z-source micro-inverter topologies are preferred. CMV is highly reduced in isolated Z-source topologies, where, in non-isolated topologies, modified PWM is required. For high voltage gain, L-ZSI [77] and voltage fed trans-ZSI [78] are recommended. Fig. 2.14 presents the number of

components of each topology. Classical ZSI, L-ZSI, and QZSI have the lowest number of components, which decrease the overall cost. Table 2.3 shows the voltage stress of each topology. For a turn ratio equal to 1, all Z-source micro-inverter topologies have equal switch stress except L-ZSI. The same findings for capacitor stress except for Z3, which has no capacitors making it more reliable. However, the reported THD is 11% and 8.7% in [75] and [80]. Moreover, Isolated ZSI [79] has a high number of components. The Z network's capacitor was huge and requires an electrolytic capacitor. Finally, for qZSI topology and trans-Z-source topologies [76-78], this capacitor is still 25% larger than the electrolytic-less capacitor.

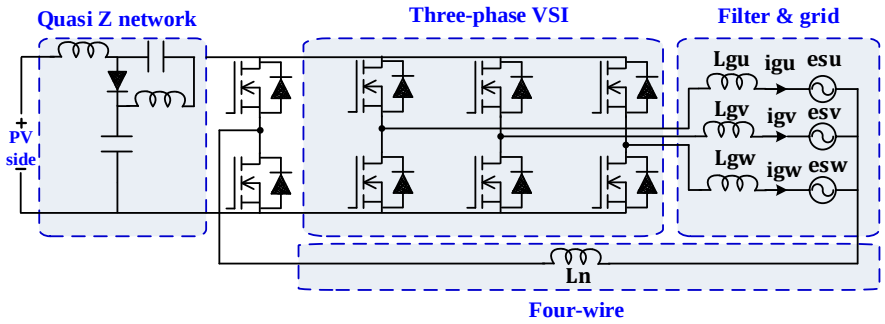


Figure 2.13: Power circuit of three-phase four-leg Quasi ZSI [80].

Table 2.2: Performance comparison for selected topologies of Z-source micro-inverters.

Topology		Power Rating kW	CM V	η	Gain $M * B * \frac{V_{dc}}{2}$	Control	Switching	THD %
Fig. Ref.	Solution topology							
(8) [75]	Z1 classical	0.26	No	NA	$B = \frac{1}{1-2D}$ $D < 0.5$	SVM	Hard	11
(9) [76]	Z2 qZSI	0.45	No	NA	$B = \frac{1}{1-2D}$ $D < 0.5$	FCS-MPC	Hard	NA
(10) [77]	Z3 L-ZSI	~0.15	No	NA	$B = \frac{1+D}{1-D}$ $D < 1$	Maximum Boost control	Hard	NA
(11) [78]	Z4 Tran-ZSI	NR	No	NA	$B = \frac{1}{1-(1+n)D}$ D < 0.5 $1-(1+n)D \neq 0$	Constant Boost control	Hard	NA
(12) [79]	Z5 I-ZSI	2.88	Yes	NA	$B = \frac{n}{1-2D}$ D < 0.5	Constant B 3rd inject	Hard	NA
(13) [80]	Z6 QZSI	~0.4	No	NA	$B = \frac{1}{1-2D}$ D < 0.5	MPC	Hard	8.7

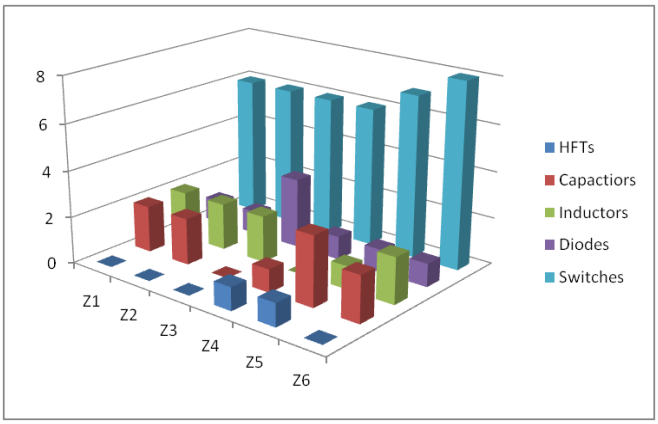


Figure 2.14: Analysis of components' count utilized in three-phase Z-source micro-inverter topologies.

2.4 Single-Stage Switched-Capacitor Inverters

In this topology, a switched-capacitor cell or circuit is used instead of the boost converters at two-stage VSI topologies. The principal operation depends on the capacitors charging in parallel then discharges the capacitors in series to magnify the input DC voltage. In [81], a Switched-Capacitor-Voltage-Doubler (SCVD) network is proposed. It includes two capacitors, two diodes, and two switches. Like boost converters, it is put between the DC and conventional VSI, as shown in Fig. 2.15. Space vector PWM is used to drive the additional two switches to reduce the CMV. In [82], a three-phase inverter utilizes a seven-level Active-Neutral-Point Clamped (ANPC) inverter instead of conventional VSI is presented. The switched-capacitor technique, which provides voltage step-up, is also developed, as illustrated in Fig. 2.16. ANPC multi-level inverter performs output voltage with a staircase voltage waveform, partially following a sine wave template. This technique leads to a low THD with high voltage levels and low voltage stress.

In [82], a single-stage boosting VSI topology is proposed. The voltage step-up is achieved using a magnetic integrated switching inductor-capacitor network. It includes an inductor, two diodes, and two-identical switching inductor-capacitor cells. The size of the magnetic circuit is reduced by magnetic coupling, as illustrated in Fig. 2.17. However, these topologies of switched-capacitor cells have many components, especially at the three-phase systems, and lack galvanic isolation and modular construction [83]. In addition to VSI, extra two switches and two diodes are added in topologies [81] and [82], respectively. Moreover, topology in [83] has 27 switches. Furthermore, it has many issues related to

the capacitors' mismatch and self-voltage balancing [84].

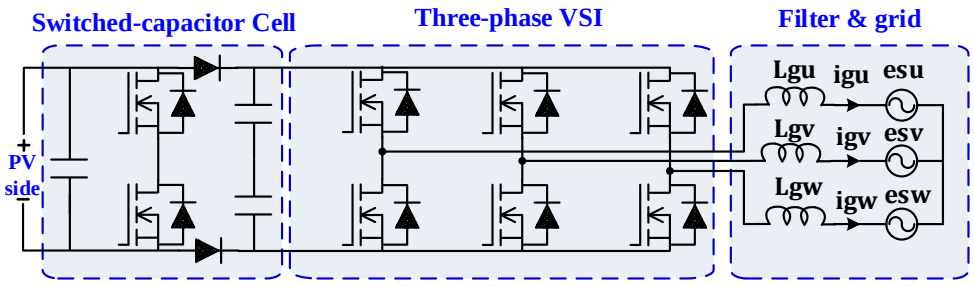


Figure 2.15: Switched-Capacitor based Inverter proposed in [81].

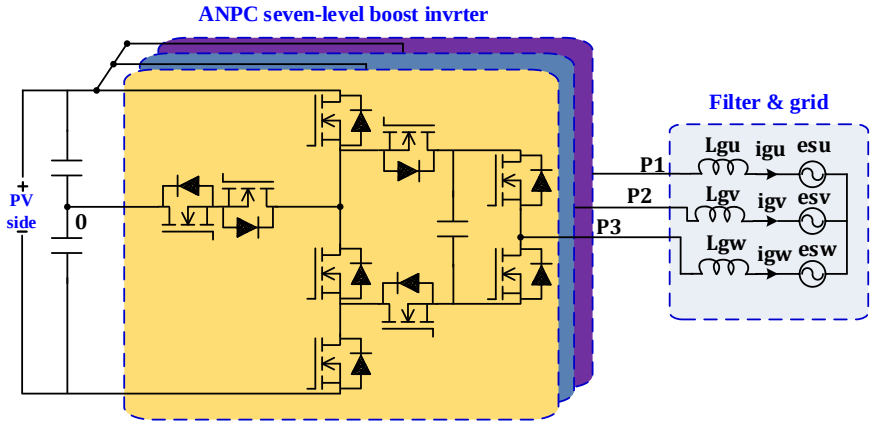


Figure 2.16: Switched-Capacitor based multi-level Inverter proposed in [82].

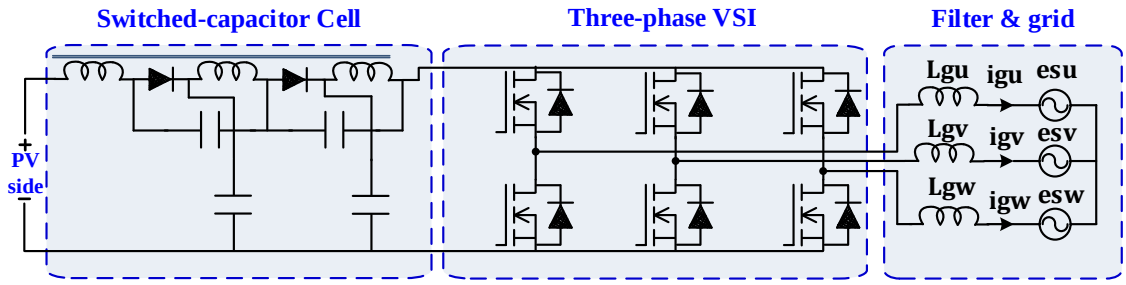


Figure 2.17: Switched-Capacitor-inductor Inverter proposed in [83].

2.5 Single-Stage Differential Inverters

Three-phase differential micro-inverters are single-input single-stage step-up/down topologies. They have high efficiency with a low number of components, hence yielding acceptable total cost and size. Moreover, these topologies can provide bi-directional power transfer. This topology's main drawback is the voltage stress resulting from the variable duty cycle operation and the circulating current produced from the differential

connection of converters. The schematic circuit of the differential inverter is illustrated in Fig. 2.18.

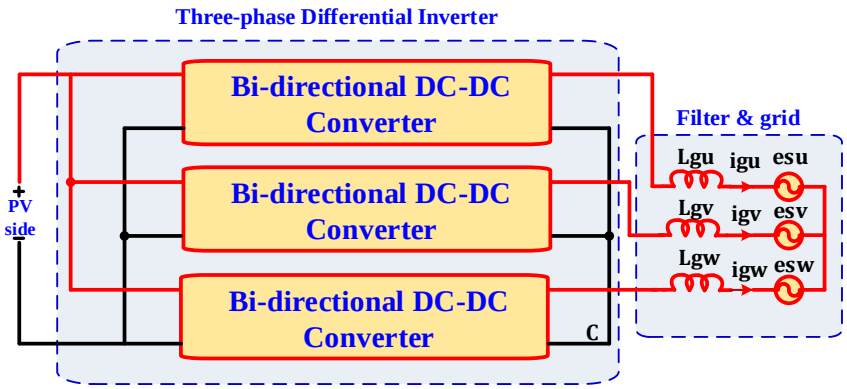
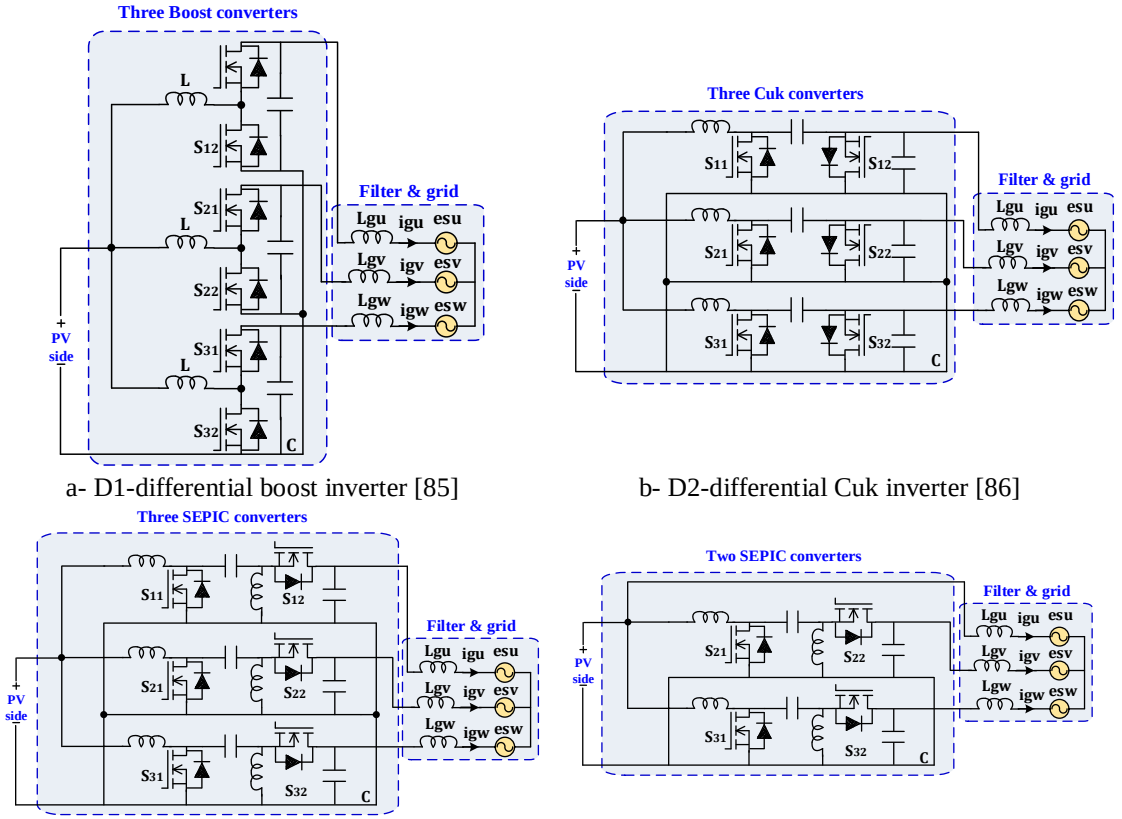


Figure 2.18: Schematic power circuit of three-phase differential inverter topology.

It composed of three DC-DC converters connected in parallel at the input and differentially at the output side. The three-phase output is produced using sinusoidal pulse width modulation (SPWM) with a 120 phase shift. This inverter can step-up/down the voltage using suitable DC-DC converters. The output voltages have both DC and AC components. The DC component values are equal for all phases, which introduce the voltage stress. It is canceled by the differential connection, while the AC component appearing on each converter's output voltage is combined to create the sinusoidal AC voltage of the inverter. The diverse characteristics of the DC-DC converters give rise to many differential inverters, as previously shown [85–110]. Fig. 2.19 and Fig. 2-20 show the various types of the non-isolated and isolated differential three-phase inverter topologies. The selected topologies are mentioned as D1 to D6. The PV modules with its MPPT are easily implemented with high tracking efficiency for DC-DC converters, which have non-pulsating input currents. For example, boost, SEPIC and Cuk converter topologies.

For CMV elimination, isolated DC-DC converters like Flyback, SEPIC, and Cuk converters are better. Otherwise, CMV elimination can be achieved by using proper modulation techniques. In buck-boost and boost converters, high voltage is effectively possible using a high duty ratio. In isolated topologies, the voltage gain is attained by the turn ratio of HFT in addition to the converter's duty ratio.



a- D1-differential boost inverter [85]

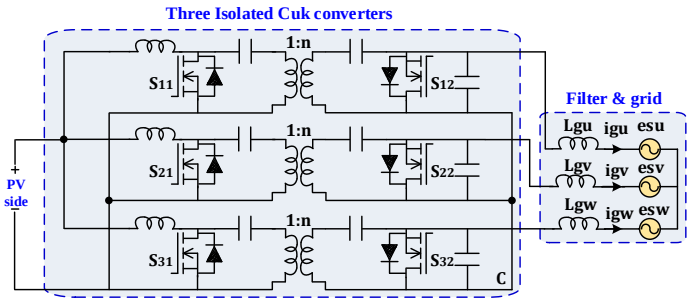
b- D2-differential Cuk inverter [86]

c- D3-differential SEPIC inverter [87]

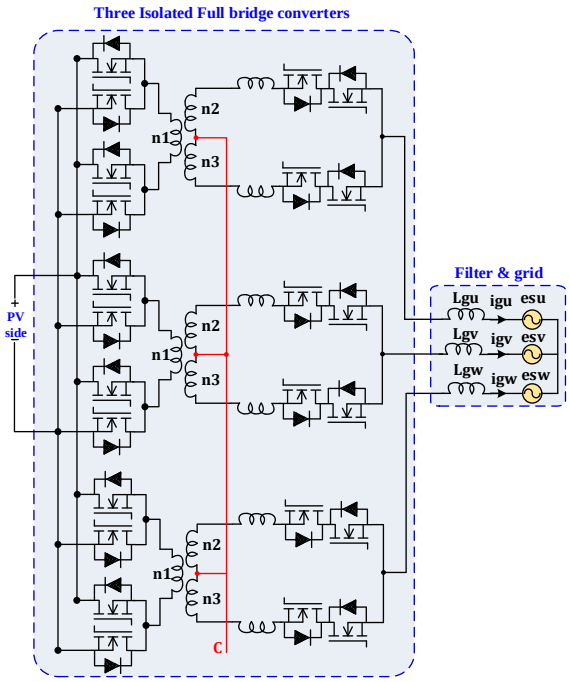
d- D4-differential based four-switch SEPIC [88].

Figure 2.19: Non-isolated three-phase differential inverter topologies.

Table. 2.3 details the comparison between different DC-DC converters, which are utilized in differential inverters. It is worth mentioning that all presented topologies are in the range of micro-inverters applications (0-5kW). The reported THD for most topologies is under 5%. As mentioned in chapter 1, this value is compatible with current grid standards. Both linear and nonlinear control methods were implemented entirely in many literature work pieces, reflecting the control function's simplicity. As mentioned before, the output of differential inverters has two different components; DC and AC. DC component is canceled on the grid side, but it increases the stress on the inverter switches. Therefore, Table 2.4 illustrates the voltage stress comparison for the selected topologies. It is worth mentioning that the buck-boost converter's topology is better from the component count and total voltage stress point of view. Between different isolated buck-boost converters, flyback and SEPIC converter is effective. Fig. 2.21 shows the component counts of the discussed topologies. The Full-bridge converter has many components. On the other hand, the four-switch SEPIC differential inverter topology has the lowest components count.



a- D5-isolated differential Cuk inverter [89]



b- D6-isolated differential full bridge inverter [90]

Figure 2.20: Isolated three-phase differential inverter topologies.

Table 2.3: Performance comparison of different DC-DC converters utilized at differential inverters.

Topology		**Power Rating kW**	**THD %**	**CMV**	**η**	Control	Mode scheme	Switching
Ref.	**Solution DC-DC**							
[85]	D1 (Boost)	1–1.5	6–7	High	NA	Sliding mode	CCM	Hard
[87]	D3 5 buck-boost	2.5	1.8	Low	95	3 control loops	CCM	Hard
[88]	D4 SEPIC	2	NR	High	NA	DI sliding mode	CCM	Hard
[89]	D5 Cuk	0.5	6	Low	93	PR + SLM FF control	CMS DMS	Hard
[90]	D6 Full bridge	NR	NR	Low	89	CSVPWM	CCM	Soft

Table 2.4: Performance voltage stress for selected topologies of differential inverters.

Topology		Switch A	Switch B	Capacitor A	Capacitor B
Ref.	Solution				
[85]	D1 Boost	$V_{dc} + 2V_{grid}$	$V_{dc} + 2V_{grid}$	--	$2V_{grid}$
[86]	D2 Cuk	$V_{dc} + 2V_{grid}$	$V_{dc} + 2V_{grid}$	$V_{dc} + 2V_{grid}$	$2V_{grid}$
[87]	D3 5 buck-boosts	$V_{dc} + 2V_{grid}$	$V_{dc} + 2V_{grid}$	V_{dc}	$2V_{grid}$
[88]	D4 SEPIC	$V_{dc} + 2V_{grid}$	$V_{dc} + 2V_{grid}$	V_{dc}	$2V_{grid}$
[89]	D5 Cuk	$nV_{dc} + 2V_{grid}$	$V_{dc}/n + 2V_{grid}$	$nV_{dc} + 2V_{grid}$	$2V_{grid}$
[90]	D6 Full bridge	$\sum V_{dc}$	$\sum 2V_{grid}$	--	$2V_{grid}$

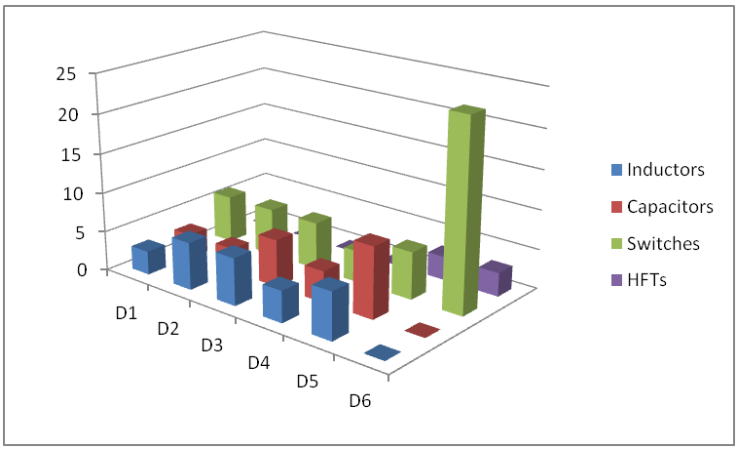


Figure 2.21: Components count utilized in three-phase differential inverters topologies [85–90].

2.6 Summary of the proposed classification

According to the previous discussion of possible best topologies for three-phase micro-inverters application at PV module architectures, the following statements are concluded:

1. The best topology at two-stage VSI topologies is LLC resonant DC-DC converter based micro-inverter.
2. L-ZSI is the superior topology at Z-source micro-inverters.
3. The best topologies of differential micro-inverters are HFT-based SEPIC and Cuk differential topologies.

In this thesis, the differential based inverters has been selected due to the following features [85-115].

✓ It provides two distinct features in one single processing stage; voltage boosting and

voltage inversion.

- ✓ Differential inverter topology having three DC-DC converters provides step-up/down voltage gain using their instantaneous duty cycle. Fortunately, many DC-DC converter topologies capable of operating on a wide range of duty cycles.
- ✓ The three DC-DC converters' symmetrical operation is implemented easily in single-phase, three-phase, or even poly-phase differential inverters. It just needs one or more DC-DC converter per phase.
- ✓ Isolated DC-DC converters, such as the SEPIC, flyback, and Cuk converters, have a small HFT. Therefore, the proposed differential inverter provides galvanic isolation and reduces leakage current, CMV, and Electro-Magnetic Interference (EMI).
- ✓ The HFT of isolated DC-DC converters is small because it works on the switching frequency. Furthermore, it can easily contribute to voltage boosting/bucking of the proposed differential inverter.
- ✓ In three-phase differential inverters, each DC-DC converter processes one-third of the inverter power and uses DC-DC converters with small passive elements, small rating, low energy storage, and high power density at low cost.
- ✓ This topology has bi-directional power capability due to DC-DC converters' symmetrical operation using the switches, which facilitates the same control.
- ✓ Simple two-switch-based DC-DC converters promote a low switches count (only six) and low-number of driver circuits that simplify the control structure.
- ✓ The redundancy of DC-DC modules topologies gives many opportunities for control robustness, low components counts, and overall system reliability.
- ✓ The research society has intensive work on DC-DC converter topologies, which get a reliable and efficient differential inverter.
- ✓ Unpretentious PWM modulation techniques such as space vector, unipolar, and bipolar modulations are easily implemented due to differential inverters' straightforward control functions.
- ✓ The simplicity of PWM circuits enables the control implementation of conventional DSP control boards. It decreases the complexity and inverter cost.
- ✓ Some DC-DC converters' continuous input current provides adjustable output voltage without electrolyte capacitor, especially for PV and fuel cell applications.

- ✓ DC-DC converters connection at differential inverters (input parallel, output differential series, or output parallel) has a modular configuration. It facilitates power extension by adding more modular DC-DC converters.

Chapter 3: Proposed SEPIC-Based Differential Inverter

3.1 Introduction

Currently, PV-based distribution systems have undergone numerous changes in their architectures. With more PV generation modules to the grid and the increasing use of the electric vehicles and its energy storage systems, it is requisite to adjust the power conversion between the various PV sources and the grid. It is imperative to use highly efficient and compact electronic inverters. For this purpose, this architecture requires an inverter with voltage step-up, which provides high efficiency and improves reliability and power density. However, besides modular construction, bidirectional power flow, and galvanic isolation requirements, these characteristics limit many possible existed inverter topologies.

According to the author's knowledge, differential inverter topologies achieve many of the requirements mentioned above efficiently due to their unique construction [85-110]. It appears as a star topology for the PV module architectures and its interesting inverter topologies. First, the differential inverter is a single-stage power circuit between many possible topologies. Second, it has a modular operation, galvanic isolation and bidirectional energy flow due to its simple construction established on isolated DC-DC converters.

A three-phase single-stage SEPIC-Based Differential Inverter SEPIC-BDI is proposed in this chapter. For galvanic isolation, it has three small HFT-based SEPIC converters. This chapter presents the differential inverter's principal operation, its SEPIC converters, and the PWM modulation. The proposed Modified Modulation Scheme (MCMS) provides static linearization for the duty cycle. It produces a grid output current free form low-order harmonics.

Furthermore, the Negative Sequence Harmonic Component (NSHC) is analyzed in detail. For this purpose, a novel mathematical model is presented. It investigates the NSHC source and its associations with the differential inverters characteristics, such as variable duty cycle, DC-DC converter unipolar operation, and circulating currents. The design process, analysis, and experimentation of the presented inverter are expressed. It includes

the parameters selection, its design criteria, small-signal modeling, and the proposed control technique. Finally, the proposed inverter's simulation and experimental results have been provided to validate its performance and workableness.

3.2 Proposed SEPIC-Based Differential Inverter (SEPIC-BDI)

Fig. 3.1 depicts the power schematic of the proposed single-stage three-phase isolated SEPIC-BDI. It utilizes three identical bidirectional isolated DC-DC SEPIC converters ($x = u, v, w$). It is worth noticing that x indicates the SEPIC converter and its related phase, connecting it with the grid, as illustrated in Fig. 3.1. All three SEPIC converters are supplied from the same input DC source at the input side (input parallel connection) and star-connected at the grid side. Every SEPIC converter has two MOSFET devices (main switch S_{mx} and synchronous switch S_{rx}), one input inductor L_x , one HFT with magnetizing inductance L_{mx}, and two film capacitors (coupling capacitor C_x and output capacitor C_{ox}). This low number of components diminishes the proposed inverter size and enhances the overall power density. Moreover, the utilized film capacitors have a long life-time and enhance inverter reliability. SEPIC converters' uniform operation enables inverter modularity with plug-and-play activity and can be extended to higher power without additional control circuits. The differential inverter uses bidirectional SEPIC converters to produce AC output voltage greater or smaller than the input DC voltage. This feature is essential in RES to the grid with wide range operating conditions.

Since the three SEPIC converters process the differential inverter power, each SEPIC converter's power rating equals one-third of the total inverter power. This exciting feature facilitates using small active and passive components with lower power ratings. It also reduces the size of the power stage. Moreover, the switches operate over one-half of the line-frequency cycle, decreasing the inverter power losses and improving inverter efficiency.

Between different DC-DC converter topologies [111-130], the SEPIC converter is selected in the proposed inverter because it has the following advantages:

1. DC-DC SEPIC is a step-up/down converter. It’s extremely utilized in many applications like RES [119, 122 and 130], Point of Load (POL) converters [113], DGs [117,120, and 124], and Power Factor Correction (PFC) [115, 127 and 128].

2. SEPIC converter provide galvanic isolation using small HFT [116].
3. It's a non-inverting buck-boost circuit and simplify the implantation of utilized HFT.
4. The input inductor of SEPIC converter validate continuous input current and prevent issues related to short circuit current [115, 124 and 130] .
5. The input inductor of SEPIC converter eliminates the large electrolyte input capacitor integrated between the PV modules and the inverter. This capacitor is used to decrease the switching ripples and reflected harmonics as discussed in Ch. 2.
6. The SEPIC converter has the lowest energy storage passive elements that enhance power density between many isolated buck-boost converter topologies [87, and 91].

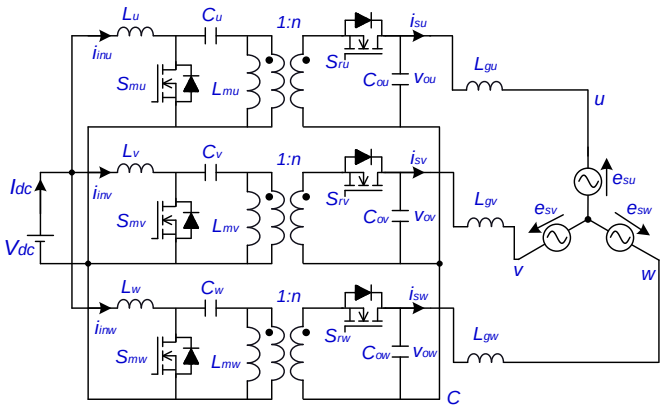


Figure 3.1: Proposed single-stage three-phase grid-connected isolated SEPIC-BDI.

3.2.1 Proposed PWM modulation Scheme of SEPIC-BDI

The unipolar operation of most DC-DC converters generates DC voltage even at a variable duty cycle. Since the differential inverter is constructed from three DC-DC converters, the PWM modulation should generate a sinusoidal output voltage imposed on a DC voltage component. This voltage can be issued using sinusoidal duty cycle d_x changing over the utilized DC-DC converter's operating range. The other two DC-DC converters' duty cycle is displaced with 120°, which in turn produces three-phase output voltages on the output terminals. The DC voltage components of all DC-DC converters are ideally equal. Therefore, they cancel each other at the output terminals due to the differential connection. Finally, the AC voltage components of all converters appear on the grid terminals and inject pure alternating currents.

This concept of modulation is called Continues Modulation Scheme (CMS). It is straightforward with quick implementation because the PWM of the conventional DC-DC converter circuits does not change. The PWM of DC-DC converters utilized at different applications such as POL converters and PFC circuits have the same configuration. In these applications, once the desired output voltage is expressed, the duty cycle becomes steady. It only changes at transient conditions and control compensation for the desired output voltage. For the differential inverter case, the duty cycles change continuously over the grid line-frequency cycle.

CMS PWM modulation, illustrated in Fig. 3.2, has been used in many differential inverter topologies [85, 88, 89, 91-103, and 108]. It drives the switches of the utilized DC-DC converters by a sinusoidal duty cycle modulated on the grid line-interval. It is given as $T_L = 1/F_{line}$. Where F_{line} represents the grid line-frequency. The utilized DC-DC converter switches must operate at a high switching-frequency to get higher power density. This is accomplished by obtaining a triangle signal operated at switching interval $T_s = 1/F_{sw}$. Here F_{sw} presents the switching frequency, as illustrated in Fig. 3.2. Therefore, the gate signals of the utilized DC-DC converter switches generate from comparing the variable duty cycle (operated at F_{line}) with the saw-tooth signal (operated at F_{sw}).

The originality of the CMS PWM backs to the conventional VSI modulation. The research society uses a sinusoidal waveform compared with the inverter modulation index. That is why CMS utilizes a variable sinusoidal duty cycle. However, this modulation is better for DC-DC converters that have similar characteristics to VSI. This modulation gives good results with differential inverters based on buck converters. The VSI inverter is a voltage step-down or bucking topology.

However, using this modulation with buck-boost DC-DC converters introduces a mismatch between the actual output voltage and its reference signal [86-87, 91]. The source of this mismatch is the dynamic behavior of the passive elements (such as inductors and capacitors), in the DC-DC converters, toward this modulation. Technically, this mismatch produce low-order harmonics such as third-order, fourth-order, and fifth-order components on the output terminals of DC-DC converters.

To solve this issue, additional controller loops at third, fourth, and fifth order compensators can be designed to mitigate its effect form the grid-current. However, this

solution is hard to implement because it disturb the stability of the inverter by limiting the overall bandwidth of the proposed control. Therefore, many linearization strategies have been developed in many works to mitigate the source of this mismatch. In [99-100], a Linearization strategy, between the static gain of differential inverter and its output voltage, is proposed for the boost and buck-boost converters based differential inverter.

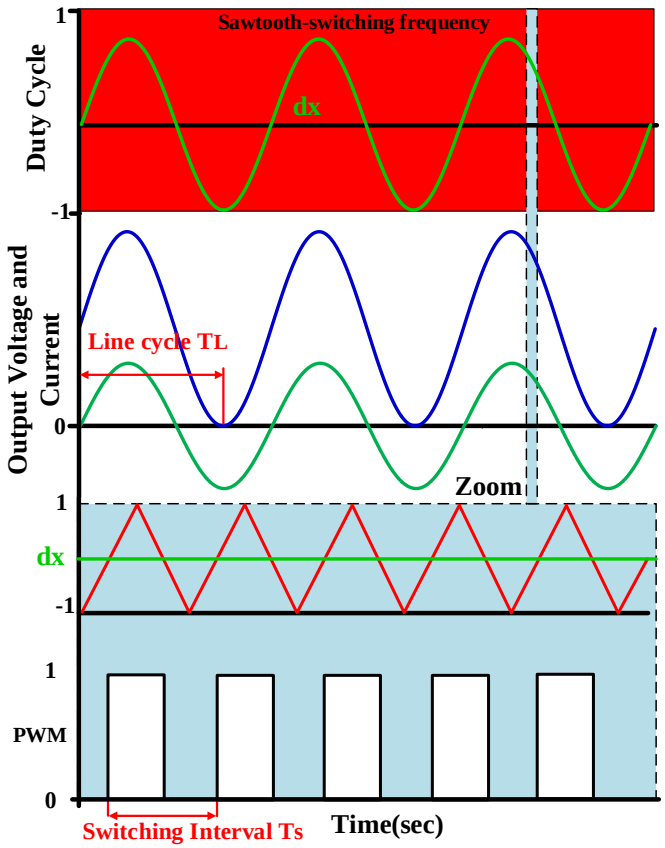


Figure 3.2: Continuous Modulation Scheme CMS of differential inverters.

Table 3.1: Voltage gain of different basic DC-DC converters.

Converter Topology	**Voltage gain** $\frac{V_{ox}}{V_{dc}}$
DC-DC Buck Converter	d_x
DC-DC Buck-Boost Converter	$\frac{1}{1-d_x}$
DC-DC Boost Converter	$\frac{d_x}{1-d_x}$

In contrast, this issue can be easily solved by comparing the characteristics of buck, buck-

boost as well as boost converters, which is based on the voltage gain as obtained in Table 3.1. It is worth noticing that all DC-DC converter's output voltage gain depends on the duty cycle and the DC input voltage. So the output voltage mismatch resulted from sinusoidal duty cycle can be easily mitigated by emerging the voltage gain of utilized DC-DC converters in CMS.

This step modulate the variable duty cycle to make it compatible with the utilized DC-DC converter. This proposal is developed in [86-87 and 89]. The voltage ratio of the utilized buck-boost converters is emerged in the duty cycle calculations. It is applied for five different three-phase buck-boost differential inverter topologies. In [89], it's developed by adding a DC voltage feedforwarding signal at three-phase and single-phase Cuk-based differential inverters.

Therefore, the proposed Modified CMS modulation (MCMS) which have duty cycle calculation of buck-boost SEPIC converter is presented in the proposed SEPIC-BDI. It is derived from the duty-voltage ratio of the SEPIC converter as:

$$d_x = \frac{V_{ox}}{V_{ox}+V_{dc}} \tag{3.1}$$

Fig. 3.3 illustrates the distinction between the conventional CMS and proposed MCMS PWM modulation. Its successfully mitigate the mismatch of the output voltage by modifying the calculated duty cycle. Moreover, it does not need any feedforwarding signals like [89] which reflects its simplicity and feasibility at the proposed SEPIC-BDI.

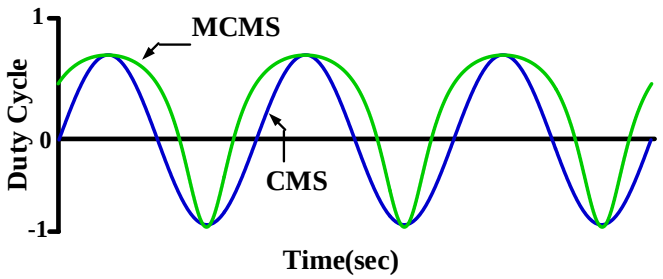


Figure 3.3: Duty cycle calculation at CMS and MCMS schemes for differential inverters.

3.2.2 Operational Principals of Proposed SEPIC Converters in Differential Inverter

Fig. 3.4 shows the operational waveforms of the proposed SEPIC-BDI for one phase using the proposed MCMS scheme. M represents the static gain of the proposed inverter.

V_{dc} and $v_{ox}(t)$ present DC input voltage and variable AC output voltage of SEPIC converter x. Similarly, $i_{inx}(t)$ and $i_{sx}(t)$ express the input and output current of the SEPIC converter x. When the instantaneous AC output voltage is larger than the DC input voltage, the DC-DC SEPIC converter process the power of one phase in two directions: forward and reverse power (circulating power) [89, 94].

Fig. 3-5 exhibits the equivalent circuit of one isolated SEPIC converter x and its operational modes at both frequency states (line-frequency and switching-frequency). For proper operation, the SEPIC converter should processes both powers and validate the smooth operation of the differential inverter and the MCMS modulation. The complimentary switching of the main switch S_{mx} and body diode of the synchronous switch S_{rx} processes the forward power as depicted in Fig. 3.5-a. The reverse power, proceeding the circulating power between the parallel SEPIC converters is implemented by using the complementary switching operation of the synchronous switch S_{rx} and the body diode of the main switch S_{mx}. The SEPIC converter achieves both powers according to the passive elements' energy storage and energy release mechanisms [116]. High frequency states of SEPIC converter switches maintain these mechanisms, as demonstrated in Fig. 3.5-b, c for forward power operation.

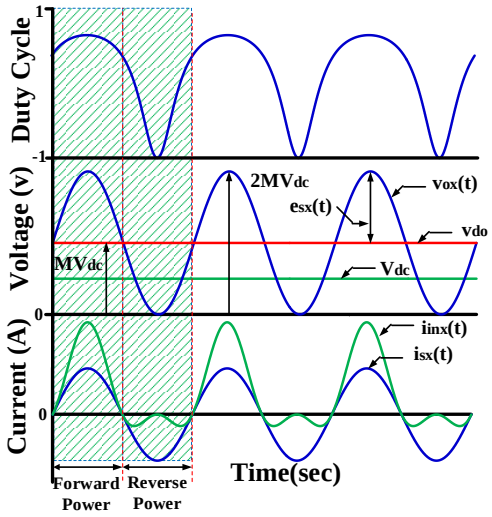
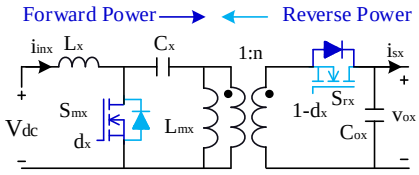
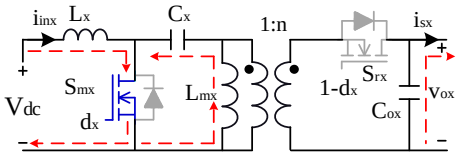


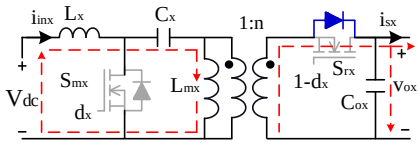
Figure 3.4: Operational waveforms of the proposed single-stage three-phase isolated grid-tied SEPIC-BDI.



a- SEPIC converter circuit



b- Forward power switching state of SEPIC converter for dx



c- Forward power switching state of SEPIC converter for (1-dx)

Figure 3-5: Schematic of proposed SEPIC converter and its operational states for line and switching-frequency.

Due to the symmetrical operation, forward power operation is analyzed in this chapter. During the first interval, d_xT_s shown in Fig. 3.5-b, the main switch S_{mx} is on to charge the inductance L_x of input inductor from the DC source. The stored energy of the coupling capacitor C_x is discharged also at the magnetizing inductance of HFT. At the secondary side of HFT transformer, the output capacitor C_{ox} discharges its energy at load. During the second interval, $(1-d_x)T_s$ turning off the main switch enables the series connection of input inductor, coupling capacitor and magnetizing inductance of HFT transformer. This connection lets the charged energy of the input inductor L_x and the power of the DC source, to charge the coupling capacitor C_x and the magnetizing inductanceL_{mx}. At the same time, the stored energy of magnetizing inductance moving across HFT transformer to charge the output capacitor $C_{ox}$and load, benefiting from the on-state of the body diode of the synchronous switch S_{rx} as shown in Fig. 3.5-c .

Applying DC averaging over on complete switching cycle T_s provides the voltage gain of the SEPIC converter that given as [116]:

$$\frac{V_{ox}}{V_{dc}} = \frac{nd_x}{1-d_x} \tag{3.2}$$

Where n represents the turn's ratio of utilized HFT. The voltage and the current formulas for inductors and capacitors of the SEPIC converter are illustrated at Table. 3.2. The switches, its ripple components and its accompanying stresses, are derived. The voltages and currents of the passive elements are also outlined. It worth noticing that these parameters define the size of the SEPIC converter, its elements ratings and, the whole size of the proposed SEPIC-BDI.

Table 3.2: Isolated SEPIC converter components with its operational voltages, current and ripple components.

Component	Voltage	Current	Ripple component
L_x	--	$\frac{ni_{sx}d_x}{1-d_x}$	$\frac{d_x(t)V_{dc}}{2L_xF_{sw}}$
L_{mx}	--	ni_{sx}	$\frac{d_x(t)V_{dc}}{2L_{mx}F_{sw}}$
C_x	V_{dc}	--	$\frac{ni_{sx}d_x(t)}{2C_xF_{sw}}$
C_{ox}	v_{ox}	--	$\frac{i_{sx}d_x(t)}{2C_{ox}F_{sw}}$
S_{mx}	$V_{dc}+\frac{v_{ox}}{n}$	$\frac{ni_{sx}}{1-d_x}$	$\frac{d_x(t)V_{dc}}{2(L_x+L_{mx})F_{sw}}$
S_{rx}	$V_{dc}+nv_{ox}$	$\frac{ni_{sx}}{1-d_x}$	$\frac{d_x(t)V_{dc}}{2(L_x+L_{mx})F_{sw}}$

3.2.3 Mathematical Analysis of Proposed SEPIC-BDI

For the convenience of analysis, the balanced three-phase voltages at the grid side, shown in Fig. 3.1, are expressed as:

$$\begin{bmatrix} e_{su}(t) \\ e_{sv}(t) \\ e_{sw}(t) \end{bmatrix} = e_m \begin{bmatrix} sin(\omega t) \\ sin\left(\omega t - \frac{2\pi}{3}\right) \\ sin(\omega t + \frac{2\pi}{3}) \end{bmatrix} \tag{3.3}$$

Where e_m is the peak phase voltage and, ω is the angular frequency. Time-variant output voltage on each SEPIC converter can be generated using variable duty cycle as portrayed in proposed MCMS, see Fig. 3.4. The duty cycles are displaced with a 120º

phase shift angle to generate three-phase voltages. Therefore, according to equation (3.1), the duty cycle of the SEPIC converters is formulated as:

$$\begin{bmatrix} d_u(t) \\ d_v(t) \\ d_w(t) \end{bmatrix} = \frac{n*M(1+K)}{n*M(1+K)+1} \tag{3.4}$$

The term k presents the behavior of the grid and given, for three-phase grid as:

$$K = \begin{bmatrix} \sin(\omega t) \\ \sin\left(\omega t - \frac{2\pi}{3}\right) \\ \sin\left(\omega t + \frac{2\pi}{3}\right) \end{bmatrix} \tag{3.5}$$

It's interesting to notice that equation (3.4) considers the static linearization without any feedforward signals and mitigates low-order harmonics which discussed in the previous section.

The output voltages of the SEPIC converters v_{ou}, v_{ov}, v_{ow}, have two different components; a line-frequency sinusoidal component e_m, synchronized with the grid side and a DC offset component v_{do}, which generated from the changeable duty cycle and the SEPIC converters unipolar operation. They are expressed as follows:

$$\begin{bmatrix} v_{ou}(t) \\ v_{ov}(t) \\ v_{ow}(t) \end{bmatrix} = v_{do} + e_m \begin{bmatrix} \sin(\omega t) \\ \sin\left(\omega t - \frac{2\pi}{3}\right) \\ \sin\left(\omega t + \frac{2\pi}{3}\right) \end{bmatrix} \tag{3.6}$$

Owing to the differential connection of SEPIC modules at the grid side as presented in Fig. 3.1. At the line-to-line terminal voltages, these DC offset voltages cancel each other, and in turn, decouple the DC offset voltage from three-phase grid voltages.

Since both components results from SEPIC converters, the output voltages of SEPIC converter, derived at (3.6) can be rewritten as:

$$\begin{bmatrix} v_{ou}(t) \\ v_{ov}(t) \\ v_{ow}(t) \end{bmatrix} = nMV_{dc} + nMV_{dc} \begin{bmatrix} \sin(\omega t) \\ \sin\left(\omega t - \frac{2\pi}{3}\right) \\ \sin\left(\omega t + \frac{2\pi}{3}\right) \end{bmatrix} \tag{3.7}$$

It worth noticing that, according to equation (3.7), $\mathrm{v_{do}}$ equals e_m and, the voltage gain of the differential inverter depend on static gain M and the turn's ratio of HFT n.

3.3 Proposed Mathematical Model for NSHC of Differential Inverters

The mathematical analysis presented in the previous section deals with the fundamental equations of the differential inverters. It considers only the ideal waveforms, proposed MCMS scheme, and considers ideal SEPIC converters. However, any buck-boost converters (including SEPIC converters) or boost converters introduce low-order harmonics at the output current due to the paralleled DC-DC converters at differential inverters.

The parallel operation of utilized SEPIC converters introduces a reverse power in between, as depicted in Fig. 3.6. When the output AC voltage of the SEPIC converter larger than DC input voltage, this reverse power does not go back to input DC source. Nevertheless, it circulates between the DC-DC converters as shown in Fig. 3-6. One complete cycle of the duty cycle, output current, input current, and output voltage of three SEPIC converters is presented to show this issue.

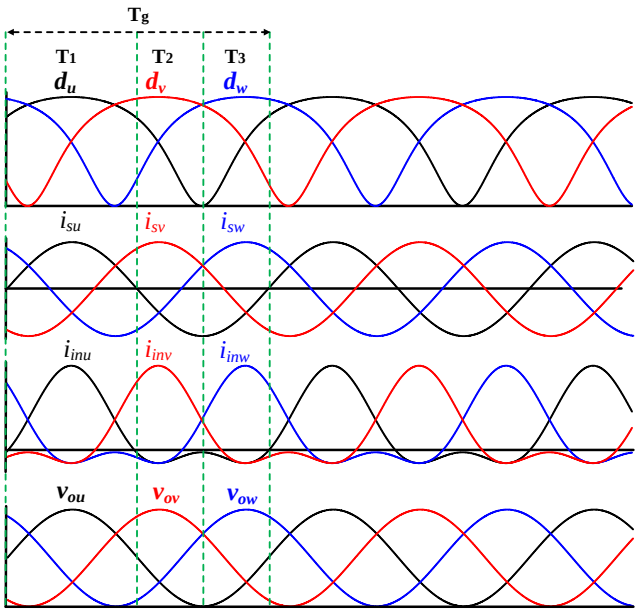


Figure 3.6: Mathematical representation of duty cycle, output voltage, output current and input current of the SEPIC-BDI.

For the first SEPIC converter, this cycle is divided into three different periods. In the first period T_1, the duty cycle d_u is high. Hence, the input DC current and the output grid AC current (i_{inu} and i_{su}) are positive. The converter power flows from the DC source to the grid. For the second period T_2, the duty cycle d_u is low and the currents

(i_{inu} and i_{su}) are negative. It means that the power moves from the other two SEPIC converters and circulates into this SEPIC converter. The same issue is for the third period T_3. However, the difference between T_2 and T_3 is the origin of the current. In T_2, the current flows from the second SEPIC converter because the duty cycle d_v is high. In T_3, the current flows from the third SEPIC converter because the duty cycle d_w is high. In the last two periods, the current rotates through first SEPIC converter two times in every cycle. Moreover, the same operation is repeated for the other two SEPIC converters.

Here, two important points should be interpreted:

1- There is a circulating power between three DC-DC converters of the three-phase differential inverter.

2- It is periodically happened two times in every line-cycle.

According to this circulating power, a Second-order Negative Sequence NSHC is imposed on the differential inverters output current, whatever the utilized DC-DC converter.

Looking at literature work, the NSHC of the differential inverters was studied in many papers. It covered many buck-boost DC-DC converters such as SEPIC, Cuk, and flyback converter [86-87, 89, 96 and 106]. In all, the differential inverter's results still have this harmonic component on the output current even in applications rather than grid-connected applications such as standalone applications. Moreover, the most published works state an inverse relationship between NSHC and the passive components of associated DC-DC converters (inductors and capacitors). Although huge passive components damp it a little bit, this solution is not accepted. It adds more size, weight, and cost for the differential inverters and hinders its practical applications. Therefore, all papers solve this issue by adding supplementary control loop to the primary loop (voltage control or current control). The proposed additional control loop mitigate it entirely from the output current without adding complexity to the differential power stage.

The Cuk-based differential inverter proposed in [86] adds a control loop for NSHC mitigation. The main loop, introduced for grid-current control, could not mitigate NSHC even at the proposed static linearization strategies. Therefore, in this loop, a band-path filter was presented to extract NSHC from the output current. The proposed Proportional

Resonance (PR) compensator is then designed to modulate its error signal and add it to the primary control signal. The same approach is implemented for grid-connected differential inverter topologies based on five different DC-DC buck-boost converters, as presented in [87].

Unlike the CMS scheme, which was proposed in [86-88, 91], three-phase and single-phase Cuk-based differential inverters using Discontinuous Modulation Scheme (DMS) was presented in [89, 94] and [104-105], respectively. This modulation disconnects the variable duty cycle for a while (about one-third of the line-cycle). This technique has decreased the circulating currents between different Cuk converters in both topologies, thereby circulating power loss, and NSHC will be decreased. However, the DMS modulation scheme does not completely remove the whole NSHC, especially for three-phase differential inverter, but decreases its amplitude and still needs an extra loop.

Also, DMS scheme adds odd harmonic component (especially third-order) that needs further control loop and complicates the overall control performance [94].

Although the previous literature has improved the performance of differential inverter topologies by mitigating NSHC. They successfully investigated the NSHC and proposed the additional loop for its compensation. The following points are common to all:

- There is no general NSHC mathematical model that investigates and accurately detects its real source.
- Detailed design of the utilized DC-DC converters, its active and passive elements are not well covered by including the effect of NSHC.

In this chapter, an in-depth mathematical model is derived. This model investigates the differential inverter practical issues such as variable duty cycle, low-order harmonics, and circulating power. For this purpose, the grid current of differential inverters is assumed as:

$$\begin{bmatrix} i_{su}(t) \\ i_{sv}(t) \\ i_{sw}(t) \end{bmatrix} = i_m \begin{bmatrix} \sin(\omega t) \\ \sin\left(\omega t - \frac{2\pi}{3}\right) \\ \sin\left(\omega t + \frac{2\pi}{3}\right) \end{bmatrix} + i_x \begin{bmatrix} \sin(h\omega t) \\ \sin\left(2\left(ht - \frac{2\pi}{3}\right)\right) \\ \sin\left(h\left(\omega t + \frac{2\pi}{3}\right)\right) \end{bmatrix} \tag{3.8}$$

Where i_x and h represent the absolute value of the assumed unknown low-order NSHC and its order, respectively. Input current of each SEPIC converter can be formulated by multiplying voltage ratio of SEPIC converter (3.2) and grid current assumed at (3.8) as

follows:

$$\begin{bmatrix} i_{inu}(t) \\ i_{inv}(t) \\ i_{inw}(t) \end{bmatrix} = 0.5nMi_m + nMi_m \begin{bmatrix} sin(wt) \\ sin\left(wt - \frac{2\pi}{3}\right) \\ sin\left(wt + \frac{2\pi}{3}\right) \end{bmatrix} - 0.5\ nMi_m \begin{bmatrix} cos(2wt) \\ cos\left(2wt - \frac{4\pi}{3}\right) \\ cos\left(2wt + \frac{4\pi}{3}\right) \end{bmatrix} +$$

$$nMi_x \begin{bmatrix} \sin(hwt) \\ \sin\left(h\left(wt - \frac{2\pi}{3}\right)\right) \\ \sin\left(h\left(wt + \frac{2\pi}{3}\right)\right) \end{bmatrix} + 0.5nMi_x \begin{bmatrix} \cos\big((1-h)wt\big) \\ \cos\left((1-h)\left(wt - \frac{2\pi}{3}\right)\right) \\ \cos\left((1-h)\left(wt + \frac{2\pi}{3}\right)\right) \end{bmatrix} -$$

$$0.5nMi_x \begin{bmatrix} \cos\big((1+h)wt\big) \\ \cos\left((1+h)\left(wt - \frac{2\pi}{3}\right)\right) \\ \cos\left((1+h)\left(wt + \frac{2\pi}{3}\right)\right) \end{bmatrix} \quad (3.9)$$

Based on (3.9), the input power of the proposed SEPIC-BDI can be obtained as follows:

$$P_{in} = V_{dc}I_{dc} = V_{dc}(i_{inu} + i_{inv} + i_{inw}) = \frac{3nMi_mV_{dc}}{2} + nMi_xV_{dc}\Big[sin(hwt) + sin\left(h\left(wt - \frac{2\pi}{3}\right)\right) + sin\left(h\left(wt + \frac{2\pi}{3}\right)\right)\Big] + 0.5nMi_xV_{dc}\Big[cos\big((1-h)wt\big) + cos\left((1-h)\left(wt - \frac{2\pi}{3}\right)\right) + cos\left((1-h)\left(wt + \frac{2\pi}{3}\right)\right)\Big] - 0.5nMi_xV_{dc}\Big[cos\big((1+h)wt\big) + cos\left((1+h)\left(wt - \frac{2\pi}{3}\right)\right) + \ cos\left((1+h)\left(wt + \frac{2\pi}{3}\right)\right)\Big] \quad (3.10)$$

Similarly, the output power of the proposed SEPIC-BDI can be obtained, based on (3.3) and (3.8), as follows:

$$P_o = e_m \begin{bmatrix} sin(\omega t) \\ sin\left(\omega t - \frac{2\pi}{3}\right) \\ sin(\omega t + \frac{2\pi}{3}) \end{bmatrix} * \left[i_m \begin{bmatrix} \sin(\omega t) \\ \sin\left(\omega t - \frac{2\pi}{3}\right) \\ \sin\left(\omega t + \frac{2\pi}{3}\right) \end{bmatrix} + i_x \begin{bmatrix} \sin(h\omega t) \\ \sin\left(2\left(ht - \frac{2\pi}{3}\right)\right) \\ \sin\left(h\left(\omega t + \frac{2\pi}{3}\right)\right) \end{bmatrix} \right] \quad (3.11)$$

The output power in (3.11) can be simplified as follows:

$$P_o = \frac{3e_mi_m}{2} + \frac{e_mi_x}{2}\Big[cos\big((1-h)wt\big) + cos\left((1-h)\left(wt - \frac{2\pi}{3}\right)\right) + cos\left((1-h)\left(wt + \frac{2\pi}{3}\right)\right)\Big] - \frac{e_mi_x}{2}\Big[cos\big((1+h)wt\big) + cos\left((1+h)\left(wt - \frac{2\pi}{3}\right)\right) + \ cos\left((1+h)\left(wt + \frac{2\pi}{3}\right)\right)\Big] \quad (3.12)$$

Assuming lossless DC-DC SEPIC converters, input power and output power are equal that enable the following condition:

$$nMi_xV_{dc}\left[sin(hwt)+sin\left(h\left(wt-\frac{2\pi}{3}\right)\right)+sin\left(h\left(wt+\frac{2\pi}{3}\right)\right)\right]=0 \quad (3.13)$$

It worth noticing that the even number of harmonic orders h satisfy the condition in equation (3.13). For example, second or fourth or sixth…..). This finding is very important because the NSHC is at even order. Moreover, considering only the second-order NSHC simplify the theoretical assumptions and closely matches the previous published works [86-87, 89 and 94]. Using this assumption, the practical input current of the SEPIC converters that equals the inductor current L_x can be expressed as:

$$\begin{bmatrix} i_{inu}(t) \\ i_{inv}(t) \\ i_{inw}(t) \end{bmatrix} = 0.5nMi_m + nMi_m \begin{bmatrix} sin(wt) \\ sin\left(wt-\frac{2\pi}{3}\right) \\ sin\left(wt+\frac{2\pi}{3}\right) \end{bmatrix} + 0.5nMi_x \begin{bmatrix} cos(-wt) \\ cos\left(-wt+\frac{2\pi}{3}\right) \\ cos\left(-wt-\frac{2\pi}{3}\right) \end{bmatrix} -$$

$$0.5\ nMi_m \begin{bmatrix} cos(2wt) \\ cos\left(2wt-\frac{4\pi}{3}\right) \\ cos\left(2wt+\frac{4\pi}{3}\right) \end{bmatrix} + nMi_x \begin{bmatrix} sin(2wt) \\ sin\left(2wt-\frac{4\pi}{3}\right) \\ sin\left(2wt+\frac{4\pi}{3}\right) \end{bmatrix} -$$

$$0.5nMi_x \begin{bmatrix} cos(3wt) \\ cos\left(3wt-\frac{6\pi}{3}\right) \\ cos\left(3wt+\frac{6\pi}{3}\right) \end{bmatrix} \quad (3.14)$$

According to (3.14), the input of the SEPIC converter which integrated at differential inverter considering second-order NSHC includes the following components:

- ✓ **DC offset current component**, representing the shared average current of each SEPIC module from the DC source.
- ✓ **Line-frequency component**, representing the fundamental sinusoidal waveform imposed on the DC component and declares the injected current injection in the grid side.
- ✓ **Second-order component**, representing the circulating currents at reverse power operation and generates the NSHC imposed on grid-current.

- ✓ **Third-order component**, representing the component that generates from the current interaction between the reflected NSHC and the circulating currents.

With NSHC, the input and the output current of SEPIC modules are affected according to equations (3.8, 3.14). Here, it's very important to notice that the current of switches, inductors, and HFTs of SEPIC converters depends on them. Moreover, this effect continues to the input current of the DC input source based on the following expression:

$$I_{dc} = i_{inu} + i_{inv} + i_{inw} = \frac{3}{2} nMi_m + \frac{3}{4} nMi_x cos(3wt) \quad (3.15)$$

According to (3.15), the DC input current is distorted with a third-order component which has many harmful effects, especially for RES.

Regarding this, the features of the proposed mathematical model are summarized as

- ✓ The real source of NSHC is the modulation scheme (variable duty cycle) and DC-DC converters' unipolar operation such as the SEPIC converter. They generate the circulating power and introduce NSHC on the differential inverter output current. That is why the unfolding Flyback-based differential inverter does not have NSHC because the converter's output is bipolar [108].
- ✓ Equation (3.15) proves that no extra loop is demanded to mitigate the third-order harmonic component because the NSHC is the source of this component. Therefore, the NSHC compensation loop on the grid side is enough. This new finding is very important because it simplifies the control structure of the differential inverters.
- ✓ This model successfully explicates why the DCM modulation scheme does not wholly mitigate NSHC. It interestingly decreases the circulating current between the utilized DC-DC converters. However, it's worth noticing that the DMS modulation scheme moves part of the NSHC from second-order to the fourth-order [89].

3.4 Design Example of the Proposed SEPIC-BDI

The proposed SEPIC-BDI is assumed to convert $1.6kW$ to a three-phase utility grid of $200V$ line-line RMS voltage from a $100V$ DC source. The line-frequency and the switching-frequency is assumed $F_{line} = 60Hz$ and $F_{sw} = 50kHz$. The grid inductance is also presented and assumed as $L_{gx} = 4mH$ as shown in Fig. 3.1. As mentioned before, every SEPIC converter process one-third of the inverter power. Therefore, the power of each SEPIC converter is obtained as:

$$P_{con} = \frac{P_{inv}}{3} = \frac{1600}{3} = 533.33W \quad (3.16)$$

Based on this, the RMS output current of every SEPIC converter is given as:

$$i_{sx} = \frac{P_{con}}{e_m} = \frac{533.33}{200/(\sqrt{3})} = 4.6187A \quad (3.17)$$

The variable duty cycle of the proposed SEPIC-BDI is changes periodically from $d_x = 0.1 - 0.8$ over the line-frequency cycle to realize the proposed MCMS modulation scheme. From Table 3.2, the maximum input inductor current is obtained as:

$$i_{inx} = i_{Lx} = \frac{ni_{sx}d_x}{1-d_x} = \frac{1*\ 4.6187*\sqrt{2}*0.8}{1-0.8} = 26.1273A$$

(3.18)

Similarly, the maximum current of magnetizing inductance is obtained as:

$$i_{Lmx} = ni_{sx} = 1 * 4.6187 * \sqrt{2} = 6.5318A \quad (3.19)$$

Using the same approach, the coupling capacitor voltage is expressed as:

$$V_{Cx} = V_{dc} = 100V \quad (3.20)$$

In contrast, the maximum voltage of the output capacitor is expressed as:

$$V_{Cox} = v_{ox} = v_{do} + e_m = 2 * \frac{200}{\sqrt{3}} * \sqrt{2} = 326.598V \quad (3.21)$$

3.4.1 The Parameters Selection and the Design Criteria

The variable duty cycle introduces variable current and voltage ripples. The ripple window for both is expressed by the available duty range. However, the important limit is the high duty $d_x = 0.8$. The percentage of peak to average value of current ripple in input inductor L_x and magnetizing inductance of HFT L_{mx} is assumed 20% and 25%, respectively [116]. Therefore, the input inductance is expressed as:

$$L_x = \frac{d_x V_{dc}}{2\Delta i_{lx} F_{sw}} = \frac{0.8*100}{2*0.20*26.1273*50000} = 153.0965\mu H \quad (3.22)$$

Similarly, the magnetizing inductance is expressed as

$$L_{mx} = \frac{d_x V_{dc}}{2\Delta i_{lmx} F_{sw}} = \frac{0.8*100}{2*0.25*6.5318*50000} = 489.9109\mu H \quad (3.23)$$

The percentage of peak to average value of voltage ripple in coupling capacitor C_x and output capacitor C_{ox} is assumed 5% and 3%, respectively. Therefore, the capacitance of coupling capacitor is expressed as:

$$C_x = \frac{ni_{sx}d_x}{2\Delta V_{Cx}F_{sw}} = \frac{1*6.5318*0.8}{2*0.05*100*50000} = 10.4509\mu F \quad (3.24)$$

Also, the capacitance of the output capacitors is expressed as:

$$C_{ox} = \frac{ni_{sx}d_x}{2\Delta V_{Cox}F_{sw}} = \frac{1*6.5318*0.8}{2*0.03*326.598*50000} = 5.333\mu F \quad (3.25)$$

The final chosen parameters of the proposed SEPIC-BDI are summarized in Table. 3.3. It worth noticing that, the inductances and capacitances is larger than the calculated values in equations (3.22: 3.25). This is important to compensate the voltage drop of the parasitic resistances of the selected passive components. For the switches devices, the maximum current stress of the main switch is expressed as:

$$i_{Smx} = \frac{ni_{sx}}{1-d_x} = \frac{1*4.6187*\sqrt{2}}{1-0.8} = 32.6591A \quad (3.26)$$

The maximum current ripple of the main switch is also expressed as:

$$\Delta i_{Smx} = \Delta i_{lx} + \Delta i_{lmx} = (0.25 + 0.20) * 4.6187 * \sqrt{2} = 2.9393A \quad (3.27)$$

This means that the peak current of the main switch is:

$$i_{Smx}(peak) = 32.6591 + 2.9393 = 35.5984A \quad (3.28)$$

For the synchronous switch, the maximum current stress is obtained as:

$$i_{Srx} = \frac{ni_{sx}}{1-d_x} = \frac{1*4.6187*\sqrt{2}}{1-0.8} = 32.6591A \quad (3.29)$$

Table 3.3: The designated parameters of the proposed isolated SEPIC-BDI.

component	value	Unit
Rated Power, P_{inv}	1600	W
Input DC Voltage, V_{dc}	100	V
Grid Voltage, v_{ll}, ω	200, $2\pi * 60$	V, rad/sec
Switching Frequency, F_{sw}	50	kHz
Input inductor, L_x	180	μH
HFL transformer inductance, L_{mx}	500	μH
HFL transformer turns ratio n	1	--
Coupling capacitor, C_x	14	μF
Output capacitor, C_{ox}	14	uF
Grid inductance, L_{gx}	4	mH

The maximum current ripple of the synchronous switch is also expressed as:

$$\Delta i_{Srx} = \Delta i_{lx} + \Delta i_{lmx} = (0.25 + 0.20) * 4.6187 * \sqrt{2} = 2.9393A \quad (3.30)$$

This means that the peak current of the synchronous switch is:

$$i_{Srx}(peak) = 32.6591 + 2.9393 = 35.5984A \quad (3.31)$$

The voltage stress peak of the main switch is calculated as:

$$V_{Smx} = V_{dc} + \frac{v_{ox}}{n} = 100 + \frac{326.598}{1} = 426.598V \quad (3.32)$$

The maximum voltage ripple is obtained as:

$$\Delta V_{Smx} = \Delta V_{Cx} + \Delta \mathrm{V_{Cox}} = (0.05 * 100) + (0.03 * 326.598) = 14.7979V \quad (3.33)$$

This means that the peak voltage of main switch is:

$$V_{Smx}(peak) = V_{Smx} + \Delta V_{Smx} = 426.598 + 14.7979 = 441.3959V \quad (3.34)$$

Following the same approach for synchronous, the maximum voltage stress is:

$$V_{Srx} = V_{dc} + nv_{ox} = 100 + (1 * 326.598) = 426.598V \quad (3.35)$$

The maximum voltage ripple is obtained as:

$$\Delta V_{Smx} = \Delta \mathrm{V_{Cx}} + \Delta \mathrm{V_{Cox}} = (0.05 * 100) + (0.03 * 326.598) = 14.7979V \quad (3.36)$$

This means that the peak voltage of main switch is:

$$V_{Smx}(peak) = V_{Smx} + \Delta V_{Smx} = 426.598 + 14.7979 = 441.3959V \quad (3.37)$$

By considering the voltage and the current peaks of the main and synchronous switches that derived in previous equations. The maximum switch current and the maximum voltage will be larger than $35.5984A$ and $441.3959V$ because there is a voltage drop introduced from the SEPIC converter elements' parasitic resistances. Therefore, SiC devices with a part number C2M0040120D are selected for both switches of the proposed SEPIC converter. It is worth mentioning that this stress happens at the forward power cycle. Therefore, the main switch and body diode of the synchronous switch should handle this current and voltage stress. Furthermore, SiC devices are preferred because they have low conduction and low switching losses, implying high efficiency. Moreover, they have a high blocking current and voltage capability to withstand the current and voltage strength of the proposed SEPIC-BDI.

Fig. 3.7 illustrates the designated PCP board of the utilized SEPIC DC-DC converter, for reliable operation, film capacitors with part number (C4AEOBW5140A3JJ) are selected for both the coupling and output capacitance. Also, film capacitors is used for the clamp capacitor which is introduced as a part of clamping circuit to mitigate the high voltage

spikes over switches which come from the leakage inductance of HFTs. Also, Heatsink is introduced for stable heat dissipation. Finally, the gate-drives which drive SIC switches is implemented on the same board to validate the modular construction of the proposed SEPIC-BDI.

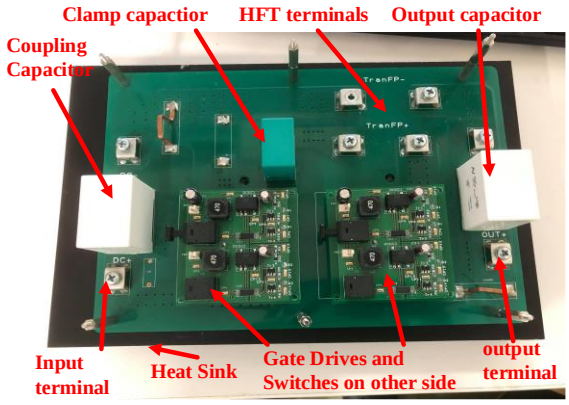


Figure 3.7: PCB board implementation of one SEPIC converter utilized at the proposed SEPIC-BDI.

In contrast, superior materials suitable for the HFT and input inductor design are monocrystalline, amorphous, and ferrites. For the proposed SEPIC converters, a soft ferrite core (EER-94) is used, for both to achieve low loss and cost [131-132]. The permeability of this core is $\mu_r = 2500$. $A_e = 712mm^2$and $V_e = 158000mm^3$ are the effective area and effective volume, respectively. The maximum flux density is $B_m = 470mT$. To reduce the magnetic eddy currents and the hysteresis losses, LITZ wire has been used for their windings.

For many years, the basic magnetic theory of the traditional line-frequency transformers was used to design HFTs. The turns of HFT can be expressed using equation (3.38). This equation assumed that the primary and secondary windings of an HFT behave like inductors [133-136], and the magnetic material is composed of one heterogeneous structure. Moreover, it designs HFTs as an independent block by considering only the magnetic elements of an HFT, such as the core geometry and number of turns.

$$N = \sqrt{\frac{L_{mx} * V_e}{\mu_o * \mu_r * A_e}} \tag{3.38}$$

Recently, most isolated DC-DC converters have intricate magnetic structures, consist of many windings and diversified heterogeneous elements (air gaps as well as cores). These

converters require air gaps to store energy during the complementary switching operation [116]. For the proposed SEPIC-BDI, the SEPIC converter has a variable terminal voltage at the HFT due to its variable duty cycle. Therefore, the number of turns can be obtained as follows:

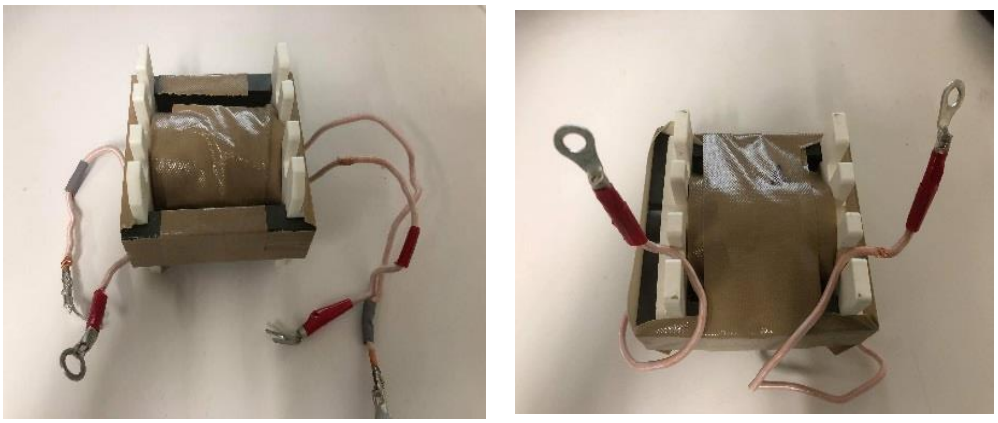
$$N = \frac{V_{on}*(1-D)*T_S}{\Delta B_m * A_e} \tag{3.39}$$

Equation (3.39) considers the circuit parameters of the SEPIC converter, as well as the core geometry. The circuit parameters is introduced by the maximum volt-second V_{on}, on the primary turns of the HFT when the main switch S_{mx} is off. From (3.39), the number of turns is 9. To mitigate the reduction in magnetizing inductance coming from existed air gap, 15 turns is used in the HFT design.

On the other hand, the number of turns for input inductors can be expressed as follows:

$$N = \frac{L_x * I_{pk}}{A_e * \Delta B} \tag{3.40}$$

I_{pk} is the maximum current of the inductor before saturation. As the maximum current of input inductor is $26.1273A$. $I_{pk} = 35A$ is selected for the maximum saturation current. From (40), the turn's number for the input inductor is 32. Practically, for higher saturation current, the turn's number is increased to 37 in the proposed SEPIC converter. The implemented HFT and input inductor of the proposed SEPIC module are manifested in Fig. 3.8. Finally, the experimental measurable values of the proposed SEPIC converters including the parasitic components are illustrated at Table. 3.4.



Designed HFT Designed Input inductor

Figure 3.8: Photographs of implemented passive elements of proposed SEPIC-BDI.

Table 3.4: Experimental Parameters of proposed Isolated SEPIC-BDI.

component	specifications	
Input Inductor	L_x	181.9µH
	R_{dcr}	200mΩ
	core	EER-94
	No. of turns	37
HFL transformer	L_{mx}	493.18µH
	R_{pri}	50mΩ
	R_{sec}	65mΩ
	core	EER-94
	Turns ratio 1:n	1:1
	No. of turns (primary)	15
Switches	R_{dson}	40mΩ
	V_F	1.8v
	t_{rise}	52ns
	t_{fall}	34ns
Capacitors	C_x	C4AEOBW5140A3JJ
	C_{ox}	C4AEOBW5140A3JJ
	R_{esr}	5.4mΩ
Grid inductance,	L_{gx}	4mH
	R_{gx}	0.2Ω

3.4.2 Small-Signal Model of the Proposed SEPIC Converters

The provided SEPIC converter is a buck-boost converter with four passive elements (two inductances and two capacitances) [137]. These passive elements decide the dynamic response of the SEPIC-BDI. The open-loop transfer function of the SEPIC converter generally a fourth-order transfer function [138-142]. A dynamic, accurate model representing the following variables (i_{Lx} , i_{Lmx} , v_{Cx} , v_{ox}) should be derived to design a reasonable control for SEPIC-BDI, shown in Fig. 3.1.

A linearization strategy of the SEPIC converter dynamic response using the AC Modeling approach is obtained to solve this issue [116]. It is based on the SEPIC operating modes at switching frequency that is illustrated in Fig. 3.5. This approach is the simplest one

between other methods such as switch averaging and the state-space averaging. It is worth mentioning that the dynamic response in forward and reverse power is similar because the voltage gain and operating modes are identical. Averaging the previous variables over one complete cycle of switching operation (at forward power) and linearizing it over the quiescent operating point result the following equations:

$$\left.\begin{aligned}
L_x \frac{d}{dt} i_{Lx}^{\sim}(t) &= V_{dc}^{\sim}(t) - (1-d_x) v_{Cx}^{\sim}(t) - (1-d_x)\frac{v_{ox}^{\sim}(t)}{n} \\
&\quad + d_x^{\sim}(t)[V_{Cx} + \frac{V_{ox}}{n}] \\
L_{mx} \frac{d}{dt} i_{Lmx}^{\sim}(t) &= -d_x v_{Cx}^{\sim}(t) + (1-d_x)\frac{v_{ox}^{\sim}(t)}{n} - d_x^{\sim}(t)[V_{Cx} + \frac{V_{ox}}{n}] \\
C_x \frac{d}{dt} v_{Cx}^{\sim}(t) &= d_x i_{Lmx}^{\sim}(t) + (1-d_x) i_{Lx}^{\sim}(t) + d_x^{\sim}(t)[I_{Lmx} - I_{Lx}] \\
C_{ox} \frac{d}{dt} v_{ox}^{\sim}(t) &= -i_{sx}^{\sim}(t) + (1-d_x)\frac{i_{Lx}^{\sim}(t)}{n} - (1-d_x)\frac{i_{Lmx}^{\sim}(t)}{n} \\
&\quad + d_x^{\sim}(t)[\frac{I_{Lmx} - I_{Lx}}{n}]
\end{aligned}\right\} \quad (3.41)$$

Where $i_{Lx}^{\sim}(t)$ is the small-signal component of inductor current $i_{lx}(t)$. $v_{Cx}^{\sim}(t)$ represents the small-signal component of the coupling capacitor voltage $v_{cx}(t)$. $V_{dc}^{\sim}(t)$ is the small signal of DC input voltage V_{dc}. The small-signal components for the rest of the passive elements are also the same. The small-signal AC equivalent circuit model based on the previous equation (3.41) was constructed, as shown in Fig. 3.9. It's assumed that each variable has two distinct components, DC component and AC small-signal component around it and neglect nonlinear terms. The output voltage dynamics is based on the duty cycle and DC input voltage.

To control this converter, the control-to-output transfer equation is derived as:

$$G_{vd}(s) = \frac{v_{ox}(s)}{d_x(s)} = G_o \frac{a_3 s^3 + a_2 s^2 + a_1 s + a_0}{s^4 + b_3 s^3 + b_2 s^2 + b_1 s + b_0} \quad (3.42)$$

Where, $G_o$is the dc gain of SEPIC converter, $a_o - a_3$represent the constants of zeros, and $b_o - b_3$ are the constants of its poles. The coefficients of these constants which depend on circuit parameters are presented in Table 3.5.

Table 3.5: Coefficients of the open-loop transfer function of SEPIC converter utilized at proposed SEPIC-BDI.

coefficient	value
G_o	$\frac{nd_x}{1-d_x}$
a_3	$\frac{-i_{sx}}{v_{ox}C_{ox}}$
a_2	$\frac{d_x(L_{mx}L_x)}{C_{ox}(L_{mx}+L_x)}$
a_1	$\frac{d_x i_{sx}}{v_{ox}C_xC_{ox}L_{mx}}$
a_0	$\frac{d_x}{C_xC_{ox}L_{mx}L_x}$
b_3	$\frac{i_{sx}}{v_{ox}C_{ox}}$
b_2	$\frac{k_a-k_b}{nC_xC_{ox}L_xL_{mx}}$
k_a	$d_x^2(C_x+n^2C_{ox})(L_{mx}+L_x)$
k_b	$(2d_x-1)(C_xL_{mx}+n^2C_{ox}L_{mx}+C_xL_x)$
b_1	$\frac{i_{sx}}{v_{ox}C_{ox}C_x}[\frac{(1-d_x)^2}{L_x}+\frac{{d_x}^2}{L_{mx}}]$
b_0	$\frac{(1-d_x)^2}{n^2C_xC_{ox}L_xL_{mx}}$

The selected parameters of the utilized SEPIC converter, derived in previous section, is used to draw the open-loop transfer function and define the exact location of zeros and poles and also decide the stability range of the converter. Using high switching frequency enhances the overall size of the SEPIC-BDI by implementing small passive elements. It worth noticing that, the high switching-frequency also improves the performance of the closed-loop control because its effect on the line-frequency response is neglected, especially over the entire range of the variable duty cycle. Fig. 3.10 illustrates the bode plot of the open-loop transfer function of the SEPIC converter.

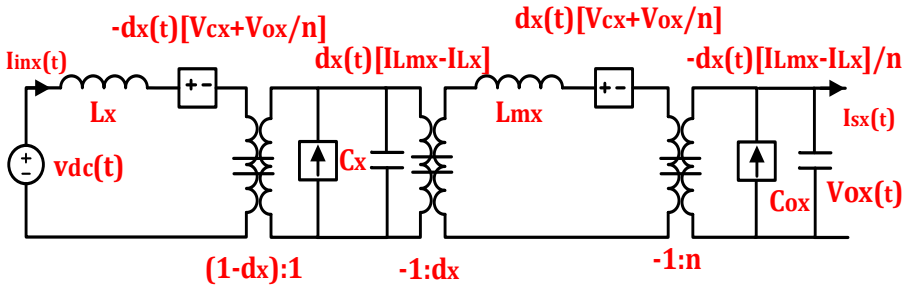


Figure 3-9: AC equivalent circuit of the SEPIC converter utilized at proposed SEPIC-BDI.

It has been seen that the system is unstable at some values of the duty cycles, which makes the differential inverter prone to instability. Moreover, the phase delay of the SEPIC converter increases at a higher duty cycle. Therefore, the closed-loop control should compensate for the phase delay and stabilizes the inverter transfer function. Regarding this, the control design should be designed according to the worst status of control to the output transfer function, which was at the highest duty cycle $d_x = 0.8$.

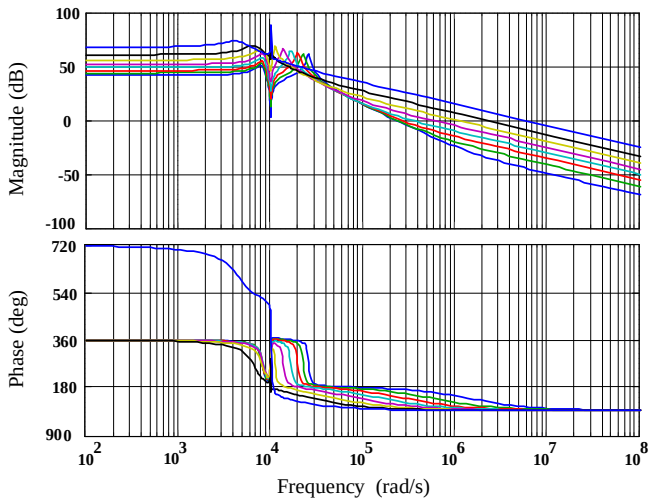


Figure 3.10: Bode plot of $G_{vd}(s)$ of SEPIC converter at ($d_x = 0.1 - 0.8$ from bottom to above).

3.4.3 Proposed Control Technique

Fig. 3.11 shows the proposed control strategy based on synchronous d-q control, with the proposed harmonic compensator loop. Existing RHP zeros of the SEPIC converters that introduces the phase delay of the converter places limits the maximum allowable phase

margin. Phase lead controller based on PID compensator is proposed to solve this issue [143-147]. The proportional part of the PID compensator accelerates the dynamics of the system. The transfer function of PID compensator is expressed as:

$$G_c(s) = K_p + \frac{K_i}{s} + k_d s \tag{3.43}$$

The proportional gain of the PID K_p increases the DC gain, which enhances the sensitivity of the controller to change and react more quickly. The integral term K_i improves the accuracy of the system by reducing the steady state error. Moreover, the derivative gain decrease its error by comparing it with previous gains. At final, PID control is easy to design, which simplifies the design process and ensures stable operation of the main controller.

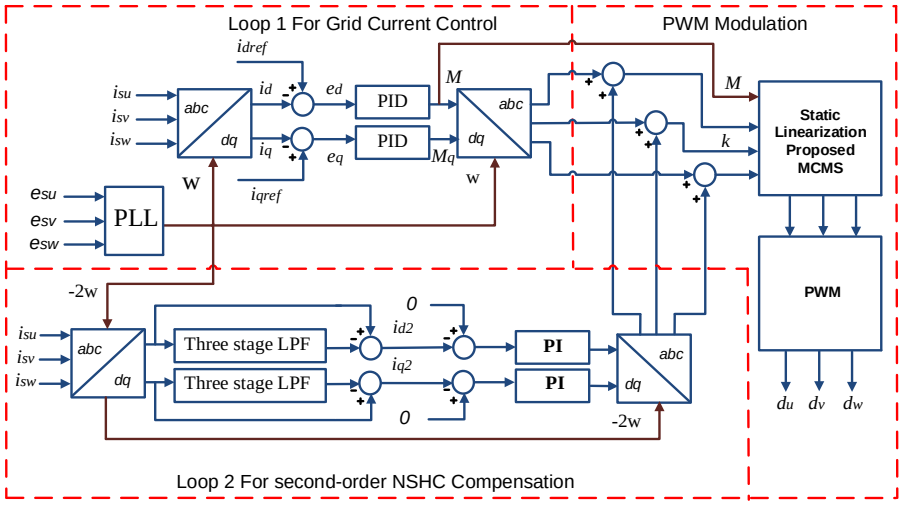


Figure 3.11: Proposed control of the SEPIC-BDI.

On the other hand, the harmonic compensator loop is realized by using three cascaded first-order Low Pass Filter (LPFs). The cascaded connection of three LPFs can accurately detect the NSHC from the grid current. As shown in Fig. 3.11, the three-phase grid-current is mutated into the stationary d-q axis frame based on the grid voltage phase angle. The Clark transformation is expressed as:

$$\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \frac{\sqrt{2}}{\sqrt{3}} \begin{bmatrix} cos(\omega t) & cos\left(\omega t - \frac{2\pi}{3}\right) & cos\left(\omega t + \frac{2\pi}{3}\right) \\ cos(\omega t) & -sin\left(\omega t - \frac{2\pi}{3}\right) & -sin\left(\omega t + \frac{2\pi}{3}\right) \end{bmatrix} \begin{bmatrix} i_{su} \\ i_{sv} \\ i_{sw} \end{bmatrix} \tag{3.44}$$

It worth mentioning that the angular frequency of the line component (positive

component) in the d-q frame is (ω), where the angular frequency of NSHC in the same frame is (-2ω). The three LPFs will assure NSHC attenuation from the grid current. Then the output of LPFs is subtracted from the actual grid current to obtain only the accurate component of NSHC. Finally, the conventional PI controller is used to eliminate the NSHC by modulating each converter's duty cycle. The attenuation gain of the cascaded LPFs is 1. It is worthy to notice that the dynamic action of PI controllers is slow in the second loop. It prevents any distortion on the first loop and, at the same time, does not affect the whole system's bandwidth. Therefore, the output of main loop is transferred to ABC frame using inverse Clark transformation as follows:

$$\begin{bmatrix} M_u \\ M_v \\ M_w \end{bmatrix} = \frac{\sqrt{2}}{\sqrt{3}} \begin{bmatrix} cos(\omega t) & -\sin(\omega t) \\ cos\left(\omega t - \frac{2\pi}{3}\right) & -sin\left(\omega t - \frac{2\pi}{3}\right) \\ cos\left(\omega t + \frac{2\pi}{3}\right) & -sin\left(\omega t + \frac{2\pi}{3}\right) \end{bmatrix} \begin{bmatrix} M \\ M_q \end{bmatrix} \quad (3.45)$$

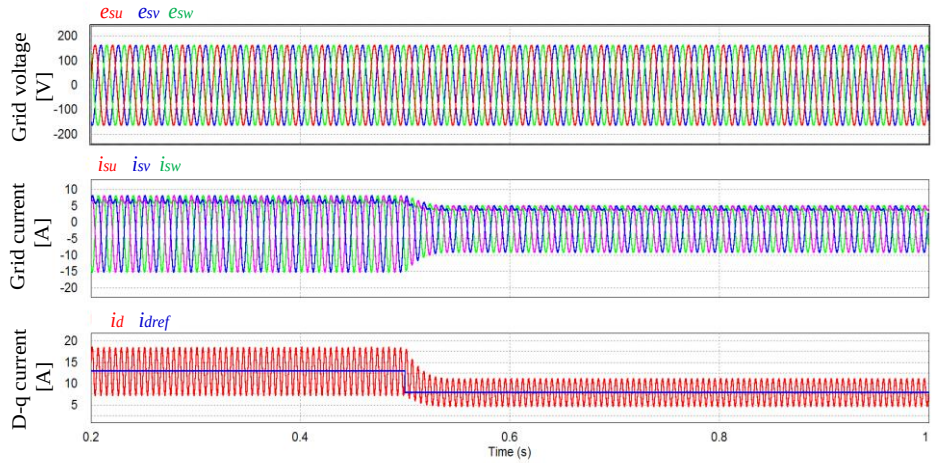
The same transformation is applied to the NSHC compensation loop. Finally, the odd harmonics resulting from SEPIC converters' nonlinear dynamics have been eliminated using the proposed MCMS modulation.

3.5 Results of the Proposed SEPIC-BDI

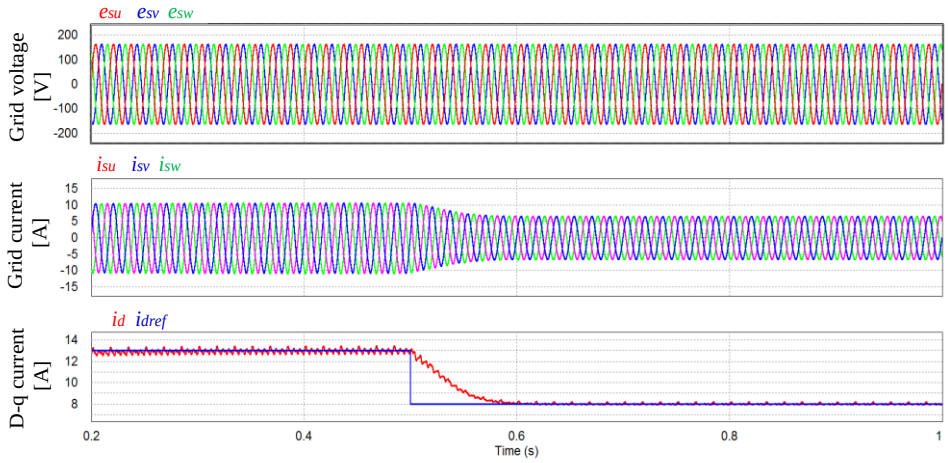
3.5.1 Simulation Results

To verify the designated synchronous d-q control and NSHC compensation technique. The SEPIC-BDI circuit and its control technique have been tested using PSIM 11.1.3 software. The simulation parameters is presented in Table 3.3. The control dynamics is verified by varying reference current from $13A$ to $8A$ $(2.6 - 1.6kW)$ before and after NSHC compensation as demonstrated in Fig. 3.12. The grid-current is distorted at a positive peak, which means an NSHC component.

Moreover, the distortion also appears on the controller output by making significant oscillation as shown in Fig. 3.12-a. Fig. 3.12-b reveals the compensation technique which cleared NSHC from the grid output current and control output and optimizes control dynamics.



A-Before NSHC compensation.

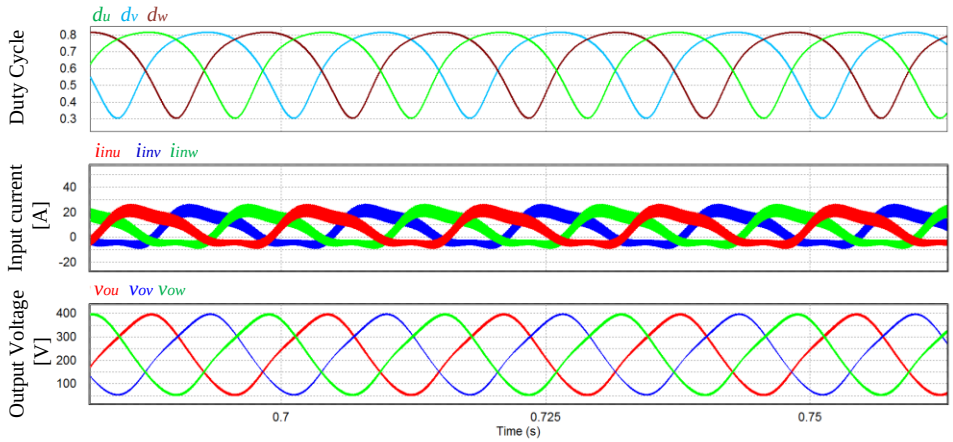


B- After NSHC compensation.

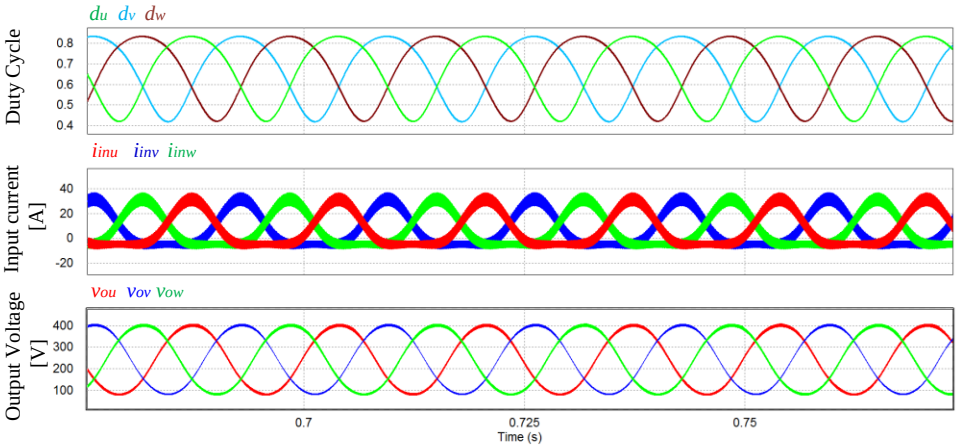
Figure 3.12: Simulation results of grid phase voltage, output grid current and control parameters.

Fig. 3.13 provides the duty cycle, the input inductor, and the SEPIC converters' output voltages. The distorted waveforms at the input inductor current and the output voltage of every SEPIC module effectively appear before NSHC compensation. It results from the circulating current and the SEPIC converters' unipolar operation, as illustrated in Fig. 3.13-a. The proposed compensation technique effectively cleared this distortion by narrowing the periods of T_2 and T_3, as illustrated in Fig. 3.13-b.

Finally, the proposed compensation technique's feature over the coupling capacitor voltage, HFT current, and switches current is illustrated in Fig. 3.14.



A-Before NSHC compensation.



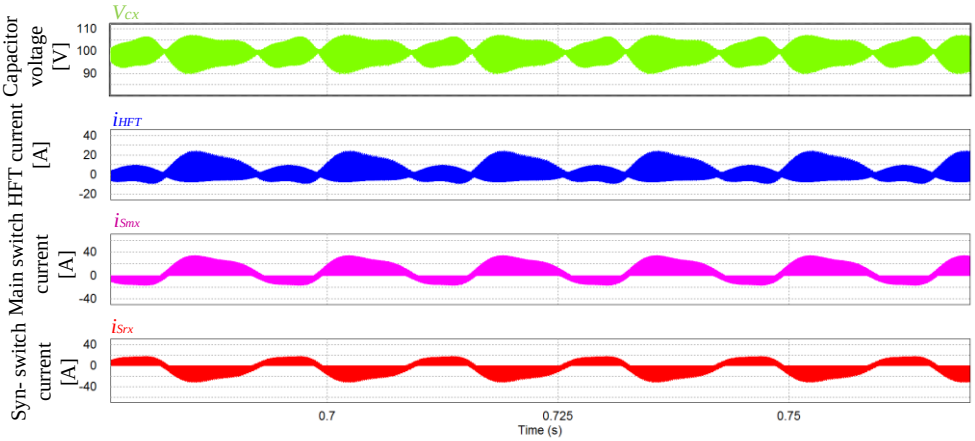
B- After NSHC compensation.

Figure 3.13: Simulation results of duty cycle, input inductor currents and output voltages.

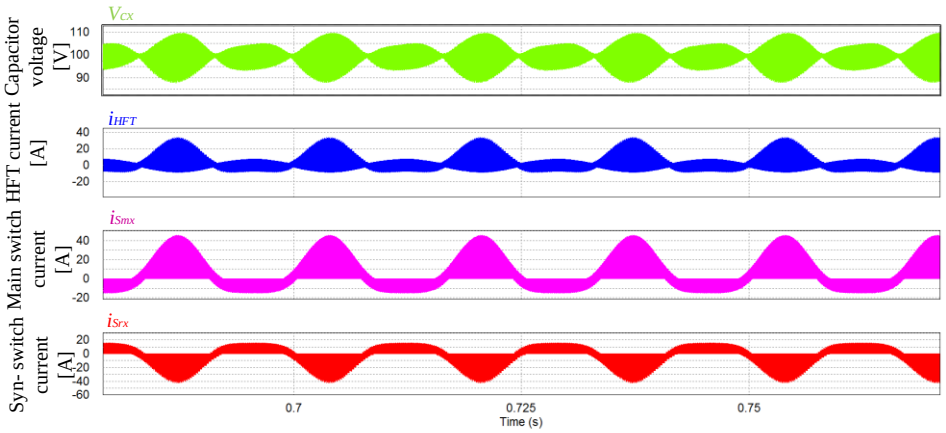
3.5.2 Experimental Results

The feasibility of the proposed SEPIC-BDI with the suggested NSHC compensation is verified using a 1.6 KW system setup, as offered in Fig. 3.15. The parameters are provided in Table 3.4. The system parameters, components, and measurement tools are depending on the proposed inverter, which depicted in Fig. 3.1. The variable DC source, which emulates the input DC source, is implemented by variable AC supply, diode bridge rectifier, and input capacitor. The 3-phase AC supply (S3P-240-30) manufactured by Yamabishi company is used in this setup with 0-240 V and 10.4kVA ratings. This power supply is connected to a six-diode bridge-rectifier (75L6P41) manufactured by Toshiba and cascaded with 6000uF to provide pure variable DC

voltage. Another variable 3-phase AC supply (S3P-240-15) with 0-240 V and 5.2kVA rated power is included to simulate the grid-side.



A-Before NSHC compensation.



B- After NSHC compensation.

Figure 3.14: Simulation results of coupling capacitor voltage, HFT current and switches currents.

The voltage, current, and power analysis is recorded experimentally by Yokogawa DL850 Scope and Yokogawa WT 1800 power analyzer, respectively. LA 55-P and LV25-P are used to sense three phase currents as well as two grid line-to-line voltages, introducing only five sensors in total. The isolated DC-DC converter (ISE0524A) from XP power is integrated in the designated gate drive to form gate isolation and provide cost effective solution in driving low-side (main switch) and high-side (synchronous switches) using the same driver chip.

The MWPE3 C6713A Expert III DSP board develops the control task of the proposed

control technique. . The proposed control is realized using PE-Expert 3 digital control system. It is embedded with TI high-speed floating-point DSP TMS320C6713. Moreover, the MWPE3 Xilinx FPGA board with part number XC3S500E is linked with the DSP board for pulses generation with a carrier frequency of 50 kHz. The integration of previous boards with PE-View9 computer-based interface features easy modifications for the control variables and high performance.

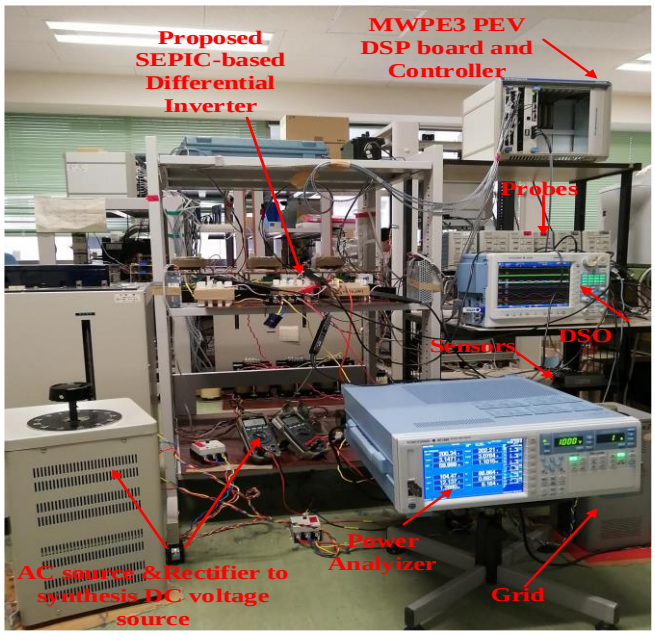
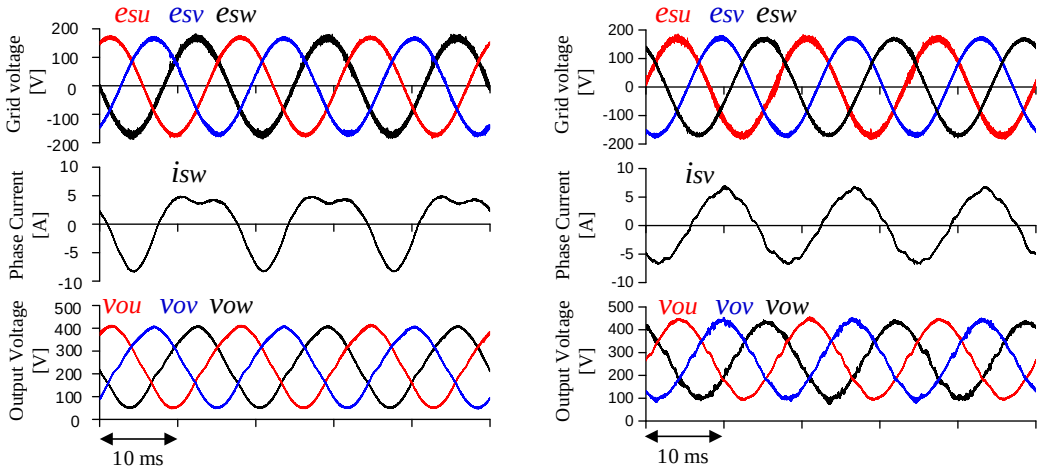


Figure 3.15: Experimental Setup of the proposed single-stage SEPIC-BDI.

Fig. 3.16 illustrates the experimental verifications of grid voltage, grid current, and output voltages of the SEPIC converters utilized at proposed SEPIC-BDI. Suppose the leakage inductance of HFTs is effective. In that case, this means that the percentage of NSHC is high because of the circulating current increases with it. After NSHC compensation, the proposed control technique modulates the duty cycle to clear NSHC and decreases the circulating current even at high leakage inductance.

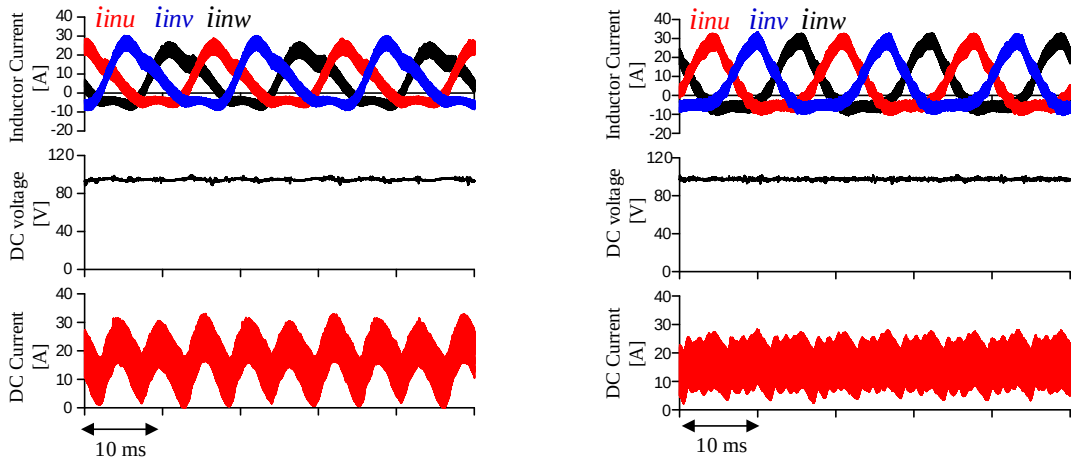
Fig. 3.17 appears the input inductor currents, DC voltage, and DC current before and after harmonic compensation. In particular, inductor currents and DC current is also effected by circulating current and the existed NSHC. On the other hand, after NSHC, the waveforms is free from distortion.



A-Before NSHC compensation. B- After NSHC compensation.

Figure 3.16: Experimental results of grid voltage, output grid-current and output voltages of SEPIC-BDI.

Fig. 3.18 shows the FFT harmonic spectrum of the grid current before and after NSHC compensation, respectively. Without harmonic compensation, the grid current is totally distorted, especially in the positive cycle, with NSHC component, which is 41.6% of the RMS line current. Otherwise, the proposed harmonic compensation technique minimized the NSHC to be 1.93% of the total RMS line current, which results in a pure sinusoidal waveform at the grid-current.



A-Before NSHC compensation. B- After NSHC compensation.

Figure 3.17: Experimental results of input currents, DC voltage and DC current of SEPIC-BDI.

The THD of the grid-current is 48.5% without NSHC compensation due to the circulating current and the high leakage inductance, whereas THD of the grid-current is 5.7 % with the proposed NSHC compensation technique.

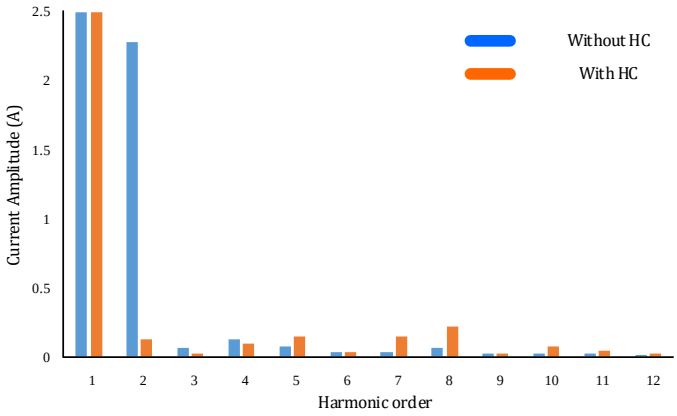


Figure 3.18: FFT Harmonic Spectrum of grid current before and after NSHC for proposed SEPIC-BDI.

Chapter 4: SEPIC-BDI: Improved Control with High Performance

4.1 Introduction

The simple circuit based on the DC-DC SEPIC DC-DC converters is the prime attractive feature of the propositioned differential inverter. It has a single-stage which provides great power density. The NSHC introduced at the output of the differential inverter may suppress its practicality. Therefore, the proposed mathematical model successfully investigates NSHC and its issues for the proposed SEPIC-BDI. Moreover, a two-loop-based grid current control is proposed to mitigate NSHC and achieve grid current control effectively. The results of the proposed SEPIC-BDI has two important notices:

- ✓ The THD of the proposed inverter is still more extensive than the standards of the recent grid codes (>5%).
- ✓ The DC input current of the proposed inverter has significant switching harmonics, disturbing the smooth operation of MPPT controllers and it's tracking efficiency and deteriorating PV modules during inverter applications at RES [148-151].

This chapter, motivated by this, presents two modified control techniques (Control-I, Control-II) to enhance the inverter performance and decrease THD under acceptable limits.

- In Control-I, a Type-II compensator, which enhances SEPIC converters' stability, is used instead of the PID controller. The proposed Type-II compensator effectively damp the resonance of the SEPIC converter [152-154]. This resonance comes from the passive elements of the proposed SEPIC converter and increases THD's previous results. In the second loop, the NSHC detection circuit depending on the LPFs is also used.
- In Control-II, the proposed control is redesigned based on the parasitic components of SEPIC converters. According to [155-156], The Right half-Plane (RHP) zeros may moves to the Left Half-Plane (LHP) because of the parasitic resistances of the SEPIC converter. This occurrence dramatically reduces the phase delay of proposed SEPIC converters shown in the open-loop transfer function in Fig. 3.10 in the previous section. Finally, LPF still used for NSHC compensation in the second loop.

Furthermore, this chapter presents the proposed SEPIC-BDI results when integrating a small film capacitor at the DC input side. It clears the aforementioned high switching harmonics. The voltage and the current range of the proposed SEPIC-BDI is also investigated. Finally, this chapter presents the proposed mathematical losses model to check the proposed inverter's efficiency profile at different conditions.

4.2 Proposed Control Technique (Control-I)

Fig. 4.1 illustrates the bode-diagram of the open-loop transfer function at a high duty cycle $d_x = 0.8$. There is a resonance between the inductors and the capacitors of the proposed SEPIC-BDI. This resonance should be damped by resistances of the passive elements and parasitic resistances of the proposed SEPIC converter. However, the dynamic response makes some subharmonics that increase THD. The previous proposed PID compensator did not completely solve this issue. To solve this issue, a Type-II compensator is proposed in this chapter. Type-II compensator replaces the derivative part of the PID compensator with a pole. This pole has -20DB/decade which decrease the gain of SEPIC converter before resonance frequency. Therefore, this pole damps effectively the previously mentioned resonance.

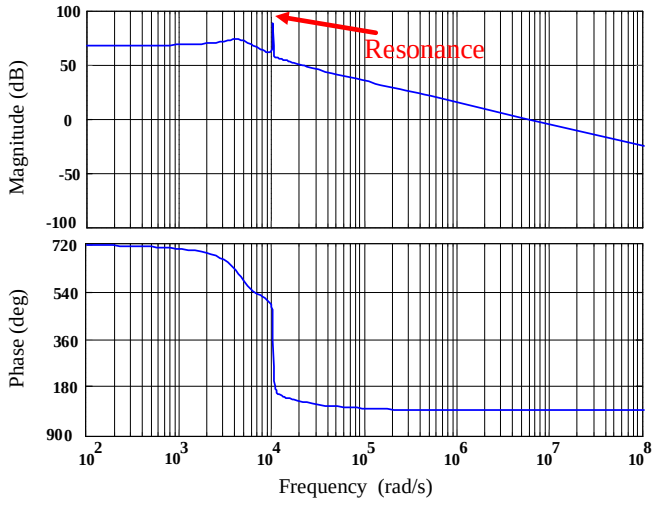


Figure 4.1: Open Loop transfer function of the bode blot of isolated SEPIC-BDI.

This compensator is realized as follows [116, 152-154]:

$$G_c(s) = G_{co}\frac{(1+\frac{s}{w_{z1}})}{(1+\frac{s}{w_{p1}})(1+\frac{s}{w_{p2}})} \tag{4.1}$$

The gain of Type-II, G_{co} increases the zero-frequency gain of the open-loop transfer function of the SEPIC, and improves the steady-state error. Zero of PID, w_{z1} boosts the phase delay of the SEPIC and enhance the overall inverter stability by expanding the system bandwidth. The first pole w_{p1} that put at low frequency flattens the DC gain and increases the control accuracy. The second pole frequency w_{p2} is high, located between resonance frequencies and switching frequency, to damp the switching harmonics. It eliminates the resonance effects from the control path. As shown in Fig. 4.2, the compensator outputs (M, M_q), indicate the differential inverter's static gain in the rotating frame. Then, the static gain is transferred to the ABC frame using inverse Clark transformation, representing the first component of each SEPIC's modulation index.

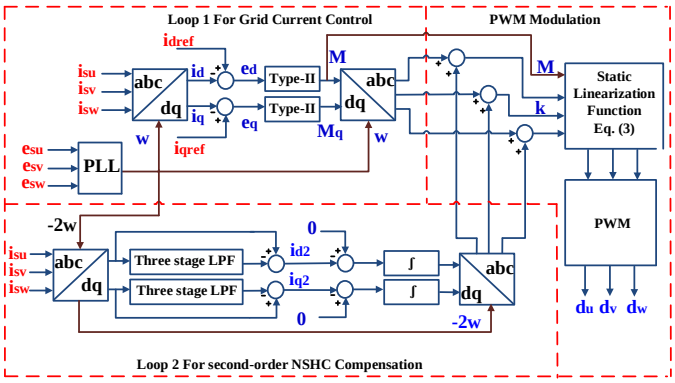


Figure 4.2: Proposed control diagram (Control-I) with NSHC compensation circuit of isolated SEPIC-BDI.

In the second loop, the proposed detection circuit of NSHC is based on three LPFs. The output sensors of the grid current have delivered to the proposed LPFs. These LPFs accurately mitigate all low-order harmonics and obtain fundamental components of grid currents. Then, the output of LPFs is subtracted from the actual grid currents to detect the second-order NSHC, as shown in Fig. 4.2. The dynamic transfer function of the LPF has formulated as:

$$G_s(s) = \frac{1}{(1+\frac{s}{w_l})^3} \tag{4.2}$$

This transfer function of LPFs has -60DB per decade response due to the located three poles. In addition to pole of Type-II, there are four poles in the system and, all damp the switching harmonics and the resonance produced between capacitors and inductors of

SEPIC converter. The Clark transformation achieves the operation between ABC frame and d-q frame at the angular frequency (-2ω). Then, the cascaded integrator attenuates the errors of the NSHC loop by modulating the duty cycle of each SEPIC converter. Here, an integrator is used instead of conventional PI to simplify the control function. Finally, the dynamic behavior of integrators in the second loop is slow to prevent any distortion on the first loop.

The closed-loop transfer function of SEPIC-based differential inverter that uses the proposed control is then expressed as follows:

$$T(s) = G_{vd}(s) * G_g(s) * G_{c2}(s) * d_x(s) \quad (4.3)$$

Here $G_{c2}(s)$ is the total transfer function of both loops. $G_g(s)$ Is the transfer function of grid-side inductance. $d_x(s)$ represents the transfer function of static linearization function based on equation (3). At frequency domain, it is expressed as:

$$d_x(s) \cong \frac{m(s)+m(s)K}{m(s)+m(s)K+1} \quad (4.4)$$

Where, $m(s)$ is the small signal component of static gain of differential inverter. According to the proposed control, the bandwidth of the full-system transfer function of the SEPIC converters is 590Hz. The DC gain and the phase margin are 52DB and 26.2, respectively, as illustrated in Fig. 4.3.

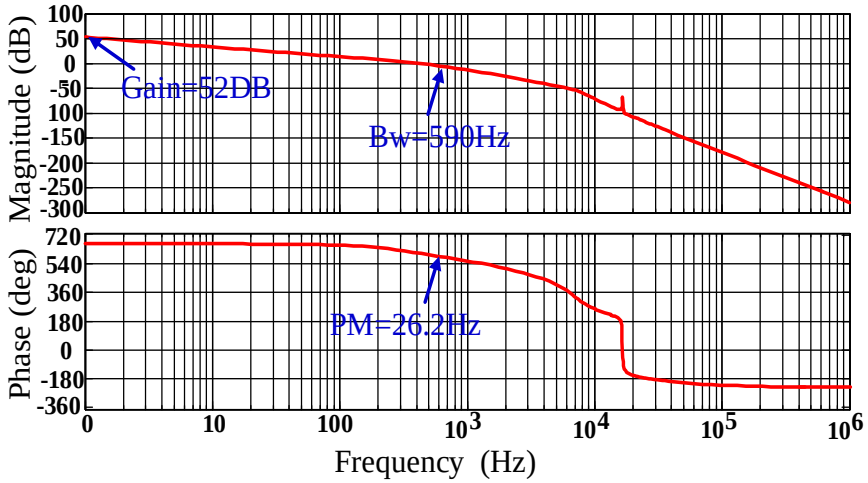


Figure 4.3: Bode diagram of closed-loop of modified grid-current control (Control-I).

4.3 System Results of Proposed Control Technique (Control-I)

Simulated-software and experimental outcomes have been conducted in this section to validate the feasibility of the proposed control technique and the theoretical assumption. To consider the mathematical analysis of NSHC, two case studies have been provided as:

- ✓ Case 1: This case discusses the effect of NSHC on the SEPIC converters, DC source, and grid. The control task includes Type-II compensators in the first loop. The second loop is disconnected.
- ✓ Case 2: This case shows the features of the proposed NSHC strategy using the proposed LPFs. The control task includes the Type-II compensator in the first loop as well as LPFs and integrator in the second loop.

Both cases have performed using PSIM 11.1.3 software and MWPE3 C6713A Expert III DSP board which utilized to implement Control-I.

Fig. 4.4 and 4.5, give both simulation and experimental results of the proposed isolated SEPIC-BDI at case 1. The proposed Type-II compensator has achieved grid-current control and injected active power. However, the grid current in both have distorted with NSHC even at applying static linearization developed by proposed MCMS scheme. These findings of both results match the theoretical assumptions as well as the literature work of differential inverters.

This NSHC component is reflected in SEPIC converters and DC voltage source, as shown in the input currents and the DC current. Again, these results are matched with our assumptions derived at proposed mathematical model at Ch. 3. Moreover, the reflection of NSHC on the DC source current generates a third-order component that also complies with the proposed mathematical model.

It is worth noticing that the NSHC distortion, in experimental results, is worse than simulation results. The additional parasitic of SEPIC converters, such as DC resistances of the PCB boards and connecting wires, are the source of this difference. This difference also introduced at the FFT harmonic spectrum of the grid-current (simulation and experimental results), as provided at Fig. 4.6.

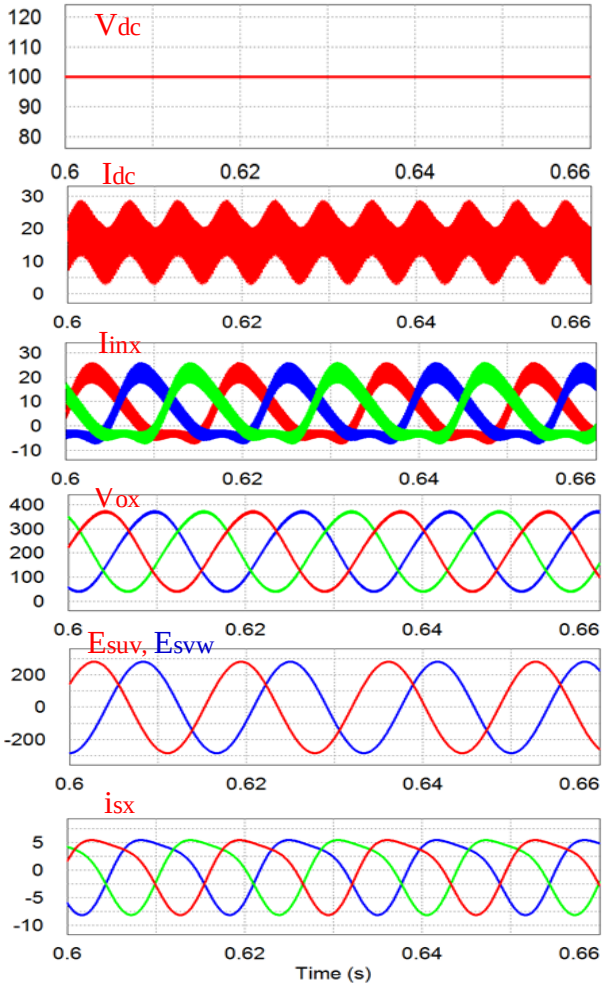


Figure 4.4: Simulation results of proposed SEPIC-BDI at case 1.

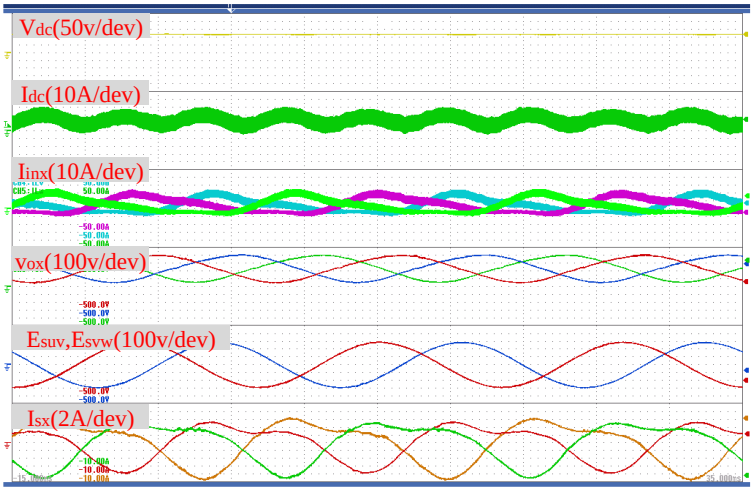
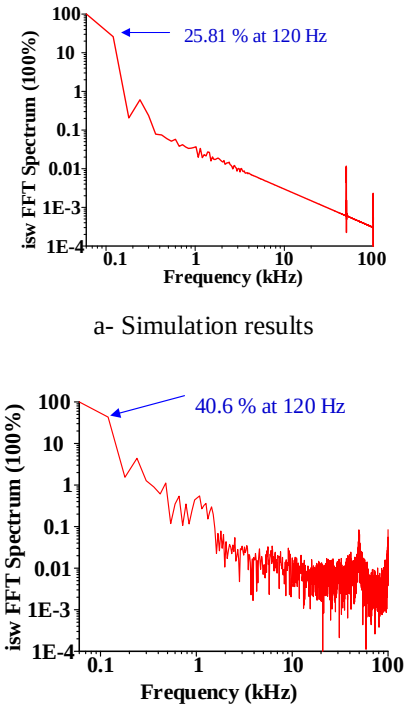


Figure 4.5: Experimental results of proposed SEPIC-BDI at case 1.



a- Simulation results

b- Experimental results

Figure 4.6: FFT Harmonic Spectrum of grid-current at case 1.

It shows that the percentage of second-order NSHC is about 25.81% and 40.6% for simulations and experiments. For the THD, the proposed inverter has 23.45% and 35.61% from simulations and experiments. Practically, Table 4.1 illustrates the percentage of other low-order harmonics. It's shown that the proposed static linearization strategy eliminates the other components, and there is a reflection of NSHC on input current of the SEPIC converter. This harmonic violates the IEC-61000 grid standards [157] and hinders the differential-based inverter's practical applications, as shown in Fig. 4.7. Finally, all previous results have shown the serious deformation of NSHC on the proposed differential inverter and the ultimate need for additional loop for NSHC mitigation.

Fig. 4.8 and 4.9 depict the simulation and experimental waveforms of case 2 that consider the proposed NSHC circuit. In both, the proposed control technique injects sinusoidal grid-current at unity power factor. Compared with case 1, the proposed control technique successfully eliminates the NSHC from the grid current. Moreover, it reduces the distortion of the three input inductor currents of SEPIC converters and their mismatch. It eliminates the third-order component from the DC source due to the successful

elimination of the NSHC of grid-current.

TABLE 4.1: Low-order harmonic components percentages of proposed inverter at case 1.

Low-order harmonics from Simulation				
Current/ Harmonic order	2	3	4	5
Grid current i_{sw}	25.81	0.204	0.605	0.235
Input Current i_{inw}	27.32	10.55	0.902	0.312
Low-order harmonics from Experiments				
Current	2	3	4	5
Grid current i_{sw}	40.6	1.127	3.4	0.923
Input Current i_{inw}	33.64	17.54	1.54	1.93

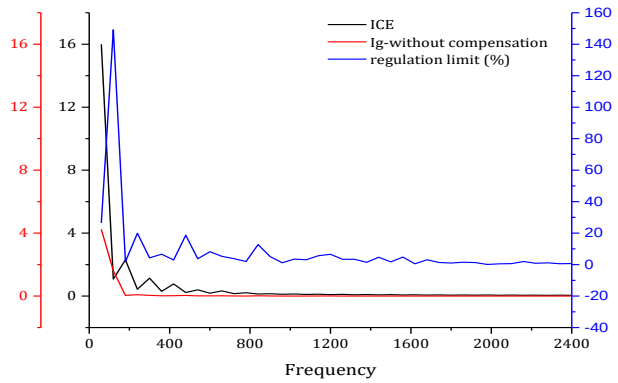


Figure 4.7: IEC-61000 standards compared with FFT Spectrum of experimental grid-current at case 1.

Fig. 4.10 demonstrates the FFT harmonic spectrum of the injected grid current at case 2 for simulation and experimental grid-currents. The percentage of second-order NSHC reduced from 25.81% to 0.278% in the simulations. Also, it reduced from 40.6% to 1.6143% in the experiments. It worth mentioning that the percentage of NSHC at proposed Control-I is less than the previously proposed PID control, which has 1.93%. It is backed to the damping effect of the proposed Type-II compensator. The successful mitigation of NSHC forces the third-order harmonies at SEPIC converters' input to reduce from 17.54% to 2.13% in the experimental results. The simulations results also have the same improvements, as illustrated in Table 4.2.

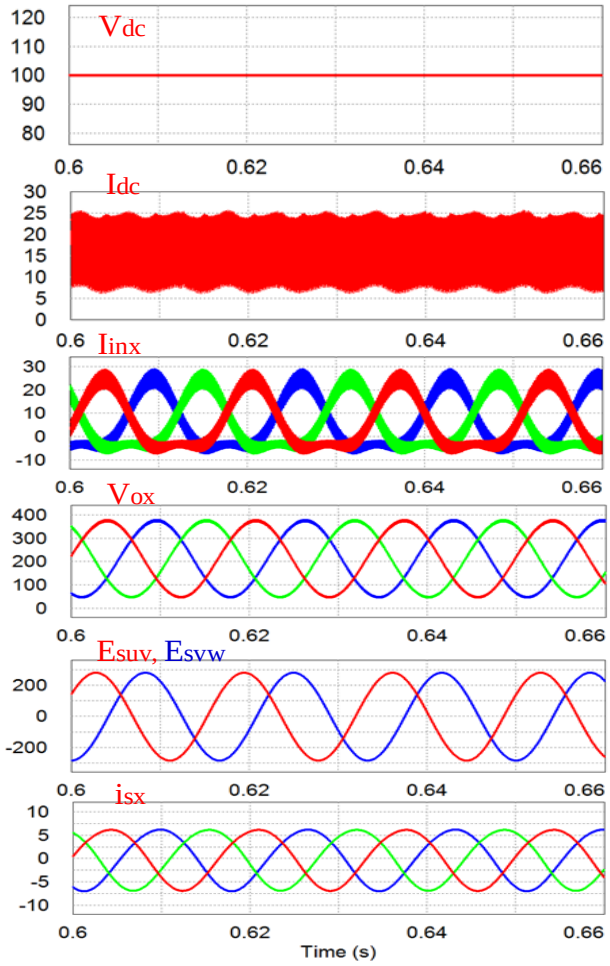


Figure 4.8: Simulation results of proposed SEPIC-BDI at case 2.

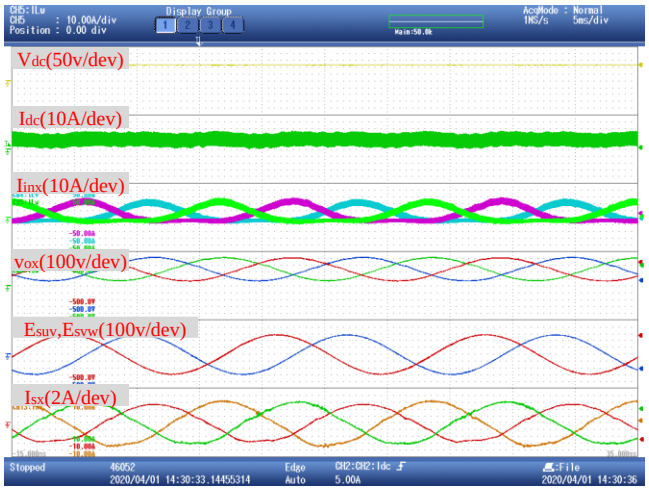
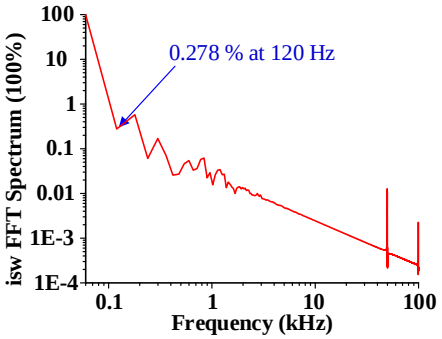
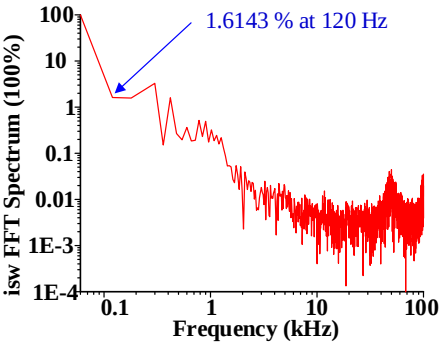


Figure 4.9: Experimental results of proposed SEPIC-BDI at case 2.



a- Simulation results



b- Experimental results

Figure 4.10: FFT Harmonic Spectrum of grid-current at case 2.

Table 4.2: Low-order harmonic components percentages of proposed inverter at case 2.

Low-order harmonics from Simulation				
Current/ Harmonic order	2	3	4	5
Grid current i_{sw}	0.278	0.575	0.06	0.169
Input Current i_{inw}	35.05	1.08	0.175	0.191
Low-order harmonics from Experiments				
Current	2	3	4	5
Grid current i_{sw}	1.614	1.572	2.385	3.278
Input Current i_{inw}	33.64	2.13	1.03	1.77

The maximum regulation limit of the harmonic components in case 2 is reduced from 150% to 70% as shown in Fig. 4.11. It confirms that the SEPIC-BDI using proposed control meets the standard limits of IEC-61000. Finally, THD is reduced from 35.61% to 4.087% and satisfy the recent grid codes (<5%).

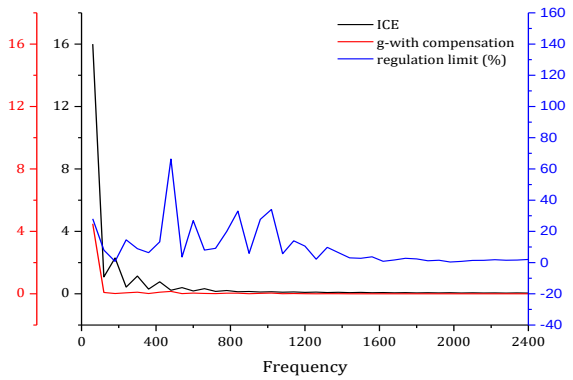


Figure 4.11: IEC-61000 standards compared with FFT Spectrum of experimental grid-current at case 2.

4.4 Proposed Control Technique (Control-II)

It worth noticing that the control loops of Control-I are symmetrical as follows:

- ✓ In the first loop, the errors e_d, e_q between fundamental values of actual and reference currents (i_d, i_q and i_{dref},i_{qref}) is the input of Type-II compensator.
- ✓ The compensator outputs (M and M_q) are then transferred to ABC frame using inverse Clark transformation, representing the first component of the modulation index of each SEPIC module.

High-order compensators, such as PID and Type-II, provide good performance, as shown in the previous section and Ch. 3. Also, nonlinear control techniques perform good performance for SEPIC converter at many applications, especially differential inverter [88]. However, it still needs excessive computational burden and mighty DSP boards and increases the cost of the proposed SEPIC-DBI. Therefore, using a low computational burden decreases the required DSP board's capability and facilitates an inexpensive one. We are motivated by this; decreasing the order of differential inverter compensator effectively simplifies the control programming code and reduces the calculation time. Low order compensators like conventional PI can be used instead of Type-II compensator by noticing the following important points

- ✓ Ref [155] states that the parasitic resistances of the SEPIC converter can move the complex RHP zeros to the left half-plane and reduce the phase delay of the SEPIC converter. The phase-delay of the open-loop SEPIC converter is 630, as shown in Fig. 4.1.

- ✓ LPFs and cascaded integrators in the second loop produces the second component of the static gain. The sum of both represents the final static gain of each SEPIC converter. In Contrast, the transfer function of LPFs has -60DB per decade response due to the located three poles, as presented in (4.2). These poles can be used to damp the switching harmonics of resonance frequencies.

This modified control, employed in Control-II, shown in Fig. 4.12, has the following advantages:

- ✓ The order of compensator, in the first loop, decreases from Type-II to PI and gives the same performance.
- ✓ The modified control-II decreases the execution burden of the controller by using lower execution time.
- ✓ The modified control-II enhances the THD especially at low static gain *M*.

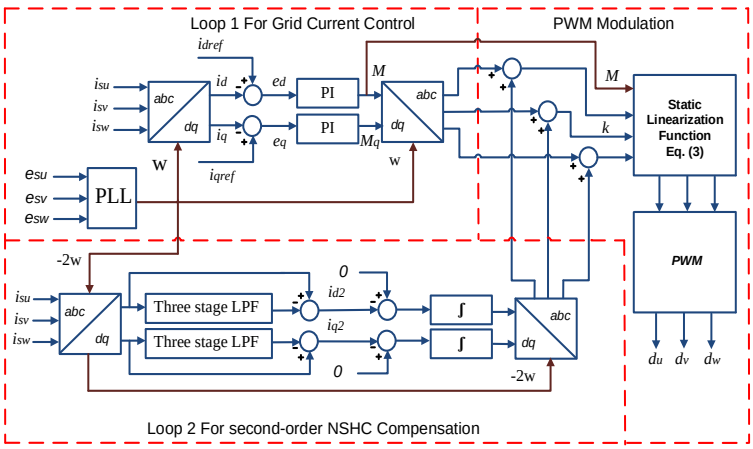


Figure 4.12: Proposed control diagram (Control-II) with NSHC compensation circuit of isolated SEPIC-BDI.

4.5 System Results of Proposed Control Technique (Control-II)

As discussed before, the high frequency switching harmonics can be mitigated by using small film capacitors. We add input capacitor to solve the high frequency switching harmonics shown in the previous results. Capacitance of the proposed SEPIC-BDI is 120uF with four parallel connected film capacitors (C4AEHBW5300A3JJ). Moreover, Table 4.3 illustrates the control variables which utilized in the proposed control. Fig. 4.13 illustrates the proposed SEPIC-BDI's experimental validations based on three SEPIC

converters at $Vdc = 120V$. The input DC current is continuous with a minimal switching ripple, which suits PV modules characteristics and enhances the utilized MPPT control tracking efficiency. As the proposed differential inverter is derived by a variable duty cycle, the input currents and output currents of utilized SEPIC converters change periodically with grid-frequency. The grid injected current is synchronized with grid voltage and introduce pure active power with unity power factor operation.

Table 4.3: Control parameters for the proposed Control-II.

	Parameters	Value
PI	K_p	0.004
	K_i	$1.34 * 10^{-6}$
LPF	Gain	0.5
	Cut off frequency	120 Hz
Integrator	Gain	1.67
	Frequency	$1 * 10^{-4}$

Fig. 4.14 shows the three SEPIC converters' duty cycles and static gain of the differential inverter at $Vdc = 120V$ and $P = 1.6kW$. The duty cycle is adjusted to compare with (-1:1) saw-tooth signal with a carrier frequency of $50kHz$ to generate switch pulses. It is worth noticing that the duty cycles are symmetrical. The static gain is constant and larger than one indicating the boosted voltage gain. Its value is greater than the ideal value due to the voltage drop of the SEPIC converter parasitic.

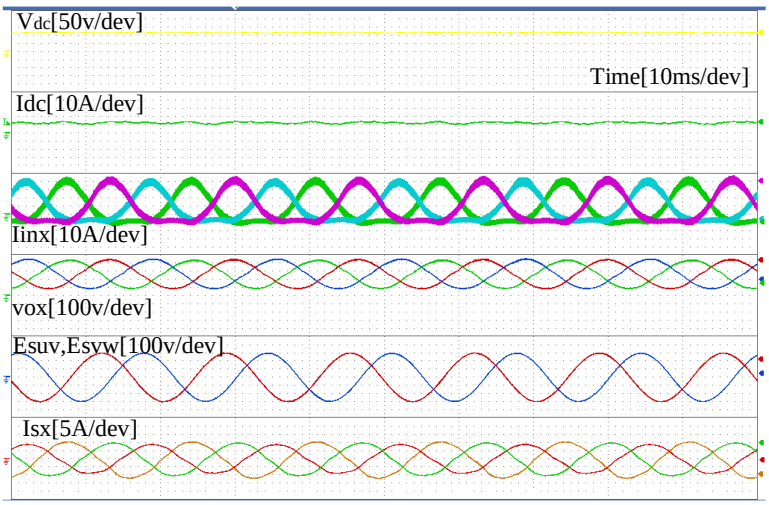


Figure 4.13: Experimental results of proposed differential inverter.

Fig. 4.15 illustrates the d-q reference and actual values. The reactive power equal to zero, and the steady-state error for both components is small that validates the stability of the proposed control system.

Figure 4.14: Duty cycle and Static gain M of proposed differential inverter.

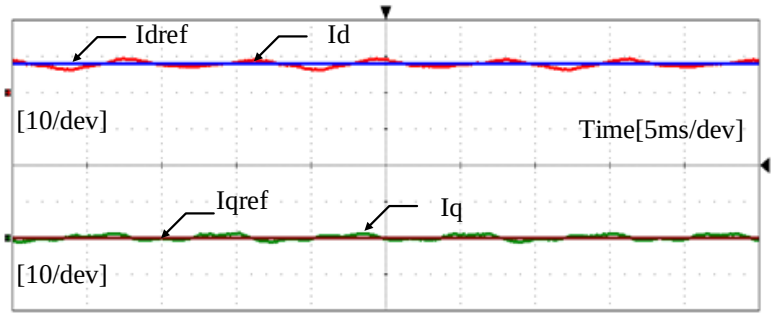


Figure 4.15: Actual and reference d-q values of proposed differential inverter.

Fig. 4.16 shows the FFT for the experimented grid-current of the SEPIC-BDI at full power $1.6kW$. The proposed control technique enhances the waveforms by reducing the NSHC to diminutive values. The percentage of NSHC is 0.624%.

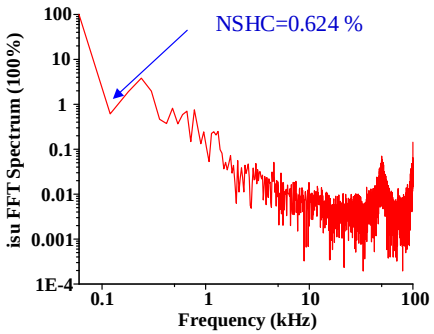


Figure 4.16: FFT analysis of the differential inverter's injected grid-current at full power.

Fig. 4.17 shows the THD values of the output grid-current for this power injected range. At full power, the THD is 3.86%. The THD is lower than 5% in the most different input DC voltage and different load conditions with maximum value 4.99% at 200W.

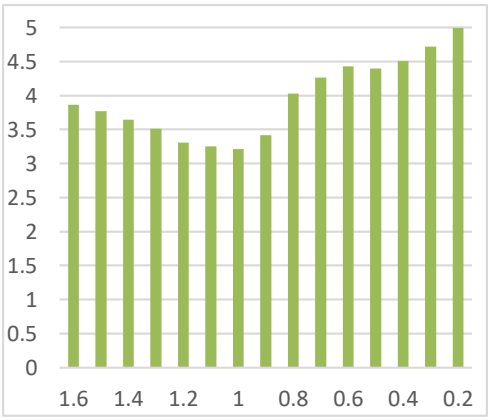


Figure 4.17: THD analysis of differential inverter's injected grid-current for internal power range.

4.6 Loss Analysis of the Proposed Inverter

The proposed SEPIC-BDI has three identical SEPIC converters with equal power (one-third of total inverter power). Although there is a 120-degree phase shift between them, they have similar duty cycle modulation over one complete cycle with the same peak, average, and valley value. Therefore, power loss distribution is also the same. This section shows the loss distribution of one SEPIC converter. It has split among the following components.

4.6.1 MOSFET Devices

The main switch S_{mx} and body-diode of the synchronous switch S_{rx} process the inverter power in the first half of line-frequency cycle $T_L/2$ or $0-\pi$ and produce conduction and switching loss. On the other hand, the synchronous switch S_{rx} and the body diode of the main switch S_{mx} process the power in the second half $T_L/2$ or $\pi - 2\pi$. To ease the power loss calculation, the conduction and switching loss are calculated depend on the switching-frequency T_s. Then the power losses are averaged over the line-frequency T_L. Therefore, the conduction loss over one switching cycle T_s of the MOSFET switch is obtained from equation (4.5) and can be given as [158]:

$$P_{cond}(t) = R_{dson} d_x(t)[{I_D}^2 + \frac{{\Delta i_D}^2}{12}] \quad (4.5)$$

Where, R_{dson} is the switch on-resistance, $d_x(t)$ is the duty cycle at this instant. I_D is average drain current over one cycle, and, Δi_D is the ripple component of switch current. Also, the switching loss can be obtained as [59]:

$$\left.\begin{aligned} P_{sw}(t) &= P_{swon} + P_{swof} + P_{coss} \\ P_{swon}(t) &= \frac{1}{6} t_{rise} F_{sw} V_{ds} \left[I_D - \frac{\Delta i_D}{2} \right] \\ P_{swof}(t) &= \frac{1}{6} t_{fall} F_{sw} V_{ds} \left[I_D + \frac{\Delta i_D}{2} \right] \\ P_{coss}(t) &= 0.5 \ C_{oss} {V_{ds}}^2 \end{aligned}\right\} \quad (4.6)$$

In (4.6),t_{rise},t_{fall},C_{oss}, are the rise-time, fall-time and drain-source capacitance of the switch, respectively. All previous parameters were found in the datasheet of the switch. Moreover, the conduction loss of the body diode can be obtained as:

$$P_{cond}(t) = d(t) I_F V_F \quad (4.7)$$

The switching loss of body diode can be obtained as:

$$\left.\begin{aligned} P_{sw}(t) &= P_{swon} + P_{swof} + P_{Qrr} \\ P_{swon}(t) &= t_{dead} F_{sw} V_F \left[I_F - \frac{\Delta i_F}{2} \right] \\ P_{swof}(t) &= t_{dead} F_{sw} V_F \left[I_F + \frac{\Delta i_F}{2} \right] \\ P_{coss}(t) &= 0.5 \ V_{ds} F_{sw} Q_{rr} \end{aligned}\right\} \quad (4.8)$$

Table 4.4: Calculated average voltages and currents of the SEPIC converter.

Component	I_d or I_F	ΔI_d or ΔI_F	$d(t)$	Conduction period
Main Switch S_{mx}	$\frac{ni_{sx}}{1-d(t)}$	$\frac{d_x(t)V_{dc}}{(L_x+L_{mx})F_{sw}}$	$d_x(t)$	0-π
Synchronous Switch S_{rx}	$\frac{ni_{sx}}{1-d(t)}$	$\frac{d_x(t)V_{dc}}{(L_x+L_{mx})F_{sw}}$	$1-d_x(t)$	$\pi-2\pi$
Body diode of Main switch	$\frac{ni_{sx}}{1-d(t)}$	$\frac{d_x(t)V_{dc}}{(L_x+L_{mx})F_{sw}}$	$1-d_x(t)$	$\pi-2\pi$
Body diode of Synchronous switch	$\frac{ni_{sx}}{1-d(t)}$	$\frac{d_x(t)V_{dc}}{(L_x+L_{mx})F_{sw}}$	$d_x(t)$	0-π

In (4.7) and (4.8), I_F is average forward current over T_s,V_F is the forward-voltage of the body-diode, Δi_F is the ripple component of diode current, t_{dead} is the dead time between main and synchronous switch of the SEPIC converter, and Q_{rr} is the reverse recovery charge of the diode. Table 4.4 states the previously calculated parameters of switches and their body diodes and their connected operating period.

4.6.2 Input Inductor

The inductor losses are generated from magnetic core losses and winding conduction losses. The winding conduction loss is a function of DC resistance of inductor wire R_{dcr} and AC resistance R_{acr} that indicting the proximity effect of inductor wire at switching-frequency. This loss can be obtained as [159]:

$$P_{cond} = {I_{lx}}^2 R_{dcr} + \frac{1}{12}{\Delta i_{lx}}^2 R_{acr} \quad (4.9)$$

Generally, R_{dcr} and R_{acr} of inductor can be determined using inductor test at switching frequency.

The magnetic core loss of inductor P_{core} depends on the maximum ac flux density B_m and the used switching frequency F_{sw} , and the volume of the core and usually obtained by Steinmetz equation to be [116]:

$$P_{core} = k f^{\alpha} B^{\beta} A_c l_m \quad (4.10)$$

Where, A_c is the cross-sectional area of the core, $l_m$is the core mean magnetic path length. α, β are constants and obtained from the datasheet of the utilized core.

4.6.3 HFT

The losses of the HFT transformers are separated into core losses and conduction losses. Conduction losses introduced from the primary and secondary resistances of the HFT transformer wires R_{pri}, R_{sec} [158]. They are calculated as

$$P_{cond} = [\frac{V_{pri} d_x(t)}{(L_{mx}+L_{pri})F_{sw}}]^2 R_{pri} + [\frac{V_{sec} d_x(t)}{(L_{mx}+L_{sec})F_{sw}}]^2 R_{sec} \quad (4.11)$$

Where, V_{pri}, V_{sec} are the primary and secondary voltages of HFT, L_{pri}, L_{sec} are the primary and secondary winding inductances. Moreover, the core losses can be obtained using equation (4.10).

4.6.4 Coupling and Output Capacitors

From (4.12) and (4.13), the power losses of both capacitors are obtained as:

$$P_{closs} = \frac{1}{12}\left[\frac{ni_{sx}d_x(t)}{C_xF_{sw}}\right]^2 R_{esr} \quad (4.12)$$

$$P_{closs} = \frac{1}{12}\left[\frac{i_{sx}d_x(t)}{C_{ox}F_{sw}}\right]^2 R_{esr} \quad (4.13)$$

Where, R_{esr} is the ESR resistance of the capacitor. Finally, the losses of other components such as control circuit, snubber circuit of HFL transformers and connecting wires can be obtained from [59, 158-162].

4.7 Efficiency Profile of the Proposed Inverter

The power loss distribution for the proposed inverter topology has been carried out based on the theoretical calculation derived in previous section. The semiconductor devices, inductors, HFT transformer, and capacitors are modeled using their datasheets. Table 4.5 gives the power loss of all components for one SEPIC converter together with the calculated efficiency with an output power of $533W$. Then the power of proposed inverter equal to $1.6kW$ using one SEPIC converter per phase.

Moreover, the variation of efficiency against injected output power with loss calculation using mathematical, simulation and experimental measurements are shown in Fig. 4.18. The maximum experimental efficiency of the SEPIC-BDI is 89.744% at the output power of $700W$. As the output power increases, the efficiency decreases to 86.4% at full rating of the proposed inverter$1.6kW$. Finally, the developed mathematical analysis of power-loss with simulation and experimental measurements have the following important notices:

- ✓ The experimental efficiency is the lowest due to parasitic components of SEPIC-BDI.
- ✓ These parasitic is hard to calculate it or even measures it. However, the theoretical calculation is still beneficial because it gives us an in-depth investigation of the power-loss distribution and behavior of proposed inverter.
- ✓ Finally, the mismatch between simulation, experimental and theoretical calculations is small and acceptable. And the slope of theoretical calculation is matched with experimental measurements.

✓ This small drop is due to the accuracy of loss modeling derived at previous section.

Table 4.5: Calculated Power loss distribution of one SEPIC converter at Proposed Inverter topology.

component	P_{cond}	P_{Sw}	total
Main Switch S_{mx}	6.351	3.666	10.017
Body diode of main Switch S_{mx}	2.310	1.335	3.645
Synchronous Switch S_{rx}	1.558	1.429	2.987
Body diode of Synchronous Switch S_{rx}	4.739	1.884	6.623
component	P_{cond}	P_{core}	total
Input Inductor L_x	10.250	8.000	18.250
HFL transformer	11.235	8.184	19.437
Coupling capacitor C_x	0.007		
output capacitor C_{ox}	0.002		
Snubber circuit	2.2		
Grid inductance	3.07		
Control and gate drives	0.883		
Total power loss and output Power W	67.121	533	
Efficiency	87.406%		

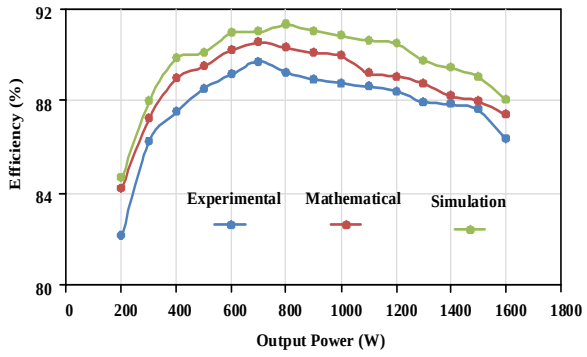


Figure 4.18: Efficiency of the SEPIC-BDI at different output power and $Vdc = 100V$.

Chapter 5: Modular Differential Inverter: Analysis and Experimentation

5.1 Introduction

The recent increase in PV modules at PV module architecture is normal to expand the system's power generation, especially at grid-connecting PV residential applications. Therefore, many inverter topologies have been widely investigated to process more power through power scalability without any additional complexity for the existing PV architecture. Regarding this, only modular inverter topologies are capable of doing this function efficiently. Moreover, the micro-inverter's most important feature is the power flexibility between MII and String inverter, as discussed in many literary works.

The design and control technique of the proposed SEPIC-BDI and its modular technique at Modular Differential Inverter (MDI) for high power application is presented in this chapter. The operation of the MDI has been described mathematically, considering input-parallel output-parallel SEPIC modules in each phase. A design example based on a three-phase MDI is then carried out in PSIM simulation software. It considers a ±20% mismatch between the parallel modules of each phase to investigate system performance in the case of unsymmetrical modules. Finally, a comparison study of the proposed inverter with similar topologies are also presented.

5.2 Proposed Modular Differential Inverter MDI

Generally, a grid-connected MDI is composed of n DC-DC modules (It's called modules in this chapter to differentiate between MDI and traditional differential inverter) per phase, as illustrated in Fig. 5.1. These modules are connected in an Input-Parallel Output-Parallel (IPOP) configuration. For a three-phase grid, the phases are connected differentially. More modules ($n > 1$) are required when the processing power at each phase is larger than the rated power of the utilized modules. In other words, the MDI processes high power using $3 * n$ small DC-DC modules.

Fundamental operation of a MDI depends on driving DC-DC modules with a variable duty cycle like the normal circuit of differential inverter discussed in previous chapters (3 and 4). This duty cycle produces an AC output voltage with a common DC offset. It is

worth noting that this offset will appear at the common point, C, as shown in Fig. 5.1. Unlike conventional DC-AC circuits, this DC offset comes from the unipolar operation of DC-DC modules and was cancelled out by the three-phase differential connection at the grid side. The derived DC-DC modules of the same phase have a 0° phase shift, whereas the DC-DC modules of different phases have a 120° phase shift.

According to Fig 1, the phase voltages and phase currents of a balanced three-phase grid is given as follows:

$$\begin{bmatrix} e_{su}(t) \\ e_{sv}(t) \\ e_{sw}(t) \end{bmatrix} = e_m \begin{bmatrix} sin(\omega t) \\ sin\left(\omega t - \frac{2\pi}{3}\right) \\ sin(\omega t + \frac{2\pi}{3}) \end{bmatrix} \tag{5.1}$$

$$\begin{bmatrix} i_{su}(t) \\ i_{sv}(t) \\ i_{sw}(t) \end{bmatrix} = i_m \begin{bmatrix} \sin(\omega t) \\ \sin\left(\omega t - \frac{2\pi}{3}\right) \\ \sin\left(\omega t + \frac{2\pi}{3}\right) \end{bmatrix} \tag{5.2}$$

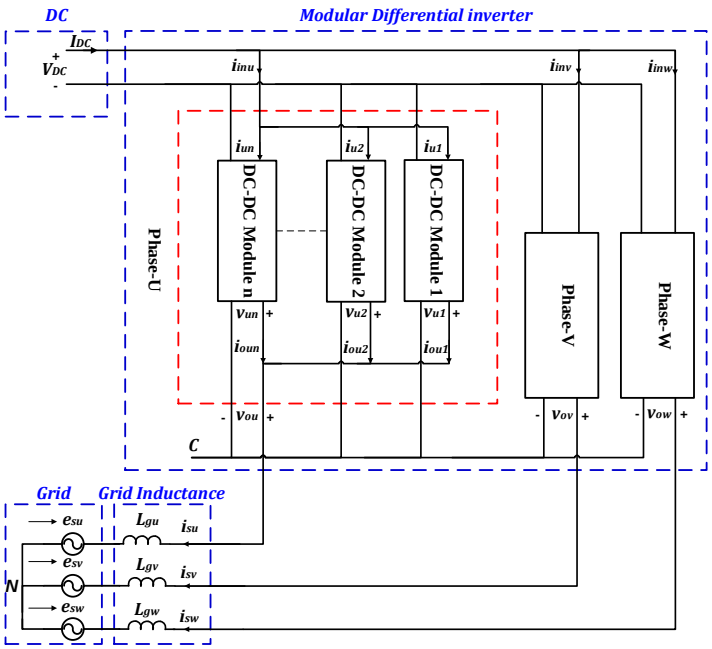


Figure 5.1: Main Circuit of proposed single-stage three-phase MDI.

Where e_m presents the maximum phase voltage, i_m presents the maximum phase current, and ω indicates the line-frequency. The simplest version of a MDI has one DC-DC module per phase for processing the power. The power of each module changes

instantaneously with line-frequency. However, all phases process the same average power, and all modules have the same peak and valley power, and work in a symmetrical operation. The only difference comes from the introduced phase shift of 120○.

To obtain a voltage step-up, any bidirectional boost or buck-boost DC-DC module can be utilized. The voltage gain and current gain of a DC-DC boost converter is obtained as:

$$\frac{v_{mx}}{V_{DC}} = \frac{i_{mx}}{i_{omx}} = \frac{1}{1-d_x} \tag{5.3}$$

The voltage and current gain of the DC-DC buck-boost converter is:

$$\frac{v_{mx}}{V_{DC}} = \frac{i_{mx}}{i_{omx}} = \frac{d_x}{1-d_x} \tag{5.4}$$

As demonstrated in Fig. 5.1, v_{mx} represents the instantaneous output voltage of the associated DC-DC module, x, in Phase m. Here, x indicates the number of DC-DC modules in each phase ($x = 1,2,3, \ldots . n$), while m indicates the associated phase ($m = u, v, and\ \ w$). For example, v_{u1} presents the instantaneous output voltage of the first DC-DC module at phase u . The same scenario can be applied for input and output currents, e.g., i_{u1}, i_{ou1} represent the input and output currents of the first DC-DC module at phase u, respectively. V_{DC} is the DC input voltage and d_x is the duty cycle of this module.

For MDI, the total input current of one phase can be expressed as follows:

$$i_{inm} = \sum_{x=1}^{n} i_{mx} \tag{5.5}$$

For all phases, the total input current can be expressed as follows:

$$I_{DC} = i_{inu} + i_{inv} + i_{inw} \tag{5.6}$$

On the other hand, the output voltages of the modules of one phase are equal and can be expressed as follows:

$$v_{m1} = v_{m2} = \ldots . . v_{mn} = v_{om} \tag{5.7}$$

For all phases, it worth mentioning that the RMS value of the output voltages are similar due to IPOP configuration. The phase current of grid can then be expressed as follows:

$$i_{sm} = \sum_{x=1}^{n} i_{omx} \tag{5.8}$$

Many modulation strategies were presented for the control of differential based inverters. It worth noticing that a simple modulation strategy, without additional feedforward sensing and complicated calculations, is required for an MDI. Therefore, the proposed modulation MCMS employed in Chapter 3 is used in this work, as it provides static

linearization and suits modularity. Moreover, it can be applied to boost and buck-boost DC-DC modules. From (5.4), the duty the duty cycle can be expressed as follows:

$$d_x = \frac{v_{mx}}{v_{mx}+V_{DC}} \tag{5.9}$$

As presented in Fig. 5.1, the differential inverter produces two voltage components at the output terminal of the DC-DC module: the DC common voltage v_{Do} and an AC voltage. For ideal operation, it is worth noticing that this common voltage is equal at all modules, despite the connected phase. The output voltage of the utilized module can then be simplified to

$$v_{mx}(t) = v_{Do} + e_{sm}(t) \tag{5.10}$$

Where $e_{sm}(t)$ is the associated phase voltage connected to the module (5.1). Since both components come from the same module, they have the same voltage gain. The output voltage from (5.10) can then be expressed as follows:

$$v_{mx}(t) = MV_{DC} + MV_{DC}K = MV_{DC}(1 + K) \tag{5.11}$$

At (5.11), M represents the accurate static gain of the differential inverter. Term K is the sinusoidal differential constant of the output voltage that introduce the behavior of grid and can then be expressed as follows:

$$K = \begin{bmatrix} \sin(\omega t) \\ \sin\left(\omega t - \frac{2\pi}{3}\right) \\ \sin(\omega t + \frac{2\pi}{3}) \end{bmatrix} \tag{5.12}$$

By comparing (5.3), (5.4), (5.10) and (5.11), the actual static voltage gain of MDI can be outlined as follows:

$$M = 0.5\frac{v_{mx}(max)}{V_{DC}} \tag{5.13}$$

The maximum value of v_{mx} is defined at $K = 1$. From (5.13), MDI gain, M, presents the half of the maximum voltage gain of the utilized DC-DC module, e.g., if the maximum voltage gain of the utilized DC-DC module is 4, then the maximum possible static gain M is 2. Practically, the voltage gain is reduced by the voltage drop of the parasitic components of the DC-DC modules. Therefore, it is imperative to use DC-DC modules with small parasitic components. By substituting equations (5.10), (5.12) into (5.9), the duty cycle of the utilized DC-DC module can be given as:

$$d_x(t) = \frac{M(1+K)}{M(1+K)+1} \tag{5.14}$$

It is worth noticing that MDI's duty cycle modulation is typical of the conventional differential inverter's duty cycle modulation (expressed in Ch. 3 and 4). This feature is critical because it facilitates power expansion without any extra complication for the modulation circuit. From (5.14), the duty cycle of the associated DC-DC module x depends on two different variables; the gain of the MDI, M, and the associated connected phase, K. Thus, this modulation supports the modularity of the MDI and each of the utilized DC-DC modules will work independently. Moreover, the control structure does not require major changing if using the MDI at a greater power.

Since the boost DC-DC modules working at MDI, their input current, according to (5.3) and (5.14), can be derived as follows:

$$i_{mx}(t) = 0.5Mi_{omx} + i_{omx}(M+1)K - 0.5Mi_{omx}K_2 \tag{5.15}$$

According to (5.4) and (5.14), the input current of buck-boost DC-DC modules working at MDI is outlined as:

$$i_{mx}(t) = 0.5Mi_{omx} + i_{omx}MK - 0.5Mi_{omx}K_2 \tag{5.16}$$

In both, term, K_2 represents the sinusoidal differential constant of input current for associated DC-DC modules and can be expressed as follows:

$$K_2 = \begin{bmatrix} \cos[2(\omega t)] \\ \cos[2\left(\omega t - \frac{2\pi}{3}\right)] \\ \cos[2\left(\omega t + \frac{2\pi}{3}\right)] \end{bmatrix} \tag{5.17}$$

The term, K_2, accurately describes the circulating current between different phases at the differential inverter. This circulating current is evaluated at the double frequency because a reverse current circulates instantaneously from the other two phases in each cycle of grid frequency, as shown in Fig. 5.1. This constant should be considered during the design process of DC-DC modules in order to achieve proper operation of the MDI. Based on (5.15), the input power of the boost DC-DC modules used at the MDI is obtained as follows:

$$p_{inmx}(t) = 0.5MV_{DC}i_{omx} + V_{DC}i_{omx}(M+1)K - 0.5MV_{DC}i_{omx}K_2 \tag{5.18}$$

Using the same process for buck-boost based DC-DC modules, according to (5.16), the input power is expressed as follows:

$$p_{inmx}(t) = 0.5MV_{DC}i_{omx} + V_{DC}i_{omx}MK - 0.5MV_{DC}i_{omx}K_2 \quad (5.19)$$

5.3 Performance of proposed SEPIC modules at MDI

Since the MDI converts power between a DC source and the grid, its parallel DC-DC modules should maintain the objectives of micro-inverters which discussed in Ch. 2. DC-DC modules having a two-switch structure are preferred for achieving low component counts and a high efficiency and can work within the maximum possible duty cycle range of $0.0 < d_x < 0.9$. From (5.3), (5.4), and (5.13), Fig. 5.2 shows the voltage gain and possible maximum static gain, M of the MDI, utilizing boost and buck-boost modules, respectively. It worth mentioning that both of them have an approximate static gain.

In perspective of voltage and current stress, according (5.11) and (5.14), and assuming $V_{Dc} = 100V$, $200V$ line-line voltage and $1.6kW$. Fig. 5.3 illustrates duty cycle, output voltage, switches' voltage and current stress of boost and buck-boost modules. Here, the static gain M and equivalent output resistance R_{mx} are assumed 2.0 and100Ω, respectively. S_{mx}, S_{rx} are the complementary switches of these modules . Notice that the voltage stress is equal for both types. However, the current stress of both switches is lower in buck-boost modules.

The continuous input current is an important factor for renewable energy DC sources, such as PVs. This will add two important features. Firstly, the input inductor of these modules prevents issues related to the short circuit current.

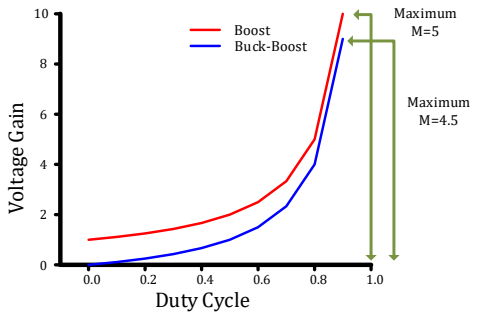


Figure 5.2: Voltage gain of boost and buck-boost modules and MDI static gain at possible duty cycle range.

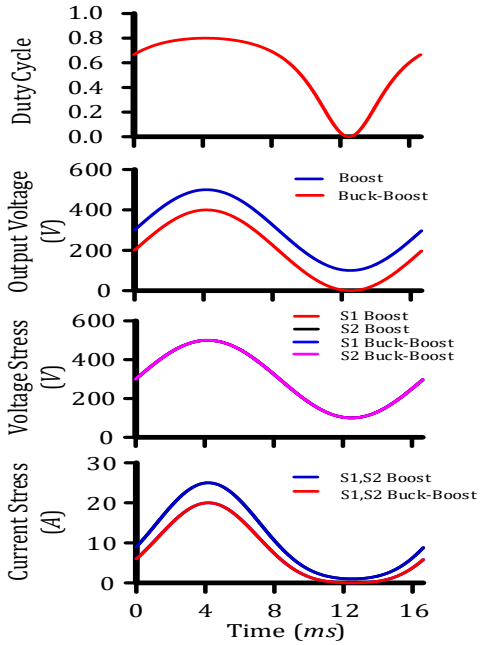


Figure 5.3: Duty cycle, output voltage, voltage and current stress of boost and buck-boost DC-DC modules at one cycle of line-frequency.

Secondly, it eliminates the large electrolyte input capacitor integrated between the DC source and the MDI, required to decrease the switching ripples [19, 30, 33, 36,87 and 124].

From this point of view, boost converters and other buck-boost converters, such as Cuk and SEPIC, are preferred due to their continuous input current. From (5.15) and (5.16), input current stress on the DC source for both modules is illustrated in Fig. 5.4 at $i_{omx} = 8A$. Obviously, buck-boost converters have a lower input current stress.

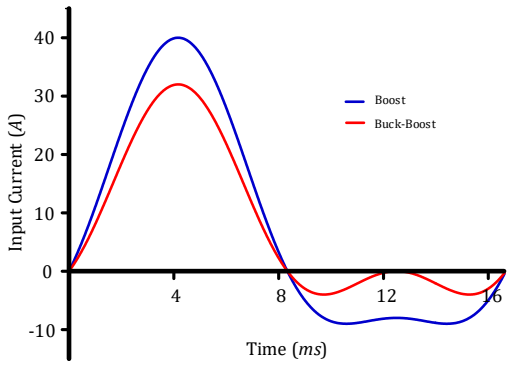


Figure 5.4: Input current of boost and buck-boost modules at differential inverter on one cycle of line-frequency.

According to the grid, voltage isolation is important for CMV and EMI. This feature is accomplished by using HFT-based DC-DC converters such as SEPIC, Cuk, and flyback. Moreover, HFT based topologies are better for low DC current injection. Finally, the THD of the grid-current should be within acceptable limits, which depends on the MDI control rather than the utilized DC-DC modules.

Based on the previous discussion, SEPIC and Cuk converters are preferred. Furthermore, the SEPIC converter is better in this MDI due to its low component count and the low energy storage of its components [87, 91].

5.4 Design Example of MDI based on Proposed SEPIC Modules

The design process of the proposed SEPIC module is shown in Fig. 5.5. In the case of more than one module per phase, the process should be repeated in the following pattern $n = 1,2, \ldots..$. The boundary conditions are defined by the following points:

- (Maximum n) is restricted by the efficiency of the utilized SEPIC. Efficiency is generally low at low rated power due to high power losses; in particular, switching losses [59, 158-162]. The DC-DC modules in the $100\ \mathrm{V}$ range are most efficient when operated at several hundred watts ($300\ \mathrm{W} \leq \mathrm{Power} \leq 700\ \mathrm{W}$). Similar converters are implemented in modular systems such as data centers, UPSs, and smart grids [163-171].
- (Minimum $n \geq 1$), is restricted by the current standing of the utilized SEPIC. Generally, the voltage gain of any DC-DC module is inversely proportional to the rated current. At high current, the voltage drop will increase and will not provide a sufficient voltage gain for MDI [116, 129-130].

Table 5.1 demonstrates the circuit variables of the presented MDI. The power of, one SEPIC module, per phase can be expressed as follows:

$$P_{module} = \frac{P_{MDI}}{3*n} = \frac{1600}{3*1} = 533.3w \tag{5.20}$$

Form grid specifications, the phase voltage and phase current of each module are $e_m = 163.29\mathrm{v}$ and $i_m = 6.532\mathrm{A}$, respectively. From (5.13), the static gain of MDI can be obtained as follows:

$$M = \frac{163.29+163.29}{2*100} = 1.63 \tag{5.21}$$

The voltage gain of SEPIC Module should be larger than $2 * M$ as shown in Fig 2. Therefore, the design is conducted based on gain $M = 2$ to consider the voltage drop of parasitic components.

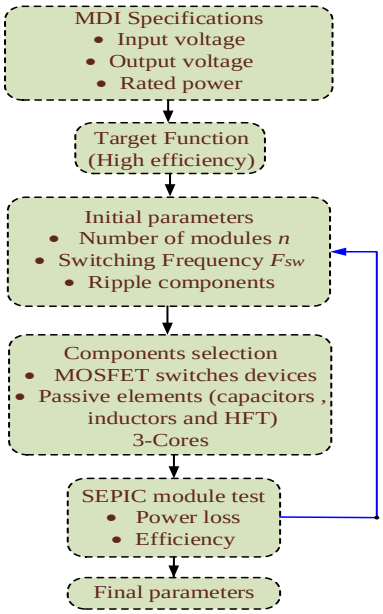


Figure 5.5: Flowchart of the design steps for the proposed SEPIC module utilized in MDI.

Table 5.1: Circuit parameters of MDI.

Rated Power P_{MDI}	4.8kW
Input voltage V_{DC}	100v
Line voltage V_{ll}	200v
Line-frequency F_{line}	60Hz
Switching-frequency F_{sw}	50kHz

5.4.1 Simulation Results

To prove the validity of the MDI proposed control technique, a circuit comprising of nine SEPIC modules is simulated in PSIM software. System parameters of the MDI used in the simulation are recorded in Table 5.1. Three modules of the SEPIC are connected in IPOP in each phase in order to process a triple high power 4.8 kW. A mismatch in components is introduced to investigate the performance of the MDI.

A $\pm 20\%$ parameter mismatch is considered in the DC resistance of the input inductor

for the first and third SEPIC modules in phase u. Fig. 5.6 illustrates the grid voltage, duty cycle (d_u, d_v, d_w), injected grid current (i_{su}, i_{sv}, i_{sw}), reference current, and actual current. The grid current is synchronized with grid voltage. The current is free from NSHC and the DC offset, even at the existing mismatch between phase u and the other phases (phases v and w).

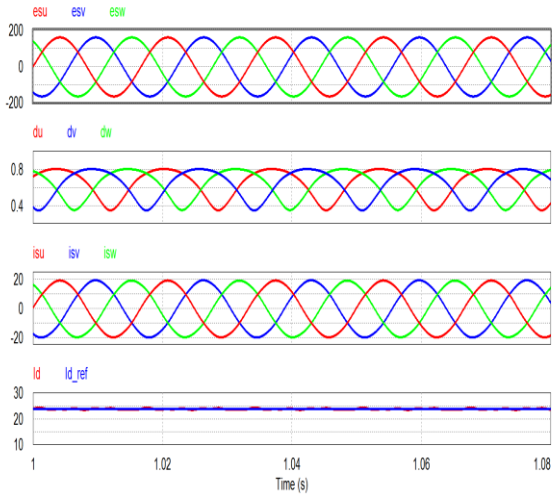


Figure 5.6: Grid voltage, duty cycles, injected grid-current, reference and actual current of MDI.

Fig. 5.7 demonstrates the duty cycles, output voltages and input currents of the SEPIC modules connected at phase u. The existed mismatch does not affect the output voltage due to the grid voltage effect.

The mismatch slightly affected input currents as shown in Fig 5.8. The maximum effect of mismatch results at high duty cycle. The average input-currents are 26.4A, 26.7A and 27.0A for I_{u1} , I_{u2} , I_{u3} respectively. Therefore, the parameter mismatch of 20% resulted in a 0.3A difference of the input current. Otherwise, Table 5.2 shows the maximum mismatch of the input-current and its percentage at $(d_u = 0.8)$ due to $\pm 20\%$ disturbance in the input inductance HFT magnetizing inductance, Coupling capacitor, and output capacitors. In all cases, the three-phase output currents were synchronized with the grid voltage and hence generated low THD.

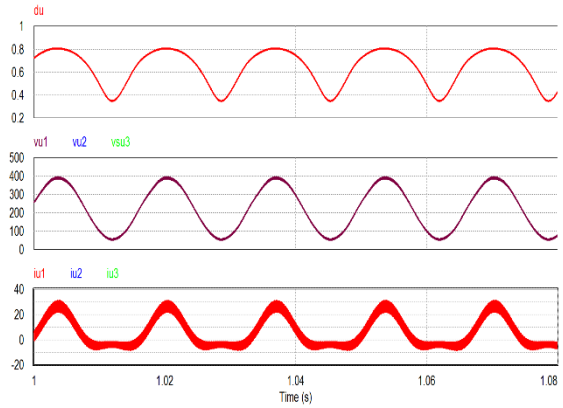


Figure 5.7: Duty cycles, output voltages, input current of SEPIC modules in phase u with $\pm 20\%$.

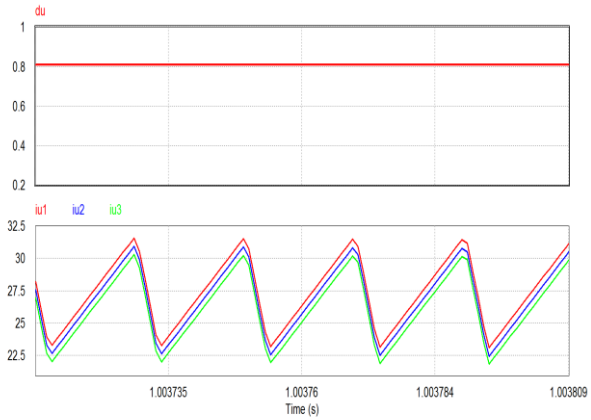


Figure 5.8: Zoomed View of Fig. 5.7 at high duty cycle of SEPIC modules connected in phase u.

5.4.2 Experimental Results

A simplified MDI based on three SEPIC modules is implemented to validate the proposed modules. In this system, only one SEPIC module is used to process the power in each phase. This because the following two reasons

- There is no effect of mismatched modules in the same phase. This finding is validated by simulation results
- The mismatch of modules at different phases can be checked in the simplified MDI based on three SEPIC modules
- The system setup of MDI needs many SEPIC modules and the laboratory experimentation is limited.

Motivated by this, the experimental results, shown in this chapter, concentrated on

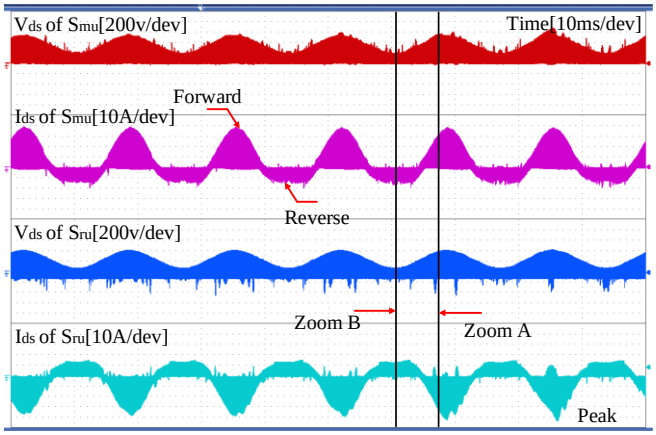
mismatch SEPIC modules and voltage and current stress.

Table 5.2: The maximum mismatch in PSIM at different mismatch cases at $d_u = 0.8$.

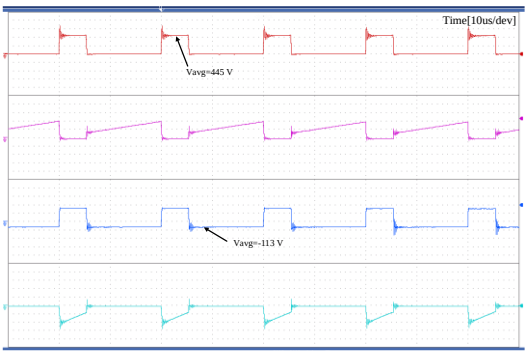
Component	Module mismatch element	Average Input current	Maximum Mismatch &Percentage
Input Inductor	$L_x(u1)$=144 µH	27.8	1A 3.73%
	$L_x(u2) = 180$ µH	26.8	
	$L_x(u3) = 216$ µH	25.9	
Magnetizing inductance	$L_{mx}(u1) = 400\ \mu H$	29.7	0.1A 0.34%
	$L_{mx}(u2) = 500\ \mu H$	29.8	
	$L_{mx}(u3) = 600\ \mu H$	29.9	
Coupling Capacitor	C_x(u1)=11.2 μF	29.8	0.04A 0.13%
	C_x(u2)=14 μF	29.76	
	C_x(u3)=16.8 μF	29.75	
output Capacitor	C_{ox}(u1)=11.2 μF	29.8	0.04A 0.13%
	C_{ox}(u2)=14 μF	29.76	
	C_{ox}(u3)=16.8 μF	29.75	

As previously discussed, the voltage and current switches' ratings should be designed for the worst-case conditions that existed at the peak voltages and currents. This is very important for MDI and SEPIC-BDI presented in Ch. 4 and this chapter. The voltage and current of the primary and synchronous switch are measured experimentally to confirm this effect, as illustrated in Fig. 5.9-a. It is worth noticing that both switches operate simultaneously and achieve two power operations. The inverter manages forward and circulating power efficaciously. The maximum peak voltage of switches has existed at the main switch and equal 700V. This value includes the drain-source voltage, voltage ripple component, and voltage spikes of leakage inductance HFT. On the other hand, the maximum current has obtained at the synchronous switch's body diode and equal 40A. Both voltage and current peaks are limited successfully under intentioned limits because of the snubber circuit, which damps it under the utilized switches' safe operation zones. Fig. 5.9-b shows the switches operation at forward power by zooming Fig 5.9-a (Zoom

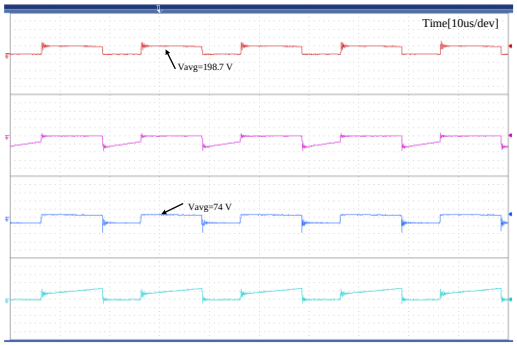
A). The instant duty cycle at this voltage is 0.75. It has validated that the main switch and body-diode process this forward power. Fig 5.9-c shows the switches operation at reverse power by zooming Fig 5.9-a (Zoom B). The instant duty cycle at this voltage is 0.32. The reverse power is diverted by the synchronous switch and body-diode of the main switch. Finally, Fig 5.9-b, c illustrates the effective operation of both switches at switching frequency, which proves the excellent performance and the designated gate drives of the proposed SEPIC-BDI.



a. Switching performance at grid frequency range.



b. Zoom A: switching frequency at forward power.

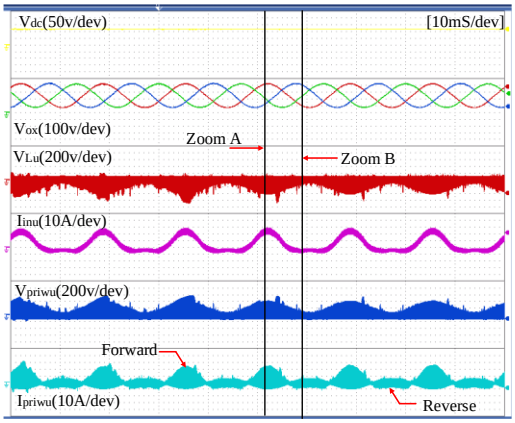


c. Zoom B: switching frequency at reverse power.

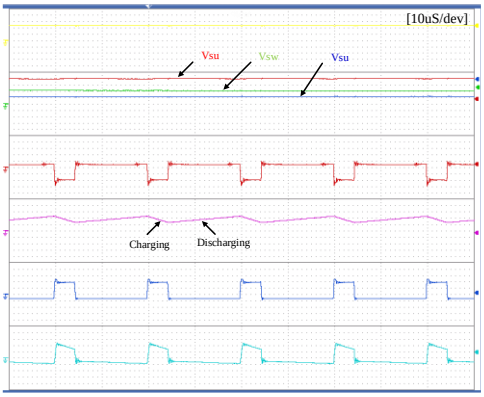
Figure 5.9: Experimental voltage and current stress of utilized MOSFET switches at proposed differential inverter.

Fig. 5.10 displays the voltage and current of input inductor and HFT at grid-frequency and switching-frequency. Both magnetic elements operate simultaneously (forward and reverse power). They manage forward and reverse power by charging and discharging

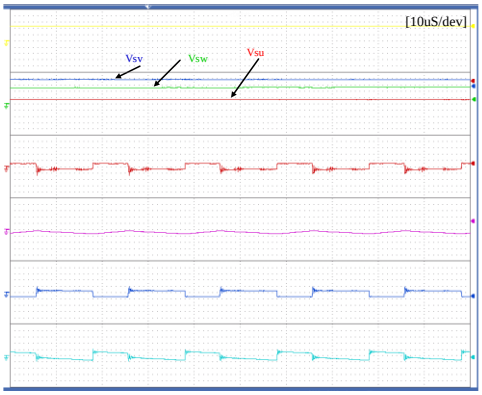
states. The maximum peak voltage and the maximum peak current of the input inductor are 666V and 28.7A. The maximum peak voltage and the maximum peak current of HFT are 567V and 29A.



a. Magnetic elements performance at grid frequency range.



b. Zoom A: switching frequency at forward power (Mode-A).



c. Zoom B: switching frequency at revers power (Mode-B).

Figure 5.10: Experimental voltage and current stress of utilized inductor and HFT at proposed differential inverter.

It is worth noticing that these worst-case of voltages and current conditions that include the average values, ripple components, and switching voltage and current spikes are under the saturation limits set during these magnetic elements' design process, as presented in Ch. 3.

Fig 5.10-b exhibits the voltage and current waveforms at forward power by zooming Fig 5.10-a (Zoom A). The instant duty cycle at this voltage is 0.75. It has validated that the

input inductor's voltage equal to the DC input voltage and the primary voltage of HFT at charging and discharging states, respectively. Fig 5.10-c displays the voltage and current at reverse power by zooming Fig 5.10-a (Zoom B). The instant duty cycle at this voltage is 0.355. The inductor current in both charging and discharging states is negative, which indicate the reverse power processing.

Finally, Fig 5.10-b and c show the tight operation of input inductor and HFT at switching frequency. Again, these findings prove the accuracy of the design criteria proposed in Ch.3 and 4 for the proposed differential inverter.

5.5 Discussion, Comparison and Evaluation

In Table 5.3, comparative evaluation between the proposed inverter and state of the art topologies have been carried out in terms of topology, voltage gain, voltage step-up/down ability, different components count and power rating. Also, it includes the feasibility of the topologies for modularity, galvanic isolation, and power efficiency. The proposed inverter requires low number of switches (six switches like the traditional VSI) which is less than the proposed topologies in [67-70], and [78-84]. Furthermore, it does not need any extra diodes like topology proposed in [73-77]. Another exciting benefit of the proposed topology is the galvanic isolation using HFT without any additional switches. Finally, it has an excellent potency to be modular and scale the power for over extension. The switched-capacitors inverters still need improvements in terms of switches, where topologies in [81] and [82] have 8 and 27 switches with many gate drive circuits. It does not have a modular configuration, and the HFT integration is still not investigated.

For Z source inverter topologies, the buck-boosting ability is excellent. However, the Z network's size is still substantial (they have inductors in mHrange) [72-76]. Again, it needs additional components to implement galvanic isolation and modularity. For multi-level inverters, the efficiency is generally high. However, the number of switches is very high and needs large filters due to low switching-frequency operation.

In contrast, Table 5.3 gives a quantitative comparison between the proposed inverter and similar differential inverter topologies. The proposed topology based on SEPIC converters has only three inductors, which is lower than the Cuk topologies (six inductors). Furthermore, the utilized inductors have small values that improve the inverter size.

Although the measured efficiency of the proposed topology is close to proposed one in [89], it has many advantages to enhance it in the future.

Table 5.3: Comparison between proposed inverter and similar topologies.

Topology	Topology	Voltage gain	Power (KW)	Capacitors % inductors	Switches Diodes	Modular	HFL & CMV	Application	Measured efficiency
Ref [81]	Switched Capacitor	Buck-Boost	NA	2 0	8 2	No	No yes	Three-phase	97.4
Ref [82]	Switched Capacitor	Buck-Boost	NA	2 0	27 0	No	No NA	Three-phase	NA
Ref [76]	Z source	Buck-Boost	0.45	2 2	6 1	No	No NA	Three-phase	NA
Ref [172]	Z source	Buck-Boost	1	2 2	6 1	No	No	Three-phase	97.1
Ref[173]	Multi-level	Buck	1.1	5 0	8 6	Yes	No yes	Single-phase	96.3
Ref[85]	Differential	Boost	1.4	3 3	6 0	Yes	No NA	Three-phase	NA
Ref[101]	Differential	Buck-Boost	0.5	3 4	4 2	Yes	No NA	Single-phase	97
Ref[86]	Differential	CUK	2.5	6 6	6 0	Yes	No NA	Three-phase	NA
Ref[87]	Differential	CUK	2.5	6 6	6 0	Yes	yes yes	Three-phase	NA
Ref[99]	Differential	Boost	0.5	2 2	4 0	NO	No NA	Single-phase	NA
Ref[89]	Differential	CUK	0.5	6 6	6 0	Yes	yes yes	Three-phase	91%
Ref[88]	Differential	Buck& 2 SEPIC	0.4	3 3	4 0	Yes	No NA	Three-phase	NA
proposed	Differential	SEPIC	1.6	6 3	6 0	Yes	yes yes	Three-phase	89.744

Table 5.4 summaries the literature work, which eliminates NSHC at differential inverters. The proposed control design provides grid-current control and excludes NSHC by using two control loops. NSHC can be decreased partially by using DCM operation, as reported at [89]. However, this will add higher-order harmonic components (i.e., third, fourth, and extra) that disturb THD, and need extra loops. The DCM Cuk-based differential inverter at [89] needs more loops to decrease THD to acceptable values, as outlined at [94]. Unlike [87], the proposed control eliminates the third-order components using the second loop from the perspective of input current distortion. It is imperative to exclude the third loop, which adds complexity and a computational burden for utilized DSP board. Moreover, it provides accurate mathematical modeling for its association with NSHC, mentioned in Ch. 3. Also, this behavior has been verified using simulations and experiments.

Table 5.4: Comparison between proposed inverter and similar control techniques.

Work		This work	Ref [87]	Ref [89]	Ref [94]
DC-DC Converter		SEPIC	Cuk	Cuk	Cuk
Modulation Scheme		CMS	CMS	DMS	DMS
Control Features	SLB	Yes	Yes	Yes	Yes
	NSHC	Yes	Yes	No	Yes
	No loops	2	3	1	5
THD		4.087	1.2	5.1	4
F_{sw} [kHz]		50	25	125	100

Table 5.5 demonstrates the performance of proposed control techniques in this thesis. It worth noticing that all controllers provide high performance. Moreover, the proposed improved controls (Control-I and Control-II) have low execution time that improves the computational burden of the DSP board. The NSHC is less than 1.6143% that enhances

the THD (less than 5%). Finally, these findings achieve the standards of recent grid codes.

Table 5.5: Comparison between the three proposed control techniques.

Control/ Parameters	Proposed PID control	Proposed Control-I	Proposed Control-II
First Loop	PID	Type-II	PI
Second Loop	LPFs	LPFs	LPFs
NSHC (%)	1.93	1.6143	0.613
Execution time (us)	21.35	19.95	18.04
THD (%)	5.7	4.087	3.86
Static gain M	1.63	1.63	1.36

Chapter 6: Conclusions

6.1 Contribution of This Work

The work outlined in this thesis has made some important contribution in the area of power-electronics in DC-AC micro-inverter circuits, especially, for single-stage three-phase inverter topologies utilized in advanced PV module architectures. The major contribution of this thesis can be highlighted as follows:

- Detailed classification of the published three-phase inverter topologies is presented. This classification is depend on the requirements and standards of the advanced PV module architectures.
- State the advantages of three-phase micro-inverter against single-phase micro-inverter topologies in the recent PV module architectures.
- The interesting topologies for three-phase micro-inverters such as Two-Stage VSI inverters, Single-Stage Z Source Inverters, Single-Stage Switched-Capacitor Inverters and Single-Stage Differential Inverters have also reviewed.
- A three-phase single-stage SEPIC-Based Differential Inverter SEPIC-BDI is proposed. It has three small HFT based SEPIC converters which enhance the power density and power scalability and modularity.
- The modified modulation (MCMS) which provides static linearization for the duty cycle of the SEPIC-BDI is presented with details. It produces a grid output current free form low-order harmonics without any extra harmonic compensation loops.
- A novel mathematical model is proposed for NSHC of the differential inverters. It investigates the NSHC source and its associations with the differential inverters characteristics, such as variable duty cycle, unipolar operation of DC-DC converters, and circulating currents.
- The proposed SEPIC-BDI, design and implementation are also described. It includes the parameters selection, its design criteria, small-signal representation, and the proposed control technique.
- The proposed inverter's simulation and experimental outcomes have been discussed to show the high performance and effectiveness of the proposed inverter.
- A novel two modified control techniques (Control-I, Control-II) has been illustrated to enhance the inverter performance and decrease THD under acceptable

limits.

- In Control-I, a Type-II compensator, which enhances SEPIC converters' stability, is used instead of the PID controller. The proposed Type-II compensator effectively damp the resonance of the SEPIC converter. In the second loop, the NSHC detection circuit added the proposed LPFs is also utilized.
- In Control-II, the proposed Control-I is redesigned to use SEPIC converters' parasitic components to move the right half-plane zeros from the right half-plane to the left half-plane. This critical feature at SEPIC converters reduces the proposed Type-II compensator's order to a conventional PI controller, especially at low static gain M. The new results show tremendous improvements with a small computational burden.
- The proposed SEPIC-BDI results when integrating a small film capacitor at the input DC side is implemented. It clears the high switching harmonics. The power range of the proposed SEPIC-BDI is also investigated to suit PV modules characteristics.
- The proposed inverter efficiency profile is presented with power loss distinction. In this direction, an accurate mathematical losses model is provided to check the proposed inverter's efficiency profile at different conditions.
- The design and control technique of the proposed SEPIC-BDI and its modular technique at Modular Differential Inverter (MDI) for high power application is presented.
- The operation of the MDI has been described mathematically, considering input-parallel output-parallel SEPIC modules in each phase.
- A design example based on a three-phase MDI is then carried out in PSIM simulation software. It considers a ±20% mismatch between the parallel modules of each phase to investigate system performance in the case of unsymmetrical modules. Finally, a comparison study of the proposed inverter with similar topologies are also presented.

6.2 Suggestions for Future Work

In continuation of this proposal, the following points are some suggestions for future work

- The proposed mathematical model reveals that the stress of switches devices and magnetic elements can be enhanced by using novel modulation schemes. This scheme is an improved version of MCMS and DMS modulation scheme.
- To validate the proposed inverter at PV module architecture, implementing MPPT control with inherent partial shading condition circuits should be developed. Also, the voltage and current range of the SEPIC-BDI ought to be tested.
- Check the capability of the proposed SEPIC-BDI for bidirectional power flow should be investigated. Also, the capability to control reactive power control.
- Future work can also be recommended for HFT design and making accurate mathematical analysis for variable duty cycle which include line-frequency variation.

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