Post Growth Annealing of MOVPE-Grown Single Crystal CdTe Epilayers on (211) Si Substrates

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***Abstract*—Effects of cyclic rapid thermal annealing of metalorganic vapor-phase epitaxy grown single crystal CdTe layers on (211) Si substrates are investigated. Typically 5 μm thick CdTe layers were grown directly on the Si substrates after some substrate pretreatments but without growing other intermediate layers, and annealed ex-situ in a flowing hydrogen atmosphere. We varied the anneal temperature from 500 to 1000 ºC, anneal times from 30 to 90s and the number of anneal cycles from 1 to 9. Improvement in the crystal quality was confirmed by the full-width at half-maximum values of double crystal rocking curves for the anneal temperatures between 800 to 900 ºC. Furthermore, the 4.2K photoluminescence measurement and the current-voltage measurements revealed that the conductivity type and the resistivity of the crystals do not change after annealing.**

***Index Terms*—CdTe/Si epitaxy, MOVPE growth, Rapid thermal anneal, X-ray gamma ray detectors**

I. Introduction

EPITAXIALLY grown thick single crystal CdTe layers on Si substrates are promising for development of X-ray, gamma ray spectrometers and large-area imaging arrays operable at room temperature. Epitaxial growth, which is carried out at temperatures lower than the melt-based bulk crystal growth, not only allows a uniform large-area growth but also offers a strict control of electrical properties of the grown crystals with the impurity doping. However, growth of detector-grade single crystal epitaxial layers with sufficient thickness as required for the efficient absorption of targeted X-ray, gamma ray imposes a considerable challenge. For example, detectors operable with photon energies up to 100 keV require 0.1-0.5 mm thick epitaxial layers to absorb the incident photons and to produce detectable output signal. In addition, the large difference in lattice constants and thermal expansion coefficients between CdTe and Si make this heteroepitaxial growth extremely difficult. Without a special substrate pre-treatment and strict control of the growth parameters, the grown layers usually become poly-crystal and easily peel-off from the substrate. There are several reports on the growth of thin (less than 10 μm) CdTe on Si substrates, mainly for the mercury cadmium telluride based infrared detector development [1]-[4]. In those reports, a thin ZnTe and/or Ge buffer layer is grown on the arsenic-passivated Si substrates prior to the CdTe growth in order to obtain the epitaxial growth. This growth technique, however, is not suitable for our X-ray, gamma ray detector development. Our detector is fabricated in a p-CdTe/n-CdTe/n^+-Si heterojunction diode structure and operated in a reverse bias mode by applying a positive bias voltage on the backside contact of the n^+-Si substrate, whereas the top contact on the p-CdTe layer is grounded. The electron hole pairs (EHP) generated due to the incident radiation in our device travel in the vertical direction before being collected at the respective electrodes. Hence, insertion of a ZnTe or Ge buffer layer hinders their movement across the interface.

We are using metalorganic vapor phase epitaxy (MOVPE) growth technique to grow high-quality and thick single crystal CdTe on (211) Si substrates. We have already achieved more than 260 μm thick single crystal CdTe epilayers on 10 x12 mm^2 size (211) Si substrates. Using these epitaxial layers, we further developed detectors in above-mentioned heterojunction diode structure, and demonstrated that the detectors were capable of detecting a resolving energy peaks from a gamma source at room temperature [5]-[7]. We overcame the above mentioned growth challenges by developing a special Si substrate pretreatment process and the crystal growth technique that does not require the ZnTe intermediate layer [5]-[7]. We further scaled up our growth using 25x25 mm^2 Si substrates, and now we can consistently obtain thick and whole wafer single crystal CdTe on these larger-area substrates. However, CdTe crystal quality strongly affects the detector performance. The CdTe/Si interface consists of a high density of the dislocation to relieve the stress resulted due to the large lattice and the thermal mismatch. These dislocations are not only confined at the interface, but propagates deep into the CdTe epilayer by forming threading dislocations deteriorating the crystalline quality. These dislocations when extends in the depletion layer formed between n-CdTe and p-CdTe, act as carrier recombination centers and also increase detector dark current, adversely affecting the detector performances. Hence, improvement of crystal quality by decreasing these kinds of

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structural defects is necessary for the detector performance improvements. In this study we performed post-growth rapid thermal annealing of thin CdTe epilayers grown on the Si substrates. Our aim was to study how the annealing affects the dislocation density near the CdTe/Si interface. Reduction of dislocation density near the interface leads to lower dark currents and improved device performances, when thicker CdTe layers are grown on the top of these annealed layers. Here we report effect of the annealing on the structural and electrical properties of the thin CdTe crystals.

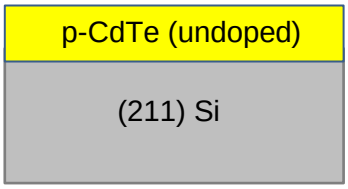

Fig. 1. Sample structure used in this study. The thickness of the undoped p-CdTe epilayer is typically 5 μm.

II. Experimental

CdTe layers were grown on (211) Si substrates using dimethylcadmium and diethyltelluride in a vertical type MOVPE reactor working at an atmospheric pressure. Prior to growth, the Si substrates and some pieces of clean GaAs crystals were placed in a horizontal quartz tube, and annealed at 800 to 900 °C in in a flowing hydrogen environment. This substrate pretreatment removes the residual surface oxide and yields a clean, As and Ga passivated Si substrate, which facilitates the single crystal CdTe growth. The details about Si substrate pretreatment and other growth processes are already described elsewhere [5]-[9]. The substrate temperature for CdTe growth in this study was kept constant at 450 °C for all growth, and the thickness of the layer was maintained at 5 μm. No intentional impurity doing was performed during the growth. These as-grown crystals, however, exhibit a high resistivity around 10^6 Ω cm with a p-type conductivity. Fig. 1 shows the sample structure used in this study. This thickness was chosen to study the crystal properties of the grown and annealed crystals around the CdTe/Si interface by the X-ray diffraction. As the penetration depth of the CuKα1 X-ray (8.04 keV) used in the XRD measurement is around 6 μm in CdTe, this means the CdTe thickness we used allows us to evaluate the crystal property around the interface. Annealing was performed ex-situ in a quartz-tube by placing two samples face-to-face (i.e. CdTe surface of one sample was covered with that of the other sample) in a flowing hydrogen environment. The anneal temperature was varied from 500 to 1000 °C, at different anneal times of 30-90 s and anneal cycles of 1-9. At each anneal cycle, the samples were kept at the fixed temperature for the set value of anneal time, and then allowed to cool to a certain intermediate temperature before starting another anneal cycle. Our aim was to thermally activate the threading dislocations motion so that they get annihilate and/or coalesce by gliding or climbing. As a result a decrease in dislocation density can be expected. The face-to-face annealing was performed to suppress the surface roughening by Cd-evaporation at higher temperatures.

We examined the crystal quality of the epilayers using full-width half-maximum (FWHM) values of X-ray double crystal rocking curve (DCRC) values. This method has been used to measure dislocation density in heteroepitaxial layers [10]. All samples were examined with the XRD before and after annealing to examine the effect on anneal on crystal quality. Lower DCRC FWHM values after annealing indicate improvement in the crystallinity, which can further be related to decrease in the dislocation density. Furthermore, 4.2 K photoluminescence (PL) measurement using a 488 nm excitation from a semiconductor laser, as well as current-voltage measurement (300K) were performed on some samples before and after annealing.

III. Results and Discussion

Several CdTe/Si samples grown at different growth runs, but with identical growth conditions were used. The DCRC FWHM of these 5 μm-thick CdTe sample are in the range of 500-600 arc sec. Fig. 2 shows percentage change (decrease) in DCRC FWHM values of the samples due to annealing at different temperatures. The anneal duration was kept constant at 60 s and number of anneal cycle was 3. At each anneal temperature in this figure, typically four samples were used and their change in FWHM values before and after annealing (in percentage) are plotted with the error bars. All new set of samples were used for different anneal temperatures. Depending upon the intrinsic crystal quality, sometimes a large variation in the anneal effect was observed. We will further discuss it below. Furthermore, no anneal effect was observed at anneal temperatures below 700 °C, while the CdTe surface became rough when the anneal temperature was increased to 1000 °C, or above. The results indicate that an improvement in the crystal quality (FWHM decrease), and hence decrease in dislocation density is observed at anneal temperatures between 800 and 900 °C.

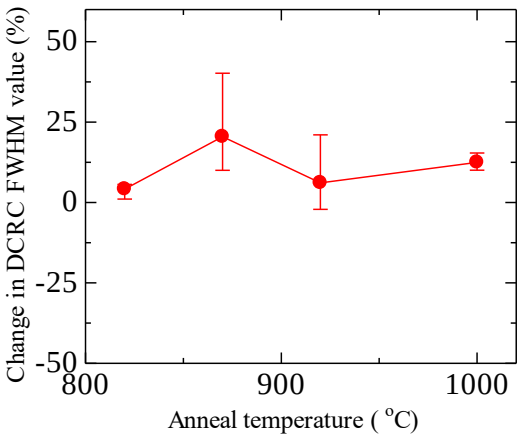

Fig. 2. Percentage change in DCRC FWHM values of the samples before and after annealing at various anneal temperatures. The anneal time and number of anneal cycles were kept constant at 60 s and 3, respectively. The positive value in percentage change corresponds to decrease of FWHM values after annealing when compared to that of non-annealed values.

Shown in Fig. 3 is the effect of anneal duration. The samples were annealed at a fixed temperature of 870 ºC, and the number of anneal cycle was also kept fixed at 3, while changing the anneal time from 30 to 90 s. The result shows annealing at 60 s, a noticeable change in the DCRC FWHM value was observed, implying an improvement in the crystal quality. However at other anneal time the improvement was nil or very small. We further examined effect of annealing by changing the number of anneal cycles, keeping the anneal temperature and duration fixed. The result is shown in Fig. 4, where the DCRC FWHM values of the samples before annealing and after aneling at a fixed temperature of 870 ºC, and anneal duration of 60 s are plotted. An apparent improvement in the crystal quality as revealed by the decrease in the FWHM values was observed at 3 cycles of annealing, however, at higher anneal cycles the improvement was less remarkable.

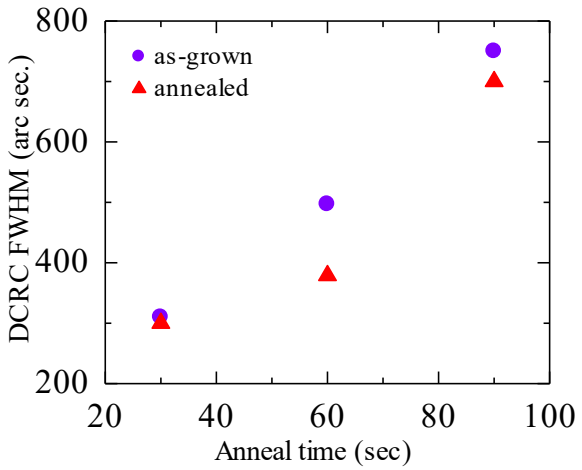

Fig. 3. Comparison of DCRC FWHM values of the samples before and after annealing at different duration. The annealing temperature and number of anneal cycles were kept constant at 870 ºC and 3, respectively.

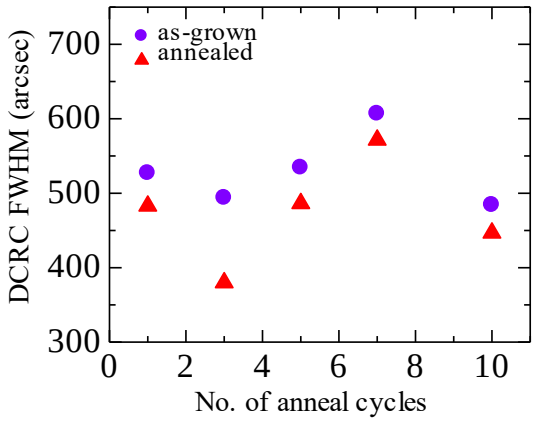

Fig. 4. Comparison of DCRC FWHM values of the samples before and after annealing at different anneal cycles, where the anneal temperature and duration were kept constant at 870 ºC and 60 s, respectively.

We now discuss on the observed variation in the anneal results. Though we are using same growth conditions for each crystal growth, however, depending on the residual stress some samples showed higher, and some showed smaller intrinsic DCRC FWHM values. The low FWHM values of the as-grown samples are considered to be due to spontaneous lattice strain relaxation during the growth process, though the mechanism is not clear. Based on this anneal study, we can say that there is no effect of annealing for samples with initially better intrinsic crystal quality. Also for samples with poor crystal quality, the effect is minimum.

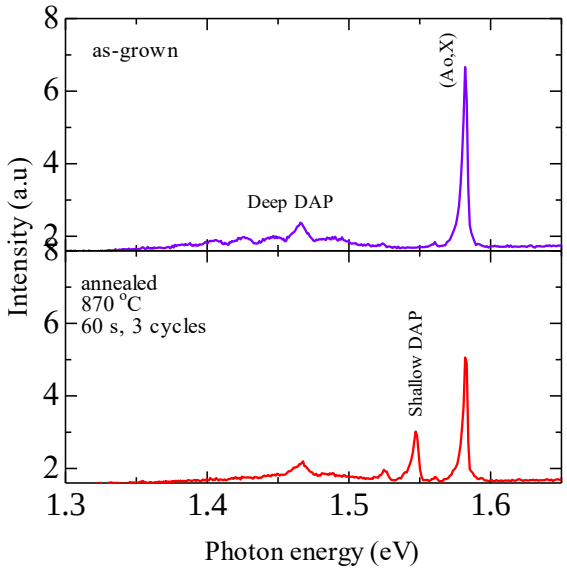

Fig. 5. 4.2 K photoluminescence spectrum of as-grown and annealed CdTe samples.

Finally effect of annealing on the electrical properties of the CdTe epilayer was examined with the 4.2 K PL measurement. Figure 5 shows PL spectrum of CdTe layer before and after annealing. We used CdTe layer that was annealed at 870 ºC, where the anneal time and number of anneal cycles were 60 s and 3 respectively. This anneal condition was found effective in this study as discussed above. The PL spectrum of CdTe epilayer before annealing shows a distinct and high intensity peak at 1.5820 eV with its LO-phonon replica at 1.5607 eV, and low intensity broad luminescence at around 1.47 eV with several phonon replicas. The 1.5820 eV line can be identified as the acceptor-bound-exciton emission (Aº,X), whereas the low intensity band around 1.47 eV is related to structural defects most probably due to dislocations [11], [12]. The position of the dominant peak at 1.5820 eV does not change after annealing (Fig. 5 bottom), indicating the conductivity type of the crystal remains same. The FWHM value of the (Aº,X) emission peak after anneal also improves slightly to 8 meV from its as grown value of 10 meV. However, there are some changes in other peaks. A new peak along with its phonon replica appeared at 1.5471 eV, and peak shape and intensity of 1.47 eV peak slightly changed. The new peak at 1.5471 eV

could be shallow DAP recombination between either shallow donor and V_{cd} acceptors, or shallow donor and substitutional oxygen acceptors [13], [14]. The resistivity measurement of the samples as described below nonetheless suggests V_{cd} formation is less likely the cause here. The slight weakening of the 1.47 eV peak as well as decrease in DCRC FWHM values of the CdTe crystals after annealing suggest the decrease in dislocation as a result of annealing, and/or due to the relax in the lattice strain [12], but it needs further verification by counting the dislocation density in the respective samples. We further measured the resistivity of the samples before and after annealing. The sample that was annealed using the same annealing conditions that were used for sample prepared for the PL measurement showed resistivity essentially the same which was in the order of $10^6\ \Omega$ cm. All other samples annealed with different conditions, also showed similar trends where the max changes in the resistivity before and after anneal were within an order of magnitude. This result indicates the resistivity of the samples can be maintained after annealing. Further electrical property such as mobility, carrier concentrations of the samples could not be evaluated because of their high resistivity and needs to be studied.

Finally we examined the effectiveness of annealing in the detector performance by fabricating a diode-type detector in a p-CdTe/n-CdTe/n^+-Si structure. The n-CdTe epilayer was subjected to a 870 ^{o}C, 60 s, 3 cycle anneal before growing an approximate 40 μm-thick undoped p-CdTe layer on top of it. The initial result of the detector performance does not show clear improvements in the detector leakage current, which was about 0.5 μA/cm^2 for an applied reverse bias of 150 V as well as gamma detection properties. It should be noted that the anneal conditions in this study were investigated on undoped CdTe layer, however, it seems further optimization of anneal conditions for n-CdTe layers and investigation of their electrical properties are needed. Our preliminary results of similar annealing study performed on n-CdTe (iodine doped) layers on Si substrates nonetheless do not show appreciable change in carrier concentration and mobility values. Further investigation on annealing of n-CdTe layers, dislocation density estimation, as well as investigation of annealing effects on detector performance in progress.

IV. Conclusion

We studied cyclic rapid thermal annealing of MOVPE grown thin single crystal CdTe epilayers on (211) Si substrates. Typically 5 μm thick CdTe epitaxial layers were annealed ex-situ in a flowing hydrogen atmosphere. Improvement in crystal properties were observed at anneal temperatures between 800 to 900 ^{o}C as revealed by decrease in the DCRC FWHM values. This suggests the decrease of dislocation density in the crystal near the interface. Furthermore anneal time of 60s and 3 anneal cycles were found optimum in this study. However, no significant effects of annealing was observed for anneal temperatures below 700 ^{o}C. On the other hand crystal surface became somewhat rough at anneal temperature above 1000 ^{o}C. The 4.2 K PL measurement as well as the current-voltage measurements confirmed that conductivity type and the electrical resistivity of the CdTe crystals can be maintained after this annealing procedure.

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