Study of AlGaN/GaN HEMTs on 3C-SiC/LR-Si by introducing a thick nitride layer for RF applications

厚いGaN層を有する3C-SiC/LR-Si上AlGaN/GaN HEMTsのRF応用に向けた研究

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Abstract

The research and development of gallium nitride (GaN)-on-silicon-based technology attracted tremendous attention for RF applications owing to its cost-effectiveness and ability to provide comparable device performance to GaN-on-SiC device technology.

To achieve the requirement, the research presented in this dissertation proceeds from the primary motivation that a thick nitride layer of around 8.0 μm can enhance the device performance than the conventional GaN-on-Si devices. However, there are some critical challenges such as low resistivity of Si, charge carrier generation at high temperatures, and high-frequency transmission loss need to be addressed.

Chapter 1 gives the principal motivation for the work presented in this dissertation. In addition, the working principle of AlGaN/GaN heterostructure and cubic silicon carbide (3C-SiC) structure is briefly explained. Thereafter the outline of this dissertation is given.

In chapter 2, a structure of AlGaN/GaN on 3C-SiC/low resistive (LR)-Si with an introduction of 8.0 μm thick nitride layer is proposed. The crack-free high-quality nitride layer was grown by metal organic chemical vapor deposition (MOCVD). The

buffer layer condition was verified by Hall measurements which showed excellent electron transport characteristics compared to conventional epi-structures. Successful fabrication of AlGaN/GaN high electron mobility transistors (HEMTs) was achieved on the reported epitaxial structure.

In chapter 3, the FET operation in DC was analyzed. The DC drain $I - V$ and transfer characteristics exhibited drain current density of 625 mA/mm with pinch-off characteristics ($I_{\text{on}}/I_{\text{off}} \sim 10^6$). The off-state leakage current was stable at high temperatures and a small degradation of DC performance was observed at high temperatures because of the temperature dependency of mobility.

In chapter 4, a detailed temperature-dependent RF characterization is represented to evaluate the high-frequency performance of the device.

The small-signal RF characteristics of 2-μm gate length devices exhibited cut-off frequency (f_{T}) and a maximum frequency of oscillation (f_{max}) of 4.8 and 10.0 GHz, respectively. The obtained f_{T} attained remarkable competitiveness compared with previously reported results. A primitive study of the frequency response of RF loss was estimated using S-parameter measurements of open pad structures. It exhibited an ideal-like frequency response which confirmed suppression of loss even at the high temperature of 125 °C. At high temperatures, degradation of small-signal performance was observed. It was assumed that temperature dependency of intrinsic properties was solely responsible for the degradation of device performance at a high temperature. This was confirmed by comparing transconductance from S-parameters, calculated f_{T} values and DC characteristics with varying temperature.

The load-pull measurement exhibited 47 % power added efficiency (PAE) while delivering 2 W/mm output power with a linear gain of 17.2 dB for class A amplifier operation. A deterioration of output power and PAE was observed after a drain bias of + 22.5 V because of the current collapse. Temperature-dependent load-pull

measurement exhibited a declination of output power, gain, and PAE. As in our case, the drain bias was fixed at its optimum point, the decrement was mainly because of the deterioration of drain current *i.e* the mobility or the intrinsic property of the device.

In chapter 5, the high-frequency transmission loss evaluation is outlined. The loss was characterized by S-parameter measurements of microstrip lines designed and fabricated on three different epitaxial structures by varying nitride layer thickness (3.2, 5.3, and 8.0 μm). Attenuation constants of all three samples were evaluated which showed that a thick nitride layer can suppress the RF transmission loss compared to the sample with the thinnest nitride layer. EM simulation results also confirmed the above observation. Furthermore, the sample with 8.0 μm thick nitride layer showed minimal loss compared to the sample with 3.2 μm nitride layer at a high temperature of 125 °C.

Chapter 6 concludes the dissertation.

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List of Abbreviations

HEMT	high electron mobility transistor
GaN	gallium nitride
AlGaN	aluminium gallium nitride
MOCVD	metal organic chemical vapor deposition
MBE	molecular beam epitaxy
3C-SiC	cubic silicon carbide
RF	radio frequency
2DEG	two dimensional electron gas
BCl_3	boron tri-chloride
Au	gold
LR/HR-Si	low/high resistive silicon
PR	photoresist

RIE	reactive ion etching
RTA	rapid thermal annealing
$L_{gs}/L_{g}/L_{gd}$	gate-to-source/gate/gate-to-drain length
I_{d}/I_{g}	drain current/gate current
V_{d}/V_{g}	drain voltage/gate voltage
V_{th}	threshold voltage
g_{m}	transconductance
f_{T}	cutoff frequency
f_{max}	maximum frequency of oscillation
PAE	power added efficiency
DE	drain efficiency
P_{out}	output power
TL	transmission line
ML	microstrip line

Chapter 1

Introduction

1.1 History and background of HEMTs

In the 1970s, when the molecular beam epitaxy (MBE) growth technique and modulation doping came into the market, several discoveries started to happen and high electron mobility transistors (HEMTs) was originated as a result of different significant research and discoveries [1]. In parallel, the T. Mimura group at Fujitsu were working on GaAs MESFETs [2] to achieve high-speed performance over Si technology and they produced depletion type MOSFETs using modulation-doped heterojunction superlattice [2]. The T. Mimura group also gave birth to the AlGaAs/GaAs HEMT by introducing a Schottky gate contact over a single heterojunction [3]. With this discovery, Mimura et al. also reported the first HEMT based integrated circuit [4]. Along with the Mimura group, other industrial and academic institutions came into the market with discoveries like AlGaAs/InGaAs pseudomorphic HEMTs (pHEMTs), AlInAs/ InGaAs/InP HEMTs with a target of achieving higher cutoff fre-

quency [5,6]. With this development in research, HEMTs started to converge into the commercial cellular, satellite market along with the military and space applications. With the emergence of metal organic chemical vapor deposition (MOCVD) system, AlGaN/GaN heterostructure based HEMTs on sapphire substrates are made. Consequently, after seeing the potential of AlGaN/GaN HEMTs due to the polarization charges, the research and development shifted to AlGaN/GaN heterostructure [7, 8]. The AlGaN/GaN-based semiconductor technology was then developed and modified by introducing concepts such as field plate, AlN barrier between GaN and AlGaN, double heterojunction structure. With continuous academic and industrial research and development, the GaN market size was valued at 1.65 billion USD last year and it is expected to see a compound annual growth rate (CAGR) of 21.5 % from 2021 to 2028 [9].

1.2 Group-III nitrides: GaN

With the development of semiconductor technologies, group-III nitrides such as aluminum nitride (AlN), gallium nitride (GaN), and indium nitride (InN) are found to have a huge potential in the scientific and technological development of the semiconductor industry [10]. High breakdown voltage and bandgap are some of those criteria that enable them to perform better than the conventional semiconductors in high-power transistors, optoelectronic devices, and more. Group-III compound semiconductors are formed by bonding group-III elements such as boron (B), aluminum (Al), gallium (Ga), or indium (In) with group-V elements such as nitrogen (N), arsenic (As), or phosphorus (P) [11]. These materials and their compounds cover an energy bandgap range of 0.7 eV (for InN), 1.4 eV (for GaAs), 3.4 eV (for GaN) to 6.2 eV (for AlN), as shown in Fig. 1.1 [12, 13]. Initially, in the 1980s, gallium arsenide (GaAs) was the first choice for the high-frequency applications. In the RF or microwave domain, the Si technology was steadily replaced by GaAs FETs, HBTs,

and HEMTs. In wireless technologies such as smartphones, tablets, and Wi-Fi devices, the use of GaAs monolithic microwave integrated circuits (MMICs) was also acknowledged. Having said that, with an increased requirement of higher power and frequency, wide bandgap material GaN is being commercialized and extensively used due to its higher efficiency at millimeter-wave frequencies compared to GaAs along with the ability to provide high power [14].

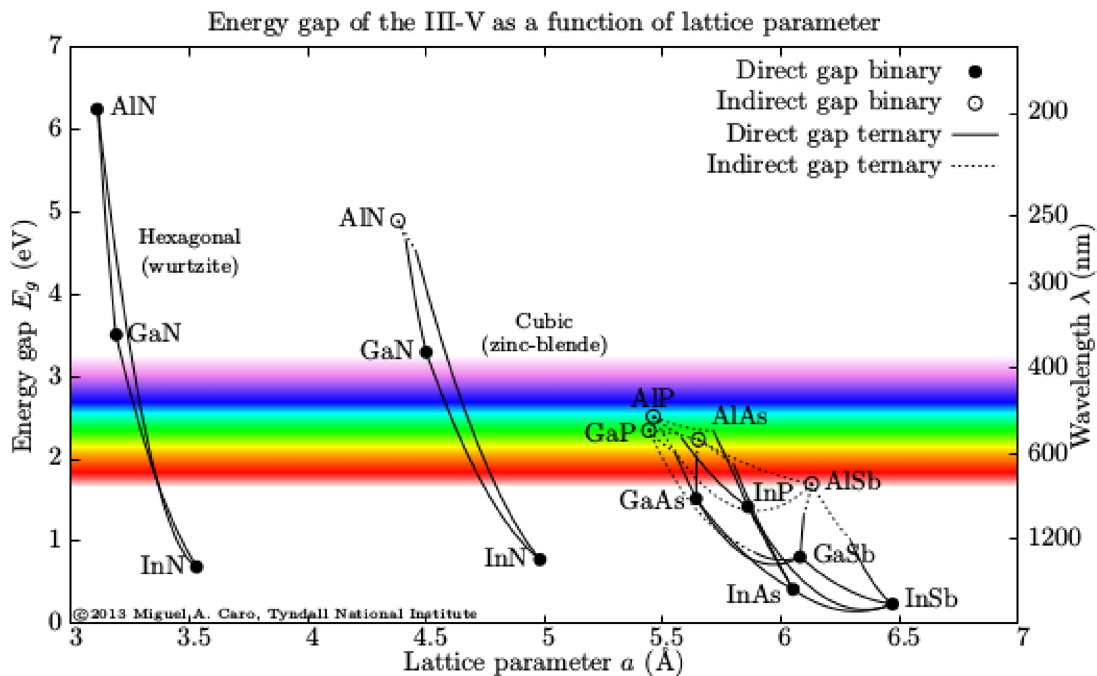

Figure 1.1: Band gaps of the wurtzite III-nitride semiconductors as a function of lattice parameter [12].

GaN semiconductor technology came into the market quite late after the GaAs. Having substantial advantages, they were developed to operate at high-frequency and high-power applications. GaN-based active devices which are used in amplifiers can operate at voltages of + 48 V dc and higher [14]. Owing to that, GaN-based power amplifiers are being used in wireless base stations, military radars, and other high-frequency applications [15–17]. It is established that GaN can provide higher energy and power compared to GaAs. The comparison of properties of conventional

and III-nitrides was summarized in Table 1.1. It can be seen that the saturation velocity, breakdown field, and critical breakdown voltage of GaN are superior to other semiconductors. In addition, having the capacity to operate at high-voltages, GaN-based devices can accommodate to much smaller space than GaAs-based devices. Moreover, having higher thermal conductivity, the power handling capacity of GaN is much higher than GaAs, having the same device structure. Though GaN technology is expensive than usual semiconductor technologies, the properties such as high voltage, large heat dissipation, high efficiency, and performance ability in high-power and high-frequency applications make the extra cost worth it.

Table 1.1: Comparison of properties of different semiconductors in power electronics at 300 K [18].

Properties	Si	GaAs	4H-SiC	6H-SiC	**GaN**
Mobility (μ) (cm^2/V-s)	1500	8500	800	460	2200
Breakdown Field (E_B) (MV/cm)	0.3	0.4	2.4	2.2	3.0
Bandgap (E_g) (eV)	1.12	1.43	2.86	3.02	3.45
Dielectric Constant (ϵ)	11.9	13.1	10.1	9.7	9.5
Drift Velocity ($\nu_{s,max}$) ($10^7 \times$ cm/S)	1	2.0	2.0	2.7	3.0
Thermal Conductivity (κ) (W/cm-K)	1.5	0.46	4.9	4.9	1.7
BFOM[a]	1	14.8	223.1	125.3	186.7
JFM[b]	1	1.8	215.1	277.8	215.1
CFOM[c]	1	7	295	222	290

[a] Baliga's figure of merit is a measure of the specific on resistance of the drift region of a vertical FET.
[b] Johnson's figure of merit is a measure of the ultimate high frequency capability.
[b] CFOM, which can be expressed as $\kappa.\epsilon.\mu.\nu_s E_B{}^2$ / $(\kappa.\epsilon.\mu.\nu_s E_B{}^2)_{Si}$ is Combined Figure Of Merit for high temperature, high power and high frequency applications.

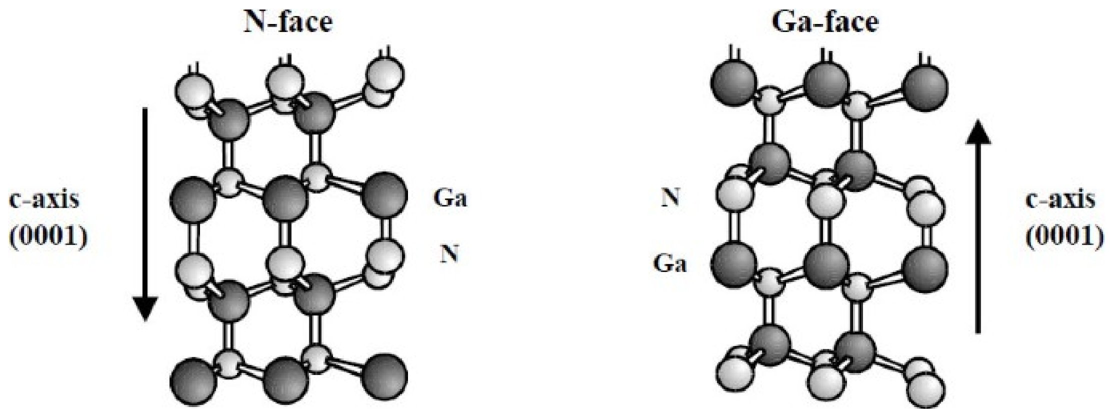

Figure 1.2: Schematic of the wurtzite crystal structure with Ga and N faces. [19].

The most common growth direction of hexagonal GaN is normal to the $(000\overline{1})$ basal plane. In this plane, atoms are arranged in a bilayer that comprises two closely spaced hexagonal layers containing cations and anions. The GaN crystal surface can have either Ga-polarity or N-polarity, as shown in Fig. 1.2, depending on the nucleation layer and the growth method. Polarity is an important factor as it can influence the formation of defects which can affect the device performance [20]. Over the years different growth methods are used to grow GaN films on different substrates. The MBE (molecular beam epitaxy) [21], MOCVD (metal-organic chemical vapor deposition) [22], or HVPE (hydride vapor phase epitaxy) [23] are the techniques that are being used and each of them gives a varying degree of surface roughness and the quality of epitaxial layers. The first report on the epitaxy of GaN was in the year 1969 [24]. GaN layers were primarily grown on the $(000\overline{1})$ sapphire substrates (Al_2O_3). Typically GaN-on-GaN typically is the best choice as it can avoid the problem of hetero-epitaxy. Unfortunately, high prices and large-size wafer unavailability hinder the wide applications. On the other hand, sapphire substrates have a large lattice mismatch with GaN and provide poor thermal conductivity. For that, SiC and Si are the substrates that proved to be effective in GaN-based device technology within which SiC is the most preferable having high thermal conductivity and very low

lattice mismatch to GaN [25]. Nonetheless, SiC substrates are also expensive and unavailable in big-size wafers. Considering that silicon is a very attractive substrate for GaN epitaxy as it offers large wafer availability (12 inches) at a low cost with a good thermal conductivity (1.5 W/cm-K). Moreover, it is believed that GaN-on-Si technology can achieve comparable device performance to GaN-on-SiC technology.

1.3 AlGaN/GaN heterostructure

The wurtzite III-nitrides offer an amazing feature or property of the quantum well formation. A heterostructure or heterojunction is formed between two semiconductors with different energy band-gaps (E_g), permittivities (ϵ_s), work functions ($q\phi_s$), and electron affinities (χ_s) (see Fig. 1.3). When wide and narrow bandgap semiconductors combine, a discontinuity in the conduction band (ΔE_C) and valence band (ΔE_V) occurs. The discontinuity in the conduction band creates a triangular quantum well (shown in blue dashed line in Fig. 1.3). A highly concentrated two dimensional electron gas (2DEG) accumulates in the quantum well that is created near the AlGaN/GaN heterointerface. The reason is a large conduction band discontinuity and built-in piezoelectric (P_{pz}) and spontaneous polarization (P_{sp}) effects in AlGaN/GaN material system. This property makes the AlGaN/GaN heterostructure system suitable for high-power and high-frequency electronics.

The AlGaN/GaN heterostructure is created when the AlGaN barrier (doped or undoped) is grown on a relatively thick GaN layer. There is a lack of symmetry along the C-direction in the tetrahedrally coordinated Wurtzite group III-nitrides. This lack of symmetry along the c-direction and the large ionicity of the covalent bond in wurtzite GaN are the reason for the occurrence of a large spontaneous polarization (P_{sp}) that orients along the hexagonal c-axis. The piezoelectric coefficients of III-nitrides (P_{pz}) are almost an order of magnitude larger than in many traditional III-V semiconductors. Hence, in the case of AlGaN/GaN heterostructure, there are

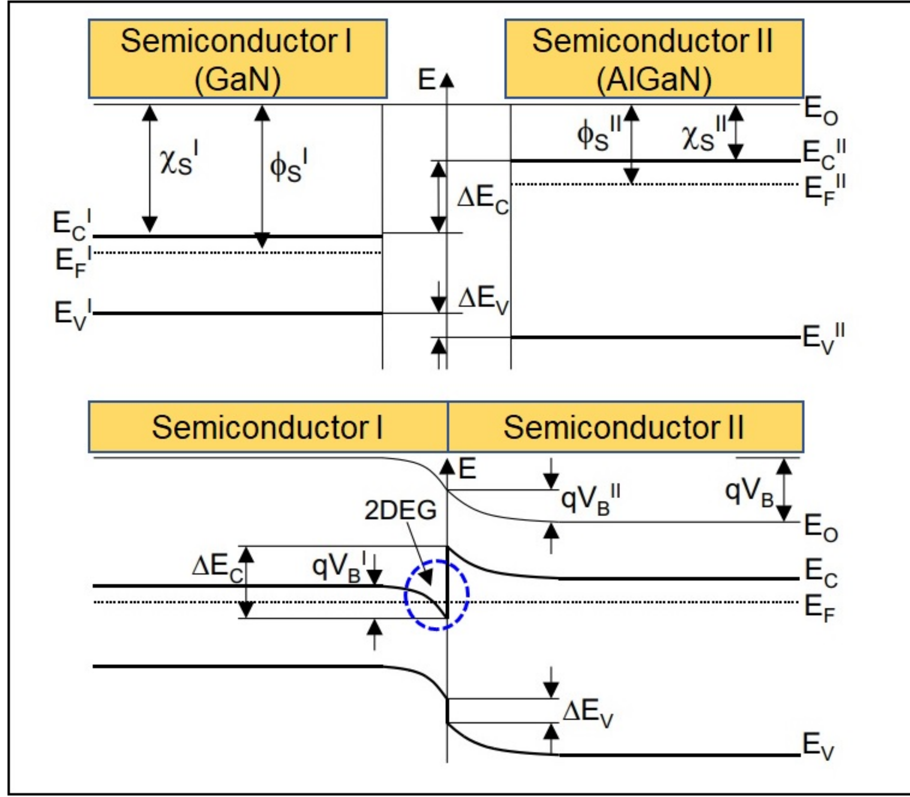

Figure 1.3: Band diagram of a narrow-gap semiconductor (I) (GaN) and a wide gap semiconductor (II) (AlGaN). E_C , E_V, E_F, ϕ_s, χ_s are already mentioned and V_B is the built-in voltage [26].

two sources from which polarization charge arises. The piezoelectric effect by strained AlGaN and the difference in spontaneous polarization between AlGaN and GaN are those two sources of polarization charge. Total polarization of the AlGaN layer is larger than that of the GaN buffer layer. The reason is piezoelectric constants and spontaneous polarization increase from GaN to AlN. Because of that, a positive polarization charge is present at the lower AlGaN/GaN interface (for Ga-face structure). This positive polarization charge is compensated by electrons which in turn creates the 2DEG in the triangular quantum well at the AlGaN/GaN interface and this 2DEG will drop below the Fermi level (E_F) [27].

AlGaN/GaN HEMTs in general exhibit normally-on operation with a negative

threshold voltage (V_{th}). The electrical properties of the heterostructure are determined by the piezoelectric (P_{pz}) and spontaneous polarization (P_{sp}) arise due to the difference in lattice constant between $Al_xGa_{1-x}N$ and GaN.

$$\begin{aligned} P(x) &= P_{pz} + P_{sp} \\ &= \left[\left(3.2x - 1.9x^2\right) \times 10^{-6} - 5.2 \times 10^{-6} x\right] \end{aligned} \tag{1.1}$$

where, $P(x)$ is the net total polarization, and x is an Al composition of the AlGaN barrier [18, 28, 29]. As a result, positive polarization charges are generated that accumulates 2DEG at the AlGaN/GaN hetero-interface.

The transport properties of the 2DEG channel are very crucial for HEMT applications. The Al composition in the AlGaN barrier layer as well as the AlGaN barrier layer thickness are important to generate maximum sheet carrier charge. Usually, the higher composition of Al causes higher 2DEG mobility and charge carrier concentration. However, the Al mole fraction in AlGaN/GaN heterostructure is in the range of 15-30 % for barrier thickness of 15-30 nm [29–31]. In this work, an Al composition of 26 % was used in the AlGaN barrier layer to achieve high electron mobility and sheet career density. Electron transport properties of nitride semiconductors are briefly reported in Ref. [32, 33].

1.4 AlGaN/GaN HEMTs on 3C-SiC/LR-Si

The unavailability of large single large crystal substrate for homo-epitaxial growth leads to the use of SiC, sapphire, and/or GaN as substrates to grow AlGaN/GaN heterostructure. However, it is already mentioned that availability in small size and the high market price of those substrates hinder wide applications. In this scenario, Si emerges as a potential candidate. However, it is difficult to grow a crack-free, high-quality GaN film on Si due to high thermal and lattice mismatches which generate

large tensile stress resulting in dislocation and huge cracks in the epi-structure [34–37]. To overcome these challenges, different approaches were implemented, such as use of an AlN layer, a strained layer superlattice (SLS) structure, an InAlN buffer layer and a SiC intermediate layer on Si substrate [38–46]. For RF applications of GaN HEMTs, typically SiC substrates are used owing to its certain advantages, such as high thermal conductivity and very low lattice mismatch to GaN [25,47]. To combine the advantages of high-quality SiC with Si substrates, Takeuchi et al., first proposed the idea of the 3C-SiC intermediate layer on Si as a buffer or transition layer [48]. It is reported that a 3C-SiC intermediate layer can minimize the lattice and thermal mismatch along with the prevention of the melt-back reaction. In addition, the three-dimensional (3D) growth technique successfully eliminated the threading dislocations (TDs) on the surface of GaN [49, 50].

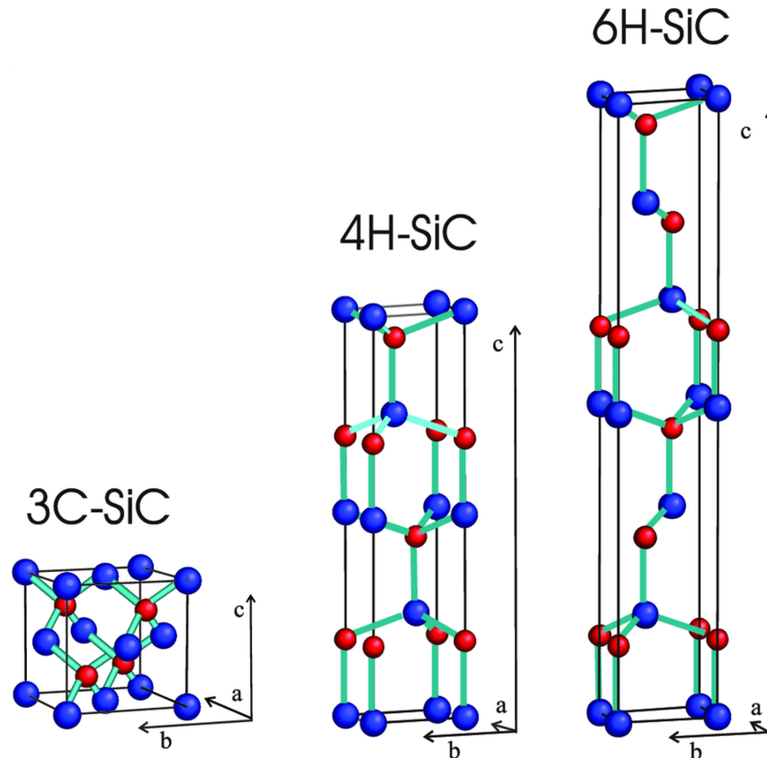

Figure 1.4: Unit cells of 3C-SiC, 4H-SiC and 6H-SiC [51].

There are already reported more than 250 polytypes of SiC, which are in the shape of cubic, hexagonal or rhombohedral [52]. However, regarding the aspect of commercial availability, only two hexagonal structures (4H-SiC and 6H-SiC) and the cubic (3C-SiC) are available. All the three structures are depicted in Fig. 1.4. The SiC can achieve a much higher breakdown field (2 – 4 MV/cm), electron saturation velocity, thermal conductivity, and energy band gap (2.3 – 3.2 eV) than Si substrates. These features automatically establish the SiC as favorable for high-power and high-frequency applications. In the early '80s, Nishino et al. first described an efficient method to grow 3C-SiC on Si [53]. The lattice mismatch of 3C-SiC with GaN is 3% for the hexagonal phase of GaN. With a 3C-SiC intermediate layer, several groups reported reduced crack generation in GaN along with enhanced crystal quality of GaN [48, 54–56].

The price of high-resistivity Si substrates is higher than that of low-resistivity Si substrates [57]. Moreover, at high temperatures, the intrinsic carrier density significantly increases in high-resistivity substrates. These charge carriers generate huge RF loss in the device [58]. Because of these reasons, we used a low resistive commercially prepared 6-inch Si (111) substrate. However, at high temperatures, there is also a possibility of the generation of charge carriers in the buffer layers for GaN devices on low resistivity (LR-Si) substrates. As described earlier, the generation of these charge carriers results in the degradation of the device performance [59]. Another problem with LR-Si is that it generates large parasitic capacitance which also deteriorates the high-frequency performance of the device. Hence, the generation of charge carriers and the effect of low resistivity need to be eliminated to effectively use GaN-on-Si HEMTs on 3C-SiC/LR-Si in RF applications. A general comparison of performances obtained on HR-Si and LR-Si substrates is presented in Table 1.2.

Table 1.2: A comparative study of GaN HEMTs performance obtained on HR-Si and LR-Si.

Refs.	Substrate	I_{d} (A/mm)	$g_{\mathrm{m,max}}$ (mS/mm)	f_{T} (GHz)	f_{max} (GHz)	L_{g} (μm)
[60]	HR-Si	0.6	157	90	150	0.1
[61]	HR-Si	1.0	250	50	100	0.25
[62]	HR-Si	0.55	215	46	92	0.17
[63]	HR-Si	1.43	415	143	176	0.08
[64]	HR-Si	0.6	157	90	150	0.1
[57]	LR-Si	1.4	425	55	121	0.3
[65]	LR-Si	0.89	370	83	95	0.16
[66]	LR-Si	2.0	390	52	102	0.2
[67]	LR-Si	0.6	157	90	150	0.1
[68]	LR-Si	0.6	123	4.8	10	2.0

1.5 RF applications of GaN HEMTs

The research and development of GaN HEMTs expanded the RF GaN market astoundingly which boomed the RF power device industry. In 2020, the market size of GaN semiconductors was estimated to be valued at 1.65 USD. According to reports, this market looks forward to perceiving a compound annual growth rate (CAGR) of 21.5% from 2021 to 2028 [69]. The rising demand and significant growth of this market are mainly attributed to the demand for power electronics. As mentioned previously, higher saturation velocity and high breakdown voltage of GaN devices make it the most potential candidate. Among many applications of GaN HEMTs, the telecommunication, space, and defense applications in the form of radars have boosted the growth of the RF industry and with 5G implementation in cellular communications, the RF GaN market size is expanding hugely [70].

In broadband communication, the performance of power amplifiers is the most crucial factor, and to increase its efficiency, GaN emerged as an excellent candidate

over GaAs. The frequency range of GaN HEMT amplifiers extended from L-band [71,72] and S-band [73,74] to X-band [75] and Ka-band [76]. Moreover, GaN HEMTs are highly potential in space, radar, and satellite communications [77–79]. It is well established that GaN HEMT technology not only provides suitability for high power but also for low noise amplifiers (LNA) [80]. There are several reports on high-performing LNAs configured with GaN HEMT technology [81–84]. The high gain, high switching speed, and high power density are the crucial criteria that enable GaN HEMTs advantageous for these applications. The other significant areas where GaN plays a pivotal role are automotive industries [85,86] and LEDs [87]. The application of GaN semiconductor technology in different domains is graphically shown in Fig. 1.5.

Generally, GaN-on-SiC based HEMTs and MMIC's (Monolithic Microwave Integrated Circuits) enable state-of-the-art performance for RF, microwave, and mmW (Millimeter-wave) applications owing to the advantages of using SiC as substrate. However, GaN-on-Si technology is also emerged as a front-runner in device performance and commercialization by providing cost-effectiveness and as comparable or superior performance relative to GaN-on-SiC based devices. In addition, the increment of producibility is largely followed by the overall cost structure, manufacturability, and supply-chain ecosystem. The Si substrates offer wafer sizes from 150 to 300 mm, which is a deciding factor for bulk commercial cost-effective scaling [14]. Moreover, isotropic single-crystal Si is advantageous for lateral two-dimensional heat flow [17]. There are many reports available which showed the significant RF performance in GaN-on-Si HEMTs [17,57,59–68,88–92].

1.6 Purpose of this dissertation

It is already well established that GaN-on-Si based device technology is a growing area of research in RF, microwave, and mmW applications. However, GaN-on-Si

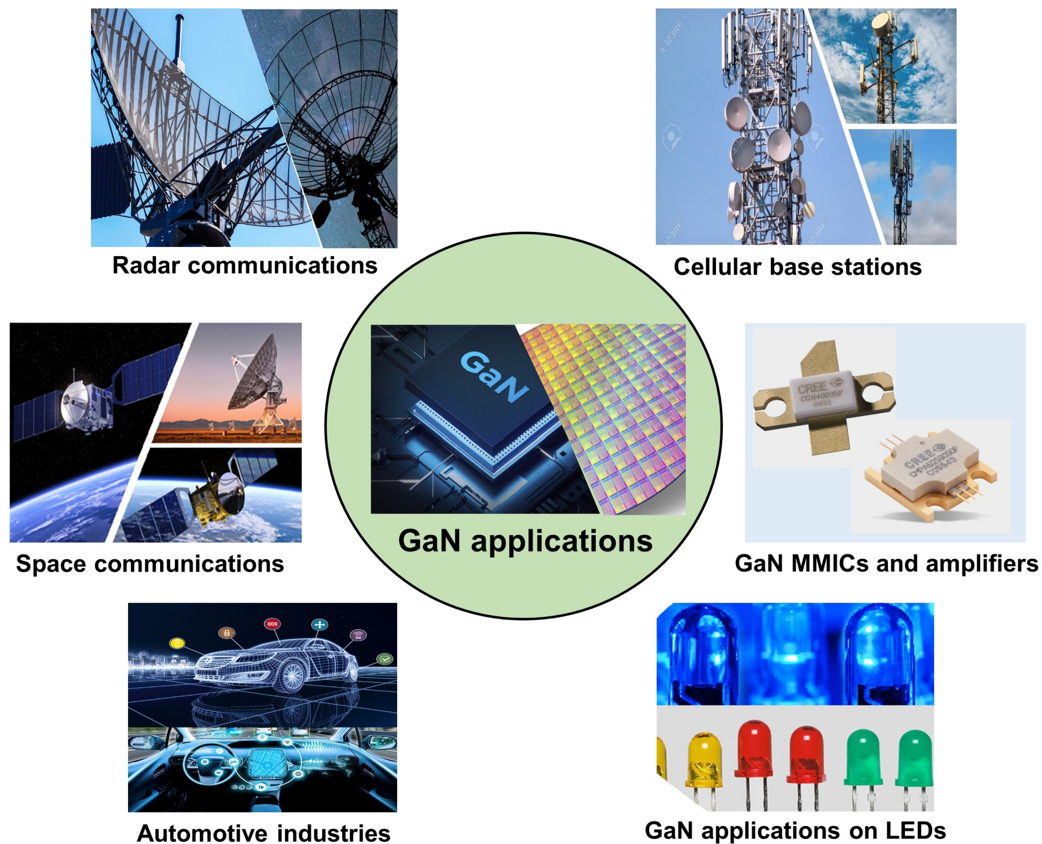

Figure 1.5: Applications of GaN semiconductor technology in high power and high frequency applications.

based devices face some challenges which are needed to be addressed first. The large lattice and thermal mismatch between GaN and Si hinder the growth of a crack-free, high-quality nitride layer on Si. In addition, the low resistivity of Si can generate large parasitic capacitances causing substantial RF leakage in high-frequency applications. Moreover, for high-power applications, thermal stability is an important aspect. At elevated temperatures, there is a possibility of the generation of intrinsic charge carriers in the buffer layers or substrate. Hence our purpose was to eliminate these challenges and achieve a significant RF performance. In summary, the purpose of this work can be summarized in the following points:

- Successful growth of a thick nitride layer on Si via a 3C-SiC intermediate layer

by reducing the lattice and thermal mismatch.

• Elimination of low resistivity effect of Si to suppress the effect of parasitic elements, so that GaN-on-LR-Si based HEMTs can exhibit significant RF performance.

• Achieve comparable cutoff frequency in GaN HEMTs on 3C-SiC/LR-Si.

• Attain comparable and significant output power characteristics and their thermal stability for stable amplifier operation.

• Minimization of high-frequency transmission loss in AlGaN/GaN HEMTs on 3C-SiC/LR-Si.

1.7 Outline of this dissertation

The dissertation consists of five main chapters followed by a chapter on conclusions drawn from this research. A comprehensive outline of the work contained in this dissertation is given below on a chapter-by-chapter basis. An outline of this dissertation is presented in Fig. 1.6.

Chapter 2 : Fabrication of AlGaN/GaN HEMTs on 3C-SiC/LR-Si.

This chapter mainly focuses on the epitaxial structure of AlGaN/GaN on 3C-SiC/Si with an 8.0 μm thick nitride layer and the fabrication of HEMTs. Though the substrate was commercially prepared, detailed steps of fabrication are described in this chapter along with the designed photomask and initial measurements for the evaluation of the epitaxial structure's buffer quality.

Chapter 3 : DC characterization of AlGaN/GaN HEMTs on 3C-SiC/LR-Si with an 8.0 μm thick nitride layer.

This chapter deals with the detailed DC characterization of fabricated AlGaN/GaN HEMTs, mentioned in the previous chapter. DC performance evaluation is impor-

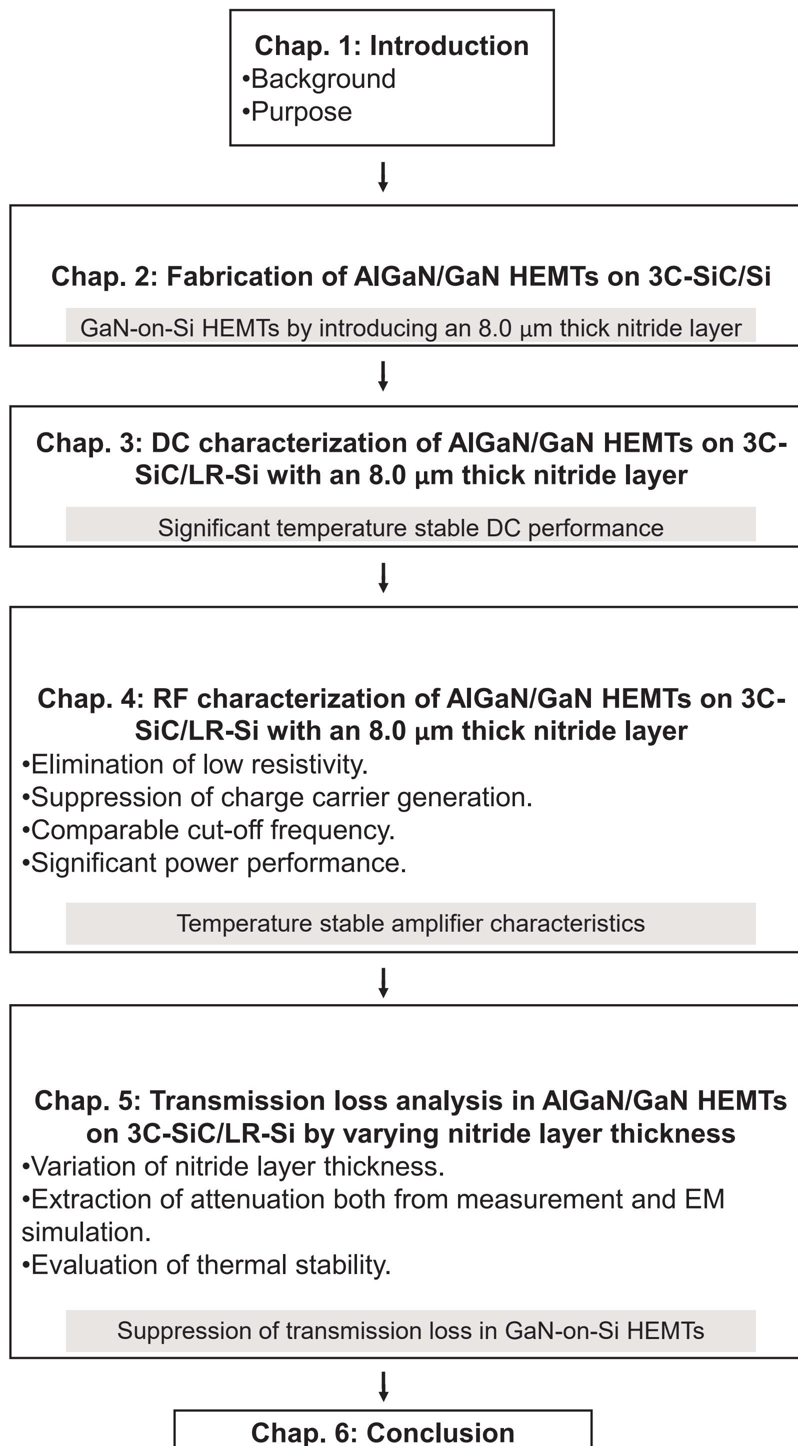

Figure 1.6: Outline of this dissertation.

tant to confirm the potency of the fabricated HEMTs. Evaluation of DC drain $I - V$ and transfer characteristics exhibited successful FET operation by achieving comparable current density and transconductance along with temperature stability up to a temperature of 125 °C.

Chapter 4 : RF characterization of AlGaN/GaN HEMTs on 3C-SiC/LR-Si with an 8.0 um thick nitride layer.

This chapter focuses on the ability and effectiveness of the fabricated HEMTs to perform in the high-power and high-frequency domains. A detailed analysis of the RF performance of the fabricated AlGaN/GaN HEMTs was carried out. Elimination of the effect of low resistivity of Si substrate combined with temperature stable amplifier characteristics was obtained by introducing the thick nitride layer. A significant high-frequency performance was confirmed by comparing the cutoff frequency and output power with the previously reported results.

Chapter 5 : Transmission loss analysis of AlGaN/GaN on 3C-SiC/LR-Si.

This chapter explores the effect of the thick nitride layer on the transmission loss in AlGaN/GaN HEMTs on 3C-SiC/LR-Si. With the increasing development and interest in GaN-on-Si based RF technology, the influence of epitaxial structure on the RF loss becomes a crucial factor. For that, a detailed analysis of transmission loss in terms of attenuation was evaluated and the observation was also confirmed with the EM simulation results obtained from the ADS Keysight momentum platform. It was observed that a thick nitride layer of 8.0 μm can successfully reduce the transmission loss, thus improving the RF performance.

Chapter 6 : Conclusion.

This chapter concludes the dissertation by establishing the fact that a thick nitride layer of 8.0 μm can successfully enhance the RF performance of AlGaN/GaN HEMTs on 3C-SiC/LR-Si. A brief future prospect of this research work is also included in this chapter.

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Chapter 2

Fabrication of AlGaN/GaN HEMTs on 3C-SiC/LR-Si

2.1 Introduction

In this chapter, the detailed technological process of AlGaN/GaN HEMTs fabrication is described. The fabrication process includes designing mask data, sample preparation, mesa isolation, UV photolithography, and preparation of Ohmic and Schottky contacts. The processed HEMTs are based on commercially prepared AlGaN/GaN heterostructures on 3C-SiC/LR-Si substrates. All the processes that will be mentioned in this chapter were done in the cleanroom facility of the Nagoya Institute of Technology.

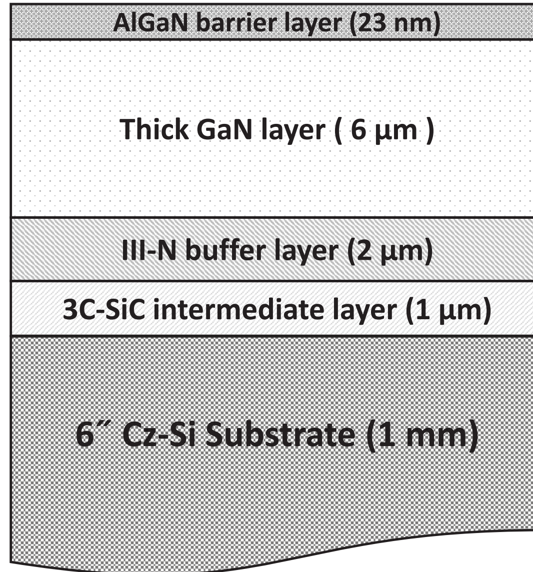

Figure 2.1: The epitaxial structure of AlGaN/GaN on 3C-SiC/Si.

2.2 AlGaN/GaN epitaxial structure on 3C-SiC/LR-Si

The growth of AlGaN/GaN heterostructure on 3C-SiC/Si substrates was done by the SiC division of Air water Inc., Nagano, Japan. Epitaxial growth by metal organic chemical vapor deposition (MOCVD) and AlGaN/GaN HEMTs fabrication were achieved on a commercially prepared 3C-SiC(111)/Czochralski(Cz)-Si (111) substrate with a 6-inch diameter. The thickness of the Si substrate was 1 mm and the resistivity was ≤ 3 Ω-cm. The 1 μm thick 3C-SiC layer was formed by heteroepitaxial growth on Si substrate. At high temperatures, charge carriers generate in high resistivity-Si (HR-Si) which results in reduced resistivity and increased substrate loss [1,2]. In addition, the manufacturing cost of GaN-on-HR-Si is higher than GaN-on-LR-Si technology [3]. Because of the above reasons, LR-Si substrate is used in this work. Though Si substrate with an orientation of 100 is more popular, in this work p-type Si with orientation 111 was used. It is reported that the growth

of GaN on Si (111) can exhibit higher crystallinity than Si (100). The reason is a smaller misorientation on the Si(111) substrate. The above report was confirmed by W. -K. Wang et al., through their study by X-ray rocking curve (XRC) analysis [4]. A schematic cross-section of the AlGaN/GaN heterostructure on 3C-SiC/Si is shown in Fig. 2.1. The epitaxial layers, from the substrate up, consist of a 1 μm thick 3C-SiC intermediate layer followed by a 2 μm thick III-N buffer layer containing Al, a 6 μm thick GaN layer, and a 23 nm AlGaN barrier layer with an Al composition of 26%. The thick GaN layer comprises a carbon-doped GaN (C-GaN) region to attain high resistivity along with an unintentionally doped GaN (u-GaN) region. The carbon doping concentration in the C-GaN region, measured by secondary ion mass spectroscopy (SIMS), was $<10^{19}/\text{cm}^3$. The thickness of the u-GaN layer was approximately one-tenth of the total GaN layer thickness. According to the SEMI standard, there are three indicators generally used to define the substrate displacement, which are SORI, BOW, and WARP [5]. Here the SORI index was used to denote the substrate displacement which was stably controlled at less than 50 μm to secure the chucking during the device process and reduce the risk of cracking during the back-grinding and die process. A crack-free nitride surface with edge exclusion of 5 mm was successfully attained on the 6-inch 3C-SiC/Si substrate.

2.3 Hall measurements

The mobility of 2DEG in AlGaN/GaN HEMT structures is very crucial for the functionality and performance of fabricated devices. For that, before going to the fabrication of devices, the Hall parameters were estimated to analyze the efficacy of the epitaxial structure [6, 7]. The information about the intrinsic properties of the heterostructures such as the sheet carrier densities, 2-DEG mobilities, and sheet resistances can be extracted from this measurement [8]. The Hall effect measurement is based on the measurements of an induced voltage of the sample in a magnetic field

oriented perpendicular to the sample surface. Eq. 2.1 is representation of the Lorentz force exerted on charged carriers moving with velocity v_{d}. The electrons and holes are moving in the magnetic field under the impact of this Lorentz force [9]. The direction of the charge carrier's movement depends on the polarity. Therefore the advantage of the Hall effect is the identification of the majority carriers and their type by using the direction of current flow in the semiconductor.

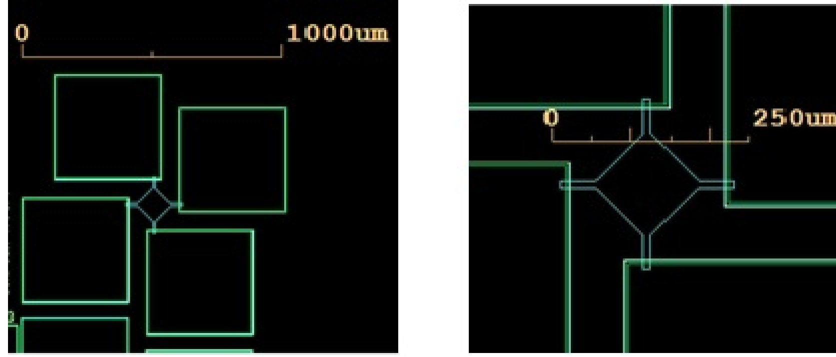

Figure 2.2: Electrode patterns used for the four probe Hall measurements.

$$F = q.(v_{\mathrm{d}} \times B) \tag{2.1}$$

where q is the elementary charge, v_{d} is the velocity, and B is the inductance of the magnetic field. The current density $\mathrm{J_x} = qnv_{-x} = -\,env_{-\mathrm{x}} = env_{-\mathrm{x}}$ for electrons and electric field intensity E will give us:

$$\frac{J_{\mathrm{x}}}{en_{\mathrm{H}}} B_{\mathrm{z}} = -E_{\mathrm{y}} \tag{2.2}$$

where the Hall-coefficient (R_{H}) is

$$R_{\mathrm{H}} = \frac{1}{en_{\mathrm{H}}} \tag{2.3}$$

The Hall factor, n_{H} can be replaced by n for electrons and with p for holes and

when the conductivity is known, the Hall mobility μ can be determined by following expressions:

$$\mu_{\mathrm{n}} = \frac{\sigma_{\mathrm{n}}}{en} \text{ or } \mu_{\mathrm{p}} \text{ (for holes)} = \frac{\sigma_{\mathrm{p}}}{ep} \tag{2.4}$$

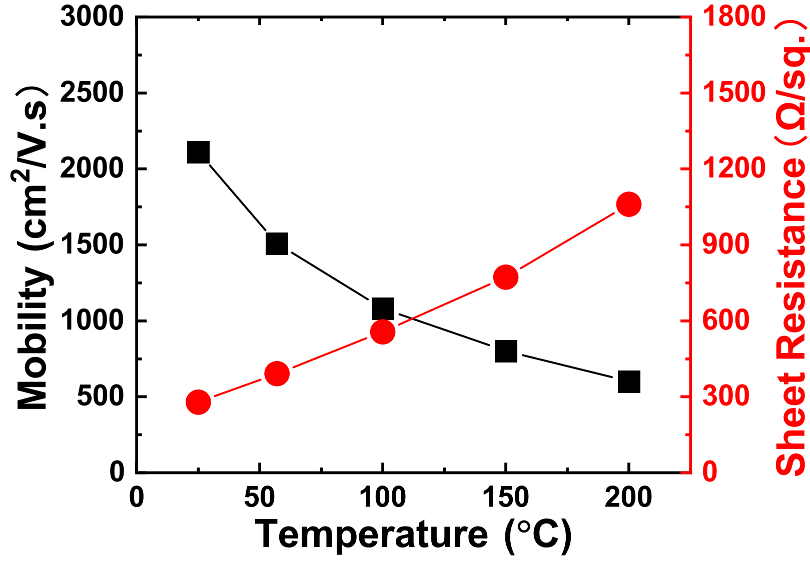

Figure 2.3: Temperature-dependent μ and R_{sh} at 20, 55, 100, 150, and 200 °C.

In this work, a metal scheme of Ti/Al/NI/Au was used to make ohmic contacts on four contacts of the sample having an area of 1 mm^2. Temperature-dependent Hall measurements were performed on the epitaxial structure to estimate the temperature dependency of the electron transport parameters, such as mobility (μ), two-dimensional electron gas (2DEG) carrier concentration (N_{s}), and 2DEG sheet resistance (R_{sh}). Temperature-dependent μ and R_{sh} are shown in Fig. 2.3 where the temperature was varied from 20 to 200 °C. The extracted values of all the Hall parameters are listed in Table 2.1. At high temperatures, a significant increment of phonon concentration causes increased scattering which lowers the mobility and increases the sheet resistance of the epitaxial structure significantly [10–12] which is attributed to the degradation of DC and RF performance of the device.

Table 2.1: Electron transport parameters measured from temperature-dependent Hall measurements.

Temperature	μ (cm^2/V-s)	N_s (cm^{-2})	R_{sh} ($\Omega/\square$)
20 °C	2110	1.06×10^{13}	279
55 °C	1510	1.05×10^{13}	391
100 °C	1080	1.04×10^{13}	556
150 °C	802	1.01×10^{13}	773
200 °C	601	9.83×10^{12}	1060

2.4 Device processing

2.4.1 Design of mask data

The device processing starts with the preparation of mask data which was designed using computer-aided design software, in this case, L-edit from Tanner EDA [13]. The GSG FET patterns with varying gate lengths (L_g) and gate-to-drain lengths (L_{gd}) for both DC and RF characterizations were designed in the mask. The mask design also contains the patterns for Hall measurements and S-parameter measurements of pads. The layout of the designed mask is shown in Fig. 2.4. As the mask contains three basic layers which are (a) Isolation, (b) Ohmic contact, and (c) Gate contact, three different layered masks were prepared. An enlarged GSG patterned FET is shown in Fig. 2.5.

2.4.2 Mesa isolation

The as-grown AlGaN/GaN wafers are cut into 15 x 10 mm^2 for HEMTs fabrication. Before performing the mesa isolation, the sample surface was thoroughly cleaned using organic solvents like acetone and isopropyl alcohol (IPA) followed by cleaning with de-ionized water which removed the impurities from the AlGaN surface. The mesa

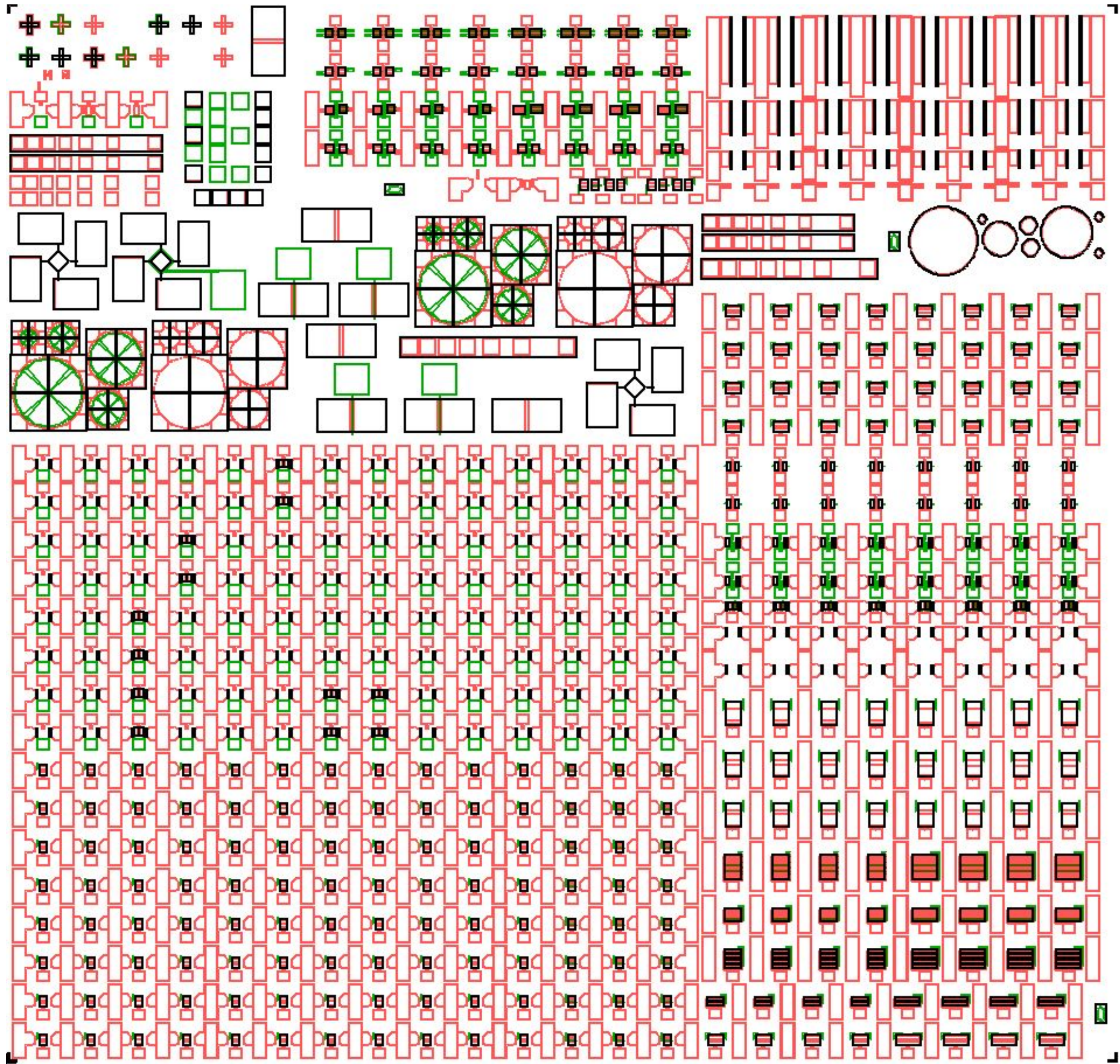

Figure 2.4: Layout of mask design used to fabricate the AlGaN/GaN HEMTs.

isolation is a crucial step in device processing to create islands of active layers on the wafer surface that can interrupt the conductive DEG and provide electrical insulation between two adjacent structures. The position of 2DEG defines the depth of mesa isolation. At first, the S1813G photoresist (PR) was coated using a spin coater and loaded for UV photolithography. A Karl Suss MA6 mask aligner was used to align the isolation mask (GaNHEMT-IS) and expose the PR coated wafer with UV light. UV exposed samples were then developed using MF-319 developer to get the isolation

pattern. Afterward, the samples were baked in an oven at an ambient temperature of 90 °C for 30 min and taken for the etching process to form the insulating islands.

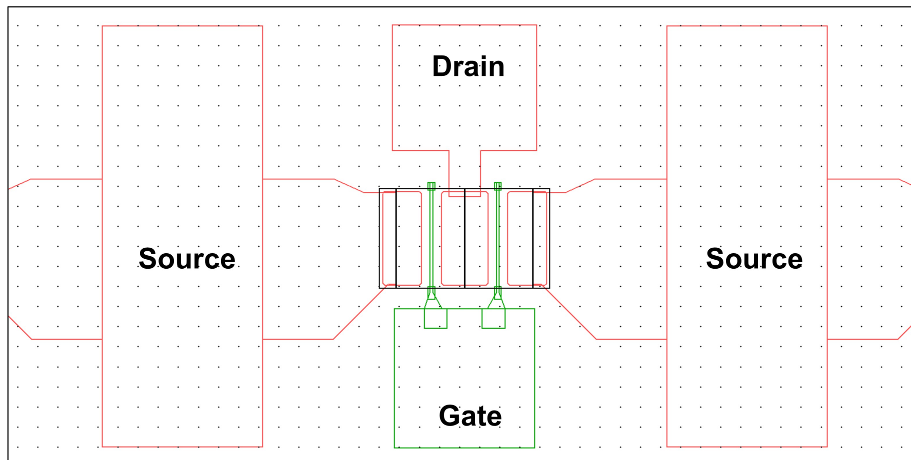

Figure 2.5: The GSG patterned layout of FET with double fingered gate of width 2 × 50 μm.

2.4.3 Reactive ion etching (RIE)

As wet chemical etching is not suitable for GaN because of slow etching rate and the problem of finding a suitable mask [14,15], the dry etching process drew the attention. The inductively coupled plasma (ICP), electron cyclotron resonance (ECR) or reactive ion etching (RIE) techniques showed the most promising results [16]. Though the ICP and ECR techniques are proved to be an effective way of etching, RIE is also extensively used for the dry etching of GaN. In the case of RIE, a single RF plasma source is used which determines both ion density and energy. On the other hand, the ICP has separate RF and ICP generators [17] which allow separate control over ion energy and ion density, which helps in process flexibility. During this research, the

BCl_3 plasma-based Anelva RIE machine was used in the cleanroom facility.

After the mesa isolation pattering, samples were etched using the above-mentioned BCl_3 plasma-based RIE technique. 300-nm deep mesa isolation was formed using 10 Watt plasma power and 10 sccm BCl_3 flow for 60 minutes. The depth of isolation was measured with the Alpha step D-500 stylus profiler. The residual PR remains on the substrate after the RIE was removed by oxygen plasma ashing. Afterward, the samples were cleaned with acetone and IPA to remove any type of residue on the wafer.

2.4.4 Ohmic contacts

Ohmic photolithography and metallization were the next steps to form the source and drain areas. The formation of ohmic contacts is very important to control the contact resistance as low as possible. Being large current and small voltage devices, transconductance and saturation velocity both are very sensitive to contact resistance. Following that, many studies were reported on an optimized metal scheme for good ohmic contacts. In this case, Ti/Al/Ni/Au metal stack was used to form the ohmic contacts where Ti/Al plays a crucial role to form a good ohmic contact between semiconductor and metal [18–21]. Moreover, the Au metal layer helps to prevent the oxidation of the upper surface and better contact for characterization.

- **Bi-layer process:**

The bi-layer process was used for easy and smooth lift-off after every metallization process. In the bi-layer process, firstly PMGI PR was coated and baked at 180 °C for 1 minute followed by a coating of the S1813G PR, which is also called the imaging PR. The NMD developer was used to develop the PMGI film where PMGI develops isotropically, creating a bi-layer re-entrant sidewall profile [22]. The created re-entrant sidewall profile or the overhang structure easily lift-off the metal deposited on S1813G.

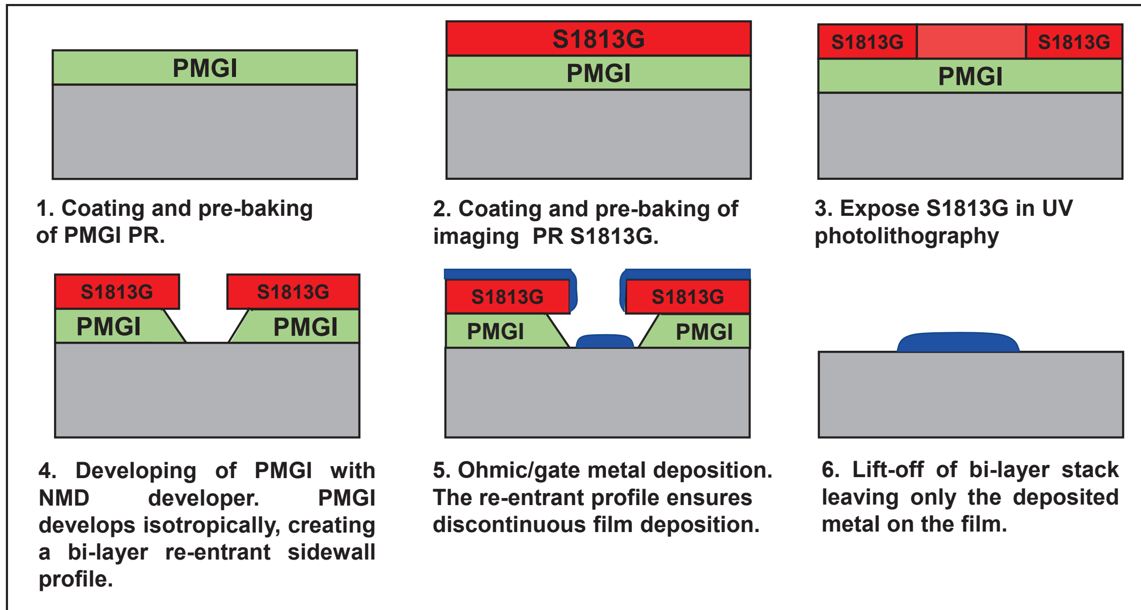

Figure 2.6: Flowchart of the bi-layer lift-off process applicable for both ohmic and Schottky contacts.

A schematic is shown in Fig. 2.6 to represent the working principle of the bi-layer process.

After the bi-layer process, ohmic patterns were formed by UV photolithography using an ohmic GaNHEMT (GaNHEMT-OM) mask. Before Ohmic metallization, the samples were etched with 99.9 % HCl to remove the native oxides. The metal stack of Ti/Al/Ni/Au (15/80/12/40 nm) was deposited using the electron-beam (E-beam) evaporation technique. The pressure of the chamber was kept at the order of $\sim 10^{-4}$ Pascal with a varying deposition rate of 0.1 to 1.0 Å/sec, depending on the metal. Lift-off procedures were carried out with only acetone to remove the unwanted metallic layers outside the contact regions and the above-mentioned bi-layer process played a pivotal role in the fine lift-off of the metals. The metal alloy of Ti/Al/Ni/Au metal stack was carried out using a rapid thermal annealing (RTA) system at an elevated temperature of 850 °C for 30 sec at nitrogen gas ambiance.

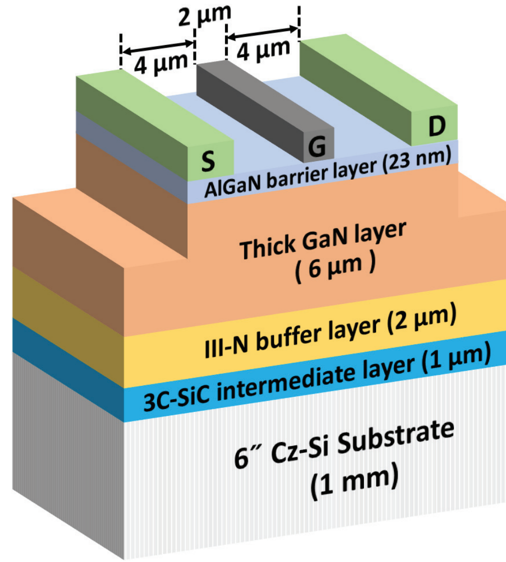

Figure 2.7: The schematic of cross-sectional structure of the fabricated AlGaN/GaN HEMT on 3C-SiC/LR-Si.

2.4.5 Schottky contact

For the effective function of transistors, rectifying or Schottky gate contacts with sufficiently high barrier height and low reverse leakage current are very essential. During this research, devices with L_g of $2 \sim 3$ μm were fabricated using UV photolithography. However, for L_g under 300 nm, electron beam lithography (EBL) is more suitable because EBL allows achieving higher reproducibility and reduces alignment mistakes. Similar to the ohmic contact process, the samples went through the bi-layer process followed by the photolithography using a gate GaNHEMT (GaNHEMT-GT) mask. For typical AlGaN/GaN HEMTs, Schottky gate metals such as Pd, Pt, Ni are widely used [23–25]. In this case, we used Ni of thickness 30 nm with Au of 150 nm and both are deposited via an e-beam evaporation system keeping the pressure and metal deposition rate as same as the ohmic metal deposition. The metal scheme of the Schottky contact was previously optimized after using multiple ratios of Ni and Au. Afterward, lift-off was carried out and gate electrodes were ready to measure. No

passivation was used in the samples.

The above steps are very important in device processing and these steps may vary according to the specifications and requirements. The Schematic representation of the fabricated AlGaN/GaN HEMT is shown in Fig. 2.7. Among the different dimensional fabricated FETs, the devices with $L_{\text{gs}}/L_{\text{g}}/L_{\text{gd}} = 4/2/4$ μm are taken for the characterization purposes. The gate width W_{g} of the fabricated HEMTs is 50 μm. However, because of double fingered gate electrodes, the effective W_{g} is 50×2 μm. The optical microscopic image of the actual HEMTs is also shown in Fig. 2.8.

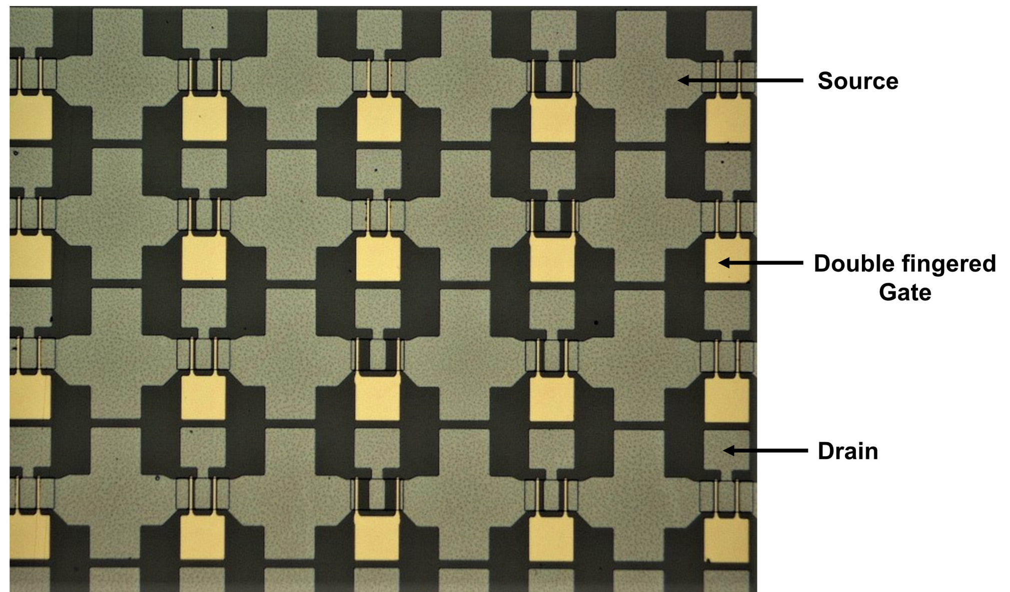

Figure 2.8: The optical microscopic image of fully fabrucated AlGaN/GaN HEMTs on 3C-SiC/Si.

2.5 Summary

In semiconductor technology, device fabrication or processing is very crucial for the successful operation of the devices in both DC and RF fields. This chapter gave a detailed explanation of the fabrication process of AlGaN/GaN HEMTs on 3C-SiC/LR-Si. However, the techniques and methodologies used in this fabrication process are not exclusive to AlGaN/GaN HEMTs. These processes can be modified and optimized according to the need or requirements. The next chapters will go on to describe the characteristics of the fabricated devices in the DC and RF domains.

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Chapter 3

DC characterization of AlGaN/GaN HEMTs on 3C-SiC/LR-Si with an 8.0 μm thick nitride layer

3.1 Introduction

It is a well known fact that GaN HEMTs have a high potential in high-power and high-frequency applications. Initially for the analysis of FET operation, DC characterization plays a pivotal part. HEMTs primarily work in depletion mode or the on-state where without any gate voltage, the current flows through the device. The amount of voltage requires to stop the flow of current is called the pinch-off voltage $V_{\rm p}$. With the increasing demand of high power, GaN emerged as the one of the best potential candidates. In the case of fabricated devices with conventional semiconductors such as Si and GaAs, the RF output power is limited because of low inherent

breakdown voltage. However, for group-III nitrides such as AlGaN and GaN, they have higher breakdown fields than Si and GaAs which in turn helps the device to operate in high DC bias and generate large RF output power [1, 2]. The additional physical mechanism which plays a significant role is two dimensional electron gas (2DEG) which exists with a high density in AlGaN/GaN heterostructures [3–5]. The limitation of applied drain bias voltage to any power device like HEMTs corresponds to the breakdown of the gate electrode. Having higher breakdown voltage, GaN-based devices can operate at voltages of + 48 V DC and higher [6] compared to GaAs field-effect transistors (FETs), whose activity is limited to drain bias of 8 – 12 V [7]. Having the advantages, GaN-based devices steadily replaced the existing technologies with conventional semiconductors in the fields such as wireless base stations, military radars, and even in commercial applications.

In this chapter, the detailed DC characterizations of fabricated AlGaN/GaN HEMTs are presented. The epitaxial structure is the same as that was shown in Chapter 2. DC static and transfer $I - V$ characteristics and their temperature dependency were evaluated. It was observed that the HEMT exhibited significant DC performance along with excellent temperature stability even at a high temperature of 125 °C. Moreover, the transient response *i.e* gate and drain lag characteristics were also evaluated.

3.2 Static I-V characteristics

Fig. 3.1 (a) depicts the DC (I_d- V_d) characteristics of the fabricated AlGaN/GaN HEMT on 3C-SiC/Si. The drain voltage (V_d) was varied from 0 to + 20 V and the gate bias (V_g) was swept from − 6 to + 2 V in 1 V increments. The device attained a drain current density (I_d) of 625 mA/mm at V_g = + 2 V. The ohmic contact resistance extracted from the transmission line method (TLM) was approximately ∼ 1.2 Ω-mm.

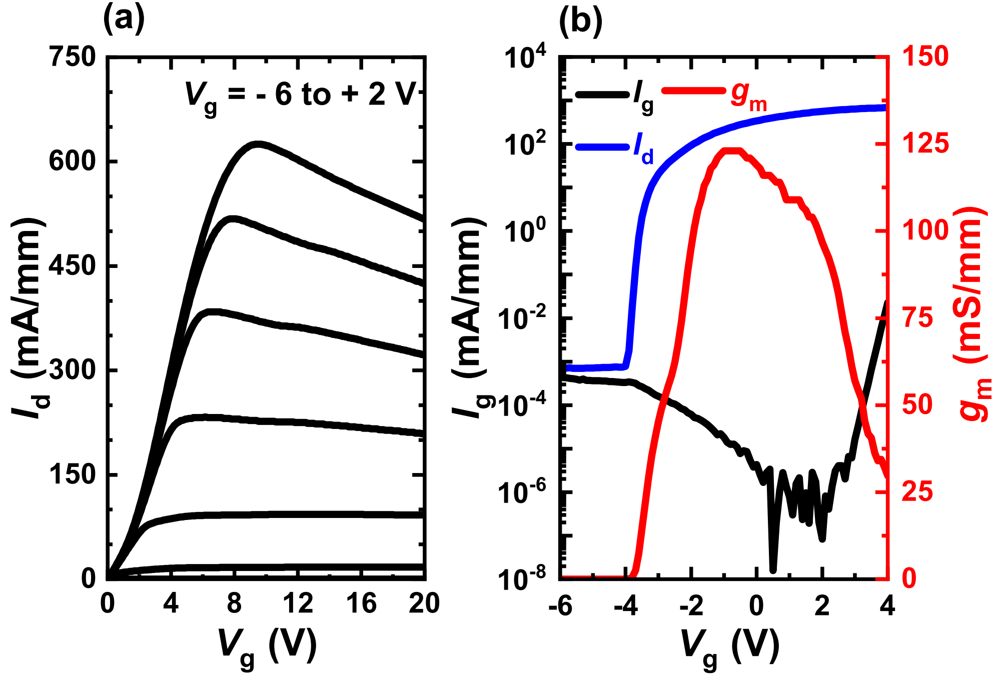

Figure 3.1: (a) Static I_d- V_d characteristics of the device where gate voltage (V_g) was varied from -6 V to + 2 V in 1 V increments. (b) Transfer characteristics of the device at $V_d = +\ 10$ V and V_g was swept from -6 V to + 4 V. The device dimension was $L_{gs}/L_g/L_{gd} = 4/2/4$ μm.

• Temperature-dependent static I-V characteristics

The temperature-dependent DC characteristics of the fabricated sample were evaluated. The temperature was varied from 25 to 125 °C with a step of 25 °C. Fig. 3.2 (a) represents the temperature-dependent I-V characteristics, where it can be seen that the with increasing temperature I_d decreases. Maximum drain current densities ($I_{d,max}$) and on resistances at each temperature were plotted in Fig. 3.2 (b). An increment of 1.9 mA/mm/°C of maximum current density is observed where the R_{on} was increased to 1.5 from 1.1 mΩ-cm^2. It is well-known fact that a significant increment of phonon concentration at high temperature causes increased scattering which lowers the mobility and increases the sheet resistance significantly [8–10]. Because of the above fact a slight increment in both I_d and R_{on} was observed.

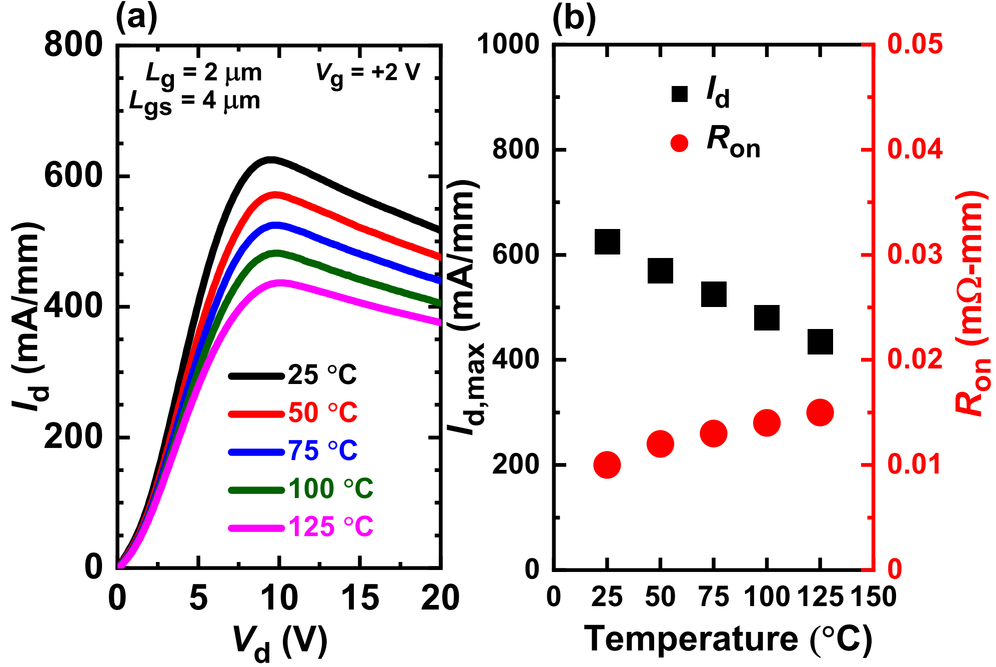

Figure 3.2: (a) Temperature-dependent I_d- V_d characteristics at V_g = +2 V, and (b) $I_{d,max}$ and R_{on} at 25, 50, 75, 100, and 125 °C. The device dimension was $L_{gs}/L_g/L_{gd}$ = 4/2/4 μm.

3.3 Transfer I-V characteristics

The transfer characteristics of the sample is depicted in Fig. 3.1 (b), where the V_g was swept from − 6 to + 4 V, keeping the drain bias V_d fixed at + 10 V. A gate leakage current density (I_g) of ∼ 4.5 × 10^{-4} mA/mm and a peak transconductance ($g_{m,max}$) of 123 mS/mm at V_g = − 1 V were attained. Good pinch-off characteristics ($I_{on}/I_{off} \sim 10^6$) were observed from the above characteristics. The threshold voltage (V_{th}) was − 2.8 V.

Temperature-dependent transfer I-V characteristics

The transfer characteristics of the device with varying temperature are also evaluated. In Fig. 3.3 (a), the off-state leakage currents are plotted at 25, 75, and 125 °C. It is

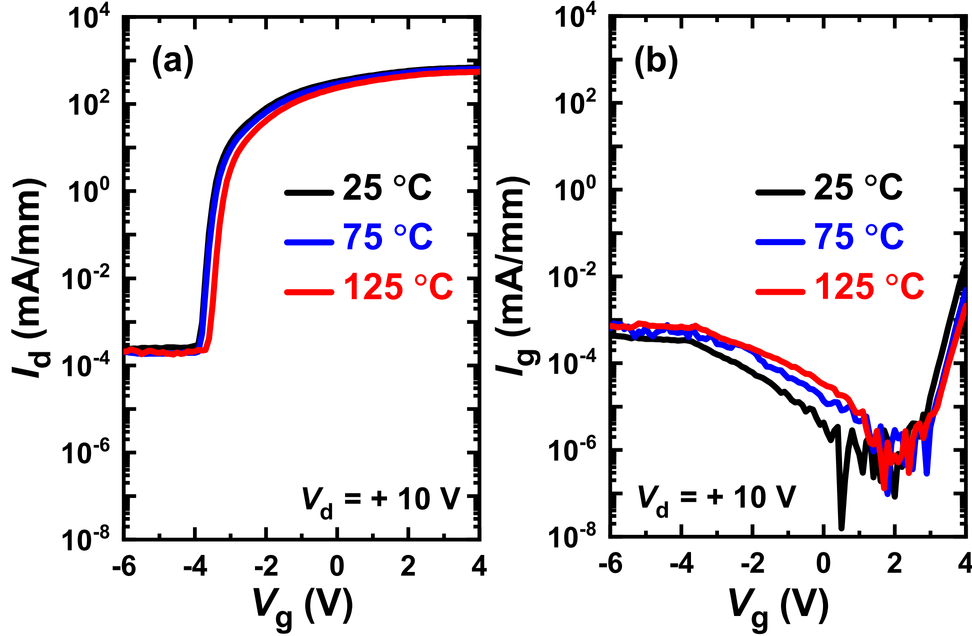

Figure 3.3: Transfer (a) I_{d}-V_{g}, and (b) I_{g}-V_{g} characteristics of the device where V_{g} was varied from -6 V to + 4 V and V_{d} was fixed at + 10 V. The device dimension was $L_{\mathrm{gs}}/L_{\mathrm{g}}/L_{\mathrm{gd}} = 4/2/4$ μm.

evident from the figure that there is no such significant increment of off-state leakage current even at 125 °C. In addition, the gate leakage currents at 25, 75, and 125 °C are shown in Fig. 3.3 (b). It was observed that the gate leakage was significantly stable while the temperature is increased from RT to 125 °C. The V_{d} was fixed at + 10 V, for both the I_{d}-V_{g} and I_{g}-V_{g} characteristics.

Temperature dependency of g_{m} was also measured for the same temperature range. In Fig. 3.4 (a), g_{m} at 25, 50, 75, 100 and 125 °C are shown where a gradual decrement of g_{m} was observed with increasing temperature. It is mainly because of degraded 2DEG mobility with temperatures due to phonon scattering phenomenon, as discussed earlier [8]. In addition, electron saturation velocity also decreases at high temperatures along with an increment in device non-linearity [10]. For the above reason, peak transconductance was reduced to 86 mS/mm and R_{on} was increased to 0.015 mΩ-mm at 125 °C. In Fig. 3.4 (b), the values of peak transconductance $g_{\mathrm{m,max}}$

at every temperature points were plotted. However, the threshold voltages remained almost constant over the temperature range because of the invariant 2DEG density at AlGaN/GaN interface even at high temperatures. Temperature dependence of V_{th} is shown in the inset of Fig. 3.4 (b).

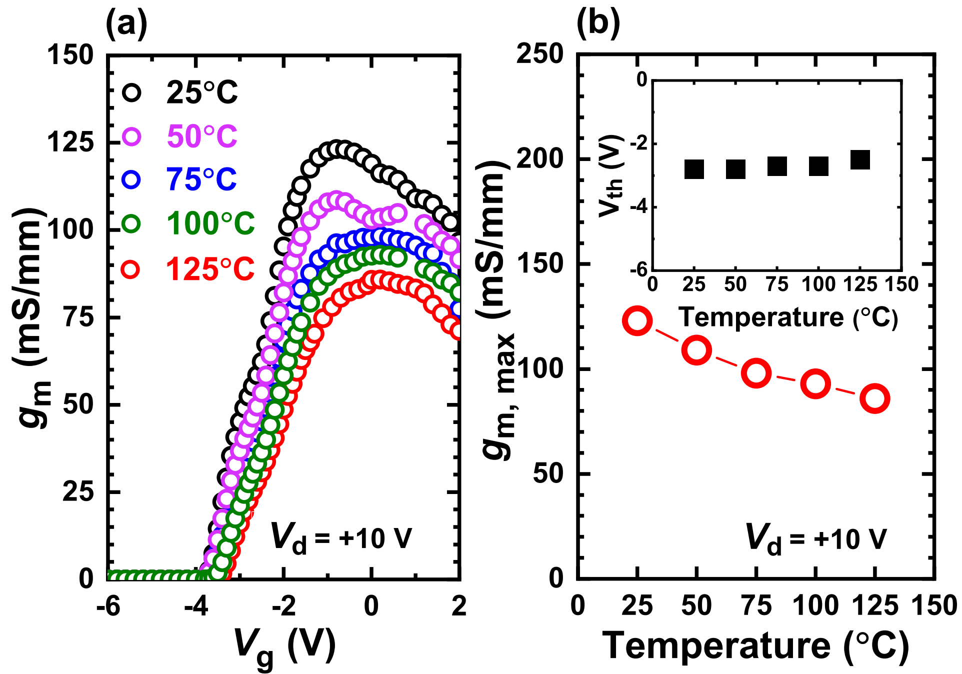

Figure 3.4: (a) Temperature-dependent transconductance density g_{m} for 25 to 125 °C. (b) Peak transconductance $g_{\mathrm{m,max}}$ at 25, 50, 75, 100, and 125 °C. Inset: Temperature dependence of threshold voltage (V_{th}).

From the above results, we observed that the degradation of the DC performance was quite low and consistent with temperature. Temperature dependency of mobility is solely responsible for the obtained slightly degraded DC characteristics. Moreover, at high temperatures, there is a possibility of high leakage from the buffer or epitaxial layers due to the generation of charge carriers which hugely affects the RF performance of the device. However, in our case, very small detrimental high temperature effect on DC performance indicates the suppression of generation of charge carriers, thus no buffer leakage even at high temperature of 125 °C. Thus, the introduction of thick

nitride layer not only provides significant electrical properties, but also improved the temperature stability of DC performance of the AlGaN/GaN HEMT on 3C-SiC/Si substrate. The evaluated temperature-dependent dc parameters are listed in Table. 3.1.

Table 3.1: Temperature-dependent DC parameters.

Temperature	$I_{\mathrm{d,max}}$ (mA/mm)	R_{on} (mΩ-mm)	$g_{\mathrm{m,max}}$ (mS/mm)	V_{th} (V)
25 °C	625	0.01	123	−2.8
50 °C	570	0.012	109	−2.8
75 °C	525	0.013	98	−2.7
100 °C	480	0.014	93	−2.7
125 °C	435	0.015	86	−2.5

3.4 Summary

In summary, a temperature stable and significant DC performance are observed in the fabricated HEMTs. The off-state leakage current was low and showed excellent thermal stability even at 125 °C. The temperature-dependency of 2DEG properties is solely responsible for the slight detrimental effect that we observed in the DC performance. At high temperatures, there is a possibility of high leakage from the buffer or epitaxial layers due to the generation of charge carriers which hugely affects the RF performance of the device. However, in our case, a very small detrimental high-temperature effect on DC performance primitively indicates minimal buffer leakage even at a high temperature of 125 °C.

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Chapter 4

RF characterization of AlGaN/GaN HEMTs on 3C-SiC/LR-Si with an 8.0 μm thick nitride layer

4.1 Introduction

After analyzing the DC properties of the fabricated HEMTs, more about their quality is obtained from studying high-frequency behavior. It is already a well know fact that GaN is a superior material for RF applications owing to its reliability, high efficiency, and high output power. The global market is expanding by transiting from 4 to 6-inch wafer fabrication in GaN-on-SiC technologies. However, the GaN-on-Si technology can also gain a firm foothold in next-generation RF applications due to its expandable wafer size, cost-effectiveness, and scalable Si substrate supply chain [1–3]. To successfully establish the ability to perform in the high-power and high-frequency

domain, a detailed analysis of RF performance of the fabricated AlGaN/GaN HEMTs was carried out. The initial challenge was to eliminate the effect of low resistivity of Si substrate as it can generate high parasitic capacitance which significantly degrades the RF performance [4]. In addition, for high-power applications, the thermal stability of a device is a crucial aspect. At high temperatures, there is a possibility of the generation of charge carriers in the buffer layers for GaN devices on LR-Si substrates. The generation of these charge carriers results in the degradation of the device performance [5]. Hence, the generation of charge carriers and the effect of low resistivity need to be eliminated to effectively use GaN-on-3C-SiC/LR-Si HEMTs in RF applications. After successfully achieving thermally stable and significant DC performance in the reported structure, we assume that it can also enhance the RF performance of the device. Hence, the overall RF performance of the device was analyzed with the 8.0 μm thick nitride layer on 3C-SiC/Si.

4.2 High-frequency operation

The measurement and evaluation of Scattering parameters (S-parameters) is a pivotal aspect to analyze the high-frequency performance of AlGaN/GaN HEMTs. When an N-port network is placed into a transmission line, the traveling waves scatter or reflect. The response of that N-port network to signal(s) incident to any or all of the ports is described by S-parameters [6]. Fig. 4.1 represents a two-port network corresponding to a HEMT where the input port corresponds to gate-source and the output port to drain-source.

S-parameters of a two-port network can be expressed as follows [7] :

$$S_{11} = \frac{b_1}{a_1},\ when\, a_2 = 0 \tag{4.1}$$

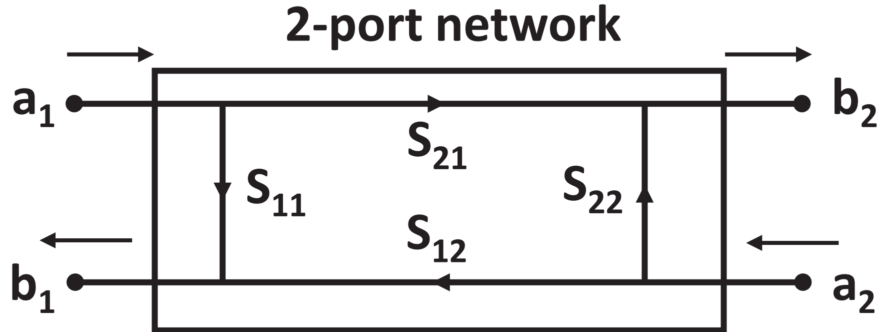

Figure 4.1: S-parameters of two-port network.

$$S_{21} = \frac{b_2}{a_1},\ when\, a_2 = 0 \tag{4.2}$$

$$S_{12} = \frac{b_1}{a_2},\ when\, a_1 = 0 \tag{4.3}$$

$$S_{22} = \frac{b_2}{a_2},\ when\, a_1 = 0 \tag{4.4}$$

where $a_{1,2}$ and $b_{1,2}$ are incident and reflected waves at input and output of the transistor, respectively (Fig. 4.1). S-parameters are measured as the function of the frequency. The S_{11} is called the input reflection coefficient,S_{12} the reverse transmission coefficient, S_{21} the forward transmission coefficient, and S_{22} the output reflection coefficient.

The important parameters needed for RF characterization of a HEMT can be derived from S-parameters.

- **Short circuit current gain ($|H_{21}|$):**

$$| H_{21} |= \frac{-2S_{21}}{(1-S_{11})(1+S_{22})+S_{22}S_{21}} \tag{4.5}$$

It gives the current gain when the output of the transistor is in short-circuit.

- **Maximum available power gain (MAG):**

$$MAG = \frac{S_{21}}{S_{12}}(K-\sqrt{K^2-1}) \tag{4.6}$$

It is a figure of merit of a transistor. MAG is a theoretical power gain of a transistor with its reverse transfer admittance set to zero. The stability factor K can be expressed as

$$K = \frac{1+| S_{11}S_{22}-S_{12}S_{21} |^2 - | S_{11} |^2 - | S_{22} |^2}{2| S_{12} || S_{12} |} \tag{4.7}$$

- **Maximum Stable gain (MSG):**

$$MSG = \frac{S_{21}}{S_{12}} \tag{4.8}$$

It is the maximum achievable power gain of a potentially unstable device at the stability border, K = 1.

- **Unilateral Power gain (U):** The unilateral power gain of two port network was published by Mason in 1954. This Mason's Invariant (U), is the only device characteristic that is invariant under lossless, reciprocal embeddings. In practical, a very useful figure of merit, maximum frequency of oscillation ($f_{\max}$) is extracted from U, where U($f_{\max}$) = 1.

$$U = \frac{\left| \frac{S_{21}}{S_{12}} - 1 \right|^2}{2(K \mid \frac{S_{21}}{S_{12}} \mid - Re \mid \frac{S_{21}}{S_{12}} \mid)} \tag{4.9}$$

The parameters on which the performance criteria of a microwave transistor depends are:

- **Output Power (P_{out}) :** Total microwave power that a transistor can generate (W/mm).
- **Gain :** It is the ratio of Output power (P_{out}) and input power(P_{in}). The measurement of gain is usually calculated in dB, but P_{in} and P_{out} are in dBm.
- **Cut-off frequency (f_T) :** It is the frequency of oscillation when the short circuit current gain is 1. It is defined as:

$$f_T :\mid H_{21} \mid (f_T) = 1 \tag{4.10}$$

- **Maximum oscillation frequency (f_{max}) :** The frequency at which the Mason's unilateral power gain is 1.
- **Power added efficiency (PAE) :** (P_{out} / P_{in})/P_{DC}, where P_{in} = input microwave power, P_{out} = output microwave power, P_{dc} = DC power.
- **Linearity :** The measure of gain against input signal level. High linearity means lower harmonic content in the output signal.
- **Noise Figure :** It is the difference in decibels (dB) between the noise output of the actual receiver to the noise output of an "ideal" receiver with the same overall gain and bandwidth when the receivers are connected to matched sources at the standard noise temperature [8].

The flowchart of RF analysis that were done in this work are depicted in Fig. 4.2. The evaluation of transmission loss is described in chapter 5.

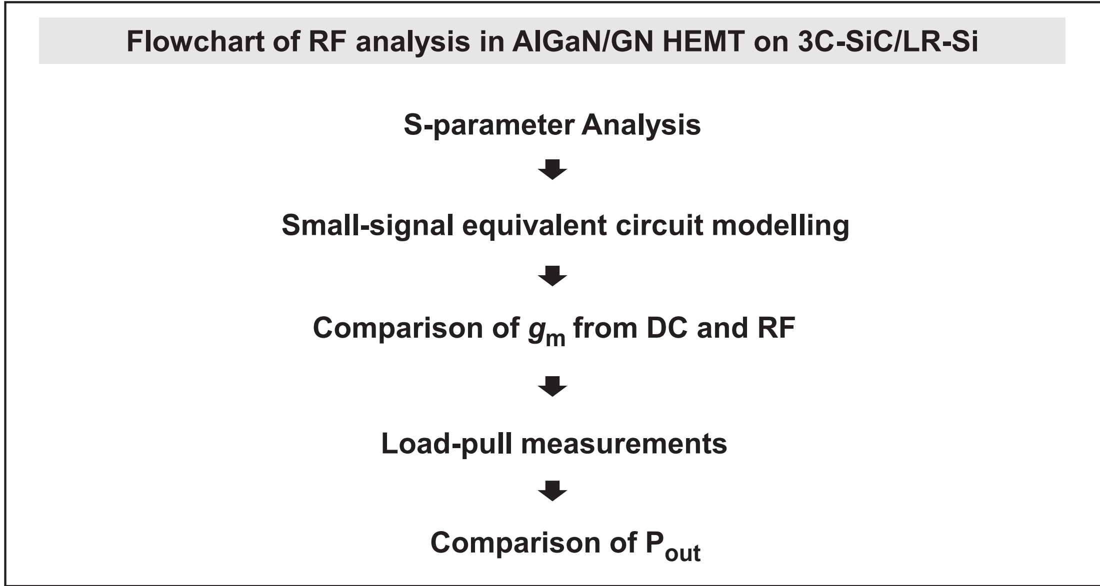

Figure 4.2: The flowchart of RF analysis that were performed on the fabricated HEMTs.

4.3 Small-signal characteristics

4.3.1 Cut-off-frequency (f_T) and maximum frequency of oscillation (f_{max})

Small-signal RF characteristics of the device with gate length (L_g) and gate width (W_g) of 2 and 2 × 50 μm, respectively was characterized by a P5004A vector network analyzer. On-wafer temperature-dependent S-parameters were evaluated in the frequency range of 0.5 to 20 GHz. The system was precisely calibrated with the open-short-load-through calibration standard. The cutoff frequency (f_T) and maximum frequency of oscillation (f_{max}) were obtained from the current gain ($|H_{21}|$) and Mason's unilateral gain (U) curves, respectively. In Fig. 4.3, the U and $|H_{21}|$ were plotted against frequency for the 2-μm gate length device at $V_d = +10$ V and $V_g = -1.0$ V. The de-embedded values of f_T and f_{max} were 4.5 and 11.5 GHz, respectively. A relatively low f_T was obtained due to the inverse relationship between L_g and f_T [9].

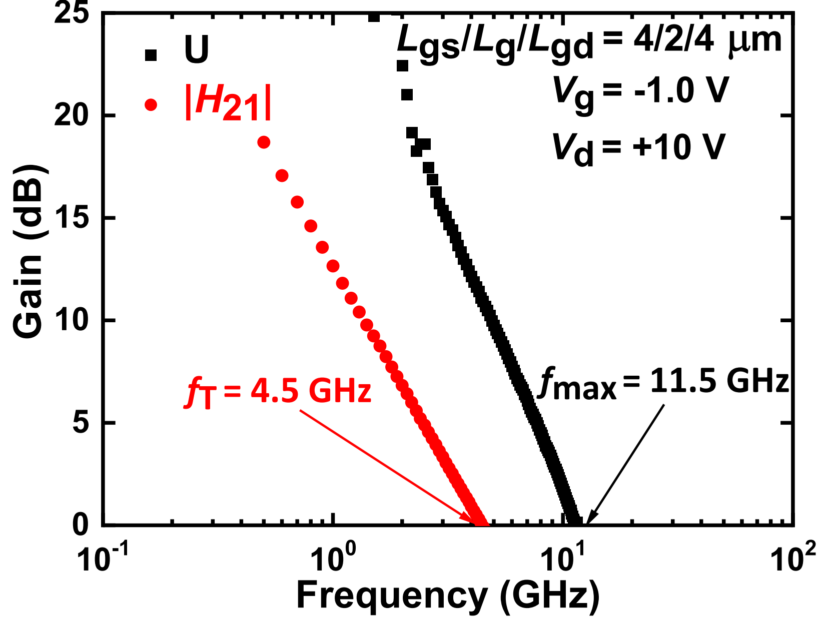

Figure 4.3: Mason's unilateral gain (U) and the current gain $|H_{21}|$ vs frequency of the 2 μm gate-length device where f_T and f_{max} are 4.5 and 11.5 GHz, respectively.

To establish the significance of the value of f_T, a comparative analysis of f_T vs L_g was done with previously reported results on GaN-on-Si, GaN-on-SiC, GaN-on-SiC/Si and GaN-on-sapphire substrates, represented in Fig. 4.4. It is very evident from the results that our device showed excellent competitiveness in the f_T performance [10–26]. Hence, if we are able to decrease the L_g of our device, we can achieve a higher f_T than that obtained previously.

4.3.2 Temperature dependency of f_T and f_{max}

The temperature-dependent small-signal RF performance of the fabricated AlGaN/GaN HEMT was characterized in the same frequency range of 0.5 to 20 GHz with a Keysight P5004A vector network analyzer. The device dimension was also kept the same as L_{gs} / L_g / L_{gd} = 4/2/4 μm. The temperature was varied from 25 to 125 °C with a 25 °C interval. In Fig. 4.5 (a) and (b), U and $|H_{21}|$ vs frequency were plotted at 25, 75, and 125 °C. The f_T and f_{max} were estimated from $|H_{21}|$ and U, respectively.

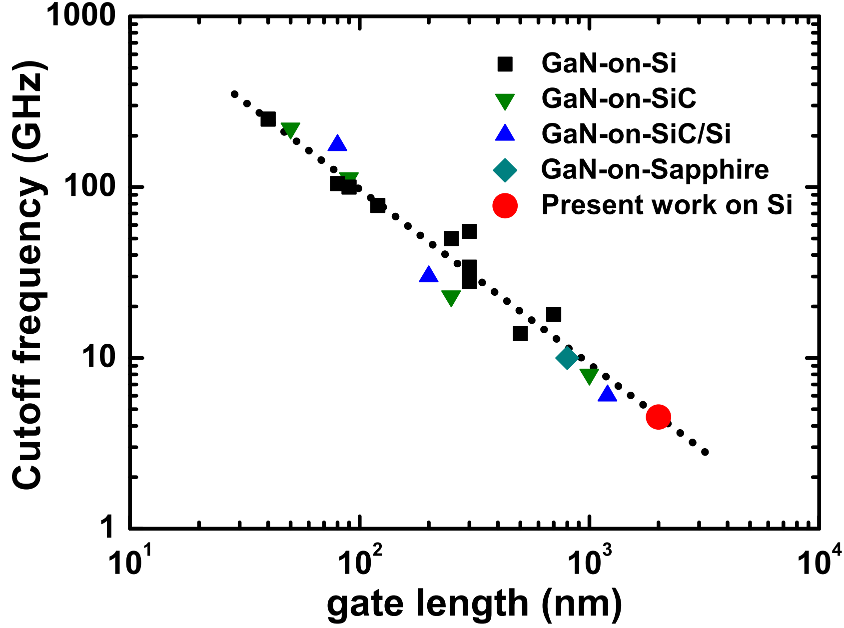

Figure 4.4: Comparison of f_T vs L_g with previous reports of GaN-on-Si [10–18], GaN-on-SiC [19–22], GaN-on-SiC/Si [23–25] and GaN-on-sapphire [26].

Evaluated values of f_T and f_{max} at room temperature ($\sim$ 25 °C) were 4.8 and 10 GHz, respectively under $g_{m,max}$ biasing condition of $V_g = -1$ V and $V_d = +$ 10 V. A different device with same dimensions was used for temperature-dependent studies. For that reason, the room temperature values of f_T and f_{max} were slightly changed. Obtained values of f_T and f_{max} at all temperatures are plotted in Fig. 4.6 where it can be seen that f_T and f_{max} were slightly deteriorated with increasing temperatures. The degradation of f_T is also associated with deterioration of 2DEG likewise the DC performance at high temperatures. Because f_T is an intrinsic property like g_m and their relationship is shown in Eq. 4.11, [27,28] where C_{gg} is the total gate capacitance. The C_{gg} can also be expressed as (C_{gs} + C_{gd}), where C_{gs} and C_{gd} represent intrinsic gate-to-source and gate-to-drain capacitances, respectively.

$$f_T = \frac{g_m}{2\pi C_{gg}} = \frac{g_m}{2\pi(C_{gs} + C_{gd})} \tag{4.11}$$

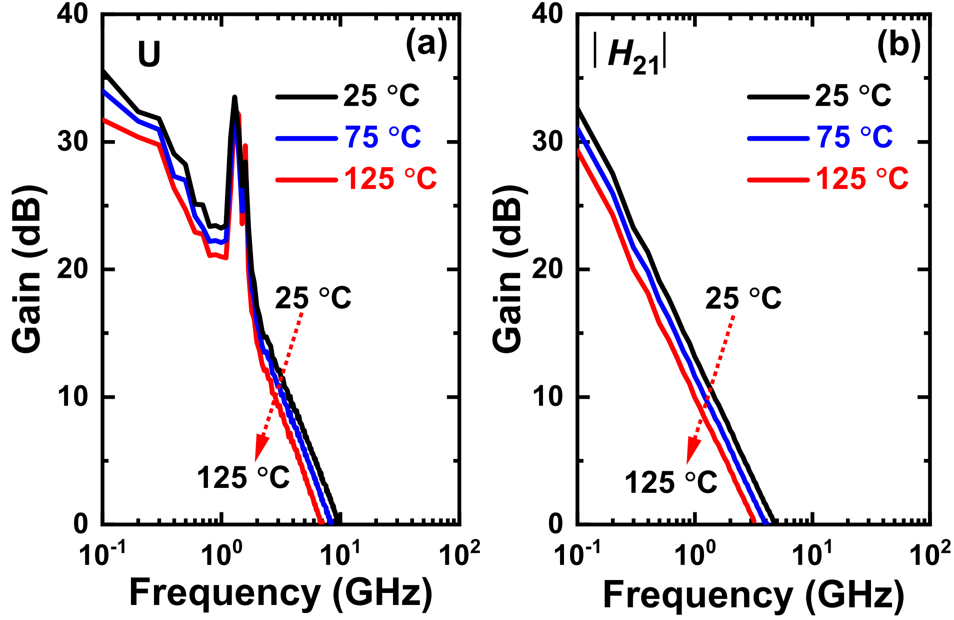

Figure 4.5: (a) Temperature-dependent Mason's unilateral gain (U), and (b) current gain $|H_{21}|$ vs frequency. U and $|H_{21}|$ were plotted at 25, 75, and 125 °C for 2 μm gate length device at $V_{\mathrm{d}} = +\ 10$ V and $V_{\mathrm{g}} = -\ 1$ V.

4.3.3 Small-signal equivalent circuit parameters extraction

A typical small-signal equivalent circuit model of AlGaN/GaN HEMTs is illustrated in Fig. 4.7 [29]. The parameters of the small-signal equivalent circuit are divided into two groups, which are the intrinsic (*i.e.* g_{m}, g_{d}, C_{gs}, C_{gd}, C_{ds}, R_{i}, and τ) and extrinsic (*i.e.* C_{pg}, C_{pd}, L_{g}, L_{s}, L_{d}, R_{g}, R_{s}, and R_{d}) parameters. It is assumed that the extrinsic parameters are bias-independent. They are designed to model the interconnections between the transistor and outside world. The extrinsic capacitances C_{pg} and C_{pd} originate from the capacitive coupling pads or previously mentioned open pads, the extrinsic inductances L_{g}, L_{s}, and L_{d} represent the inductive effects which arise from the metal pads and access transmission lines. These inductances are also referred as parasitic inductances. Extrinsic resistances R_{s} and R_{d} usually generate from the source and drain ohmic contacts. The resistance of gate metal *i.e* Ni/Au is the source of R_{g}. An input series RC network (C_{gs} and R_{gs}), a feedback

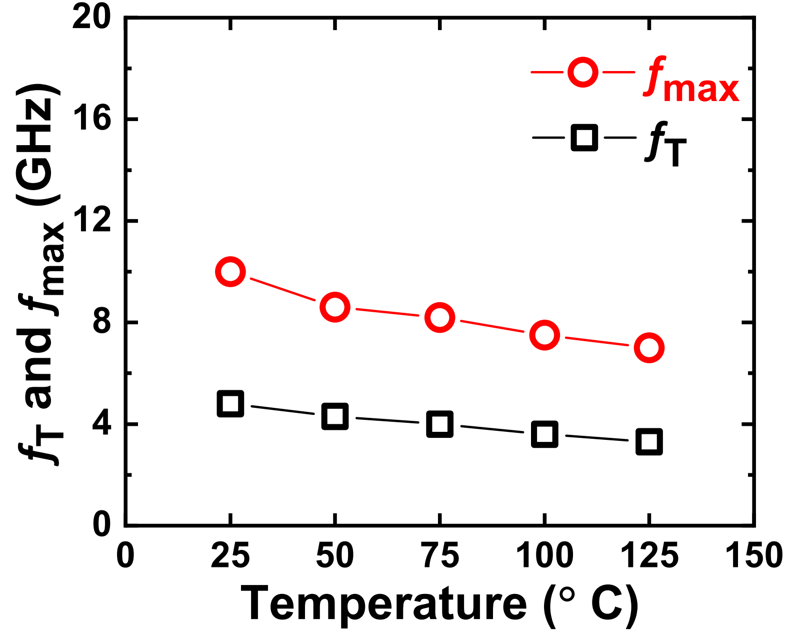

Figure 4.6: f_{T} and f_{max} at 25, 50, 75, 100, and 125 °C for the 2 μm gate length device at $V_{\mathrm{d}} = +\,10$ V and $V_{\mathrm{g}} = -\,1$ V.

series RC network (C_{gd} and R_{gd}), an output parallel RC network (C_{ds} and g_{d}), and a voltage-controlled current source (g_{m} and τ) are the main elements of the small-signal equivalent circuit's intrinsic part [30]. The change of depletion charge for the gate to source and drain to source voltages are modelled using C_{gs} and C_{gd}, respectively. These two parameters are very crucial for the RF performance of the device. The C_{ds} is the intrinsic capacitance between drain and source of the device. The intrinsic and output transconductances are g_{m} and g_{d}, respectively and R_{i} represents the intrinsic channel resistance *i.e* the sheet resistance. In this work, the extrinsic parameter L_{s} was not included as its significance was almost negligible.

The small-signal equivalent circuit model which is depicted in Fig. 4.7 was applied to analyze the fabricated HEMT performance and extract the intrinsic and extrinsic parameters. Evaluated parameters are listed in Table 4.1. Taking the value of C_{gs} and g_{m} from Table 4.1, the f_{T} was estimated to be 5.5 GHz, using Eq. 4.11. This

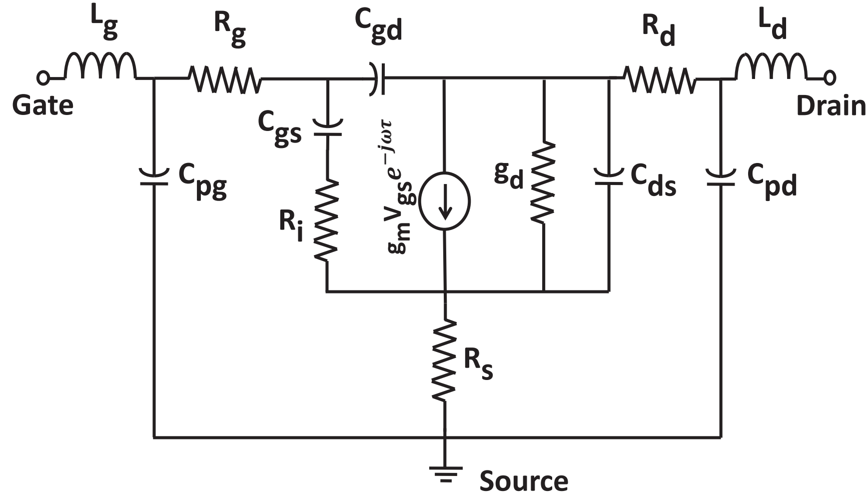

Figure 4.7: The small-signal equivalent circuit model.

value is in accordance with our measured f_T of 4.8 GHz at room temperature. Hence, the extracted parameters verified the accuracy of the pad capacitances and f_T, which indicates the effectiveness of the applied small-signal equivalent circuit model.

Table 4.1: The small-signal equivalent circuit parameters.

g_m	R_i	R_d	R_s	R_g
15.0 mS	23.4 Ω	74 Ω	0.003 Ω	9 Ω

C_{gs}	C_{gd}	C_{pg}	C_{pd}	C_{ds}
0.43 pF	0.031 pF	0.059 pF	0.061 pF	0.016 pF

g_d	L_g	L_d	τ	Calculated f_T
2700 Ω	0.0001 nH	0.003 pH	5 pS	5.5 GHz

• Temperature dependency of small-signal equivalent circuit parameters :

The mentioned small-signal equivalent circuit model is used to estimate the temperature dependency of the extracted parameters. The temperature was varied from 25 to 125 °C with a 25 °C step. All the temperature-dependent equivalent circuit parameters are listed in Table 4.2.

Table 4.2: Temperature-dependent extracted small-signal equivalent circuit parameters.

Parameters	25 °C	50 °C	75 °C	105 °C	125 °C
C_{gs} (pF)	0.39	0.39	0.4	0.4	0.4
C_{gd} (pF)	0.037	0.036	0.035	0.035	0.035
C_{pg} (pF)	0.06	0.06	0.06	0.06	0.06
C_{pd} (pF)	0.041	0.046	0.045	0.045	0.46
C_{ds} (pF)	0.053	0.05	0.044	0.04	0.045
g_{m} (mS)	14.8	14.4	13.2	12.03	10.6
R_{i} Ω	19.9	20	23.9	25.9	28.4
R_{s} Ω	0.003	0.003	0.003	0.003	0.003
R_{d} Ω	74	74	74	74	74
R_{g} Ω	13	13	13	13	13
g_{d} Ω	2700	2700	2700	2700	2700
τ (pS)	3	3	3	4	4

In the previous section, we assumed that the reason for degradation of f_{T} is associated with the intrinsic property of device *i.e* on g_{m}. However, to confirm the dependence of f_{T} on g_{m}, we extracted g_{m} at every temperature point using Eq. 4.11 and compared with the measured g_{m} from DC characteristics. For the evaluation of

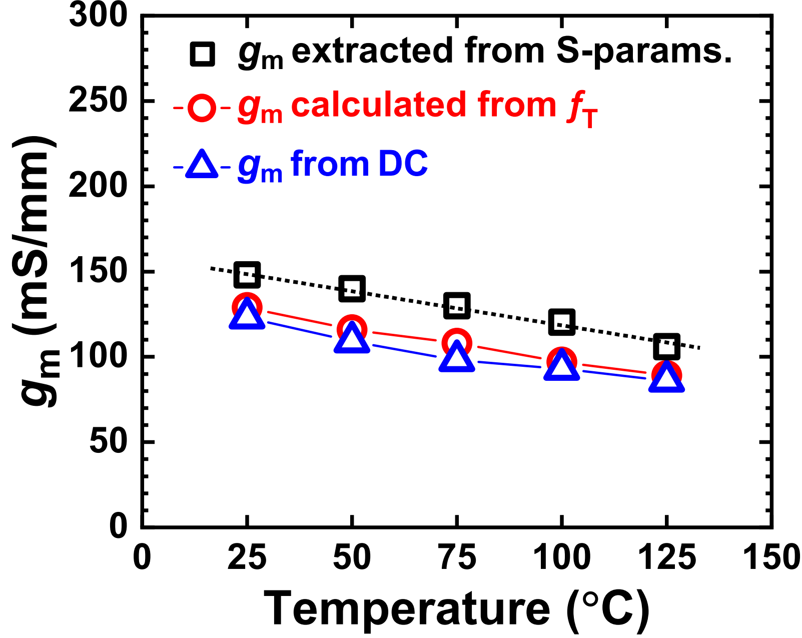

Figure 4.8: A Comparison between extracted g_m from S-parameters, calculated g_m from Eq. 4.11, and measured $g_{m,max}$ from DC characteristics with varying temperature.

g_m from f_T, C_{gg} was taken as 0.43 pF, extracted using the small-signal equivalent circuit model that was depicted in the previous section as Fig. 4.7 [29]. Moreover, to gain a better understanding of the achieved microwave characteristics, we also extracted temperature-dependent small-signal equivalent circuit parameters. The extracted temperature-dependent intrinsic and extrinsic parameters showed minimum temperature sensitivity except for the intrinsic g_m and input resistance (R_i) (as shown in Table 4.2) and the trend of these parameters agrees with Ref. [31]. As R_i denotes the channel resistance, it increased with temperature because of the temperature dependency of 2DEG sheet resistance. The extracted values of intrinsic g_m and R_i at room temperature were 148 mS/mm and 19.9 Ω, whereas at 125 °C, it were 106 mS/mm and 28.4 Ω, respectively. The comparison between g_m measured from DC characteristics, extracted from S-parameters and calculated from Eq. 4.11, is presented in Fig. 4.8. It can be seen that both the g_m measured from DC characteristics

and calculated from Eq. 4.11, are very closely comparable which confirmed that the small degradation in small-signal performance was mainly due to the 2DEG properties of the AlGaN/GaN interface. If there was a generation of charge carriers at high temperatures, the g_{m} values were not comparable owing to high leakage through the epitaxial layers. In addition, the extracted intrinsic g_{m} from S-parameters is also consistent with our measurement results. Thus, suppression of RF leakage at high temperatures was successfully attained and significant temperature stability was observed in the reported GaN HEMT on 3C-SiC/Si [32].

4.3.4 RF loss estimation with S-parameter measurement of pads

For a primitive study of the frequency response of RF loss, the open pad de-embedding method was used in our device structure [33]. Open pads are nothing but metallic pads made of Ti/Al/Ni/Au metal stack on the etched 2DEG layer, as shown in Fig. 4.9 where the designed open pad structure on photo-mask and its cross-sectional structure on the fabricated device is represented. It can be seen that both the metallic pads have no connection between them, thus can be termed as open pads. The parasitic pad capacitances and resistances were evaluated from the S-parameter measurements of the open pad structures.

S-parameters describe the response of an N-port network to signal(s) incident to any or all of the ports, where S_{11} is the ratio of reflected signal and input signal at one port network. Here the open pads can be assumed as a one-port network as the S-parameter measurements were performed individually on each side by connecting only one port, while the other port was kept open. The response of S-parameter measurements (S_{11}) of open pads can be described using Fig. 4.10. In the case of ideal pad characteristics, S_{11} should move along the periphery of the smith chart, as shown with a black line in Fig. 4.10. On the other hand, in the case of lossy response, the trend of S_{11} will be inward or toward the center of the smith chart, as represented

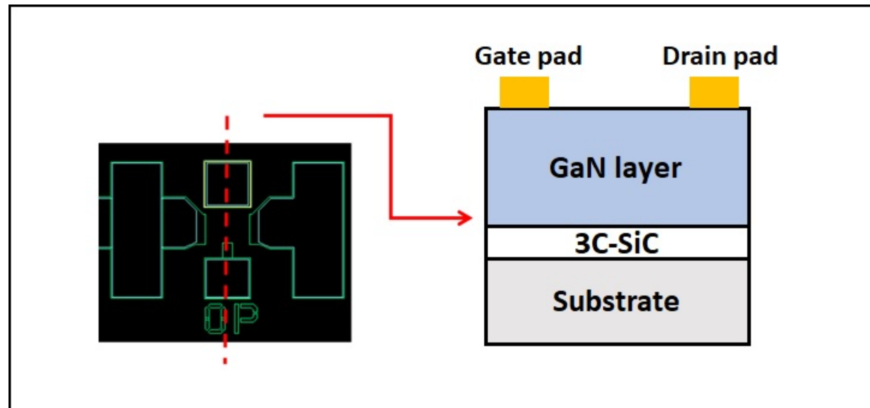

Figure 4.9: A cross sectional structure of open pads fabricated on the etched 2DEG layer.

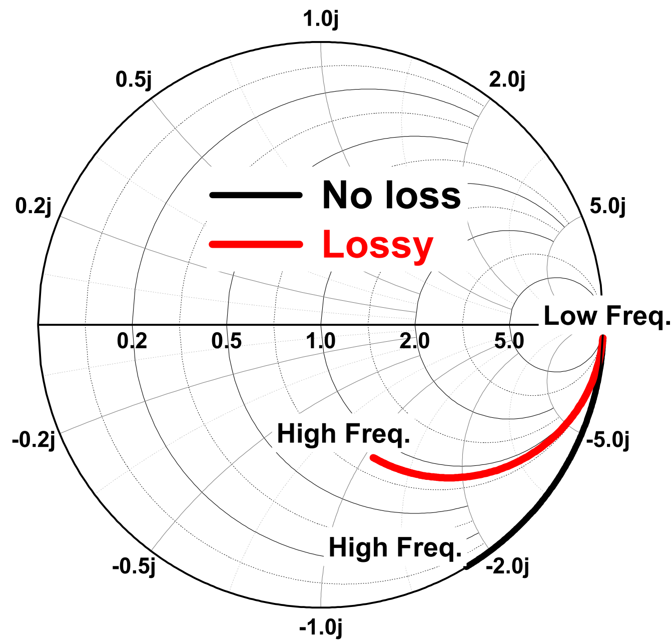

Figure 4.10: Comparison of ideal and lossy pad characteristics.

with a red line in Fig. 4.10. For a better understanding of the lossy parameters *i.e* the parasitic capacitances and resistances, the S_{11} data can be fitted with a simple RC series circuit, as shown in Fig. 4.11.

In this work, S-parameter measurements of pads were performed in the frequency range of 0.5 to 20 GHz with a Keysight P5400A vector network analyzer. The system

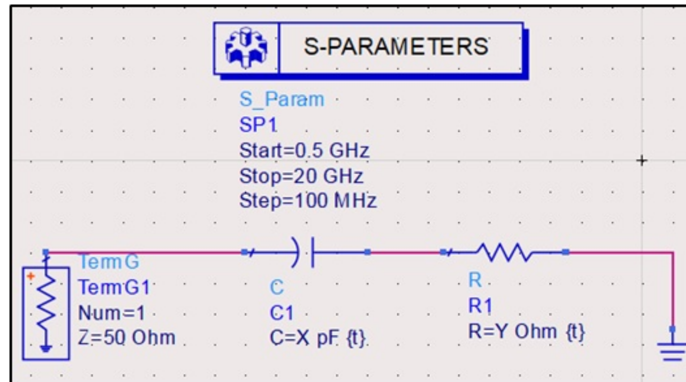

Figure 4.11: RC circuit to extract the parasitic capacitances and resistances from the pad characteristics.

was calibrated with the previously mentioned open-short-load-through calibration setup. As the pads of both sides were measured independently, only the S_{11} was evaluated from both the gate and drain sides. The evaluated pad characteristics were almost the same for both the sides and because of that only the S_{11} of the gate side

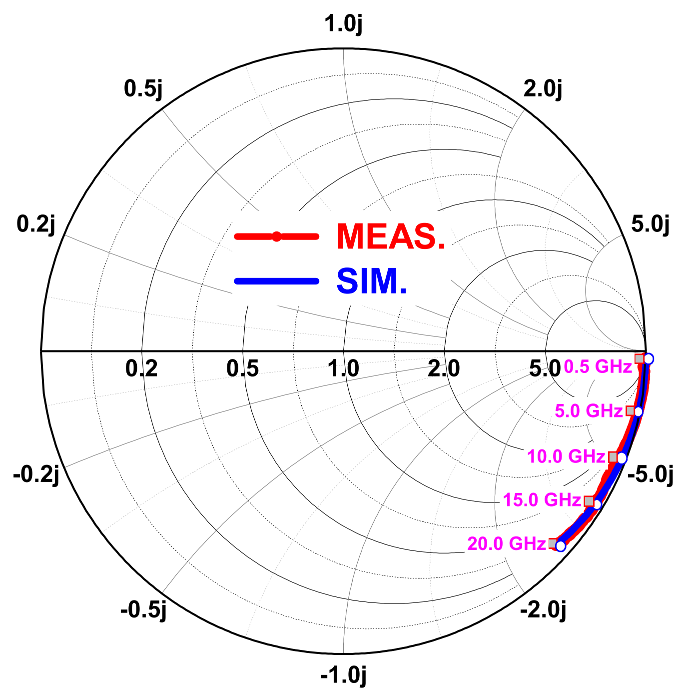

Figure 4.12: S_{11} of open pad structure in the frequency range of 0.5 to 20 GHz.

is represented in Fig. 4.12. The previously mentioned RC circuit was used to extract the parasitic capacitance and resistance. Extracted values of the gate (C_{pg}) and drain (C_{pd}) side capacitances were 0.059 and 0.061 pF, respectively. Similarly, the gate and drain side parasitic resistances were 9.5 and 11.5 Ω, respectively. Afterwards, taking the value of C_{pg} and total gate pad area (S_{g}) of 4.9×10^{-5} cm^2, the nitride layer thickness (d) was calculated using Eq. 4.12.

$$C_{\mathrm{pg}} = \epsilon \frac{S_{\mathrm{g}}}{d} \tag{4.12}$$

where ϵ is the permittivity of GaN. The estimated value of d is 7.1 μm. As the etching depth was $\sim$ 300 nm, the actual effective nitride layer thickness was (8.0 μm $-$ 300 nm), which is 7.7 μm. Hence, the pad measurement confirms the nitride layer thickness. It is also evident that if we can increase the d, we can significantly reduce the parasitic capacitances, thus improve the high-frequency performance of the device.

• Temperature-dependent open pad characteristics :

Further, loss evaluation at high temperatures was analyzed by temperature-dependent on-wafer S-parameter measurements on the open pad structures in the 0.5 to 20 GHz frequency range. In the same way, the temperature was varied from 25 to 125 °C in 25 °C increments. Very low and unaltered S-parameter (S_{11}) of the open pad structures were observed from Fig. 4.13, where S_{11} at 25, 75, and 125 °C are represented. The above observation also indicates the thermal stability of the device. Hence, it can be said that the thick nitride layer efficiently suppressed the increment of charge carrier density at high temperatures and there was no evidence of leakage from the epitaxial layers of the device.

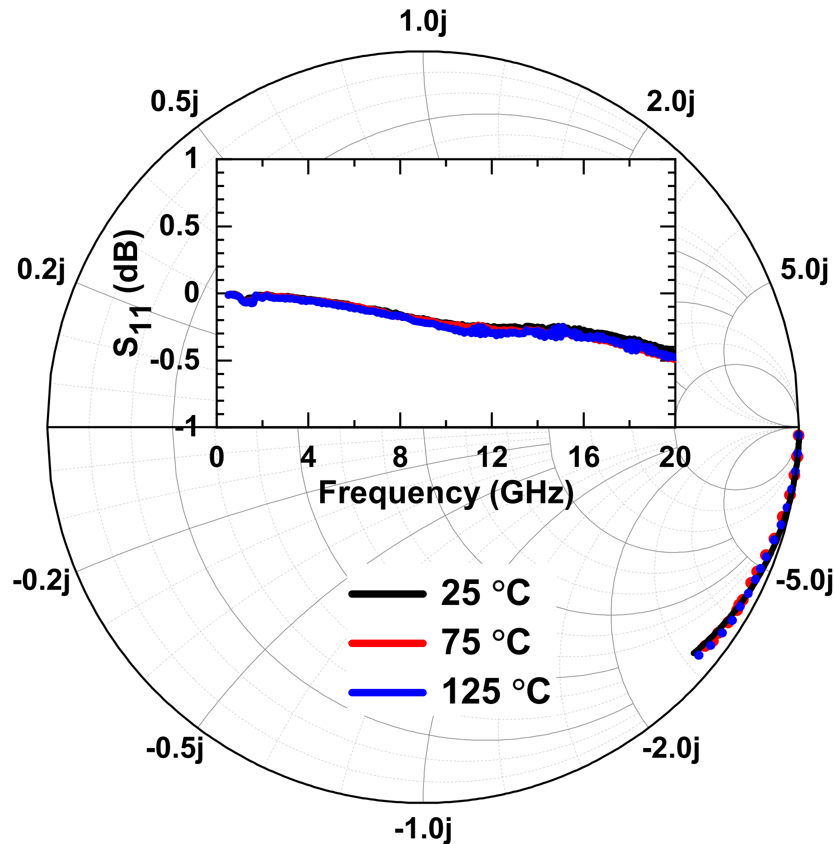

Figure 4.13: S_{11} of the open pad structures at 25, 75, and 125 °C in the frequency range of 0.5 to 20 GHz.

4.4 Large signal characteristics

To effectively use the AlGaN/GaN HEMTs for high-power and high-frequency applications, the attainment of high output power and high associated gain is required. Other desirable parameters are large drain breakdown voltage, power added efficiency, and high drain efficiency. In this work, the HEMTs were biased for class A amplifier operation at a fundamental frequency of 2 GHz (L-band). For choosing the right mode of amplifier operation, selection of the operating point on $I-V$ characteristics is crucial as AC microwave signal swings about the operating point [34].

• Class A amplifier operation

To achieve a class A amplifier operation, the biasing of the HEMT is done in a way that the Q-point stays at the middle of the load line, as shown in Fig. 4.14. The reason for choosing the Q-point in the middle is to conduct current over the full input 360 degrees cycle without driving to cut-off or saturation region. However, because of this working principle, the transistor never turns off, which is considered to be a disadvantage of class A amplifier. Nevertheless, with proper design of operating points and biasing conditions, class A amplifiers provide some advantages such as excellent linearity, high gain, and low signal distortion.

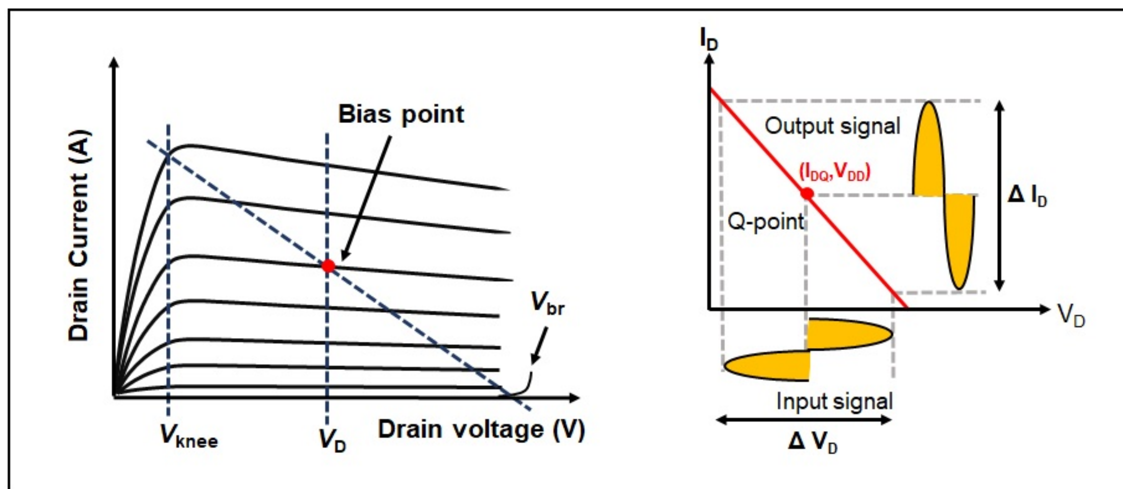

Figure 4.14: $I-V$ characteristics of HEMT with a load line and biasing point (Q-point) set for a Class A amplifier operation.

As shown in Fig. 4.14, for class A operation, the device conducts through a full cycle of the output waveform. Since class A amplifier operates in the linear region, selection of dc biasing point is very crucial to ensure appropriate operation. It is already mentioned that the device is always on as the input and output signal waveform conducts in a full cycle of 360 degrees. As a reason, the device is continuously carrying current which in turn generates a continuous loss of power, thus heat generation occurs.

This phenomenon tremendously affects efficiency and inevitably makes it unsuitable for high-power applications. The choice of Q-point and waveform of input and output signal is clearly shown in Fig. 4.14. The expected maximum output power from class A amplifier is given by Eq. 4.13 [35],

$$P_{\text{max}} = \frac{I_{\text{DSS}}(V_{\text{br}} - V_{\text{knee}})}{8} \tag{4.13}$$

where I_{DSS}, V_{br}, and V_{knee} are the maximum drain current, the drain breakdown voltage, and the knee voltage, respectively, as presented in Fig. 4.14. From this equation it is very clear that to achieve higher output power, the I_{DSS} and V_{br} needs to be large enough. For that, the GaN-based RF amplifier is preferable because GaN has a much higher breakdown voltage than conventional group-III nitrides.

However, for the simplification purpose, the output power of the fabricated HEMT in class A operation can be modelled as Eq. 4.14, following the Fig. 4.14. The $\Delta\ V_{\text{D}}$ and $\Delta\ I_{\text{D}}$ are the full voltage and current swing, respectively.

$$P_{\text{out}} = \frac{1}{8}\Delta V_{\text{D}}\Delta I_{\text{D}} \tag{4.14}$$

Now if the input ac power is termed as P_{in} and output DC power is termed P_{DC}, the maximum theoretical efficiency of a class A amplifier can be defined as the Eq. 4.15.

$$\eta = \frac{P_{\text{out}}}{P_{\text{DC}}} \tag{4.15}$$

P_{out} is already mentioned in Eq. 4.14 and P_{DC} can be defined as Eq. 4.16

$$P_{\text{DC}} = I_{\text{DQ}} V_{\text{DD}} \tag{4.16}$$

The Eq. 4.14 can be further defined as

$$\begin{aligned}
P_{\text{out}} &= \frac{1}{8}\Delta V_{\text{D}}\Delta I_{\text{D}} \\
&= \frac{1}{8}(2V_{\text{DD}} \times 2I_{\text{DQ}}) \\
&= \frac{1}{8}(R \times P_{\text{DC}}),\ as\ P_{\text{DC}} = I_{\text{DQ}}V_{\text{DD}} \\
&= \frac{1}{2}P_{\text{DC}}
\end{aligned} \tag{4.17}$$

where the current and voltage at the selected Q-point are defined as I_{DQ} and V_{DD}, respectively. Now again from Eq. 4.15,

$$\begin{aligned}
\eta &= \frac{P_{\text{out}}}{P_{\text{DC}}} \\
&= \frac{1}{2} \times 100\% \\
&= 50\%
\end{aligned} \tag{4.18}$$

which means that the maximum theoretical output efficiency that we can achieve from a class A amplifier is 50%.

4.4.1 Load-pull measurement

With a given load impedance, the achievable maximum output power of an active device can be obtained using a load-pull measurement system. By driving the active device into compression and varying the load, the device's performance and characteristics can be evaluated in both its non-linear region and across the impedance plane [36].

In this work, Focus Microwave's on-wafer load-pull measurement system was used to analyze the power performance. The schematic of the load-pull measurement set-up is shown in Fig.4.15 and the actual setup of the system used at the Nagoya Institute of Technology, is shown in Fig. 4.16. The Focus Microwave load-pull set-up comprises two automated tuner systems with electromechanical tuners at both the

input and output sides. A signal generator (in this case: a Rigol DSG6030 signal generator of frequency range 9 kHz to 6 GHz) produces input power, which is then amplified by 35 dB using an amplifier. Afterward, the amplified input power is fed via an input coupler, coaxial-switch, and bias-T through the tuner to the GSG probe tips at the device. A power sensor was also used to measure the power for both the input and output ports. The output port of the device is also connected with the same coupler, bias T, and power sensor. A power meter was also used to monitor the power measured by the sensor. As mentioned earlier, the main parameters that are extracted from the power measurements are output power and PAE which follows the Eq. 4.19.

$$PAE = \frac{P_{\text{out}} - P_{\text{in}}}{P_{\text{DC}}} \tag{4.19}$$

where P_{in}, P_{out}, and P_{DC} are the input power, output power, and the DC power, respectively. Using computer-controlled automated tuners, we can find contours of constant output power plotted on a smith chart, and from that, the optimum point of operation can be estimated with optimum accuracy. The ratio of output and input power (at a given frequency) is termed as gain. To successfully perform the load-pull, the impedance or the reflection point needs to be controlled which is presented to the DUT. Most importantly selecting the correct biasing point is necessary to obtain the maximal power in a given mode of amplifier operation [37].

Continuous-wave (CW) on-wafer RF power measurements were carried out at 2 GHz fundamental frequency on the device with L_{g} and W_{g} of 2 and 2 × 50 μm, respectively. The gate was biased at − 1.5 V for class A amplifier operation and V_{d} was varied from + 10 to + 30 V. Input and output impedances were matched for the optimum PAE. At V_{d} = + 22.5 V, the input (P_{in}) vs output power (P_{out}) response exhibited a maximum PAE of 47 % while delivering 23.1 dBm output power with a maximum linear gain of 17.2 dB, displayed in Fig. 4.17. The associated drain

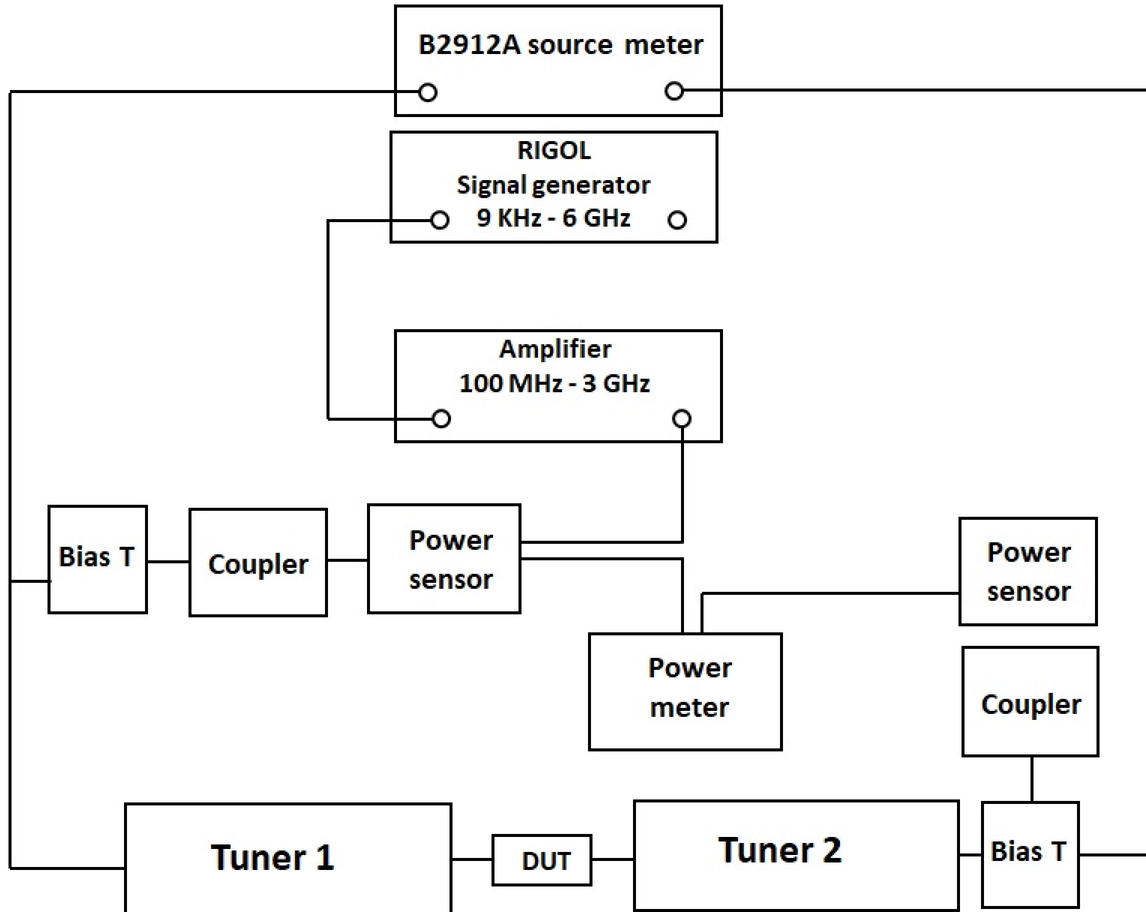

Figure 4.15: Schematic of the setup of Focus microwave load-pull measurement system used to characterize the power performances.

efficiency (DE) or output efficiency was calculated to be 51.5 %, which is almost similar to the theoretical output efficiency of an ideal class A amplifier which is 50 % (as mentioned in Eq. 4.18). Drain bias dependency of PAE and P_{out} is shown in Fig. 4.18, where the output power and PAE saturated at V_d of + 22.5 V and start deteriorating beyond that. We assume that current collapse beyond drain bias of + 22.5 V is the reason for the degradation of P_{out} and PAE. It was described in Chapter 3, that the device suffered a current collapse at drain bias of +20 V. RF output power of a class A amplifier follows the equation 4.17, where P_{out} is proportional to maximum drain voltage swing or (2 × V_d) and maximum drain current swing (I_{max}

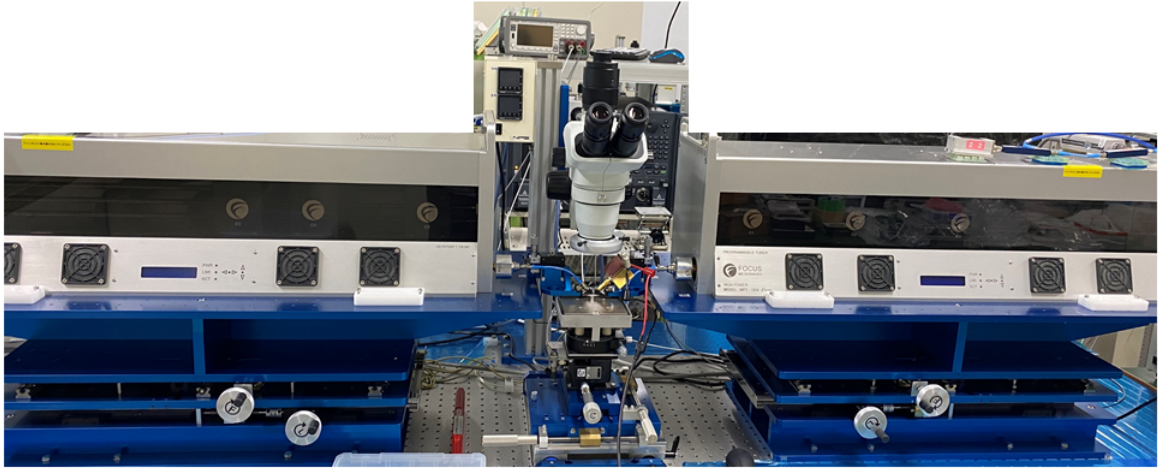

Figure 4.16: The setup of Focus microwave load-pull measurement system used in the measurement laboratory at Nagoya Institute of Technology.

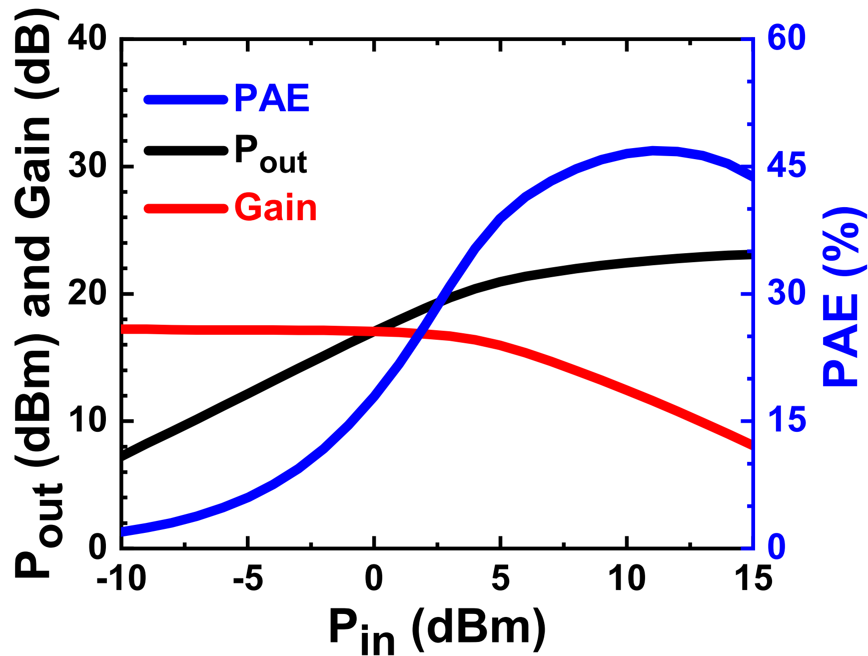

Figure 4.17: CW power measurement at 2 GHz fundamental frequency of the AlGaN/GaN HEMT with L_g of 2 μm and W_g of 2 $\times$ 50 μm. The biasing condition for optimum PAE was $V_d = +$ 22.5 V and $V_g = -$ 1.5 V.

or 2 $\times$ I_d). Using Eq. 4.17, P_{out} was calculated for 10, 15, 17.5, 20, and 22.5 V drain bias taking I_{max} as drain current at V_g = 0 V. Extracted data was compared with

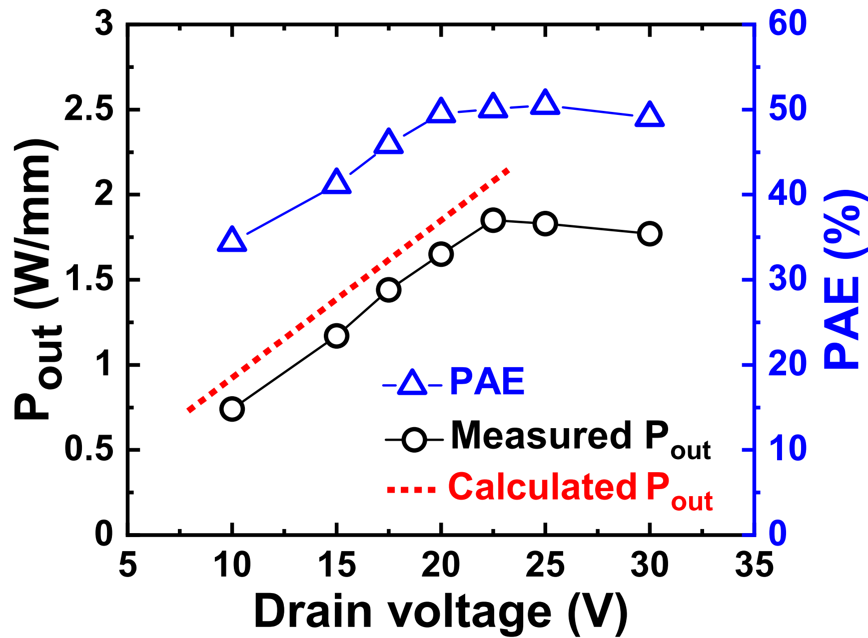

Figure 4.18: Drain bias dependency of P_{out} and PAE where V_d was varied from + 10 to + 30 V and V_g was − 1.5 V. The red line is the calculated P_{out} from Eq. 4.17 at each drain biasing point.

P_{out} obtained from CW power measurement. As represented in Fig. 4.18, both the P_{out} up to + 22.5 V showed excellent comparability and continuity.

• Temperature-dependent load-pull measurement

The temperature-dependent power performance of the device was also evaluated. The biasing was set at optimum conditions for maximum PAE and P_{out}, which were $V_d =$ + 22.5 V and $V_g =$ − 1.5 V. The temperature was varied from 25 to 125 °C in a 25 °C increment. P_{out}, linear gain, and PAE vs P_{in} characteristics with varying temperatures is shown in Fig. 4.19 (a) and (b). With increasing temperature, a small degradation of linear gain, P_{out} and PAE were observed. As in our case, as the drain bias was fixed at + 22.5 V, there was no change in the voltage swing which means the decrement of P_{out} is mainly because of the deterioration of I_d. It is already discussed that a significant increment of phonon concentration at high-temperature causes increased

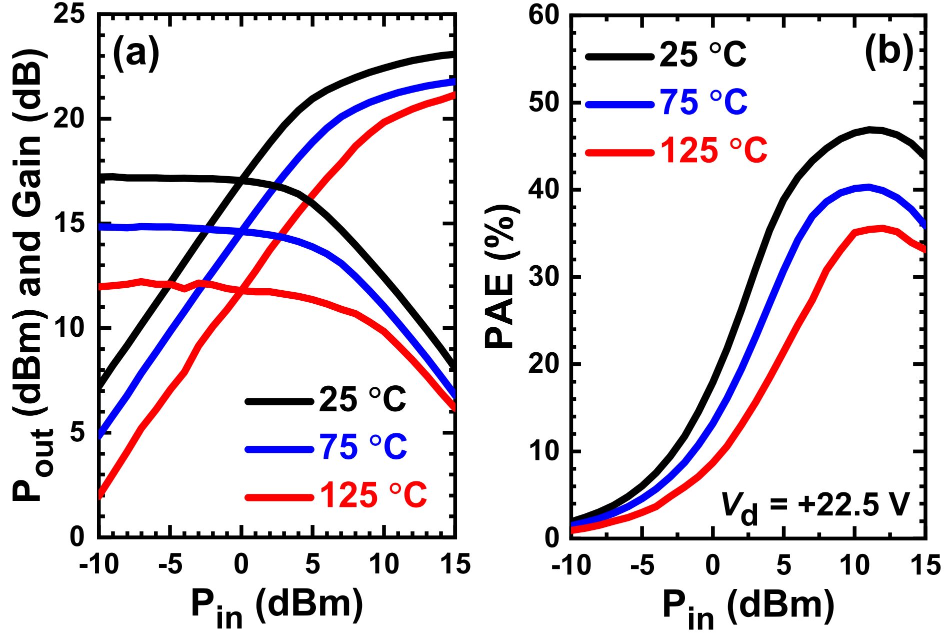

Figure 4.19: (a) Temperature-dependent P_{out} and gain, and (b) Temperature dependence of PAE at $V_d = +\ 22.5$ V and $V_g = -\ 1.5$ V of the device with $L_g = 2\ \mu$m and $W_g = 2 \times 50\ \mu$m. The temperature was varied from 25 to 125 °C with a step of 25 °C.

scattering which crucially degrades the mobility of the epitaxial structure which in turn degrades the I_d [38–40].

4.4.2 Temperature-dependent output power

We calculated P_{out} at every temperature point using Eq. 4.17, where V_d was fixed at + 22.5 V and I_d was taken for $V_g = 0$ V. The calculated P_{out} at each temperature point were also compared with the P_{out} measured from load pull, as depicted in Fig. 4.20. An excellent comparability between the calculated and measured P_{out} strongly confirmed that the slightly degraded power performance was strongly due to the temperature dependency of DC performance. It further confirms that there was no buffer or substrate leakage from the device and possibility of charge carrier increment at high temperature was also eliminated. A comparative study of the decremental

rate of P_{out} and PAE is shown in Table. 4.3 [41, 42]. The rate of change of P_{out} and PAE with temperature, denoted as Δ P_{out}/temp and Δ PAE/temp, respectively are calculated by taking the rate of decrement for 1 K temperature change, which can be demonstrated as Eq. 4.20.

$$\Delta P_{\text{out}}/temp = \frac{P_{\text{out}}(RT) - P_{\text{out}}(HT)}{P_{\text{out}}(RT)}/\Delta T \tag{4.20}$$

Table 4.3: Comparison of P_{out} and PAE with previously reported results.

References	Δ P_{out} / temp (K^{-1})	Δ PAE / temp (K^{-1})	Frequency (GHz)
Present Work	0.0035	0.002	2
Ref. [41] on HR-Si	0.002	0.0013	3
Ref. [42] on SiC	0.004	–	2

In Eq. 4.20, P_{out} (RT) is the output power at room temperature, P_{out} (HT) is the output power at the highest temperature, and Δ T is the difference between the highest and room temperature. Δ PAE/temp is also calculated in the same way as Δ P_{out}/temp. The above data also demonstrates the comparable amplifier characteristics of our device.

4.5 Summary

We observed a significant and high-temperature stable L-band amplifier performance in GaN HEMTs on 3C-SiC/Si by introducing an 8 μm thick nitride layer. Temperature-dependent small-signal characteristics showed excellent stability even at high temperatures of up to 125 °C. At room temperature, the device achieved a well comparable

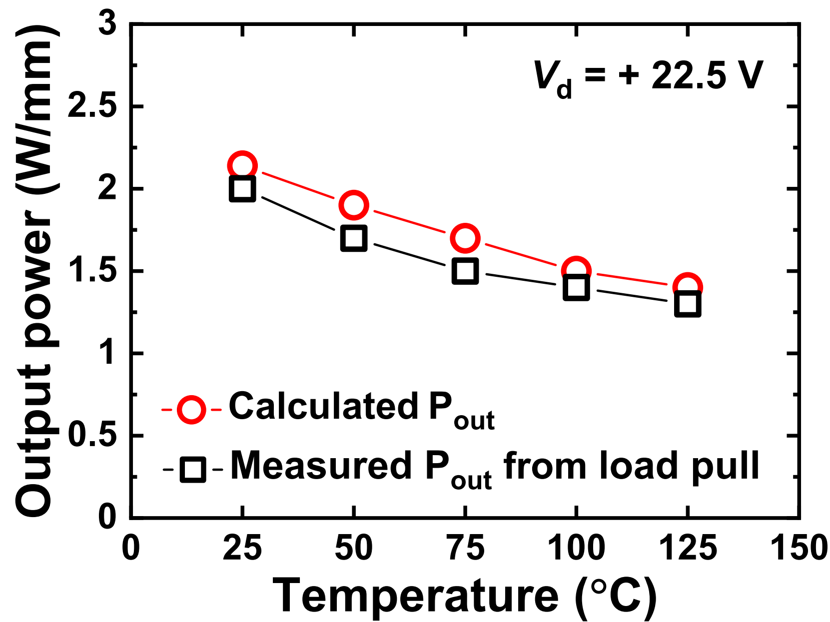

Figure 4.20: A Comparison between evaluated P_{out} from temperature-dependent load pull measurement and calculated P_{out} from Eq. 4.17 at each temperature point.

f_T of 4.8 GHz for 2 μm gate length device. Very low and identical S_{11} of the open pad structures were observed in the temperature range of 25 to 125 °C which confirmed the suppression of generation of charge carriers at high temperature. From room temperature CW power measurements, a maximum output power of 2 W/mm along with a PAE of 47 % and a 17.2 dB of maximum linear gain were obtained. A comparative study of gain and power performance further confirmed that the detrimental effect of high temperature on DC characteristics was mainly responsible for the slight deterioration in RF performance. Summing up all the results, it can be concluded that the presented GaN HEMT on 3C-SiC/Si showed excellent and stable amplifier characteristics by suppressing any sort of leakage through the epitaxial layers.

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Chapter 5

Transmission loss analysis in AlGaN/GaN HEMTs on 3C-SiC/LR-Si by varying nitride layer thickness

5.1 Introduction

In the previous chapters, it was established that the AlGaN/GaN epitaxial structure with an 8.0 μm thick nitride layer achieved a significant temperature stable DC and RF characteristics. However, for applications of GaN-on-Si HEMTs in the RF domain, evaluation of transmission loss is a crucial factor. Regarding RF performance of GaN-based devices, three main losses that contribute to total RF loss are dielectric loss in the substrate, conductor loss, and radiation loss [1]. In the case of GaN-on-Si technology, high resistivity Si (HR-Si) substrate showed improved performance by reducing the substrate loss [2–4]. However, at high temperatures, charge carriers

generate in HR-Si which results in reduced resistivity and increased substrate loss [5, 6]. In addition, the manufacturing cost of GaN-on-HR-Si is higher than GaN-on-LR-Si technology [7]. With increasing development and interest in GaN-on-Si-based RF technology, the influence of epitaxial structure on RF loss in GaN-on-LR-Si becomes a crucial factor. It was already described in the previous chapters that GaN-on-3C-SiC/LR-Si structure with a thick nitride layer exhibits very low RF loss by eliminating the low resistivity of Si and also provides better thermal stability. However, the characterization of RF loss on metal pads is not sufficient to successfully establish the effect of the thick nitride layer on the frequency response of total RF loss.

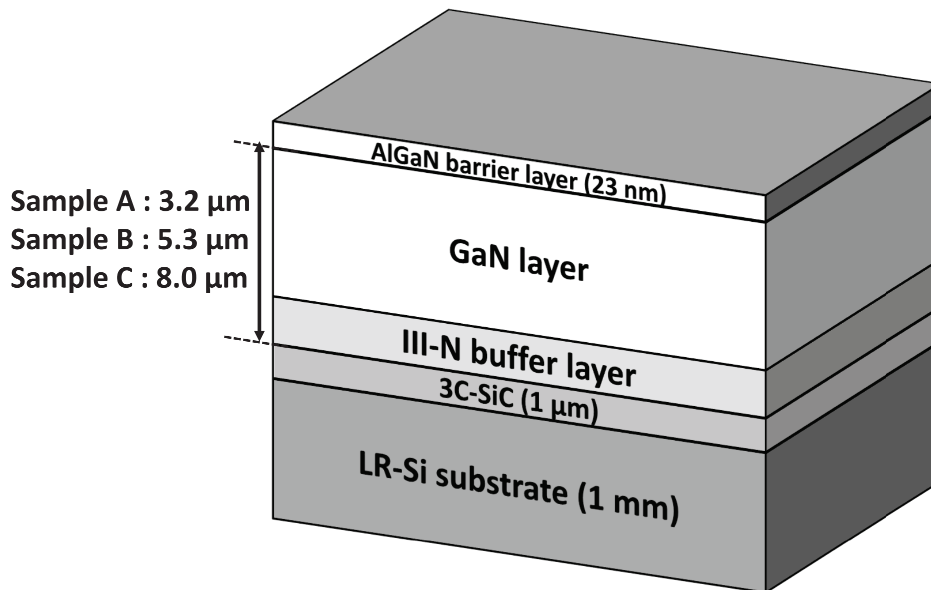

Figure 5.1: Three epitaxial structure of AlGaN/GaN HEMTs by varying nitride layer thickness, denoted by sample A, B, and C.

In this chapter, we used three different epi-structures (as shown in Fig. 5.1) with varying nitride layer thickness for a deeper understanding of the substrate RF loss. From the S-parameter measurements and EM simulated data, it was observed that the sample with the thickest nitride layer of 8.0 μm showed the minimal RF loss,

whereas the loss was almost doubled for the sample with a 3.2 μm thick nitride layer. The temperature-dependent study also confirmed the above observation.

5.2 Theory of transmission lines

A transmission line (TL) is used to transmit electrical power from source of a generating substation to a load of distribution units. Theoretically, TLs can propagate a signal at any frequency. The circuit shown in Fig. 5.2 represents a model of a TL segment. The primary constants of TLs can be defined as follows:

Resistance along the line/unit length = R

Inductance along the line/unit length = L

Conductance shunting the line/unit length = G

Capacitance shunting the line/unit length = C

where R, L, G, and C are referred to as resistance (Ω/m), inductance (H/m), conductance (S/m), and capacitance (F/m) per unit length, respectively.

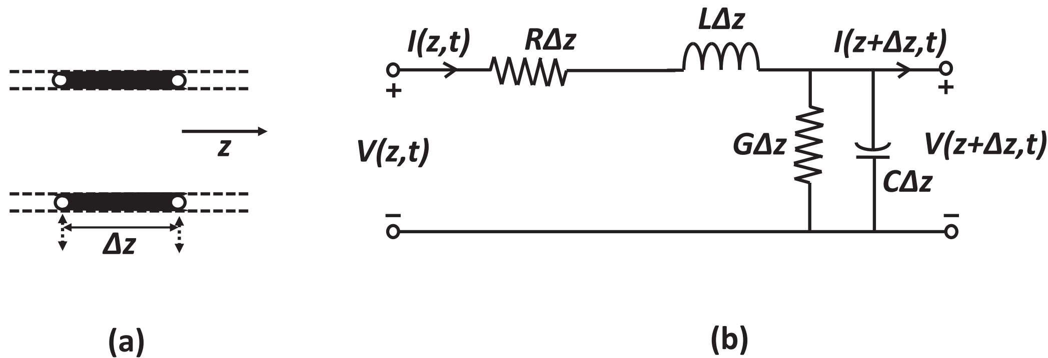

Figure 5.2: Segment of TL: (a) of length Δ z, and (b) lumped-element model.

A pair of linear differential equations that describes the voltage and current on an electrical transmission line with distance and time, is called the telegrapher's equations [8]. The Telegrapher's equations theory can be applied to all frequencies.

When a sinusoidal electromagnetic wave propagates in a given direction, the measure of change in amplitude and phase is called the propagation constant (γ). Now, the relationship between γ and RLGC components can be defined as Eq.5.1.

$$\gamma = \sqrt{(R + j\omega L)(G + j\omega C)} \tag{5.1}$$

where characteristic impedance Z is

$$Z = \sqrt{\frac{R + j\omega L}{G + j\omega C}} \tag{5.2}$$

TLs commonly met on printed circuit board are categorized in the following ways:

- **Stripline transmission line :**

Striplines consists of three layers of conductors, as shown in Fig. 5.3 (a), where the middle conductor is called the "hot conductor" and the other two conductors which are connected to the signal ground are called the "cold" or "ground" conductors. The characteristic impedance of the line is determined by the width of the hot conductor (W), the substrate thickness (h), and the relative permittivity of the substrate (ϵ_{r}). Striplines are non-dispersive and do not have any cutoff frequency as similar to the coaxial cables. Microstrips are better to have good isolation between adjacent traces. The speed of wave propagation in striplines is comparatively slow than microstrip lines, however, striplines provide enhanced noise immunity against the propagation of radiated RF emissions. Striplines have effective permittivity equal to the ϵ_r because wave propagation only happens in the substrate.

- **Microstrip line :**

Microstrip line (ML) comprises a conducting strip on the substrate with a ground plane on the backside, as shown in Fig. 5.3 (b). It is one of the most popular

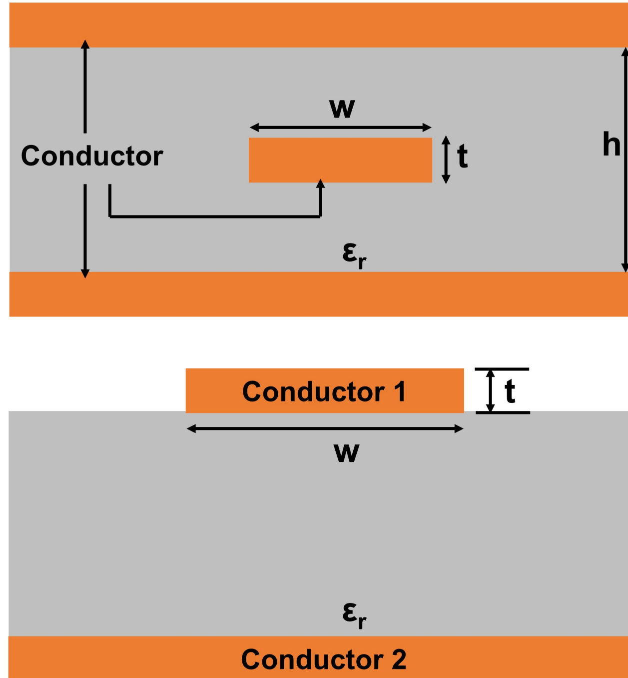

Figure 5.3: (a) Cross-sectional structure of a stripline, and (b) Microstrip line.

and widely used TL structures because it provides certain advantages such as simple planar structure, ease of fabrication, ease of integration, good heat sinking, and good mechanical support. Because of these, it is broadly used in high-power and high-frequency circuits. Among its widespread and popular applications, antennas, couplers, filters, power dividers are the ones that are usually formed with MLs. MLs are less expensive than the other available waveguide technologies. However, the power handling capabilities are very low and susceptible to cross-talk and unintentional radiation [9].

- **Coplanar waveguides (CPWs) :**

Apart from Microstrip and Stripline, another alternative TL structure is coplanar Waveguide (CPW) where the signal line or the conducting line is separated by a

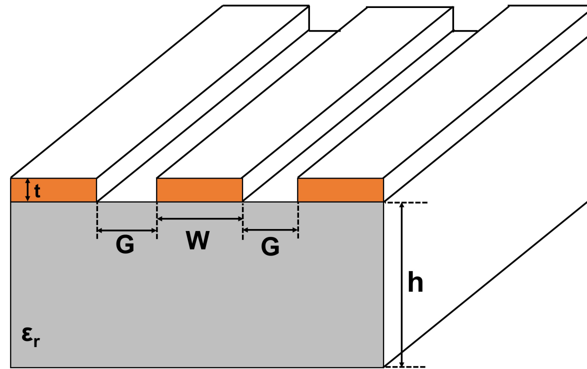

Figure 5.4: Schematic of a CPW structure, where h is the substrate thickness, W is the width of signal line, and G is the gap between signal line and ground plates.

certain gap with two ground planes situated on other sides. All the three conducting metallic strips are on the same side of the substrate and hence are termed coplanar. A schematic of a CPW structure is shown in Fig. 5.4, where W and W_g are the width of conducting strip and the side ground planes, G is the distance between ground planes and conductor, and h is the thickness of the substrate. The substrate thickness is usually kept at or higher than twice the gap (G) to concentrate the electric fields into the substrate and lower the dispersion of signals. Moreover, the dimensions of the W, G, h are very important to precisely determine the characteristics impedance of the line and also the attenuation of the signal.

5.3 Line calculation of transmission lines in ADS Keysight

Advanced Design System (ADS) is the world's leading ECAD (electronic computer-aided design) software which is extensively used in high-frequency and high-speed digital applications.‘ It is widely used both in commercial and academic institutions as it can provide enormous support to develop complex RF circuits, design, analysis in the field of RF or microwave [10]. For the simulation of the transmission line of

AlGaN/GaN heterostructure on 3C-SiC/LR-Si, the following steps are performed.

• Layout simulation using *Line Calc* of ADS.

• Creation of a physical design in *Layout workspace* of ADS for EM simulation using ADS momentum.

• Defining the substrate. In our case, it was AlGaN/GaN on 3C-SiC/Si with varying nitride layer thickness.

• Material definition. This is basically defining the dielectric constant, loss factor and other parameters to define the substrate.

• EM Momentum simulation set up, where ports, frequency plan, output plan, mesh, and other parameters are defined.

• Execution of S-parameter simulation.

To determine the finite length and width of TLs, *Line Calc* of ADS Keysight was used. The GUI of *Line Calc* is shown in Fig. 5.5. The parameters such as permittivity (ϵ_r), substrate thickness (H), loss factor (Tanδ), metal thickness (T), and conductivity of metal ($Cond$) were set according to the device dimensions and material characteristics. The *Line Calc* automatically generates the length (L) and width (W) of the CPW structure according to the set gap (G) of the signal line. The extracted dimensions of TLs are presented in Fig. 5.6. To obtain the effect of line length on the transmission loss, the CPW structure was designed by varying L. The dimensions of the L were designed as 100, 200, 400, and 800 μm. Taking the extracted parameters from *Line Calc*, a photomask was designed in L-edit, as represented in Fig. 5.7.

5.4 Design and fabrication of transmission lines

After the photomask design and fabrication, the TL fabrication was done. The TLs with a finite length of 200 μm, and width of 120 μm were taken for characterization purposes. The schematic cross-sectional structure of designed and fabricated TLs on

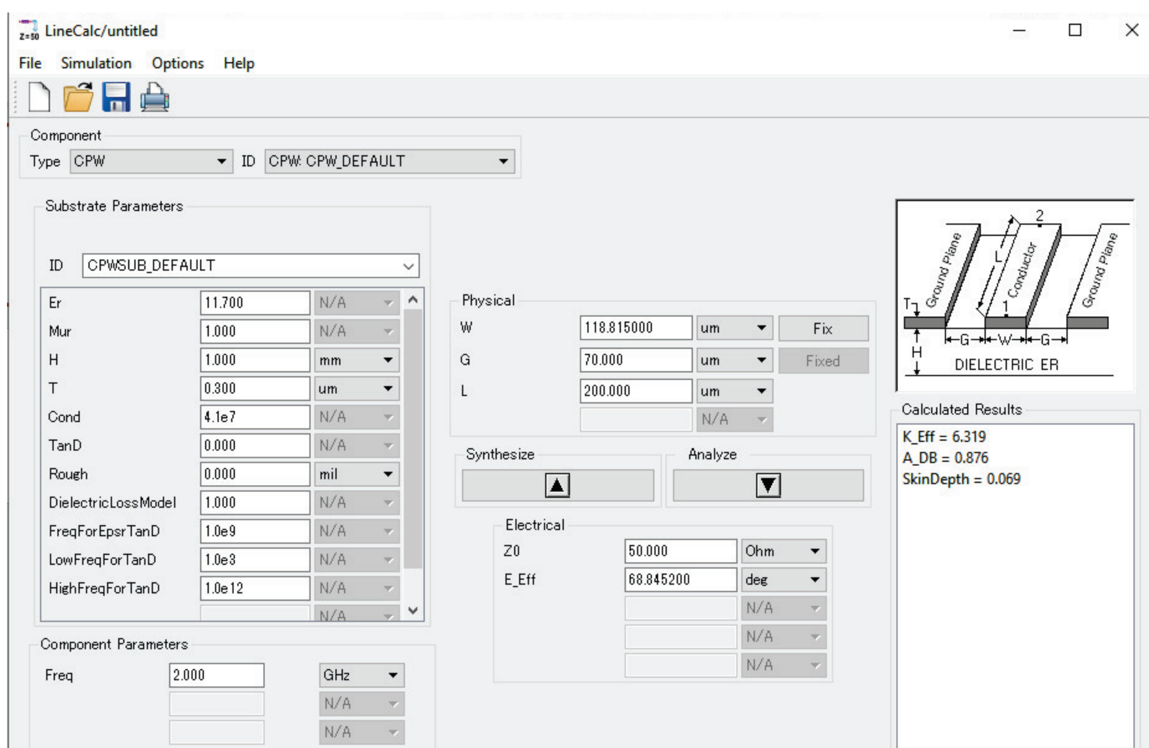

Figure 5.5: GUI of *Line calc* in ADS Keysight with set parameters.

W (µm)	G (µm)	L (µm)
120	70	100
120	70	200
120	70	400
120	70	800

W (µm)	G (µm)	L (µm)
100	60	100
100	60	200
100	60	400
100	60	800

W (µm)	G (µm)	L (µm)
85	50	100
85	50	200
85	50	400
85	50	800

Figure 5.6: Parameters of length, width, and gap of TLs extracted from *Line calc* in ADS Keysight.

three different GaN-on-3C-SiC/Si epitaxial structures (denoted by samples A, B, and C) is shown in Fig. 5.8, where only the nitride layer thicknesses were varied.

The GaN-on-3C-SiC/Si epitaxial structures (from top to bottom) consist of a GaN layer, an III-N buffer layer followed by a 1 μm thick 3C-SiC on a 1 mm thick LR-Si substrate. The combined thickness of the GaN and III-N buffer layer is termed

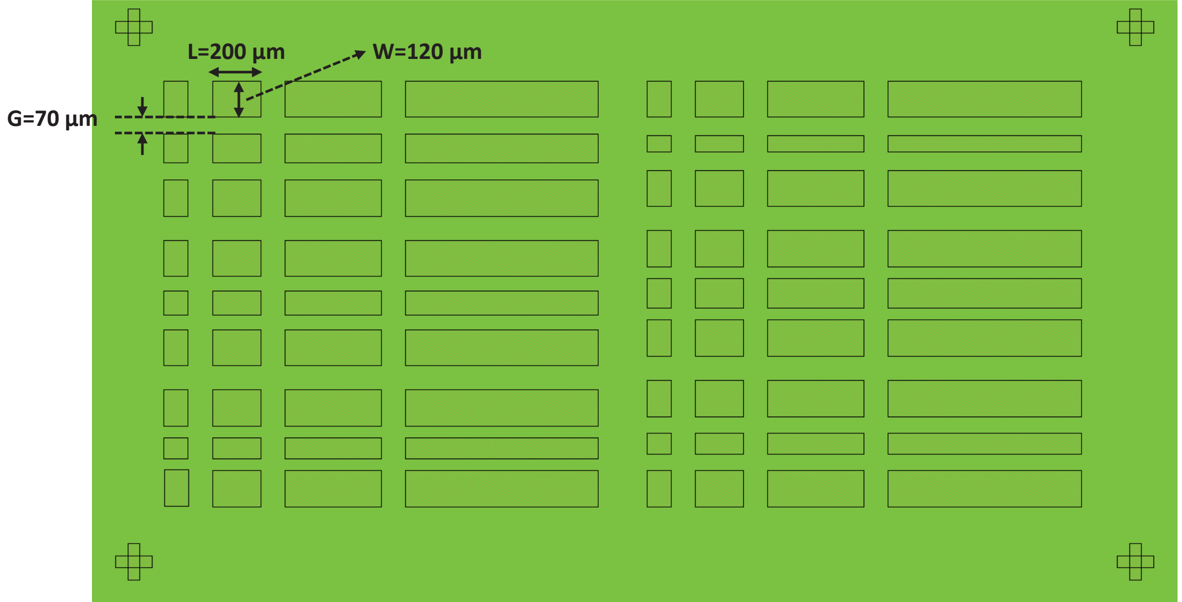

Figure 5.7: Designed photomask of different transmission lines.

as the total nitride layer (as shown in Fig. 5.8), which is 3.2, 5.3, and 8.0 μm for samples A, B, and C, respectively. For the fabrication of GaN-on-3C-SiC/Si and to maintain the equivalency of an actual HEMT device, initially, AlGaN/GaN heterostructures were grown by metal organic chemical vapor deposition (MOCVD) on commercially prepared 1 μm thick 3C-SiC(111)/low resistive ($\leq$ 3.0 mΩ-cm) Si substrate with a 6-inch diameter. After epitaxial growth, we confirmed crack-free, high-quality nitride layers on Si. To fabricate the TLs, the conductive AlGaN layer was fully removed using the BCl_3 plasma-based reactive ion etching (RIE). For the GSG probe connection, wide ground plates of 200 μm were fabricated at both sides of the signal line keeping a gap of 70 μm from the signal line. For metallization purpose, a total 0.25 μm thick metal stack (T) of Ti/Au (50/200 μm) was deposited using the electron beam evaporation technique. No backside ground plane was fabricated in all the samples, thus the metal stage acts as the ground.

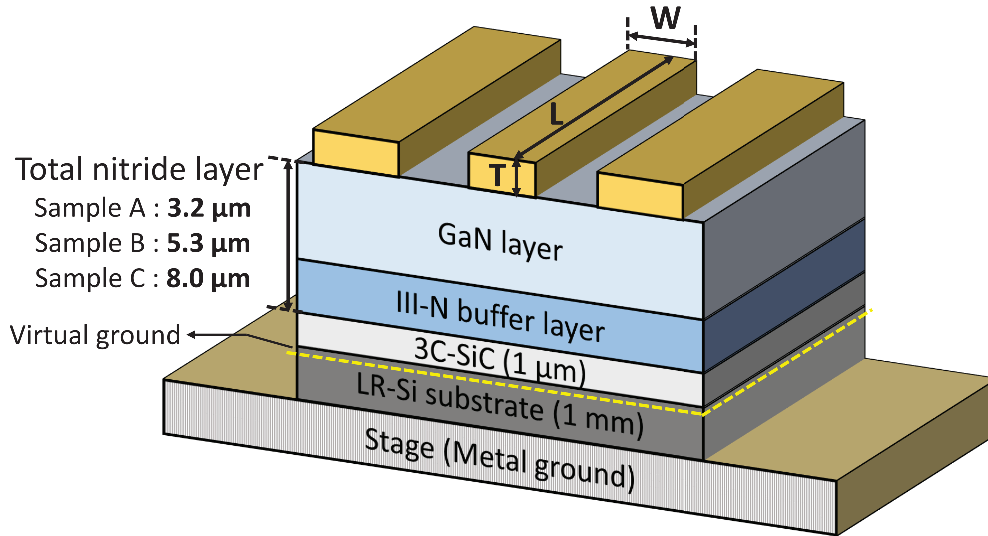

Figure 5.8: Schematic of the fabricated transmission lines on three GaN-on-3C-SiC/Si epitaxial structures, denoted by samples A, B, and C.

5.5 S-parameter analysis of transmission lines

The S-parameter measurements of the fabricated MLs were carried out with a vector network analyzer in the frequency range of 0.1 to 9 GHz. The measured S-parameter of sample C is shown in Fig. 5.9. It can be seen from the smith chart of S_{11} that the fabricated MLs were not perfectly characterized at 50 ohm. It seemed that there was an impedance transformation occurred which created a virtual ground at the interface of 3C-SiC and Si substrate. For the validation, a CPW structure (as our fabricated MLs have ground planes at both sides of the signal line which resemblance to a CPW structure) was simulated in ADS Keysight. The Fig. 5.10 (a) represents the schematic where "*Snp1*" and "*CPW1*" were used to evaluate the measured and simulated S-parameter results, respectively. The "*CPWSub*" was used to enable the substrate parameters. The fitted S_{11} is depicted in Fig. 5.10 (b). For the fitting of simulated S-parameters with the measurement data, the substrate thickness (H) was found to be $\sim$ 12 μm for sample C. It means that the virtual ground is at 12 μm

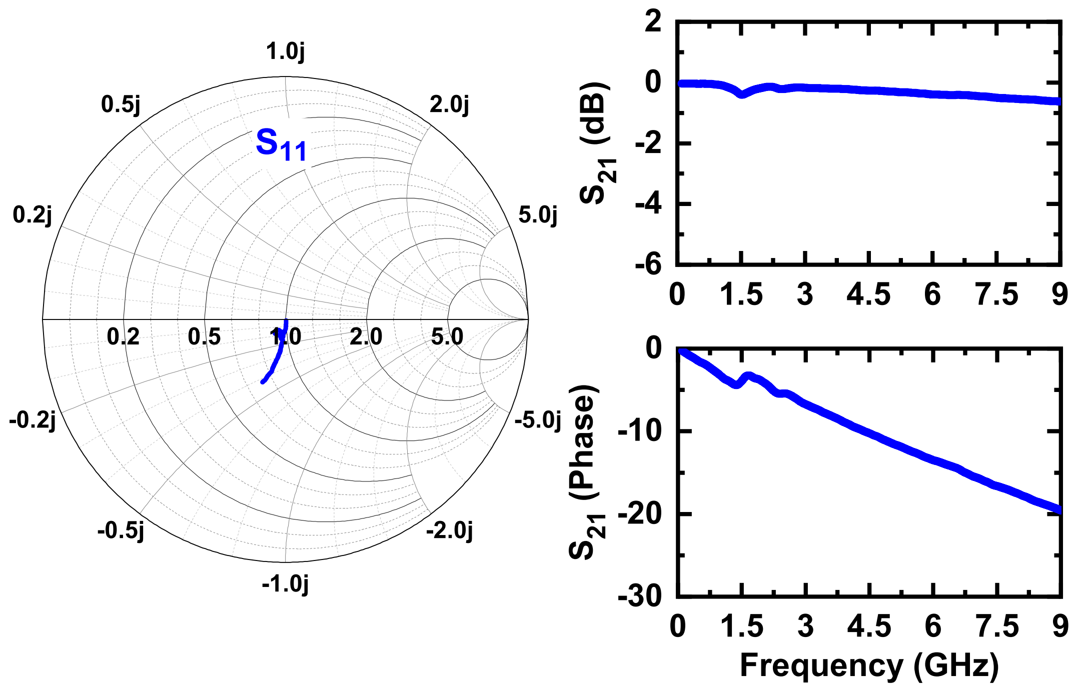

Figure 5.9: Measured S-parameter of sample C.

depth from the signal line. Accordingly, the same observation was found in the other two samples A and B.

The virtual ground at the interface of 3C-SiC and LR-Si substrate is shown with a yellow dotted line in Fig. 5.8. As the distance between the signal line and virtual ground plane becomes almost the same as the thickness of epitaxial structure on Si substrate, the capacitance becomes very high following the inverse relationship between capacitance and distance. Consequently, the gap between the signal line and ground plates does not affect the transmission line characteristics. Thus, these TLs work as microstrip lines (MLs).

5.6 EM simulation of microstrip lines in ADS

After the S-parameter analysis of the fabricated MLs, EM simulation was carried out using the ADS Keysight Momentum platform. A physical design of the fabricated

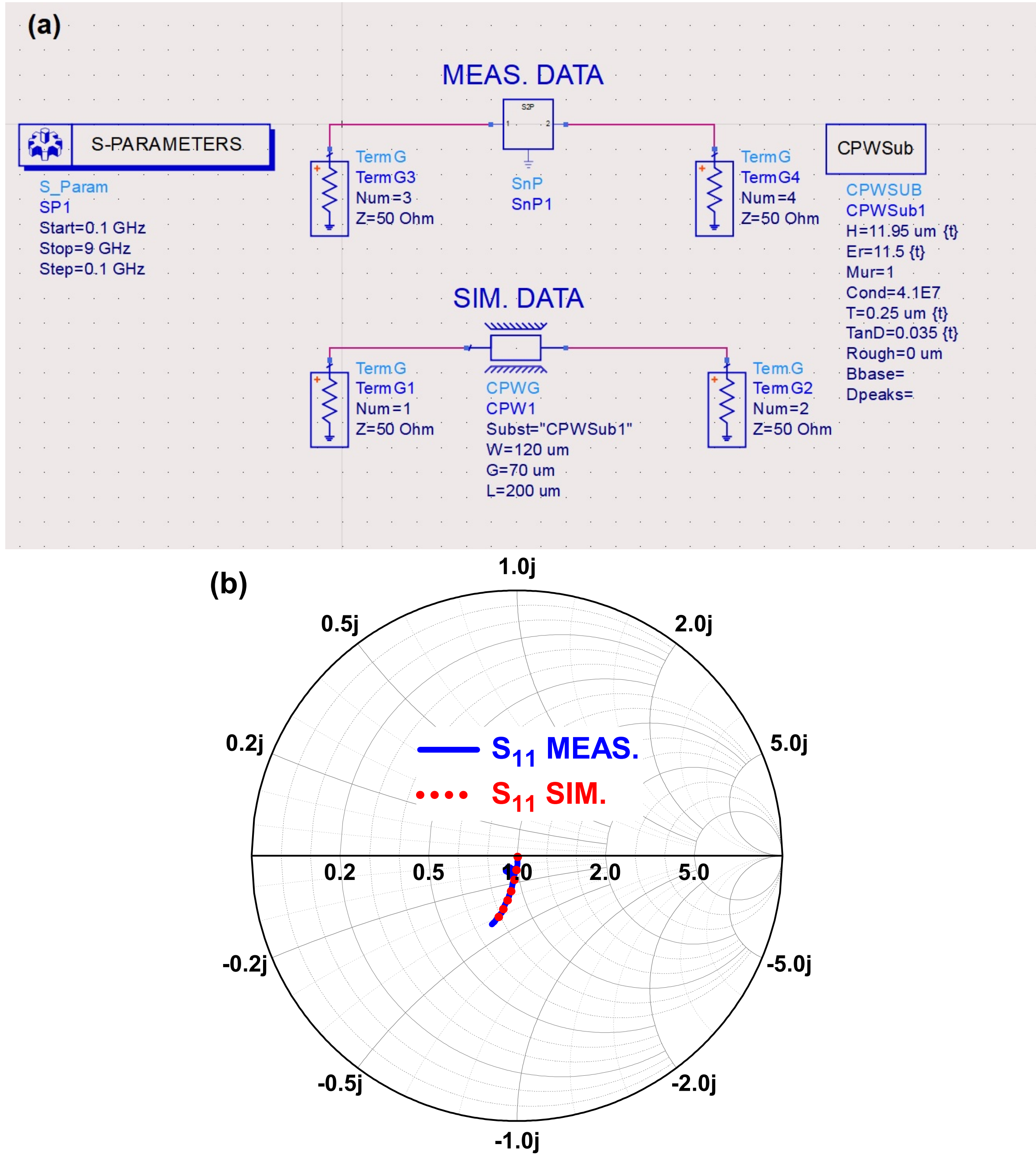

Figure 5.10: (a) Schematic of the ADS Keysight to fit the S-parameter of sample C, and (b) Fitting result of measured and simulated S_{11} of sample C.

TLs was created in the layout area of ADS keeping the line parameter same as the fabricated ones. The layout of EM simulation is depicted in Fig. 5.11.

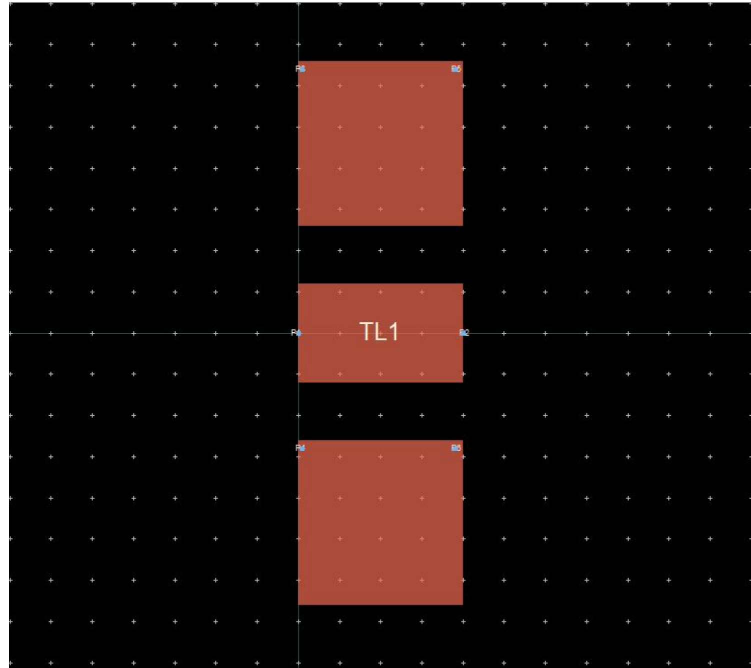

Figure 5.11: The created physical design of the transmission lines in layout platform of ADS keeping the same dimensions as the fabricated structure.

Afterward, the substrate was defined according to the epitaxial structures. There were three different substrates were designed for the samples A, B, and C. For the complexity reduction and successful evaluation of the effect of the nitride layer, the epitaxial layers on 3C-SiC/Si were treated as a single equivalent nitride layer, as shown in Fig. 5.12. For samples A, B, and C the thickness of the nitride layer was taken as 3.2, 5.3, 8.0 μm respectively.

The next step was to define the material that was used for the substrate. The permittivity, resistivity, and loss factor of the equivalent nitride layer, 3C-SiC/Si, and LR-Si are denoted in Table 5.1. As the 3C-SiC and LR-Si were taken as semiconductors, no loss factor was defined. The standard permittivity of SiC and Si were taken as 9.66 and 11.9, respectively. The resistivities were 0.03 and 0.003 Ω-cm for 3C-SiC and Si respectively. On the other hand, the equivalent nitride layer was considered as a dielectric layer with a uniform permittivity of 10.0 and a dielectric loss tangent

(Tanδ) of 0.05. The Tanδ is the measurement of the signal loss which occurs due to the inherent dissipation of electromagnetic energy in the substrate. As it denotes the measurement of loss, it should be different for different structures.

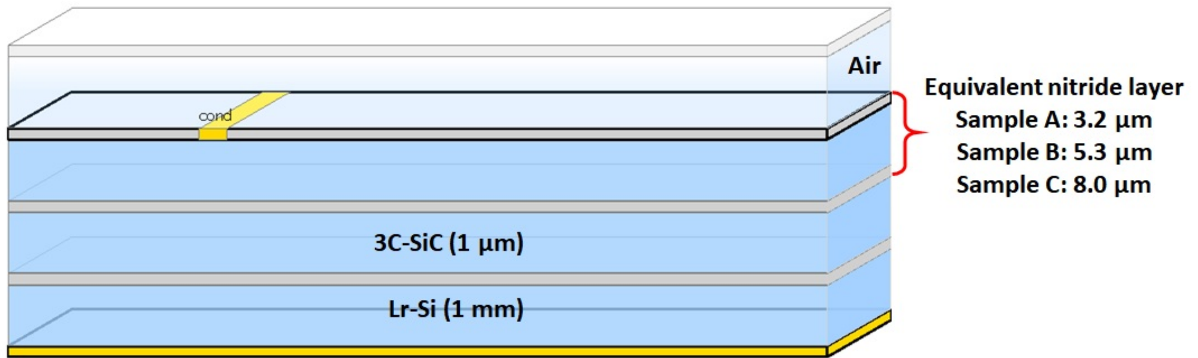

Figure 5.12: The defined substrates for EM simulation. A single equivalent nitride layer was used on 3C-SiC/LR-Si, varying the thicknesses for sample A, B, and C respectively

Table 5.1: Parameters of the used materials for the substrate definition used for EM simulation.

Materials	Thickness (μm)	Permittivity	Tanδ	Resistivity (Ω-cm)
Equivalent nitride layer	3.2 (sample A)	10	0.05	-
3C-SiC	5.3 (sample B)	9.66	-	0.03
LR-Si	8.0 (sample C)	11.9	-	0.003

The final part of the EM simulation setup is the definition of ports and set up of the frequency plan. In Fig. 5.11, it can be seen that there were 6 ports were defined. However, Pin 1 and Pin 2 are for the signal, and the other four ports (P3, P4, P5, and P6) were to define the ground. The pin configuration of the EM momentum setup is shown in Fig. 5.13. A frequency range of 0.1 to 9 GHz was used for the EM simulation purpose.

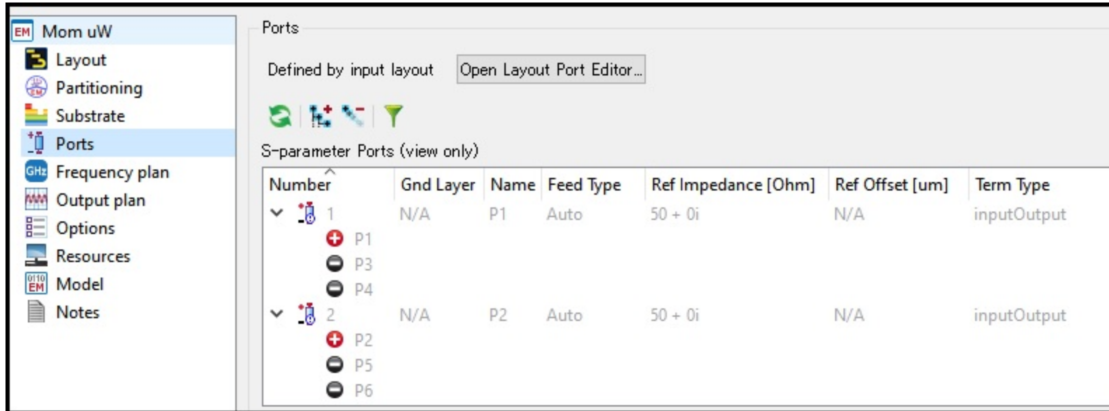

Figure 5.13: The pin configuration of 6-ports that were used for the signal and ground plates.

• S-parameter analysis from EM simulation

After successfully defining all the parameters required for the EM simulation, the S-parameters of all three samples were extracted from the simulation and then fitted with the measured data. As mentioned earlier, for the EM simulation, the epitaxial layers on 3C-SiC/Si were treated as a single equivalent nitride layer with uniform permittivity of 10.0 and dielectric loss tangent of 0.05. At the time of fitting, it was observed that for sample C, the Tanδ was least whereas, for sample A, it was the maximum, which also confirms that the thick nitride layer has a minimal loss. However, for the uniformity of the fitting result and to show the sole influence of the thickness of the nitride layer, the Tanδ was kept the same for all the structures. Because of the above, the EM simulation result only showed the influence of nitride layer thickness on transmission loss, as multiple stacks of epitaxial layers were not considered. Figs. 5.14, 5.15, 5.16 represent the S-parameters evaluated from the EM simulation and the measured data for samples A, B, and C, respectively. It can be seen that the measured S-parameters were in close fit with the EM simulated data for all three samples. Hence, the extracted attenuation of all the samples from these EM simulated data should be in accordance with the attenuation constants evaluated

from the measured S-parameter.

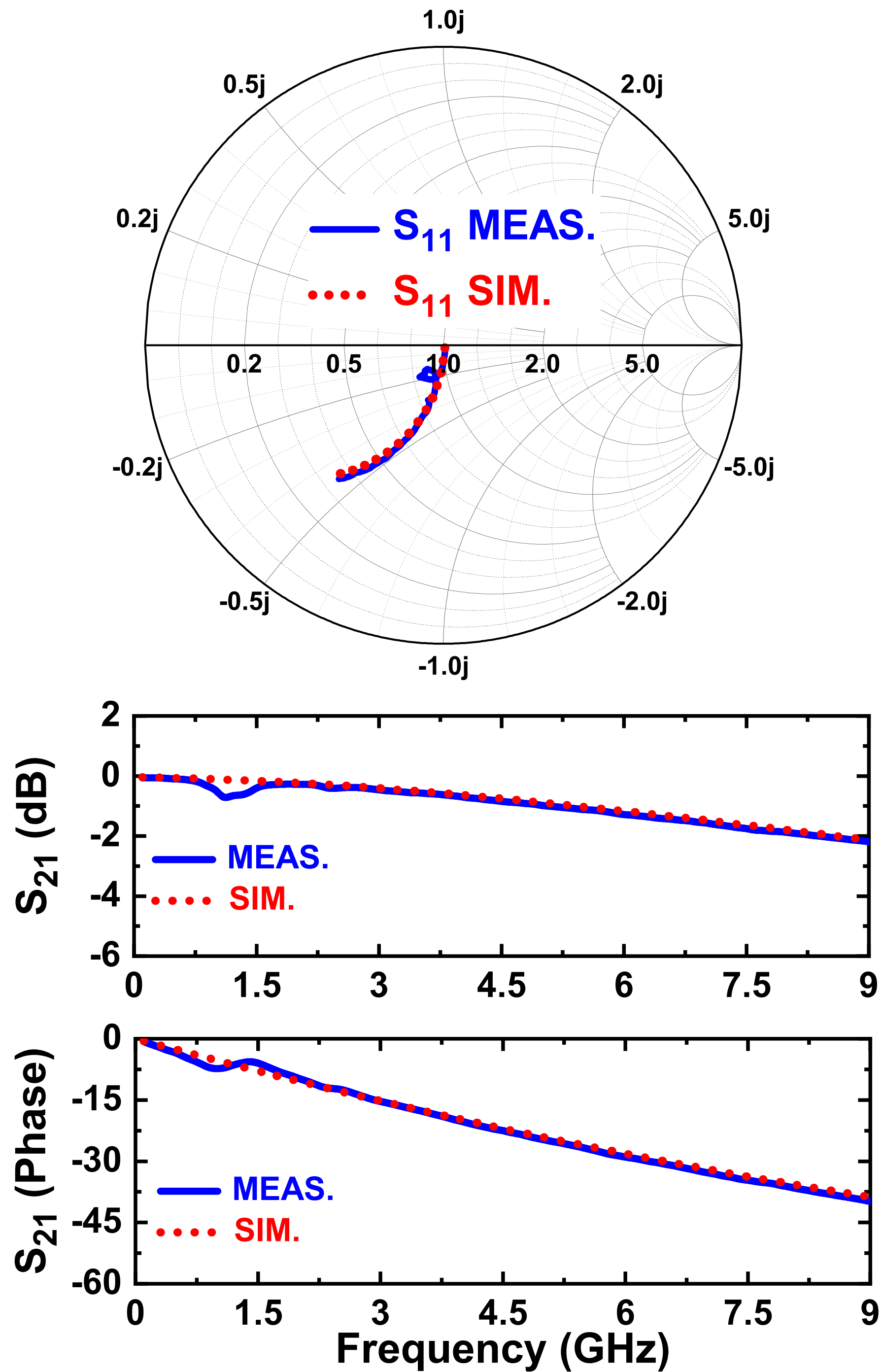

Figure 5.14: Fitting of measured S_{11} (dB), S_{21} (dB) and S_{21} (phase) with the EM simulated result of sample A for 0.1 to 9 GHz frequency range.

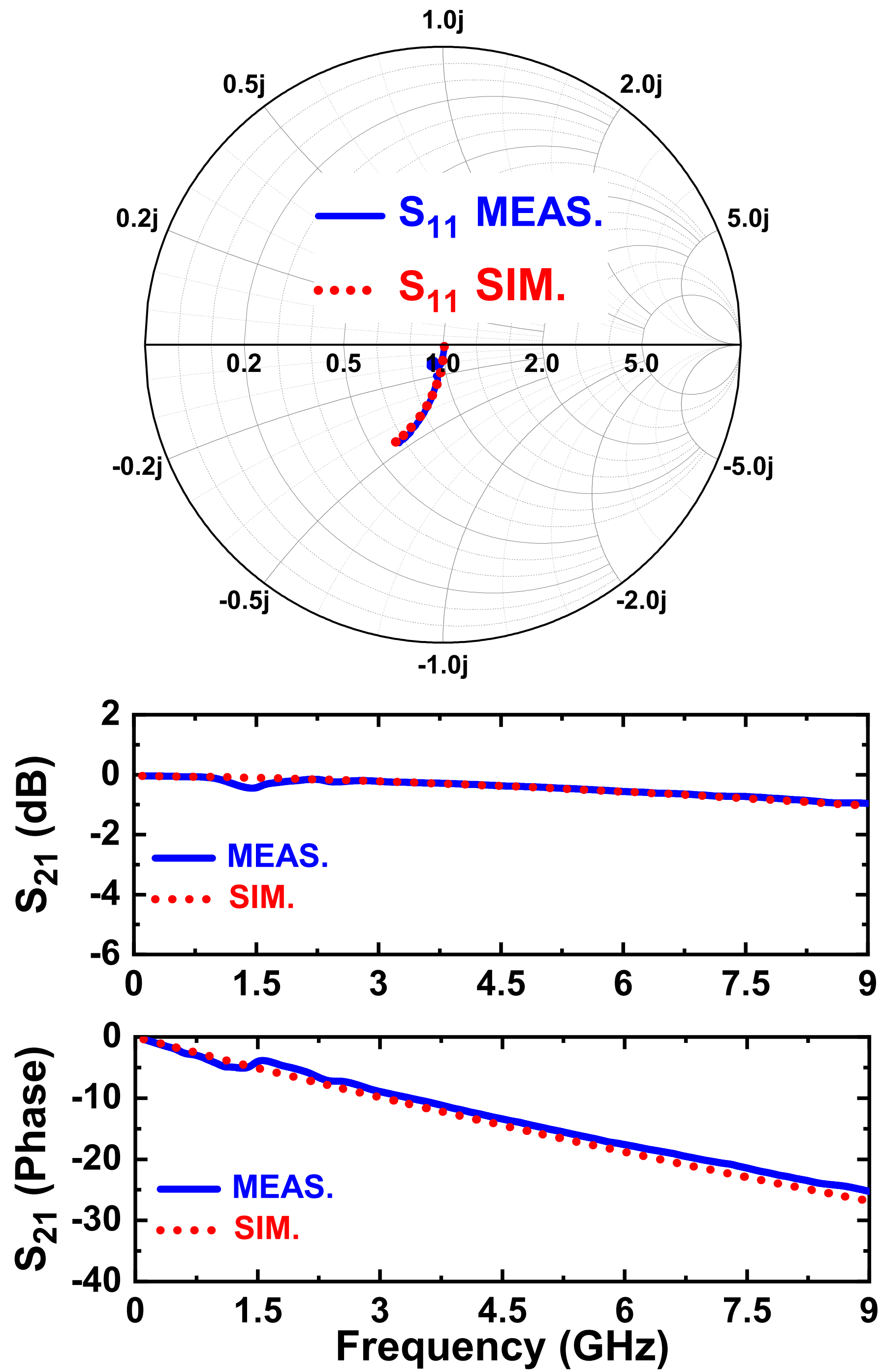

Figure 5.15: Fitting of measured S_{11} (dB), S_{21} (dB) and S_{21} (phase) with the EM simulated result of sample B for 0.1 to 9 GHz frequency range.

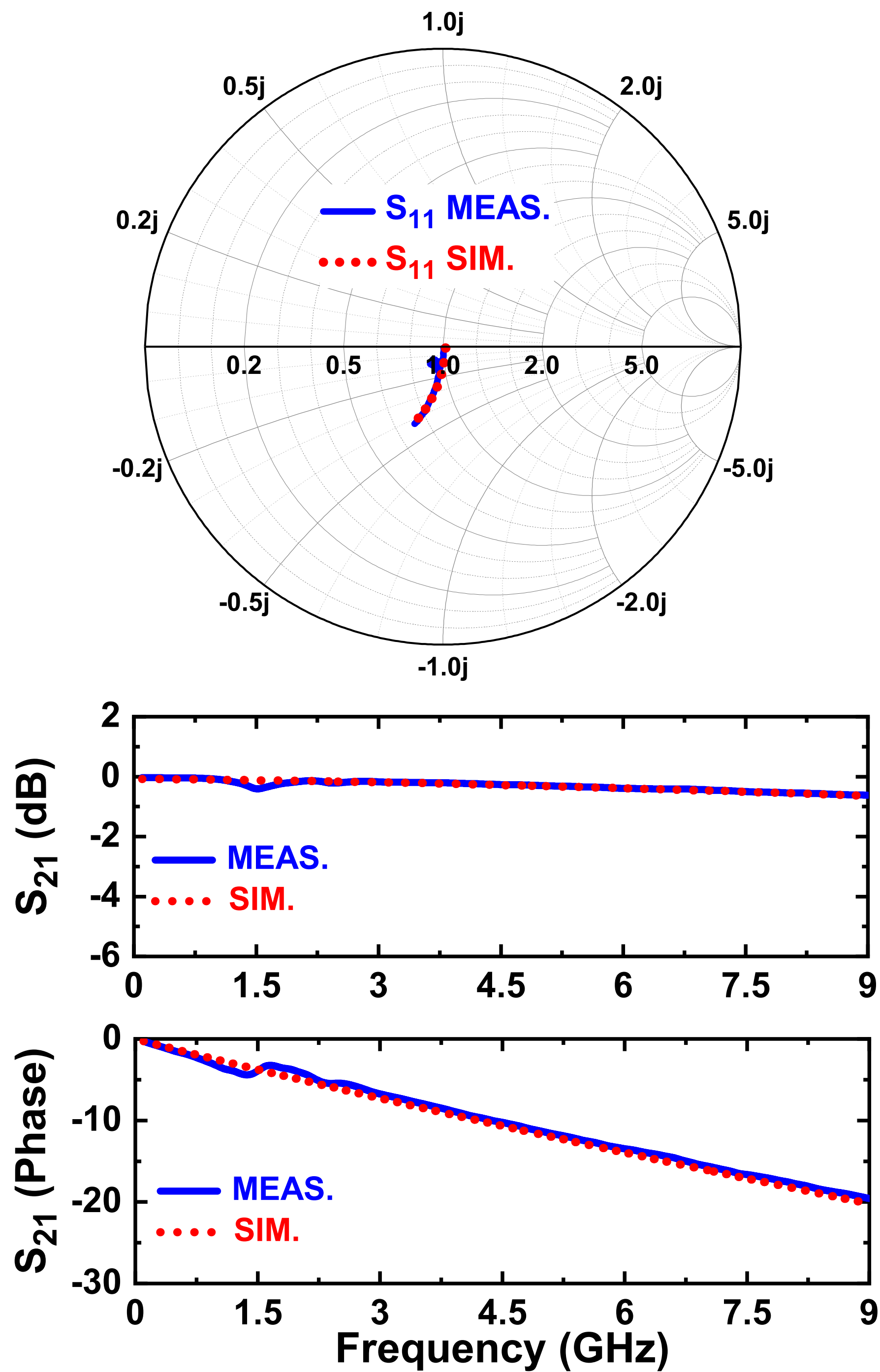

Figure 5.16: Fitting of measured S_{11} (dB), S_{21} (dB) and S_{21} (phase) with the EM simulated result of sample C for 0.1 to 9 GHz frequency range.

5.7 Characterization of transmission loss

To estimate the transmission loss, attenuation constants of all the samples were calculated from both the measured and simulated S-parameters. The S-parameters, measured from a lossy and unmatched transmission line with parameters γ and Z in a Z_0 impedance system are

$$\begin{bmatrix} S \end{bmatrix} = \frac{1}{D_s} \begin{bmatrix} (Z^2 - {Z_0}^2) sinh\gamma l & 2ZZ_0 \\ 2ZZ_0 & (Z^2 - {Z_0}^2) sinh\gamma l \end{bmatrix} \tag{5.3}$$

where $D_s = 2ZZ_0 \cosh \gamma l + (Z^2 - {Z_0}^2) \sinh \gamma l$

The above S-parameter matrix is then converted to ABCD matrix parameters which contain the propagation constant γ, and the impedance Z. The equivalent ABCD matrix and the relationship between S-parameters and ABCD matrix can be represented as Eq. 5.4 and Eq. 5.5.

$$\begin{bmatrix} ABCD \end{bmatrix} = \frac{1}{D_s} \begin{bmatrix} cosh\,\gamma l & Z\,sinh\gamma l \\ \frac{sinh\gamma l}{Z} & cosh\,\gamma l \end{bmatrix} \tag{5.4}$$

$$\begin{aligned} A &= (1 + S_{11} - S_{22} - \Delta S)/(2\,S_{21}) \\ B &= (1 + S_{11} + S_{22} + \Delta S)\,Z_0/(2\,S_{21}) \\ C &= (1 - S_{11} - S_{22} + \Delta S)/(2\,S_{21}\,Z_0) \\ D &= (1 - S_{11} + S_{22} - \Delta S)/(2\,S_{21}) \end{aligned} \tag{5.5}$$

where $\Delta S = S_{11}S_{22} - S_{21}S_{12}$

Now combining the Equations 5.3, 5.4, and 5.5, the following equation can be generated

$$e^{-\gamma L} = \frac{2S_{21}}{1 - S_{11}^2 + S_{21}^2 \pm \sqrt{(1 + S_{11}^2 - S_{21}^2)^2 - 4S_{21}^2}} \tag{5.6}$$

where γ is the propagation constant, represented as $\gamma = \alpha + j\beta$ [11, 12]. The real part of γ is considered as the attenuation constant (α) and L is the length of the transmission line.

5.7.1 Evaluation of attenuation

Attenuation constants were evaluated as an indicator of transmission loss. Eq. 5.6 was used to extract the attenuation constants from the measured S-parameters which are described in the previous section. In Fig. 5.17, the measured attenuations of fabricated TLs on samples A, B, and C are represented (the colored solid lines). At 9 GHz, the measured loss of samples A, B, and C were 0.61, 0.42, and 0.3 dB/mm. From the results, it can be seen that the loss was decreased with increasing nitride layer thickness and it was almost doubled for sample A compared to sample C while for sample B, it remained in between. Considering a lumped element equivalent circuit model of a microstrip line on GaN-on-Si structure, there exists a series combination of nitride layer capacitance (C_{nitride}) and underlying parallelly connected capacitance (C_{Si}) and resistance (R_{Si}) of the Si substrate [13]. The distance between the signal line and virtual ground plane in the Si substrate is longest in sample C because of the thickest GaN layer. Hence, following the inversely proportional relationship of capacitance and distance, the C_{nitride} is lowest in sample C and highest in sample A. Because of that, with the 8.0 μm thick nitride layer (for sample C), the effect of lossy capacitance C_{Si} is smaller than samples with 3.2 and 5.3 μm nitride layer (for samples A and B, respectively). As a result, the loss was reduced with a thick GaN layer.

In addition, the attenuation constants were also evaluated from the EM simulated data. The comparison of measured and simulated attenuation data of samples A, B, and C is shown in Fig. 5.17, where the simulated data is represented as the colored

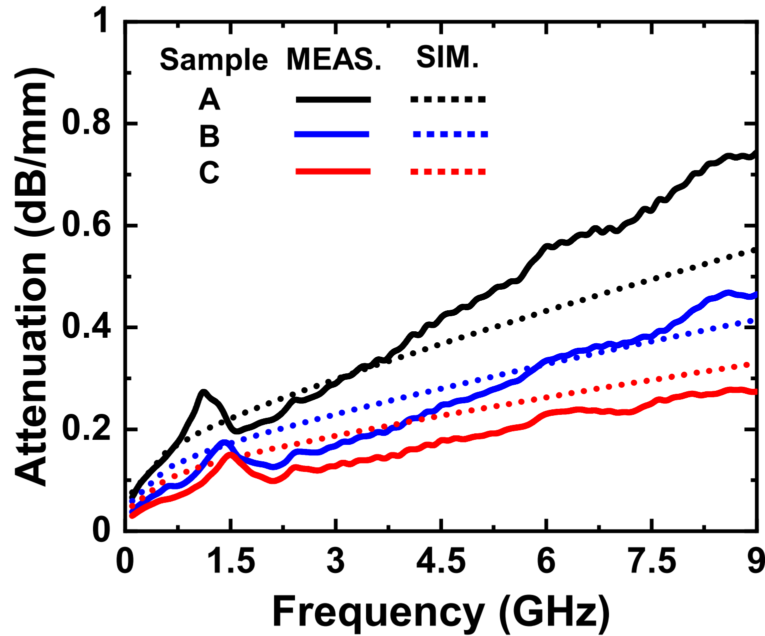

Figure 5.17: Loss comparison between the measured and EM simulated data for CPWs of samples A, B and C.

dotted lines. Compared to the measurement results, EM simulated data showed a similar trend where the loss is gradually increased with the decreasing nitride layer thickness. Therefore, it is evident from the measured and simulated data that a thicker nitride layer is better to minimize the RF loss in GaN-on-3C-SiC/LR-Si substrate.

• Evaluation of temperature-dependent attenuation

Temperature-dependent loss evaluation of MLs for samples A and C were executed using S-parameter measurements at room temperature (RT), 75, and 125 °C. Here the loss evaluation of sample B was not considered as only the temperature stability of sample C was of concern. Sample A was used for comparison purposes and to analyze the effect of the thickest and thinnest nitride layer on 3C-SiC/LR-Si. The measured loss of both the samples A and C are depicted in Fig. 5.18 at all three temperatures for 2 and 9 GHz frequency. It is clearly observed that the increment of loss for

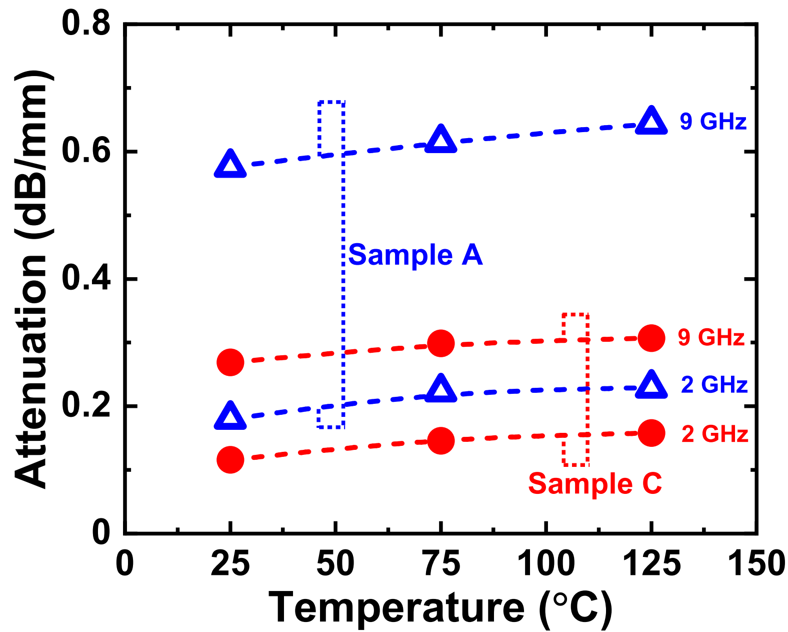

Figure 5.18: Temperature-dependent loss evaluation of sample A and C at RT, 75, and 125 °C for the frequencies of 2 and 9 GHz.

sample C from RT to 125 °C, is comparatively much lower than sample A at both the frequencies. Therefore, it is further confirmed that a thick nitride layer on GaN-on-3C-SiC/LR-Si can minimize the transmission loss significantly even at high temperatures. The above observation also corroborates with Ref. [14], where it was reported that the temperature-dependent loss evaluation by S-parameter measurements of open pads in sample C showed very good thermal stability for the temperature variation from RT to 125 °C.

5.8 Summary

An improvement of transmission loss in GaN-on-3C-SiC/LR-Si substrates was observed by introducing a thick nitride layer on Si. The same epitaxial structure of GaN on 3C-SiC/Si with three different nitride layer thicknesses of 3.2, 5.3, and 8.0 μm were used. The evaluation of loss performance exhibited that with increasing

nitride layer thickness, RF loss gradually decreases. As a result, the sample with an 8.0 μm thick nitride layer showed the minimal loss of 0.3 dB/mm compared to the sample with a 3.2 μm thick nitride layer, which showed almost double attenuation of 0.61 dB/mm at the same frequency of 9 GHz. As the GaN layer does not work as a perfect insulator, it is better to use a thick GaN layer for the suppression of transmission loss. Moreover, the EM simulation result of all samples confirmed the above observation. Furthermore, temperature-dependent loss evaluation of the sample with the thickest nitride layer also exhibited excellent temperature stability at both frequencies of 2 and 9 GHz. Hence, an introduction of a thick nitride layer of 8.0 μm in GaN-on-3C-SiC/Si can successfully minimize the RF loss compared to the same epitaxial structure with a thin nitride layer. Therefore, the above structure has successfully eliminated the low resistivity effect of Si [15], attained temperature stable amplifier characteristics, and successfully reduced the transmission loss.

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Chapter 6

Conclusion

The research presented in this dissertation proceeds from this primary motivation: fabrication and characterization of AlGaN/GaN HEMTs using 3C-SiC/LR-Si as a substrate for high-power and high-frequency operation. However, there are some challenges of getting significant RF performance in GaN-on-Si HEMTs. This dissertation is about addressing those challenges and achieving significant temperature stable amplifier characteristics in GaN-on-3C-SiC/LR-Si HETMTs.

Chapter 1 gave the primary background of HEMTs and the motivation of this research work. The working principle of AlGaN/GaN HEMTs and the advantages of using the 3C-SiC intermediate layer is also described. Finally, the outline of this dissertation is also given in this chapter.

In chapter 2, firstly the buffer layer condition was checked by Hall measurements. The wafer stability was confirmed by the SORI which is stably controlled at less than 50 μm. The electron transport characteristics achieved excellent 2DEG mobility and carrier concentration which are very important for getting particular FET per-

formance. In addition, an oversight into how AlGaN/GaN HEMTs were fabricated throughout the course of this research is also included.

Chapter 3 deals with the DC characterization of the fabricated HEMTs. The obtained DC performance confirmed the significant FET operation with the inclusion of an 8 μm thick nitride layer. The current density, transconductance, and other DC parameters are comparable. Moreover, the devices also attained thermally stable DC performance which signified their ability to perform in high-power device technology. The high-temperature stable DC performance initially confirmed the excellent quality of the HEMTs and suppression of charge carrier generation which was one of the purposes of this work.

Chapter 4 described the detailed RF performance of the devices. To be able to perform in the high-frequency domain, evaluation of amplifier performance is very crucial. Firstly, the S-parameter measurements exhibited a comparable cutoff frequency of 4.8 GHz for 2 μm gate length devices. At high temperatures, a degradation of f_{T} and f_{max} was observed. However, comparing the transconductance from S-parameter measurements, DC, and small-signal equivalent circuit, it was confirmed that the degradation was mainly attributed to the intrinsic property of the device. Primitive loss evaluation from pads verified the suppression of charge carrier generation with the 8 μm thick nitride layer. The output power characteristics showed 2 W/mm output power with 47 % PAE at room temperature. Furthermore, it has also achieved excellent temperature stability with a slightly deteriorated output power. A comparative study of output power showed that the slight deterioration was not coming from any huge leakage in the buffer layer, but mainly because of the current density *i.e* intrinsic property of the device.

In chapter 5, a comparative study of high-frequency loss evaluation was carried

out by varying the nitride layer thickness. To successfully evaluate the significance of a thick nitride layer, microstrip lines were designed and their performance was evaluated by S-parameter measurement. Attenuation constants were extracted to quantify the loss. It was seen that the sample with an 8 μm thick nitride layer showed minimal attenuation whereas the sample with 3.2 μm thick nitride layer exhibited almost double loss. EM simulated data also verified the observation. Moreover, the temperature-dependent loss evaluation also confirmed the above conclusion.

In conclusion, AlGaN/GaN HEMTs were successfully fabricated on 6-inch 3C-SiC/LR-Si. A thick nitride layer of 8 μm was grown via a 3C-SiC intermediate layer by reducing the thermal and lattice mismatch between GaN and Si. It also helped to suppress the buffer leakage due to its high bandgap. The epitaxial structure showed excellent electron transport characteristics, which was concluded by its DC performance. Elimination of the low resistivity effect of Si was confirmed from the initial small-signal performance and loss evaluation from pads. Moreover, it also achieved a thermally stable amplifier performance with the introduction of an 8 μm thick nitride layer. It was established that a thick nitride layer can suppress the charge carrier generation at high temperatures and RF transmission loss. Hence, this structure effectively addressed the challenges and showed outstanding RF performance. The presented GaN-on-3C-SiC/Si HEMTs have all the potential to become a front runner in next-generation high-power and high-frequency applications.

Future Prospects

The potential of the reported AlGaN/GaN HEMT with an 8 μm thick nitride layer is demonstrated. However, the conclusion is made based on its performance in the microwave domain. In the future, it will be important to analyze its performance

in millimeter wave (mmW) applications which enable larger bandwidth, higher data rate communication with larger antenna array facilitation in the miniature physical dimension. In addition, it was estimated that with a gate length of 100 nm, the expected cut-off frequency can reach more than 100 GHz. However, with a shorter gate length, there is a possibility of a short-channel effect. As we used a thick nitride layer, it will be a challenge to suppress the short-channel effect as we found in a simulation study that with thicker unintentionally doped (UID) GaN layer, the reverse leakage current is increased. Hence, GaN layer thickness and device dimension optimization will be important to get an optimum performance. Therefore, these two areas can be an area of future research with the reported device structure.

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Arijit Bose

Nagoya, Japan

List of Publications

Journal papers and letters

Publications related to this thesis:

1. **A. Bose**, D. Biswas, S. Hishiki, S. Ouchi, K. Kitahara, K. Kawamura and A. Wakejima, “Elimination of the low resistivity of Si substrates in GaN HEMTs by introducing a SiC intermediate and a thick nitride layer,” *IEEE Electron Device Lett.*, **41**, no. 10, pp. 1480—1483 (2020).

2. **A. Bose**, D. Biswas, S. Hishiki, S. Ouchi, K. Kitahara, K. Kawamura and A. Wakejima, “A Temperature Stable Amplifier Characteristics of AlGaN/GaN HEMTs on 3C-SiC/Si,” *IEEE Access*, **9**, pp. 57046—57053 (2021).

3. **A. Bose**, D. Biswas, S. Hishiki, S. Ouchi, K. Kitahara, K. Kawamura and A. Wakejima, “Influence of thick nitride layer on transmission loss in GaN-on-3C-SiC/low resistivity Si,” *IEICE Electron. Express*, (2022).

Other contributed articles:

1. A. Rakshit, **A. Bose**, D. Biswas, M. Roy, R. Bhar, S. Chakraborty, "Control of interfacial layer growth during deposition of high-κ oxide thin films in reactive RF-sputtering system," *Appl. Surf. Sci.*, **423**, pp. 957—960 (2017).

2. D. Biswas, S. Mondal, A.Rakshit, **A. Bose**, S. Bhattacharyya, S. Chakraborty, "Size and density controlled Ag nanocluster embedded MOS structure for memory applications," *Mater. Sci. Semicond. Process.*, **63**, pp. 1—5 (2017).

Conference Proceedings

1. **A. Bose**, D. Biswas, S. Hishiki, S. Ouchi, K. Kitahara, K. Kawamura and A. Wakejima, "Effect of thick nitride layer on the RF performance in GaN HEMTs on 3C-SiC/Si," *International Conference on Solid State Devices and Materials*, Japan, Sept. (2020).

2. **A. Bose**, D. Biswas, S. Hishiki, S. Ouchi, K. Kitahara, K. Kawamura and A. Wakejima, "A TCAD simulation study on gated-anode diodes for microwave applications," *European Microwave Week 2021*, London, Feb. (2022).